



# REALTEK

**APOLLO PON SFU**  
**Register Reference File**

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## Revision History

Revision	Date	Description	Author
v0.0.1	2010/02/11	Initial Version	NickWu
v0.0.2	2011/04/11	Add GPON registers	Scott Lin

# Table of Contents

<b>1</b>	<b>Hardware</b>	<b>1</b>
1.1	INTERFACE	1
	DIGITAL_INTERFACE_SELECT	1
	SKIP_MII_RXER	1
	EXT_RGMXF	1
	I2C_CLOCK_DIV	2
	EXT_TXC_DLY	2
	GPHY_IND_WD	2
	GPHY_IND_CMD	3
	GPHY_IND_RD	3
	EFUSE_CFG	3
	EFUSE_IND_WD	4
	EFUSE_IND_CMD	4
	EFUSE_IND_RD	4
	I2C_IND_WD	5
	I2C_IND_CMD	5
	I2C_IND_RD	5
	REGCTRL_GLB	6
	IOPAD_CFG	6
	IO_LED_EN	7
	IO_MODE_EN	7
	CFG_PCSXF	8
	CFG_PHY_CTRL	8
	CFG_PHY_POLL_CMD	9
	CFG_PHY_POLL_ADR_0	9
	CFG_PHY_POLL_ADR_1	9
	CFG_PHY_POLL_INV_0	10
	CFG_PHY_POLL_INV_1	10
	CFG_PHY_POLL_WD_0	10
	CFG_PHY_POLL_WD_1	11
	CHIP_DEBUG_OUT	11
1.2	RESET	11
	CHIP_RST	11
	SOFTWARE_RST	11
1.3	INTERRUPT	12
	INTR_CTRL	12
	INTR_IMR	12
	INTR_IMS	13
	INTR_STAT	14
1.4	BIST & BISR	14
	BIST_CFG19	14
	BIST_CFG18	14
	BIST_CFG17	14
	BIST_CFG16	15
	BIST_CFG15	15
	BIST_CFG14	15
	BIST_CFG13	15

BIST_CFG12	16
BIST_CFG9	16
BIST_CFG8	16
BIST_CFG7	16
BIST_CFG4	16
BIST_CFG3	17
BIST_CFG2	17
BIST_CFG1	17
BIST_CFG0	17
DIAG_MODE	18
DFR_TEST_RESUME	18
BIST_CFG	18
RAM_DVS_CFG0	18
RAM_DVS_CFG1	19
RAM_DVS_CFG2	19
RAM_DVS_CFG3	20
RAM_DVS_CFG4	20
RAM_DVS_CFG5	20
PON_INTEGRATION	21
1.5 CPU RELATIVE	21
1.6 LED	21
LED_LED	21
DATA_LED_CFG	22
LED_ACTIVE_LOW_CFG	22
SERI_LED_ACTIVE_LOW_CFG	23
LED_FORCE_VALUE_CFG	23
LED_BLINK_RATE_CFG	23
LOW_RATE_BLINK_CFG	24
LED_EN	25
SERI_LED_CLK_PER	25
SERI_LED_REFRESH_TIME	25
1.7 HW MISC.	25
FORCE_P_DMP	25
EN_FORCE_P_DMP	26
GLB_MAC_MISC	26
WRAP_GPHY_MISC	26
1.8 CHP INFORMATION	27
MODEL_NAME_INFO	27
CHIP_INFO	27
BOND_INFO	28
MISCELLANEOUS_CONFIGURE0	28
FORCE_P_ABLTY	29
MDX_PHY_REG1	29
UPS_CTRL2	30
GATING_CLK_1	30
ROUTER_UPS_CFG	30
P_ABLTY	30
GPIO_CTRL_0	31
GPIO_CTRL_1	31
GPIO_CTRL_2	32
GPIO_CTRL_3	32
GPIO_CTRL_4	32
RTL_OUI_CFG	33
REVISION_CFG	33
MODEL_CFG	33
WAKELPI_SLOT_PRD	33
WAKELPI_SLOT	34
RGM_EEE	34
ABLTY_FORCE_MODE	34
DEBUG_SEL	34

RST_SYNC_FIFO	35
SDS_CFG	35
MAC_ACT_CFG	35
BYPSS_ABLTY_LOCK	36
FIFO_ERR_STS	36
SDS_AN_RX_CFG	36
SDS_FIB_STATUS	36
EXT_STS	37
AFE_VER	37
PON_MODE_CFG	37
HTRAM_DVS_CFG	38
HWPKT_GEN_STA	38
ALL_PORT_LKDN_TIME	38
MODE_EXT	38
GPHY_AFE_DBG_CFG	39
AD5_CTRL	39
PWM_CTRL1	39
PWM_CTRL2	40
TM_DLY	40
TM_CTRL	41
TM_STS	41
AD5_ALARM	41
AD5_DATA	42
TM_ALARM	42
CHIP_INF_SEL	42
SLIC_INSEL_CTRL	42
SYS_PKT_BUF_CTRL	43
DYNGASP_CTRL	43
BOND_STRAP_STS0	43
BOND_STRAP_STS1	44
BOND_STRAP_STS2	44
MISCELLANEOUS_BONDING	44
MISCELLANEOUS_STRAPPING1	46
MISCELLANEOUS_STRAPPING0	47
MAC_DLYLNK	48
PLL_RGM_CTRL1	48
PLL_RGM_CTRL2	49
PLL_RGM_CTRL3	49
<b>2 MAC &amp; PHY</b>	<b>51</b>
2.1 MAC CONTROL	51
FPGA_VER_MAC	51
MAC_CPU_TAG_CTRL	51
MAC_CPU_TAG_AWARE_CTRL	51
ACCEPT_MAX_LEN_CTRL	52
MAX_LENGTH_CFG1	52
MAX_LENGTH_CFG0	53
MAX_LENGTH_LIMINT_IPG	53
IOL_RXDROP_CFG	53
CFG_BACKPRESSURE	54
CFG_UNHIOL	54
SWITCH_MAC	54
SWITCH_CTRL	55
INBW_BOUND	55
MAX_FIFO_SIZE	55
P_TX_ERR_CNT	56
P_CGSTTIMER	56
P_MISC	56
P_CFG_FRC_RATE	57
P_CUR_RATE	57

UTP_FIBER_AUTODET	58
2.2 PHY & SERDES	58
WSDS_ANA_00	58
WSDS_ANA_01	59
WSDS_ANA_02	59
WSDS_ANA_03	59
WSDS_ANA_04	60
WSDS_ANA_05	60
WSDS_ANA_06	60
WSDS_ANA_07	61
WSDS_ANA_08	61
WSDS_ANA_09	61
WSDS_ANA_0A	62
WSDS_ANA_0B	62
WSDS_ANA_0C	63
WSDS_ANA_0D	63
WSDS_ANA_0E	63
WSDS_ANA_0F	64
WSDS_ANA_10	64
WSDS_ANA_11	64
WSDS_ANA_12	65
WSDS_ANA_13	65
WSDS_ANA_14	65
WSDS_ANA_15	66
WSDS_ANA_16	66
WSDS_ANA_17	66
WSDS_ANA_18	66
WSDS_ANA_19	67
WSDS_ANA_1A	67
WSDS_ANA_1B	68
WSDS_ANA_1C	68
WSDS_ANA_1D	68
WSDS_ANA_1E	68
WSDS_ANA_1F	69
WSDS_ANA_20	69
WSDS_ANA_21	69
WSDS_ANA_22	69
WSDS_ANA_23	70
WSDS_ANA_24	70
WSDS_ANA_25	71
WSDS_DIG_00	71
WSDS_DIG_01	72
WSDS_DIG_02	72
WSDS_DIG_03	72
WSDS_DIG_04	73
WSDS_DIG_05	73
WSDS_DIG_06	73
WSDS_DIG_07	73
WSDS_DIG_08	74
WSDS_DIG_09	74
WSDS_DIG_0A	74
WSDS_DIG_0B	75
WSDS_DIG_0C	75
WSDS_DIG_0D	75
WSDS_DIG_0E	75
WSDS_DIG_0F	76
WSDS_DIG_10	76
WSDS_DIG_11	76
WSDS_DIG_12	76
WSDS_DIG_13	77

WSDS_DIG_14	77
WSDS_DIG_15	77
WSDS_DIG_16	78
WSDS_DIG_17	78
WSDS_DIG_18	78
WSDS_DIG_19	79
WSDS_DIG_1A	79
WSDS_DIG_1B	79
WSDS_DIG_1C	79
WSDS_DIG_1D	80
WSDS_DIG_1E	80
WSDS_DIG_1F	80
WSDS_DIG_20	81
WSDS_DIG_21	81
WSDS_DIG_22	81
WSDS_DIG_23	82
WSDS_DIG_24	82
WSDS_DIG_25	82
WSDS_DIG_26	82
WSDS_DIG_27	82
WSDS_DIG_28	83
WSDS_DIG_29	83
WSDS_DIG_2A	83
WSDS_DIG_2B	83
WSDS_DIG_2C	83
SDS_REG0	84
SDS_REG1	85
SDS_REG2	85
SDS_REG3	85
SDS_REG4	86
SDS_REG5	87
SDS_REG6	87
SDS_REG7	88
SDS_REG8	88
SDS_REG9	89
SDS_REG10	89
SDS_REG11	89
SDS_REG12	89
SDS_REG13	90
SDS_REG14	90
SDS_REG15	91
SDS_REG16	91
SDS_REG17	91
SDS_REG18	91
SDS_REG19	91
SDS_REG20	92
SDS_REG21	92
SDS_REG22	92
SDS_REG23	92
SDS_REG24	93
SDS_REG25	93
SDS_REG26	93
SDS_REG27	93
SDS_REG28	93
SDS_REG29	94
SDS_EXT_REG0	94
SDS_EXT_REG1	94
SDS_EXT_REG2	94
SDS_EXT_REG3	95
SDS_EXT_REG4	95

SDS_EXT_REG5	95
SDS_EXT_REG6	95
SDS_EXT_REG7	96
SDS_EXT_REG8	96
SDS_EXT_REG9	96
SDS_EXT_REG10	96
SDS_EXT_REG11	96
SDS_EXT_REG12	97
SDS_EXT_REG13	97
SDS_EXT_REG14	97
SDS_EXT_REG15	97
SDS_EXT_REG16	98
SDS_EXT_REG24	98
SDS_EXT_REG25	98
SDS_EXT_REG26	98
SDS_EXT_REG27	99
SDS_EXT_REG28	99
SDS_EXT_REG29	99
SDS_EXT_REG30	99
FIB_REG0	100
FIB_REG1	100
FIB_REG2	101
FIB_REG4	101
FIB_REG5	101
FIB_REG6	101
FIB_REG7	102
FIB_REG8	102
FIB_REG13	102
FIB_REG14	102
FIB_REG16	103
FIB_REG17	103
FIB_REG18	103
FIB_REG19	103
FIB_REG20	104
FIB_REG21	104
FIB_REG22	104
FIB_REG23	104
FIB_REG28	104
FIB_REG29	105
FIB_REG30	105
FIB_EXT_REG0	105
FIB_EXT_REG1	106
FIB_EXT_REG2	106
FIB_EXT_REG4	106
FIB_EXT_REG5	107
FIB_EXT_REG6	107
FIB_EXT_REG7	107
FIB_EXT_REG8	107
FIB_EXT_REG13	108
FIB_EXT_REG14	108
FIB_EXT_REG16	108
FIB_EXT_REG17	108
FIB_EXT_REG18	109
FIB_EXT_REG19	109
FIB_EXT_REG20	109
FIB_EXT_REG21	109
FIB_EXT_REG22	110
FIB_EXT_REG23	110
FIB_EXT_REG24	110
FIB_EXT_REG25	110



FIB_EXT_REG26	111
FIB_EXT_REG27	111
FIB_EXT_REG28	111
FIB_EXT_REG29	111
FIB_EXT_REG30	112
2.3 RTCT	112
2.4 POWER SAVING	112
EEE_TX_SEL_CTRL	112
EEE_EEEP_PORT_CFG	112
P_EEECFG	113
P_EEETXMTR	114
P_EEERXMTR	114
EEE_TX_THR_GIGA	114
EEE_TX_THR_FE	115
EEE_RX_FC_REG	115
EEE_MISC	115
EEE_GIGA_CTRL0	116
EEE_GIGA_CTRL1	117
EEE_100M_CTRL0	117
EEE_100M_CTRL1	117
EEE_BURSTSIZE	118
EEE_IFG_CFG	118
EEE_RXIDLE	118
EEE_DECISION_WINDOW	118
PS_LINKID_GATCLK_CTRL	119
P_EEEP_CFG	119
EEEP_CFG	120
EEEP_TIMER_UNIT_CTRL	120
EEEP_TX_TIMER_GIGA_CTRL	121
EEEP_TX_TIMER_500M_CTRL	121
EEEP_TX_TIMER_100M_CTRL	121
EEEP_TX_GIGA_CTRL	122
EEEP_TX_500M_CTRL	122
EEEP_TX_100M_CTRL	123
EEEP_RX_RATE_GIGA_CTRL	123
EEEP_RX_RATE_500M_CTRL	124
EEEP_RX_RATE_100M_CTRL	124
EEEP_RX_SLEEP_STEP_CTRL	124
EEEP_RX_WAKE_TIMER_GIGA_CTRL	125
EEEP_RX_TIMER_GIGA_CTRL	125
EEEP_RX_WAKE_TIMER_500M_CTRL	126
EEEP_RX_TIMER_500M_CTRL	126
EEEP_RX_WAKE_TIMER_100M_CTRL	126
EEEP_RX_TIMER_100M_CTRL	127
P_EEEPTXMTR	127
P_EEEPRXMTR	128
SW_PWRSAB_CTRL	128
2.5 AUTO FALLBACK	128
FB_CTRL	128
FB_PORT_CFG	129
FB_PORT_ERR_CNT	130
FB_PORT_MONITOR_CNT	130
<b>3 Layer 2</b>	<b>131</b>
3.1 ADDRESS TABLE LOOKUP	131
LUT_UNMATCHED_SA_CTRL	131
LUT_UNKN_SA_CTRL	131
LUT_UNKN_UC_DA_CTRL	132
LUT_LEARN_OVER_CTRL	132
LUT_CFG	132

	LUT_AGEOUT_CTRL	133
	LUT_LRN_LIMITNO	133
	L2_LRN_CNT	134
	L2_LRN_OVER_STS	134
	LUT_SYS_LRN_LIMITNO	134
	L2_SYS_LRN_OVER_STS	135
	L2_SYS_LRN_CNT	135
	UNKN_L2_MC	135
	UNKN_IP4_MC	136
	UNKN_IP6_MC	136
	UNKN_MC_PRI	136
	LUT_BC_FLOOD	137
	LUT_UNKN_MC_FLOOD	137
	LUT_UNKN_UC_FLOOD	137
	L2_EFID	138
	LUT_SYS_LRN_OVER_CTRL	138
3.2	ADDRESS LEARNING & FLUSH	138
	L2_TBL_FLUSH_CTRL	138
	L2_TBL_FLUSH_EN	139
3.3	L2 & IP MULTICAST	139
	L2_IPMC_VLAN_LEAKY	139
	L2_IPMC_ISO_LEAKY	140
3.4	(IEEE802.1Q) VLAN	140
	VLAN_PORT_ACCEPT_FRAME_TYPE	140
	VLAN_INGRESS	141
	VLAN_EGRESS_TAG	141
	VLAN_MBR_CFG	142
	VLAN_CTRL	142
	VLAN_PB_FID	143
	VLAN_PB_FIDEN	143
	VLAN_PB_PRI	143
	VLAN_PB_VIDX	144
	VLAN_EGRESS_KEEP	144
	VLAN_EXT_VIDX	145
3.5	(IEEE802.1AD) PROVIDER BRIDGES/Q-IN-Q	145
	SVLAN_UPLINK_PMSK	145
	SVLAN_LOOK_UP_TYPE	145
	SVLAN_MC2S	146
	SVLAN_C2S	146
	SVLAN_SP2C	147
	SVLAN_EP_DMAC_CTRL	147
	SVLAN_P_SVIDX	147
	SVLAN_CTRL	148
	SVLAN_CFG	149
	SVLAN_MBRCFG	149
3.6	(IEEE802.1V) PROTOCOL-BASED VLAN	150
	VLAN_PPB_VLAN_VAL	150
	VLAN_PORT_PPB_VLAN	150
3.7	LINK AGGREGATION	151
	PORT_TRUNK_GROUP_EN	151
	PORT_TRUNK_CTRL	151
	PORT_TRUNK_HASH_MAPPING	152
3.8	SPANNING TREE	152
	MSTI_CTRL	152
3.9	PORT ISOLATION	153
	PISO_P_MODE0_CTRL	153
	PISO_P_MODE1_CTRL	153
	PISO_EXT_MODE0_CTRL	153
	PISO_EXT_MODE1_CTRL	154
	PISO_CTRL	154

3.10 RMA	155
RMA_CTRL00	155
RMA_CTRL01	155
RMA_CTRL02	156
RMA_CTRL03	157
RMA_CTRL04	157
RMA_CTRL08	158
RMA_CTRL0D	159
RMA_CTRL0E	159
RMA_CTRL10	160
RMA_CTRL11	161
RMA_CTRL12	161
RMA_CTRL13	162
RMA_CTRL18	163
RMA_CTRL1A	163
RMA_CTRL20	164
RMA_CTRL21	165
RMA_CTRL22	165
RMA_CTRL_CDP	166
RMA_CTRL_SSTP	167
RMA_CFG	167
EEELDP_CTRL_0	168
EEELDP_CTRL_1	168
3.11 L2 MISC.	168
L2_SRC_PORT_PERMIT	168
L2_SRC_EXT_PERMIT	169
<b>4 NIC</b>	<b>171</b>
4.1 NIC & DMA	171
NIC_ID_CRTL0	171
NIC_ID_CRTL1	171
NIC_MC_CRTL0	171
NIC_MC_CRTL1	172
NIC_MIB0	172
NIC_MIB1	173
NIC_MIB2	173
NIC_MIB3	173
NIC_MIB4	174
NIC_MIB5	174
NIC_MIB6	174
NIC_STS	174
NIC_COM	175
NIC_INTR	175
NIC_IMR0_CFG	177
NIC_IMR1_CFG	178
NIC_ISR1_CFG	178
NIC_INT_ROUTE	179
NIC_TC	180
NIC_RC	181
NIC_CPUTAG	181
NIC_CONFIG	182
NIC_CPUTAG1	183
NIC_MS	183
NIC_MIIA	185
NIC_SWINT	186
NIC_VLAN	186
NIC_LED_CR	186
NIC_TXFPD1	187
NIC_TXCDO1	187
NIC_TXFDP2	187

NIC_TXCDO2	188
NIC_TXFDP3	188
NIC_TXCDO3	188
NIC_TXFDP4	188
NIC_TXCDO4	189
NIC_TXFDP5	189
NIC_TXCDO5	189
NIC_RRING_ROUTING1	190
NIC_RRING_ROUTING2	190
NIC_RRING_ROUTING3	191
NIC_RRING_ROUTING4	191
NIC_RRING_ROUTING5	192
NIC_RRING_ROUTING6	193
NIC_RXFDP2	193
NIC_RXCDORINGRS2	194
NIC_RX_CPU_DESN2	194
NIC_RX_DES_THRES2	194
NIC_RXFDP3	195
NIC_RXCDORINGRS3	195
NIC_RX_CPU_DESN3	196
NIC_RX_DES_THRES3	196
NIC_RXFDP4	196
NIC_RXCDORINGRS4	196
NIC_RX_CPU_DESN4	197
NIC_RX_DES_THRES4	197
NIC_RXFDP5	198
NIC_RXCDORINGRS5	198
NIC_RX_CPU_DESN5	198
NIC_RX_DES_THRES5	199
NIC_RXFDP6	199
NIC_RXCDORINGRS6	199
NIC_RX_CPU_DESN6	200
NIC_RX_DES_THRES6	200
NIC_RXFDP1	200
NIC_RXCDORINGRS1	201
NIC_SMSA	201
NIC_PROBE_SELECT	201
NIC_DIAGNOSE1	202
NIC_RX_PSE1_TXC_OUT_SEL1	202
NIC_ETNRXCPU1	203
NIC_ETN_IO_CMD	203
NIC_ETN_IO_CMD1	205
NIC_WOL	206

<b>5 Traffic Suppression</b>	<b>209</b>
5.1 STORM CONTROL (B/M/UM/DLF)	209
STORM_CTRL_UM_CTRL	209
STORM_CTRL_UC_CTRL	209
STORM_CTRL_MC_CTRL	210
STORM_CTRL_BC_CTRL	210
STORM_CTRL_UM_METER_IDX	210
STORM_CTRL_UC_METER_IDX	210
STORM_CTRL_MC_METER_IDX	211
STORM_CTRL_BC_METER_IDX	211
STORM_CTRL_ALT_TYPE_SEL	211
5.2 BANDWIDTH CONTROL (INGRESS/EGRESS)	212
IGR_BWCTRL_P_CTRL	212
IGR_BWCTRL_GLB_CTRL	213
5.3 METER MARKER	213
METER_TB_CTRL	213

METER_GLB_CTRL	213
METER_LB_EXCEED_STS	214
PON_TB_CTRL	214
METER_PKT_RATE	215
<b>6 Security</b>	<b>217</b>
6.1 802.1X	217
DOT1X_CFG_0	217
DOT1X_CFG_1	217
DOT1X_P_CTRL	218
6.2 DENIAL-OF-SERVICE ATTACK PREVENTION	218
DOS_EN	218
DOS_CFG	219
DOS_SYNFLOOD_TH	221
DOS_FINFLOOD_TH	221
DOS_ICMPFLOOD_TH	221
<b>7 Network Monitoring</b>	<b>223</b>
7.1 MIRRORING	223
MIR_CTRL	223
7.2 SFLOW	223
7.3 STATISTIC COUNTERS	224
STAT_PRIVATE_REASON	224
STAT_ACL_REASON	224
STAT_CF_REASON	224
STAT_PORT_TX_MIB	225
STAT_PORT_RX_MIB	227
STAT_PORT_OAM_MIB	230
STAT_BRIDGE_DOT1DTPLEARNEDENTRYDISCARDS	230
STAT_ACL_CNT	231
STAT_CTRL	231
STAT_ACL_CNT_MODE	231
STAT_ACL_CNT_TYPE	232
STAT_ACL_CNT_RST	232
STAT_PORT_RST	233
STAT_RST	233
OMCI_DROP_PKT_CNT	233
OMCI_TX_PKT_CNT	233
OMCI_RX_PKT_CNT	234
OMCI_TX_BYTE_CNT	234
OMCI_RX_BYTE_CNT	234
OMCI_CRC_ERROR_PKT_CNT	234
EPON_STAT_RST	235
DOT3_Q_TX_FRAMES	235
DOT3_MPCP_RX_DISC	236
DOT3_EPON_FEC_CORRECTED_BLOCKS	236
DOT3_EPON_FEC_UNCORRECTED_BLOCKS	236
DOT3_EPON_FEC_CODING_VIO	236
DOT3_NOT_BROADCAST_BIT_NOT_ONU_LLID	237
DOT3_BROADCAST_BIT_PLUS_ONU_LLID	237
DOT3_BROADCAST_NOT_ONUID	237
DOT3_CRC8_ERRORS	238
DOT3_LLID_RX_BROADCAST_DROP_FRAMES	238
DOT3_MPCP_TX_REPORT	238
DOT3_MPCP_EX_GATE	238
DOT3_ONUID_NOT_BROADCAST	239
STAT_DOT3_LLIDRXFRAMESDROP	239
DOT3_MPCP_TX_REG_REQ	239

<b>8</b>	<b>Buffer Management</b>	<b>241</b>
8.1	FLOWCONTROL & BACKPRESSURE THRESHOLD	241
	FC_CTRL	241
	FC_DROP_ALL_TH	241
	FC_PAUSE_ALL_TH	242
	FC_GLB_FCOFF_HI_TH	242
	FC_GLB_FCOFF_LO_TH	242
	FC_GLB_HI_TH	243
	FC_GLB_LO_TH	243
	FC_P_HI_TH	243
	FC_P_LO_TH	244
	FC_P_FCOFF_HI_TH	244
	FC_P_FCOFF_LO_TH	244
	FC_JUMBO_GLB_HI_TH	245
	FC_JUMBO_GLB_LO_TH	245
	FC_JUMBO_P_HI_TH	245
	FC_JUMBO_P_LO_TH	246
	FC_Q_EGR_DROP_TH	246
	FC_P_EGR_DROP_TH	246
	FC_Q_EGR_GAP_TH	247
	FC_P_EGR_GAP_TH	247
	FC_P_Q_EGR_DROP_EN	247
	FC_DBG_CTRL	248
	CLR_MAX_USED_PAGE_CNT	248
	FC_TOTAL_PAGE_CNT	248
	FC_PE_USED_PAGE_CNT	249
	FC_Q_USED_PAGE_CNT	249
	FC_TL_USED_PAGE_CNT	250
	FC_PUB_USED_PAGE_CNT	250
	FC_PUB_FCOFF_USED_PAGE_CNT	250
	FC_PUB_JUMBO_USED_PAGE_CNT	251
	FC_P_USED_PAGE_CNT	251
	FC_P_DBG_PKT_PAGE_CNT	251
	FC_PON_GLB_HI_TH	252
	FC_PON_GLB_LO_TH	252
	FC_PON_P_HI_TH	252
	FC_PON_P_LO_TH	253
	FC_PON_Q_EGR_DROP_IDX	253
	FC_PON_Q_EGR_DROP_TH	253
	FC_PON_Q_EGR_GAP_TH	254
	FC_PON_Q_USED_PAGE_CTRL	254
	FC_PON_Q_USED_PAGE_CNT	254
	TH_TX_PREFET	255
	LOW_QUEUE_TH	255
	HIGH_QUEUE_MSK	255
8.2	CONGESTION AVOIDANCE	256
	SC_P_CTRL_0	256
	SC_P_CTRL_1	256
8.3	PACKET AGING	257
<b>9</b>	<b>Quality of Service</b>	<b>259</b>
9.1	(IEEE802.1P) PRIORITY	259
9.2	QUEUE MANAGEMENT	259
	QOS_INTPRI_TO_QID	259
	QOS_PORT_QMAP_CTRL	259
	QOS_PRI_REMAP_IN_CPU	260
9.3	INGRESS PRIORITY DECISION	260
	QOS_1Q_PRI_REMAP	260
	QOS_DSCP_REMAP	260
	QOS_PB_PRI	261

	PRI_SEL_TBL_CTRL	261
	PRI_SEL_TBL_CTRL2	262
9.4	REMARKING	262
	RMK_DOT1Q_RMK_EN_CTRL	262
	RMK_1Q_CTRL	262
	RMK_DSCP_RMK_EN_CTRL	263
	RMK_DSCP_CTRL	263
	RMK_DSCP_INT_PRI_CTRL	263
	RMK_P_DSCP_SEL	264
9.5	SCHEDULING	264
	WFQ_CTRL	264
	EGR_BWCTRL_P_CTRL	265
	LINE_RATE_1G	265
	LINE_RATE_500M	265
	LINE_RATE_100M	266
	LINE_RATE_10M	266
	OUTPUT_DROP_CFG	266
	OUTPUT_DROP_EN	267
	WFQ_PORT_CFG0	267
	WFQ_PORT_CFG1_7	267
	WFQ_TYPE_PORT_CFG	268
	APR_EN_PORT_CFG	268
	CPU_PORT_RATE_CFG	268
	APR_METER_PORT_CFG	269
	P_QUEUE_EMPTY	269
	MOCIR_TH_H	269
	MOCIR_TH_L	270
	MOCIR_BPT	270
	MOCIR_FRC_MD	270
	MOCIR_FRC_VAL	270
	DBG_HSA_EP	271
<b>10</b>	<b>Packet Inspection Engine</b>	<b>273</b>
10.1	PIE TEMPLATE	273
	ACL_TEMPLATE_CTRL	273
10.2	FLOW CLASSIFICATION (FLOW TABLE)	273
	CF_OP_DS	273
	CF_OP_US	274
	CF_VALID	274
	CF_CFG	274
	RMK_DSCP_CF_PRI_CTRL	275
10.3	INGRESS ACL	275
	ACL_EN	275
	ACL_PERMIT	275
	ACL_ACTION	276
	ACL_CFG	276
10.4	RANGE CHECK (PORT/VLAN/IP/L4PORT)	277
	RNG_CHK_VID_RNG	277
	RNG_CHK_IP_RNG	277
	RNG_CHK_L4PORT_RNG	278
	RNG_CHK_PKTLEN_RNG	278
	RNG_CHK_IP_RNG_CF	279
	RNG_CHK_L4PORT_RNG_CF	279

<b>11 Management</b>	<b>281</b>
11.1 OAM	281
OAM_P_CTRL_0	281
OAM_P_CTRL_1	281
OAM_CTRL_0	282
OAM_CTRL_1	282
11.2 UDLD	282
11.3 RLDP & RLPP	283
RLDP_CTRL_0	283
RLDP_CTRL_1	283
RLDP_CHK_STS_CTRL	283
RLDP_LP_STS_CTRL	284
RLDP_RNDM_NUM	284
RLDP_MAGIC_NUM	284
RLDP_PORT_TX_EN	285
RLDP_PORT_LP_ENTER_STS	285
RLDP_PORT_LP_LEAVE_STS	285
RLDP_PORT_LP_STS	286
RLDP_PORT_CPU_LP_STS	286
RLDP_PORT_LP_PNUM	286
RLPP_CTRL	287
11.4 CODE PROTECTION	287
<b>12 Private</b>	<b>289</b>
12.1 PARSER HSB	289
HSB_CTRL	289
HSB_DATA	289
HSB_DATA_TABLE	290
12.2 HSM	292
12.3 MODIFIER HSA	292
HSA_DATA	292
HSA_DATA_NAT	292
HSA_DATA_TABLE	294
12.4 DEBUGGING (ALE, LOOPBACK, DROP MECHANISM, FC AND QM)	295
DBG_BLK_SEL	295
PORT_VM_EN	295
PORT_VM_RX	296
PORT_VM_TX	296
12.5 SMART PACKET GENERATOR	297
SPG_GLB_CTRL	297
SPG_PORT_TX_GRP_CTRL	297
SPG_PORT_STS	297
SPG_P_TX_GRP_CTRL	298
SPG_P_LEN_CTRL	299
SPG_P_TX_CNT	299
SPG_P_SA	300
SPG_P_DA	300
SPG_PAYLOAD	300
SPG_PORT_USER_PKT	301
<b>13 Layer 3</b>	<b>303</b>
13.1 L3 ROUTING	303
13.2 IGMP SNOOPING	303
IGMP_MC_GROUP	303
IGMP_GLB_CTRL	303
IGMP_P_CTRL	304
13.3 L3 MISC	305
L34_GLB_CFG	305
L34_IPMC_TRAN_TBL	305
L34_IPMC_TTL_CFG	306



L34_PORT_TO_WAN	306
L34_EXTPORT_TO_WAN	307
L34_WAN_TO_PORT	307
L34_WAN_TO_EXTPORT	307
<b>14 Table Access</b>	<b>309</b>
14.1 TABLE ACCESS	309
TBL_ACCESS_CTRL	309
TBL_ACCESS_STS	310
TBL_ACCESS_WR_DATA	310
TBL_ACCESS_RD_DATA	310
ACL_ACTION_TABLE	311
ACL_DATA	312
ACL_DATA2	312
ACL_MASK	313
ACL_MASK2	314
CF_ACTION_DS	314
CF_ACTION_US	315
CF_MASK	316
CF_MASK_L34	318
CF_RULE	319
CF_RULE_L34	320
L2_MC_DSL	322
L2_UC	322
L3_MC_DSL	323
L3_MC_ROUTE	324
VLAN	324
<b>15 Miscellaneous</b>	<b>327</b>
15.1 SPECIAL TRAP	327
15.2 ETHERNET AV	327
AVB_PORT_EN	327
AVB_PRI_REMAP	327
15.3 PTP (PRECISION TIME PROTOCOL)	328
PTP_TIME_SEC	328
PTP_TIME_NSEC	328
PTP_TIME_OFFSET_SEC	328
PTP_TIME_OFFSET_8NSEC	329
PTP_TIME_FREQ	329
PTP_TIME_CTRL	329
PTP_TRANSPARENT_CFG	329
PTP_IGR_MSG_ACT	330
PTP_EGR_MSG_ACT	330
PTP_MEANPATH_DEALY	331
PTP_RX_TIME	331
PTP_P_EN	331
15.4 PARSER	332
PARSER_FIELD_SELTOR_CTRL	332
<b>16 PON MAC</b>	<b>333</b>
16.1 PON MAC SCHEDULING CONFIG	333
PON_CFG	333
PON_SID_TO_QID	333
PON_QID_CIR_RATE	333
PON_QID_PIR_RATE	334
PON_SCH_QMAP	334
PON_WFQ_WEIGHT	334
PON_WFQ_TYPE	335
FC_PON_Q_EGR_DROP_EN	335
PON_TCONT_EN	335

QUEUE_SEL_IND	336
QUEUE_SEL_IND_DATA	336
GPON_DPRU_RPT_PRD	336
PON_PIR_CIR_IFG	337
PON_PORT_CTRL	337
PONMAC_DRN_CTRL	337
PON_OLT_BW_MTR_FULL	337
PON_WFQ_IFG_CTRL	338
<b>17 GPON MAC</b>	<b>339</b>
17.1 GPON MAC GENERAL CONFIG	339
GPON_INT_DLT	339
GPON_RESET	339
GPON_VERSION	340
GPON_TEST	340
GPON_AES_BYPASS	340
GPON_INTR_MASK	341
GPON_INTR_STS	341
17.2 GTC DOWNSTREAM	342
GPON_GTC_DS_INTR_DLT	342
GPON_GTC_DS_INTR_MASK	343
GPON_GTC_DS_INTR_STS	343
GPON_GTC_DS_ONU_ID_STATUS	344
GPON_GTC_DS_CFG	344
GPON_GTC_DS_PLOAM_CFG	345
GPON_GTC_DS_LOS_CFG_STS	345
GPON_GTC_DS_SUPERFRAME_CNT	346
GPON_GTC_DS_PLOAM_IND	346
GPON_GTC_DS_PLOAM_MSG	347
GPON_GTC_DS_ALLOC_IND	347
GPON_GTC_DS_ALLOC_WR	348
GPON_GTC_DS_ALLOC_RD	348
GPON_GTC_DS_PORT_IND	348
GPON_GTC_DS_PORT_WR	349
GPON_GTC_DS_PORT_RD	349
GPON_GTC_DS_PORT_CNTR_IND	350
GPON_GTC_DS_PORT_CNTR_STAT	350
GPON_GTC_DS_MISC_CNTR_BIP_ERR_BLK	351
GPON_GTC_DS_MISC_CNTR_BIP_ERR_BIT	351
GPON_GTC_DS_MISC_CNTR_FEC_CORRECT_BIT	351
GPON_GTC_DS_MISC_CNTR_FEC_CORRECT_BYTE	351
GPON_GTC_DS_MISC_CNTR_FEC_CORRECT_CW	352
GPON_GTC_DS_MISC_CNTR_FEC_UNCOR_CW	352
GPON_GTC_DS_MISC_CNTR_LOM	352
GPON_GTC_DS_MISC_CNTR_PLOAM_ACPT	352
GPON_GTC_DS_MISC_CNTR_PLOAM_FAIL	353
GPON_GTC_DS_MISC_CNTR_BWM_FAIL	353
GPON_GTC_DS_MISC_CNTR_BWM_INV	353
GPON_GTC_DS_MISC_CNTR_ACTIVE	354
GPON_GTC_DS_MISC_CNTR_BWM_ACPT	354
GPON_GTC_DS_MISC_CNTR_GEM_LOS	354
GPON_GTC_DS_MISC_CNTR_HEC_CORRECT	355
GPON_GTC_DS_MISC_CNTR_GEM_IDLE	355
GPON_GTC_DS_MISC_CNTR_GEM_FAIL	355
GPON_GTC_DS_MISC_CNTR_GEM_NON_IDLE	355
GPON_GTC_DS_MISC_CNTR_PLEN_CORRECT	356
GPON_GTC_DS_OMCI_PTI	356
GPON_GTC_DS_ETH_PTI	356
GPON_GTC_DS_TRAFFIC_CFG	357
17.3 BWMAP CAPTURE	357

GPON_BWMAP_CTRL	357
GPON_BWMAP_STS	358
GPON_BWMAP_DATA	358
17.4 AES DECRYPT	358
GPON_AES_INTR_DLT	358
GPON_AES_INTR_MASK	359
GPON_AES_INTR_STS	359
GPON_AES_KEY_SWITCH_REQ	359
GPON_AES_KEY_SWITCH_TIME	360
GPON_AES_KEY_WORD_IND	360
GPON_AES_WORD_DATA	361
17.5 GEM PORT DOWNSTREAM	361
GPON_GEM_DS_RX_CNTR_IND	361
GPON_GEM_DS_RX_CNTR_STAT	362
GPON_GEM_DS_FWD_CNTR_IND	362
GPON_GEM_DS_FWD_CNTR_STAT	362
GPON_GEM_DS_MISC_IND	363
GPON_GEM_DS_MISC_CNTR_STAT	363
GPON_GEM_DS_MC_CFG	363
GPON_GEM_DS_MC_IND	364
GPON_GEM_DS_MC_WR	365
GPON_GEM_DS_MC_RD	365
GPON_GEM_DS_FRM_TIMEOUT	365
GPON_GEM_DS_MC_ADDR_PTN_IPV4	365
GPON_GEM_DS_MC_ADDR_PTN_IPV6	366
17.6 GTC UPSTREAM	366
GPON_GTC_US_INTR_DLT	366
GPON_GTC_US_INTR_MASK	367
GPON_GTC_US_INTR_STS	367
GPON_GTC_US_ONU_ID	368
GPON_GTC_US_CFG	368
GPON_GTC_US_WRITE_PROTECT	369
GPON_GTC_US_TX_PATTERN_CTL	369
GPON_GTC_US_TX_PATTERN_BG	369
GPON_GTC_US_TX_PATTERN_FG	370
GPON_GTC_US_MIN_DELAY	370
GPON_GTC_US_EQD	370
GPON_GTC_US_LASER	371
GPON_GTC_US_BOH_CFG	371
GPON_GTC_US_BOH_DATA	371
GPON_GTC_US_PLOAM_IND	372
GPON_GTC_US_PLOAM_DATA	373
GPON_GTC_US_PLOAM_CFG	373
GPON_GTC_US_MISC_CNTR_IDX	374
GPON_GTC_US_MISC_CNTR_STAT	374
GPON_GTC_US_RDI	374
GPON_GTC_US_DG	374
GPON_GTC_US_OPTIC_SD_TH	375
GPON_GTC_US_PROC_MODE	375
17.7 GEM UPSTREAM	375
GPON_GEM_US_INTR_DLT	375
GPON_GEM_US_INTR_MASK	376
GPON_GEM_US_INTR_STS	377
GPON_GEM_US_PTI_CFG	378
GPON_GEM_US_ETH_GEM_RX_CNTR_IDX	379
GPON_GEM_US_ETH_GEM_RX_CNTR_STAT	379
GPON_GEM_US_PTN_CTRL	379
GPON_GEM_US_PORT_MAP	380
GPON_GEM_US_BYTE_STAT	380
TCONT_IDLE_BYTE_STAT	381

<b>18 EPON MAC</b>	<b>383</b>
18.1 EPON CONFIGURATION	383
EPON_FEC_CONFIG	383
EPON_ASIC_TIMING_ADJUST1	383
EPON_ASIC_TIMING_ADJUST2	384
EPON_RGSTR1	384
EPON_RGSTR2	385
EPON_RGSTR3	385
EPON_DEBUG1	385
EPON_DEBUG2	386
EPON_TIMER_CONFIG1	386
EPON_INTR	386
SYNC_TIME	387
LASER_ON_OFF_TIME	387
MIN_GRANT_START	387
MAX_GRANT_START	388
EPON_TIME_CTRL	388
EP_MISC	388
LLID_TABLE	389
EPON_MPCP_CTR	389
EPON_GRANT_LIST0	390
EPON_GRANT_LIST1	390
EPON_GRANT_LIST2	390
EPON_TX_CTRL	391
<b>19 NAT</b>	<b>393</b>
19.1 TABLE ACCESS	393
NAT_TBL_ACCESS_CTRL	393
NAT_TBL_ACCESS_CLR	394
NAT_TBL_ACCESS_RDDATA	396
NAT_TBL_ACCESS_WRDATA	396
ARP_TABLE	396
BINDING_TABLE	396
EXTERNAL_IP_TABLE	397
IPV6_ROUTING_TABLE	398
L3_ROUTING_DROP_TRAP	398
L3_ROUTING_GLOBAL_ROUTE	399
L3_ROUTING_LOCAL_ROUTE	400
NAPT_TABLE	401
NAPTR_TABLE	401
NEIGHBOR_TABLE	402
NETIF	402
NEXT_HOP_TABLE	403
PPPOE_TABLE	403
WAN_TYPE_TABLE	404
19.2 ALE AND TM FOR L3L4	404
NIFP	404
NIFEP	404
NIFVCH	405
NIFVCL	405
SWTCR0	406
PP_AGE	408
NB_TRF	408
V6_BD_CTL	409
BD_TRF	409
BD_CFG	409
19.3 NAT HSB HAS	411
HSBA_CTRL	411
HSB_DESC	411
HSA_DESC	412

L34_HSA	412
L34_HSB	414
19.4 L4 TRAFFIC TABLE0	415
L4_TRF0	415
L4_TRF1	415
ARP_TRF0	416
ARP_TRF1	416
<b>20 TEMP Register</b>	<b>419</b>
20.1 TEMP REGISTER	419
RGF_VER_GLB_CTRL	419
RGF_VER_ALE_GLB	419
RGF_VER_ALE_ACL	419
RGF_VER_ALE_CVLAN	420
RGF_VER_ALE_DPM	420
RGF_VER_ALE_L2	420
RGF_VER_ALE_MLTVLAN	420
RGF_VER_ALE_SVLAN	421
RGF_VER_ALE_EEE_LLDP	421
RGF_VER_ALE_RLDP	421
RGF_VER_ALE_EAV_AFBK	421
RGF_VER_INTR	422
RGF_VER_LED	422
RGF_VER_PER_PORT_MAC	422
RGF_VER_SDSREG	422
RGF_VER_SWCORE	423
RGF_VER_EPON_CTRL	423
RGF_VER_ALE_RMA_ATTACK	423
RGF_VER_BIST_CTRL	423
RGF_VER_EGR_OUTQ	424
RGF_VER_EGR_SCH	424
RGF_VER_ALE_HSA	424
RGF_VER_ALE_METER	424
RGF_VER_MIB_CTRL	425
RGF_VER_ALE_PISO	425
RSVD_GLB_CTRL	425
RSVD_ALE_GLB	426
RSVD_ALE_ACL	426
RSVD_ALE_CVLAN	426
RSVD_ALE_DPM	427
RSVD_ALE_L2	427
RSVD_ALE_MLTVLAN	427
RSVD_ALE_SVLAN	428
RSVD_ALE_EEE_LLDP	428
RSVD_ALE_RLDP	428
RSVD_ALE_EAV_AFBK	428
RSVD_INTR	429
RSVD_LED	429
RSVD_PER_PORT_MAC	429
RSVD_SDSREG	430
RSVD_SWCORE	430
RSVD_EPON_CTRL	430
RSVD_ALE_RMA_ATTACK	431
RSVD_BIST_CTRL	431
RSVD_EGR_OUTQ	431
RSVD_EGR_SCH	432
RSVD_ALE_HSA	432
RSVD_ALE_METER	432
RSVD_MIB_CTRL	433
RSVD_ALE_PISO	433

HSA_TX_DBG . . . . .	433
BYTE_TOKEN_METER . . . . .	434
HSARAM_5_CFG . . . . .	434
DBG_EP_CFG . . . . .	434
TRUNK_DROP_CFG . . . . .	434
PAUSE_ALL_LW_CFG . . . . .	435
HYS_PUSAL_CFG . . . . .	435
EPON_DECRYPT_CFG . . . . .	435
EPON_DECRYPT_KEY0 . . . . .	435
EPON_DECRYPT_KEY1 . . . . .	436
EPON_MISC_CFG . . . . .	436
CHANGE_DUPLEX_CTRL . . . . .	436
RLDP_BUZZER . . . . .	437
PON_LED_CFG . . . . .	437
FB_GPHY_ADDR_CTRL . . . . .	437
HSA_DEBUG_DATA . . . . .	437

## **Index: Alphabetical List 441**

A . . . . .	441
B . . . . .	441
C . . . . .	442
D . . . . .	443
E . . . . .	444
F . . . . .	446
G . . . . .	448
H . . . . .	451
I . . . . .	451
L . . . . .	452
M . . . . .	453
N . . . . .	454
O . . . . .	456
P . . . . .	457
Q . . . . .	458
R . . . . .	459
S . . . . .	461
T . . . . .	464
U . . . . .	464
V . . . . .	465
W . . . . .	465

## **Appendix A: Hardware Block View 469**

GLB_CTRL . . . . .	469
RESERVED . . . . .	471
CHIP_INFO . . . . .	471
ALE_GLB . . . . .	471
ALE_TABLE . . . . .	472
ALE_CVLAN . . . . .	472
ALE_SVLAN . . . . .	473
ALE_ACL . . . . .	473
RESERVED . . . . .	473
ALE_L2 . . . . .	474
ALE_MLTVLAN . . . . .	474
ALE_EEE_LLDP . . . . .	474
ALE_RLDP . . . . .	475
ALE_EAV_AFBK . . . . .	475
ALE_DPM . . . . .	476
INTR . . . . .	477
LED . . . . .	477
RESERVED . . . . .	478
PER_PORT_MAC . . . . .	478

RESERVED	479
SDSREG	479
SDS_IP	481
SWCORE	484
RESERVED	486
ALE_METER	486
ALE_RMA_ATTACK	486
ALE_PISO	487
ALE_HSB	487
ALE_HSM	487
ALE_HSA	487
ALE_DEBUG	488
ALE_PKTGEN	488
EGR_OUTQ	488
EGR_SCH	489
PKT_ENCAP	489
PKT_PARSER	490
CFM_GEN	490
BIST_CTRL	490
MIB_DATA	491
MIB_CTRL	491
MAC_PON	492
EPON_CTRL	492
TBD	493
RESERVED	493
GPON_PAGE0	493
GPON_PAGE1	493
GPON_PAGE2	494
GPON_PAGE3	494
GPON_PAGE4	495
GPON_PAGE5	495
GPON_PAGE6	496
NIC	496
NIC_DMA	497
NAT_CTRL	498
NAT_INDIR	499
NAT_HSBA	499
NAT_L4_TRF0	499
NAT_L4_TRF1	499
NAT_ARP_TRF0	499
NAT_ARP_TRF1	500

<b>Appendix B: Switch Feature View</b>	<b>501</b>
Interface	501
Reset	501
Interrupt	502
BIST & BISR	502
CPU relative	503
LED	503
HW Misc.	503
Chp Information	503
MAC Control	505
PHY & Serdes	505
RTCT	510
Power Saving	510
Auto Fallback	511
Address Table Lookup	511
Address Learning & Flush	512
L2 & IP Multicast	512
(IEEE802.1Q) VLAN	512

(IEEE802.1ad) Provider Bridges/Q-in-Q	513
(IEEE802.1v) Protocol-based VLAN	513
Link Aggregation	513
Spanning Tree	513
Port Isolation	514
RMA	514
L2 Misc.	514
NIC & DMA	515
Storm Control (B/M/UM/DLF)	517
Bandwidth Control (Ingress/Egress)	517
Meter Marker	517
802.1X	517
Denial-of-service attack prevention	517
Mirroring	518
sFlow	518
Statistic Counters	518
Flowcontrol & Backpressure Threshold	519
Congestion Avoidance	520
Packet Aging	520
(IEEE802.1p) Priority	521
Queue Management	521
Ingress Priority Decision	521
Remarking	521
Scheduling	521
PIE Template	522
Flow Classification (Flow Table)	522
Ingress ACL	523
Range Check (port/vlan/ip/L4port)	523
OAM	523
UDLD	523
RLDP & RLPP	523
Code Protection	524
Parser HSB	524
HSM	524
Modifier HSA	524
Debugging (ALE, Loopback, Drop Mechanism, FC and QM)	525
Smart Packet Generator	525
L3 Routing	525
IGMP snooping	525
L3 Misc	526
Table Access	526
Special Trap	526
Ethernet AV	527
PTP (Precision Time Protocol)	527
Parser	527
PON MAC Scheduling Config	527
GPON MAC General Config	528
GTC Downstream	528
BWMAP Capture	529
AES Decrypt	530
GEM Port Downstream	530
GTC Upstream	530
GEM Upstream	531
EPON Configuration	531
Table Access	532
ALE and TM for L3L4	533
NAT HSB HAS	533
L4 Traffic Table0	533
Temp Register	533



<b>Appendix C: Memory Map</b>	<b>537</b>
0xBB000000 . . . . .	537



## CHAPTER 1

# Hardware

The chapter describes features related to hardware components

### SECTION 1.1

## INTERFACE

Module for chip interface

### DIGITAL\_INTERFACE\_SELECT

REGISTER ADDRESS : 0xBB023000

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:2	RESERVED			
1	ORG_COL	NOT NEED simulation	RW	0x0
0	ORG_CRS	NOT NEED simulation	RW	0x0

### SKIP\_MII\_RXER

REGISTER ADDRESS : 0xBB000000

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	SKIP_MII_RXER	skip MII_rxer	RW	0x0

### EXT\_RGMXF

REGISTER ADDRESS : 0xBB000004

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:9	RESERVED			

Bits	Field	Description	Type	Default
8	EXT_RGMXF_SELPLL	1: RGMXF 250M is from GPHY PLL 0: RGMXF 250M is from SOC PLL	RW	0x0
7	EXT_RGMXF_PLLDLY	1: ext RGMXF 250M PLL with delay 0: without delay	RW	0x0
6	EXT_RGTKX_INV	ext RGMXF invert gtxc	RW	0x0
5	EXT_RGRX_INV	ext RGMXF invert grxc	RW	0x0
4:0	EXT_RGMXF	ext RGMXF configuration 4: select RTBI, 3: TXC delay 2ns, 2:0: delay cell used in rgmrxc	RW	0x0

## I2C\_CLOCK\_DIV

BASE ADDRESS : 0xBB023004  
 ARRAY INDEX : 0 - 1  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0xF9

This is a One-Dimension Common Register Array.

Bits	Field	Description	Type	Default
31:19	RESERVED			
18:12	I2C_DEV_ID	i2c device ID	RW	0x0
11	I2C_AW	i2c addr width, 0 - 8bits address, 1 - 16bits address	RW	0x0
10	I2C_DW	i2c data width, 0 - 8bits data, 1 - 16bits data	RW	0x0
9:0	I2C_CLOCK_DIV	125KHz for default ( 125MHz / (((2*I2C_CLOCK_DIV)+2)*2) )	RW	0x0F9

## EXT\_TXC\_DLY

REGISTER ADDRESS : 0xBB000008  
 DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:3	EXT_GMII_TX_DELAY	GMII delay	RW	0x0
2:0	EXT_RGMII_TX_DELAY	RGMII txc delay	RW	0x0

## GPHY\_IND\_WD

REGISTER ADDRESS : 0xBB00000C  
 DEFAULT VALUE : 0x0

GPHY indirect write data

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	WR_DAT	16-bit data write to gphy's register	RW	0x0

## GPHY\_IND\_CMD

REGISTER ADDRESS : 0xBB000010

DEFAULT VALUE : 0x0

GPHY indirect command and address

Bits	Field	Description	Type	Default
31:23	RESERVED			
22	WREN	write enable. 0: read, 1: write	RW	0x0
21	CMD_EN	command enable and auto clear. Check the BUSY bit to make sure the command is done.	RWAC	0x0
20:0	ADR	read/write address {20:16}=phyid; {15:0}=reg address	RW	0x0

## GPHY\_IND\_RD

REGISTER ADDRESS : 0xBB000014

DEFAULT VALUE : 0x0

GPHY indirect read data

Bits	Field	Description	Type	Default
31:17	RESERVED			
16	BUSY	1: busy, read/write command is not finish.	RO	0x0
15:0	RD_DAT	16-bit data read from gphy	RO	0x0

## EFUSE\_CFG

REGISTER ADDRESS : 0xBB000018

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:2	RESERVED			
1:0	EFUSE_TMRF	efuse config	RW	0x0

## EFUSE\_IND\_WD

REGISTER ADDRESS : 0xBB00001C

DEFAULT VALUE : 0x0

eFuse indirect write data

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	WR_DAT	write data.	RW	0x0

## EFUSE\_IND\_CMD

REGISTER ADDRESS : 0xBB000020

DEFAULT VALUE : 0x0

eFuse indirect command and address

Bits	Field	Description	Type	Default
31:18	RESERVED			
17	WREN	write enable. 0: read, 1: write	RW	0x0
16	CMD_EN	command enable and auto clear. Check the BUSY bit to make sure the command is done.	RWAC	0x0
15:0	ADR	read/write address	RW	0x0

## EFUSE\_IND\_RD

REGISTER ADDRESS : 0xBB000024

DEFAULT VALUE : 0x0

eFuse indirect read data

Bits	Field	Description	Type	Default
31:17	RESERVED			
16	BUSY	1: busy, read/write command is not finish.	RO	0x0

Bits	Field	Description	Type	Default
15:0	RD_DAT	read data	RO	0x0

## I2C\_IND\_WD

BASE ADDRESS : 0xBB000028  
 ARRAY INDEX : 0 - 1  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

I2C master indirect write data

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	WR_DAT	16-bit data for I2C master write command	RW	0x0

## I2C\_IND\_CMD

BASE ADDRESS : 0xBB000030  
 ARRAY INDEX : 0 - 1  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

I2C master indirect command and address

Bits	Field	Description	Type	Default
31:18	RESERVED			
17	WREN	write enable. 0: read, 1: write	RW	0x0
16	CMD_EN	command enable and auto clear. Check the BUSY bit to make sure the command is done.	RWAC	0x0
15:0	ADR	read/write address	RW	0x0

## I2C\_IND\_RD

BASE ADDRESS : 0xBB000038  
 ARRAY INDEX : 0 - 1  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

I2C master indirect read data

Bits	Field	Description	Type	Default
31:17	RESERVED			
16	BUSY	1: busy, read/write command is not finish.	RO	0x0
15:0	RD_DAT	16-bit data which read via I2C master	RO	0x0

## REGCTRL\_GLB

REGISTER ADDRESS : 0xBB02300C

DEFAULT VALUE : 0x1FFFFFFF

GPHY's ocp timeout (unit:8ns)

Bits	Field	Description	Type	Default
31:30	RESERVED			
29:25	PHY_OCP_TOF	flag indicate that gphy access failed by OCP (per GPHY)	RO	0x0
24:17	PHY_OCP_TO	Timeout setting for GPHY access via OCP (unit:16ns), default is 4096ns	RW	0xFF
16:1	PHY_ACK_TO	Timeout setting for GPHY access via SMI (unit: 8192ns), default is 537us	RW	0xFFFF
0	SMI_EN	1: regctrl arbiter only for lx_slv & afbk 0: else	RW	0x1

## IOPAD\_CFG

REGISTER ADDRESS : 0xBB023010

DEFAULT VALUE : 0x0

IO pad config for dirving, slew rate, and DP, DN, 3.3V for RGMII

Bits	Field	Description	Type	Default
31:27	RESERVED			
26:24	RGM_DP	adjust PMOS resistance for RGMII TX PAD which is inverse proportion to this setting.	RW	0x0
23:21	RGM_DN	adjust NMOS resistance for RGMII TX PAD which is inverse proportion to this setting.	RW	0x0
20	RGM_SEL33	1: 3.3v RGMII PAD	RW	0x0
19	DRI_LED	1: high dirving	RW	0x0
18	DRI_EXCK	1: high dirving	RW	0x0
17	DRI_EXDT	1: high dirving	RW	0x0



Bits	Field	Description	Type	Default
16	DRI_IFCK	1: high dirving	RW	0x0
15	DRI_IFDT	1: low slew rate	RW	0x0
14	DRI_SLIC_CK	1: high dirving	RW	0x0
13	DRI_SLIC_DT	1: high dirving	RW	0x0
12	DRI_SPI_CK	1: high dirving	RW	0x0
11	DRI_SPI_DT	1: high dirving	RW	0x0
10	DRI_OTH	1: high dirving	RW	0x0
9	SR_EXCK	1: low slew rate	RW	0x0
8	SR_EXDT	1: low slew rate	RW	0x0
7	SR_IFCK	1: low slew rate	RW	0x0
6	SR_IFDT	1: low slew rate	RW	0x0
5	SR_SLIC_CK	1: low slew rate	RW	0x0
4	SR_SLIC_DT	1: low slew rate	RW	0x0
3	SR_LED	1: low slew rate	RW	0x0
2	SR_SPI_CK	1: low slew rate	RW	0x0
1	SR_SPI_DT	1: low slew rate	RW	0x0
0	SR_OTH	1: low slew rate	RW	0x0

## IO\_LED\_EN

REGISTER ADDRESS : 0xBB023014

DEFAULT VALUE : 0x0

Enable LED IO

Bits	Field	Description	Type	Default
31:20	RESERVED			
19:18	EXT_USBLED_EN		RW	0x0
17	SERI_LED_EN		RW	0x0
16:7	PARA_LED_EN		RW	0x0
6:5	EXTLED_EN		RW	0x0
4:3	PONLED_EN		RW	0x0
2	SATALED_EN		RW	0x0
1:0	USBLED_EN		RW	0x0

## IO\_MODE\_EN

REGISTER ADDRESS : 0xBB023018

DEFAULT VALUE : 0x60000

Enable interface IO

Bits	Field	Description	Type	Default
31:24	RESERVED			
23	PTP_IO_EN		RW	0x0
22	NFBI_EN		RW	0x0
21	EXT_INTRPT_EN		RW	0x0
20:19	OEM_EN	bit 1: enable GPONPPS bit 0: enable DIS_TX, TX_SD and ToD	RW	0x0
18	SLIC_PCM_EN		RW	0x1
17	SLIC_SPI_EN		RW	0x1
16	SLIC_ZSI_EN		RW	0x0
15	SLIC_ISI_EN		RW	0x0
14:13	I2C_EN		RW	0x0
12:11	INTRPT_EN		RW	0x0
10:9	MDX_M_EN		RW	0x0
8	MDX_S_EN		RW	0x0
7	SATA_MDC_EN		RW	0x0
6	SPI_EN		RW	0x0
5:3	UART_EN		RW	0x0
2:1	SIO_EN		RW	0x0
0	RESERVED			

## CFG\_PCSXF

REGISTER ADDRESS : 0xBB000040

DEFAULT VALUE : 0x0

### CFG\_PCSXF

Bits	Field	Description	Type	Default
31:10	RESERVED			
9:6	CFG_PCSXF	bit 9: sel_org_crs bit 8: sel_org_col bit 7: reserved (phy mode) bit 6: skip rxer	RW	0x0
5:1	RST_RXFIFO	reset rx sync. fifo. 1: reset, 0: normal	RW	0x0
0	COL_10M	assert rxdv when col asserts in half-dup and 10M	RW	0x0

## CFG\_PHY\_CTRL

REGISTER ADDRESS : 0xBB000044

DEFAULT VALUE : 0x0

Config for phyad and broadcast mode

Bits	Field	Description	Type	Default
31:11	RESERVED			
10:6	MSK_MDI	mask the specific gphy's mdi	RW	0x0
5:1	BASE_PHYAD	start phyad for SMI. phy0_ad=N, phy1_ad=N+1, , phy4_ad=N+4	RW	0x0
0	BYPS_PDPHY	1: dont disable rg_pwrn(0.11) when pow-on	RW	0x0

## CFG\_PHY\_POLL\_CMD

REGISTER ADDRESS : 0xBB000048

DEFAULT VALUE : 0xB110

CFG\_PHY\_POLL\_CMD

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	HOTCMD_PRD_EN	1: The hot command will be also excuted periodically. The hot command is e.g. eeep tx/rx.	RW	0x1
14:12	HOTCMD_EN	Enable hot command. Bit 14: reserved Bit 13: auto power on gphy (rg0.11) Bit 12: HW will transfer the eeep tx/rx to OCP cmd.	RW	0x3
11:8	CMD_PRD	The period of HW polling GPHY ability (unit: 100us)	RW	0x1
7:4	CMD_RD_EN	periodic read cmds. [4]: ability, else reserved	RW	0x1
3:0	CMD_WR_EN	periodic write cmds. all reserved.	RW	0x0

## CFG\_PHY\_POLL\_ADR\_0

REGISTER ADDRESS : 0xBB00004C

DEFAULT VALUE : 0xA4340000

CFG\_PHY\_POLL\_ADR\_0

Bits	Field	Description	Type	Default
31:16	CMD0_ADR	reg address for periodic cmd0	RW	0xA434
15:0	CMD1_ADR	reg address for periodic cmd1	RW	0x0

**CFG\_PHY\_POLL\_ADR\_1**

REGISTER ADDRESS : 0xBB000050

DEFAULT VALUE : 0x0

CFG\_PHY\_POLL\_ADR\_1

Bits	Field	Description	Type	Default
31:16	CMD2_ADR	reg address for periodic cmd2	RW	0x0
15:0	CMD3_ADR	reg address for periodic cmd3	RW	0x0

**CFG\_PHY\_POLL\_INV\_0**

REGISTER ADDRESS : 0xBB000054

DEFAULT VALUE : 0x0

CFG\_PHY\_POLL\_INV\_0

Bits	Field	Description	Type	Default
31:16	CMD0_INV	invert the read data for periodic cmd0	RW	0x0
15:0	CMD1_INV	invert the read data for periodic cmd1	RW	0x0

**CFG\_PHY\_POLL\_INV\_1**

REGISTER ADDRESS : 0xBB000058

DEFAULT VALUE : 0x0

CFG\_PHY\_POLL\_INV\_1

Bits	Field	Description	Type	Default
31:16	CMD2_INV	invert the read data for periodic cmd2	RW	0x0
15:0	CMD3_INV	invert the read data for periodic cmd3	RW	0x0

**CFG\_PHY\_POLL\_WD\_0**

REGISTER ADDRESS : 0xBB00005C

DEFAULT VALUE : 0x0

CFG\_PHY\_POLL\_WD\_0

Bits	Field	Description	Type	Default
31:16	CMD0_WDAT	write data for periodic cmd0	RW	0x0
15:0	CMD1_WDAT	write data for periodic cmd1	RW	0x0

## CFG\_PHY\_POLL\_WD\_1

REGISTER ADDRESS : 0xBB000060

DEFAULT VALUE : 0x0

### CFG\_PHY\_POLL\_WD\_1

Bits	Field	Description	Type	Default
31:16	CMD2_WDAT	write data for periodic cmd2	RW	0x0
15:0	CMD3_WDAT	write data for periodic cmd3	RW	0x0

## CHIP\_DEBUG\_OUT

REGISTER ADDRESS : 0xBB000064

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	DBG0		RO	0x0

## SECTION 1.2

# RESET

Reset module

## CHIP\_RST

REGISTER ADDRESS : 0xBB000068

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	DUMMY		RW	0x0

## SOFTWARE\_RST

REGISTER ADDRESS : 0xBB00006C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:7	RESERVED			
6	PONMAC_RST	PON MAC software reset Register configurable. 0b0: disable. 0b1: enable.	RWAC	0x0
5	SW_RST	Switch global software reset. Register configurable. 0b0: normal 0b1: reset Note: write 0b1 and self-clear to 0b0.	RWAC	0x0
4	CMD_SWSYS_RST_PS		RWAC	0x0
3	CMD_CFG_RST_PS		RWAC	0x0
2	CMD_CHIP_RST_PS		RWAC	0x0
1	CMD_GPHY_RST_PS		RWAC	0x0
0	CMD_SDS_RST_PS		RWAC	0x0

## SECTION 1.3

## INTERRUPT

Interrupt module

### INTR\_CTRL

REGISTER ADDRESS : 0xBB01D000

DEFAULT VALUE : 0x0

Global switch interrupt control register

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	INTR_POLARITY	Interrupt active polarity while triggered 0:pull high 1:pull low	RW	0x0

### INTR\_IMR

REGISTER ADDRESS : 0xBB01D004

DEFAULT VALUE : 0x0

Switch interrupt mask register.

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	IMR_ADC_ALARM	IMR ADC alarm	RW	0x0
14	IMR_THERMAL_ALARM	IMR thermal alarm	RW	0x0
13	IMR_DYING_GASP	IMR dying gasp	RW	0x0

Bits	Field	Description	Type	Default
12	IMR_PTP	IMR PTP egress event	RW	0x0
11	IMR_EPON	IMR EPON event	RW	0x0
10	IMR_GPON	IMR GPON event	RW	0x0
9	IMR_SERDES	IMR serdes interrupt	RW	0x0
8	IMR_GPHY	IMR for GPHY interrupt	RW	0x0
7	IMR_ACL	IMR for ACL interrupt	RW	0x0
6	IMR_RTCT	IMR for Cable Diag finish	RW	0x0
5	IMR_LOOP	IMR for have loop detected or loop recoved situation happen	RW	0x0
4	IMR_SPE_CONGEST	IMR for TX special congest	RW	0x0
3	IMR_SPE_CHG	IMR for speed change	RW	0x0
2	IMR_L2_LRN_OVER	IMR for L2 learn over	RW	0x0
1	IMR_METER_EXCEED	IMR for meter exceed	RW	0x0
0	IMR_LINK_CHG	IMR for link change	RW	0x0

## INTR\_IMS

REGISTER ADDRESS : 0xBB01D008

DEFAULT VALUE : 0x0

Switch interrupt mask status

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	IMS_ADC_ALARM	IMS ADC alarm	RW1C	0x0
14	IMS_THERMAL_ALARM	IMS thermal alarm	RW1C	0x0
13	IMS_DYING_GASP	IMS dying gasp	RW1C	0x0
12	IMS_PTP	IMS PTP egress event	RW1C	0x0
11	IMS_EPON	IMS EPON event	RW1C	0x0
10	IMS_GPON	IMS GPON event	RW1C	0x0
9	IMS_SERDES	IMS serdes interrupt	RW1C	0x0
8	IMS_GPHY	IMS for GPHY interrupt	RW1C	0x0
7	IMS_ACL	IMS for ACL interrupt	RW1C	0x0
6	IMS_RTCT	IMS for Cable Diag finish	RW1C	0x0
5	IMS_LOOP	IMS for have loop detected or loop recoved situation happen	RW1C	0x0
4	IMS_SPE_CONGEST	IMS for TX special congest	RW1C	0x0
3	IMS_SPE_CHG	IMS for speed change	RW1C	0x0
2	IMS_L2_LRN_OVER	IMS for L2 learn over	RW1C	0x0
1	IMS_METER_EXCEED	IMS for meter exceed	RW1C	0x0
0	IMS_LINK_CHG	IMS for link change	RW1C	0x0

## INTR\_STAT

REGISTER ADDRESS : 0xBB01D00C

DEFAULT VALUE : 0x0

Interrupt status

Bits	Field	Description	Type	Default
31:28	RESERVED			
27:23	INTR_STAT_GPHY	Per gphy interrupted	RW1C	0x0
22:16	INTR_STAT_PORT_LINKDOWN	Per port had been link down state	RW1C	0x0
15	RESERVED			
14:8	INTR_STAT_PORT_LINKUP	Per port had been link up state	RW1C	0x0
7	RESERVED			
6:0	INTR_STAT_PORT_CHANGE	Per-port link speed changed status 0b0:not changed 0b1:changed	RW1C	0x0

### SECTION 1.4

## BIST & BISR

BIST &amp; BISR module

## BIST\_CFG19

REGISTER ADDRESS : 0xBB031000

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	STS_BIST_DONE		RO	0x0

## BIST\_CFG18

REGISTER ADDRESS : 0xBB031004

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	COND0_BISR_OUT_0		RO	0x0

## BIST\_CFG17

REGISTER ADDRESS : 0xBB031008



DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	COND0_BISR_OUT_1		RO	0x0

## BIST\_CFG16

REGISTER ADDRESS : 0xBB03100C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:0	COND0_BISR_OUT_2		RO	0x0

## BIST\_CFG15

REGISTER ADDRESS : 0xBB031010

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	COND1_BISR_OUT_0		RO	0x0

## BIST\_CFG14

REGISTER ADDRESS : 0xBB031014

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	COND1_BISR_OUT_1		RO	0x0

## BIST\_CFG13

REGISTER ADDRESS : 0xBB031018

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	STS_DRF_START_PAUSE		RO	0x0

**BIST\_CFG12**

REGISTER ADDRESS : 0xBB03101C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:8	RESERVED			
7	STS_BIST_NOFAIL		RO	0x0
6:1	COND1_BISR_OUT_2		RO	0x0
0	STS_DRF_BIST_NOFAIL		RO	0x0

**BIST\_CFG9**

REGISTER ADDRESS : 0xBB031020

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	STS_DRF_BIST_FAIL_1		RO	0x0

**BIST\_CFG8**

REGISTER ADDRESS : 0xBB031024

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	STS_DRF_BIST_FAIL_0		RO	0x0

**BIST\_CFG7**

REGISTER ADDRESS : 0xBB031028

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	STS_DRF_BIST_DONE		RO	0x0

**BIST\_CFG4**

REGISTER ADDRESS : 0xBB03102C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	STS_BIST_FAIL_1		RO	0x0

### BIST\_CFG3

REGISTER ADDRESS : 0xBB031030

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	STS_BIST_FAIL_0		RO	0x0

### BIST\_CFG2

REGISTER ADDRESS : 0xBB031034

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:14	RESERVED			
13	DRF_TCAMSEL		RW	0x0
12:10	STS_BISR_REPAIRED		RO	0x0
9	COND1_DRF_BIST_NOFAIL		RO	0x0
8	COND0_DRF_BIST_NOFAIL		RO	0x0
7	COND1_BIST_NOFAIL		RO	0x0
6	COND0_BIST_NOFAIL		RO	0x0
5:3	COND1_BISR_REPAIRED		RO	0x0
2:0	COND0_BISR_REPAIRED		RO	0x0

### BIST\_CFG1

REGISTER ADDRESS : 0xBB031038

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	CFG_DRF_BIST_MODE		RW	0x0

### BIST\_CFG0

REGISTER ADDRESS : 0xBB03103C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	CFG_BIST_MODE		RW	0x0

## DIAG\_MODE

REGISTER ADDRESS : 0xBB031040

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:0	DIAGNOSIS_MODE		RW	0x0

## DRF\_TEST\_RESUME

REGISTER ADDRESS : 0xBB031044

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	DRF_TEST_RESUME		RWAC	0x0

## BIST\_CFG

REGISTER ADDRESS : 0xBB000070

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:9	RESERVED			
8	BIST_DONE_ALL		RO	0x0
7:5	BIST_PASS		RO	0x0
4	DRF_BIST_DONE_ALL		RO	0x0
3	DRF_START_PAUSE_ALL		RO	0x0
2:0	BISR_COND_EN		RW	0x0

## RAM\_DVS\_CFG0

REGISTER ADDRESS : 0xBB02301C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:20	RESERVED			
19	CFG_PBRAM_DVSE	Delay option enable signal	RW	0x0
18:15	CFG_PBRAM_DVS	Delay option control word, valid when DVSE==1	RW	0x0
14	CFG_OUTQRAM_DVSE	Delay option enable signal	RW	0x0
13:10	CFG_OUTQRAM_DVS	Delay option control word, valid when DVSE==1	RW	0x0
9	CFG_MIBRAM_DVSE	Delay option enable signal	RW	0x0
8:5	CFG_MIBRAM_DVS	Delay option control word, valid when DVSE==1	RW	0x0
4	CFG_L2RAM_DVSE	Delay option enable signal	RW	0x0
3:0	CFG_L2RAM_DVS	Delay option control word, valid when DVSE==1	RW	0x0

## RAM\_DVS\_CFG1

REGISTER ADDRESS : 0xBB023020

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:20	RESERVED			
19	CFG_INQRAM_DVSE	Delay option enable signal	RW	0x0
18:15	CFG_INQRAM_DVS	Delay option control word, valid when DVSE==1	RW	0x0
14	CFG_HSARAM_DVSE	Delay option enable signal	RW	0x0
13:10	CFG_HSARAM_DVS	Delay option control word, valid when DVSE==1	RW	0x0
9	CFG_CVLANRAM_DVSE	Delay option enable signal	RW	0x0
8:5	CFG_CVLANRAM_DVS	Delay option control word, valid when DVSE==1	RW	0x0
4	CFG_ACTRAM_DVSE	Delay option enable signal	RW	0x0
3:0	CFG_ACTRAM_DVS	Delay option control word, valid when DVSE==1	RW	0x0

## RAM\_DVS\_CFG2

REGISTER ADDRESS : 0xBB023024

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:20	RESERVED			
19	PIRRAM_DVSE		RW	0x0
18:15	PIRRAM_DVS		RW	0x0
14	DBARAM_DVSE		RW	0x0
13:10	DBARAM_DVS		RW	0x0
9	QCNTAM_DVSE		RW	0x0
8:5	QCNTAM_DVS		RW	0x0
4	PTRRAM_DVSE		RW	0x0

Bits	Field	Description	Type	Default
3:0	PTRRAM_DVS		RW	0x0

### RAM\_DVS\_CFG3

REGISTER ADDRESS : 0xBB023028

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:20	RESERVED			
19	US_FRAGRAM_DVSE		RW	0x0
18:15	US_FRAGRAM_DVS		RW	0x0
14	US_DATARAM_DVSE		RW	0x0
13:10	US_DATARAM_DVS		RW	0x0
9	LBRAM_DVSE		RW	0x0
8:5	LBRAM_DVS		RW	0x0
4	CIRRAM_DVSE		RW	0x0
3:0	CIRRAM_DVS		RW	0x0

### RAM\_DVS\_CFG4

REGISTER ADDRESS : 0xBB02302C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:30	RESERVED			
29	BS3_TFARP1_DVSE		RW	0x0
28:25	BS3_TFARP1_DVS		RW	0x0
24	BS3_TFARP0_DVSE		RW	0x0
23:20	BS3_TFARP0_DVS		RW	0x0
19	BS2_L4T_DVSE		RW	0x0
18:15	BS2_L4T_DVS		RW	0x0
14	BS2_ARP_DVSE		RW	0x0
13:10	BS2_ARP_DVS		RW	0x0
9	BS1_1_DVSE		RW	0x0
8:5	BS1_1_DVS		RW	0x0
4	BS1_0_DVSE		RW	0x0
3:0	BS1_0_DVS		RW	0x0

### RAM\_DVS\_CFG5

REGISTER ADDRESS : 0xBB023030

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:15	RESERVED			
14	BS4_NB_DVSE		RW	0x0
13:10	BS4_NB_DVS		RW	0x0
9	BS3_TFL41_DVSE		RW	0x0
8:5	BS3_TFL41_DVS		RW	0x0
4	BS3_TFL40_DVSE		RW	0x0
3:0	BS3_TFL40_DVS		RW	0x0

## PON\_INTEGRATION

REGISTER ADDRESS : 0xBB000074

DEFAULT VALUE : 0x0

PON integration

Bits	Field	Description	Type	Default
31:2	RESERVED			
1	DIS_EPON_BIST	disable EPON MBIST	RW	0x0
0	DIS_GPON_BIST	disable GPON MBIST	RW	0x0

### SECTION 1.5

## CPU RELATIVE

CPU relative module

### SECTION 1.6

## LED

LED module

## LED\_LED

REGISTER ADDRESS : 0xBB01E000

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	LED_SEL	configuration system led mode 0:parallel mode 1:serial mode	RW	0x0

## DATA\_LED\_CFG

BASE ADDRESS : 0xBB01E004  
 ARRAY INDEX : 0 - 31  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

Bits	Field	Description	Type	Default
31:21	RESERVED			
20:16	LED_CFG	Select led port 00000: Disable 00001: MAC0(GPHY0) 00010: MAC1(GPHY1) 00011: MAC2(GPHY2) 00100: MAC3(GPHY3) 00101: MAC4(GPHY4) 00110: MAC5(EXT) 00111 11001:Reserved 11010: Fiber 11011: PON 11100: USB P0 11101: USB P1 11110: SATA 11111: PCIE	RW	0x0
15:13	RESERVED			
12	CPU_FORCE_MOD	cpu force LED	RW	0x0
11	UTP_SPD1000	LED light when UTP link at Speed 1000	RW	0x0
10	UTP_SPD500	LED light when UTP link at Speed 500	RW	0x0
9	UTP_SPD100	LED light when UTP link at Speed 100	RW	0x0
8	UTP_SPD10	LED light when UTP link at Speed 10	RW	0x0
7	UTP_DUP	LED light when UTP link at full duplex mode	RW	0x0
6	UTP_SPD1000_ACT	LED blink when packet access at Speed 1000	RW	0x0
5	UTP_SPD500_ACT	LED blink when packet access at Speed 500	RW	0x0
4	UTP_SPD100_ACT	LED blink when packet access at Speed 100	RW	0x0
3	UTP_SPD10_ACT	LED blink when packet access at Speed 10	RW	0x0
2	UTP_RX_ACT	LED blink when RX packet access	RW	0x0
1	UTP_TX_ACT	LED blink when TX packet access	RW	0x0
0	UTP_COL	LED blink when collision occur	RW	0x0

## LED\_ACTIVE\_LOW\_CFG

BASE ADDRESS : 0xBB01E084  
 ARRAY INDEX : 0 - 16  
 ARRAY OFFSET : 1 bit  
 DEFAULT VALUE : 0x1



This is a One-Dimension Register Field Array. (1 bit per field)

Bits	Field	Description	Type	Default
0	LED_ACTIVE_LOW	select LED led active low 0: active high 1: active low	RW	0x1

## SERI\_LED\_ACTIVE\_LOW\_CFG

REGISTER ADDRESS : 0xBB01E088

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	SERI_LED_ACTIVE_LOW	configuration if serial led active low 0: serial led active high 1: serial led active low	RW	0x0

## LED\_FORCE\_VALUE\_CFG

BASE ADDRESS : 0xBB01E08C

ARRAY INDEX : 0 - 31

ARRAY OFFSET : 2 bits

DEFAULT VALUE : 0x1

This is a One-Dimension Register Field Array. (2 bits per field)

Bits	Field	Description	Type	Default
1:0	SEL_LED_FORCE_VALUE	00: force 0 01: force 1 10: force blinking 11: reserved	RW	0x1

## LED\_BLINK\_RATE\_CFG

REGISTER ADDRESS : 0xBB01E094

DEFAULT VALUE : 0x249

Bits	Field	Description	Type	Default
31:15	RESERVED			

Bits	Field	Description	Type	Default
14:12	SEL_LED_FORCE_RATE	select CPU force mode LED blink rate 000 = 32 ms 001 = 64 ms 010 = 128 ms 011 = 256 ms 100 = 512 ms 101 = 1024 ms 110 = 48 ms 111 = 96 ms	RW	0x0
11:9	SEL_MAC_LED_RATE	select LED blink rate 000 = 32 ms 001 = 64 ms 010 = 128 ms 011 = 256 ms 100 = 512 ms 101 = 1024 ms 110 = 48 ms 111 = 96 ms	RW	0x1
8:6	SEL_USB_LED_RATE	select USB LED blink rate 000 = 32 ms 001 = 64 ms 010 = 128 ms 011 = 256 ms 100 = 512 ms 101 = 1024 ms 110 = 48 ms 111 = 96 ms	RW	0x1
5:3	SEL_SATA_LED_RATE	select SATA LED blink rate 000 = 32 ms 001 = 64 ms 010 = 128 ms 011 = 256 ms 100 = 512 ms 101 = 1024 ms 110 = 48 ms 111 = 96 ms	RW	0x1
2:0	SEL_PCIE_LED_RATE	select PCIE LED blink rate 000 = 32 ms 001 = 64 ms 010 = 128 ms 011 = 256 ms 100 = 512 ms 101 = 1024 ms 110 = 48 ms 111 = 96 ms	RW	0x1

## LOW\_RATE\_BLINK\_CFG

REGISTER ADDRESS : 0xBB01E098

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	SEL_LOW_RATE_BLINK	rate=0%,<10%,10% 25%,25% 50%,>50% 512/256/128/32 ms (TX+RX?)	RW	0x0

## LED\_EN

REGISTER ADDRESS : 0xBB01E0A0

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:28	CFG_LPI_TAG3		RW	0x0
27:24	CFG_LPI_TAG2		RW	0x0
23:20	CFG_LPI_TAG1		RW	0x0
19	LED_SERI_DATA_EN		RW	0x0
18	LED_SERI_CLK_EN		RW	0x0
17:1	LED_PARA_P04_EN		RW	0x0
0	RESERVED			

## SERI\_LED\_CLK\_PER

REGISTER ADDRESS : 0xBB01E0A4

DEFAULT VALUE : 0x1

Bits	Field	Description	Type	Default
31:2	RESERVED			
1:0	CFG_SERI_LED_CLK_PER	select clock period 00 = 3.9MHz(256ns) 01 = 7.8MHz(128ns) (default) 10 = 15.62MHz(64ns) 11 = 15.62MHz(64ns)	RW	0x1

## SERI\_LED\_REFRESH\_TIME

REGISTER ADDRESS : 0xBB01E0A8

DEFAULT VALUE : 0x2

Bits	Field	Description	Type	Default
31:2	RESERVED			
1:0	CFG_SERI_LED_REFRESH_TIME	select serial LED refresh time 00 = 16 ms 01 = 32 ms 10 = 64 ms (default) 11 = 128 ms	RW	0x2

SECTION 1.7

## HW MISC.

HW Misc. module

## FORCE\_P\_DMP

BASE ADDRESS : 0xBB011000  
 ARRAY INDEX : 0 - 6  
 ARRAY OFFSET : 7 bits  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (7 bits per field)

force mode port mask

Bits	Field	Description	Type	Default
6:0	FORCE_PROT_MASK	force mode port mask	RW	0x0

## EN\_FORCE\_P\_DMP

REGISTER ADDRESS : 0xBB011008  
 DEFAULT VALUE : 0x0

forwarding force mode

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	FORCE_MODE	forwarding force mode	RW	0x0

## GLB\_MAC\_MISC

REGISTER ADDRESS : 0xBB023034  
 DEFAULT VALUE : 0x0

Global MAC setting

Bits	Field	Description	Type	Default
31:3	RESERVED			
2	EEEP_DEFER_TXLPI	defer EEEP TX LPI assertion for at least 1us	RW	0x0
1	RX_DMA_SRC		RW	0x0
0	RX_NEW_DMA		RW	0x0

## WRAP\_GPHY\_MISC

REGISTER ADDRESS : 0xBB000080  
 DEFAULT VALUE : 0x0

wrap\_gphy misc

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	PATCH_PHY_DONE	CPU has finished GPHY patch and ASIC would issue GPHY power resume command	RW	0x0

## SECTION 1.8

## CHP INFORMATION

Chip information module

### MODEL\_NAME\_INFO

REGISTER ADDRESS : 0xBB010000

DEFAULT VALUE : 0x86906800

Specify the model name information.

Bits	Field	Description	Type	Default
31:16	RTL_ID	RTL number	RW	0x8690
15:11	MODEL_CHAR_1ST	First English character of model name 0x0: NULL character 0x1-0x1A: character A - Z 0x1B-0x1F: invalid	RW	0x0D
10:6	MODEL_CHAR_2ND	Second English character of model name 0x0: NULL character 0x1-0x1A: character A - Z 0x1B-0x1F: invalid	RW	0x0
5:1	MODEL_CHAR_3RD	Third English character of model name 0x0: NULL character 0x1-0x1A: character A - Z 0x1B-0x1F: invalid	RW	0x0
0	RESERVED			

### CHIP\_INFO

REGISTER ADDRESS : 0xBB010004

DEFAULT VALUE : 0x16266

Specify the chip information.

Bits	Field	Description	Type	Default
31:28	CHIP_INFO_EN	Enable Chip Information display. 0xA: enable. Others: disable. Note: CHIP_INFO only can be read when CHIP_INFO_EN{3:0}=0xA, otherwise the read result will return 0x0.	RW	0x0
27:21	RESERVED			
20:16	CHIP_VER	Chip version. 0x0: NULL character 0x1-0x1A: character A - Z 0x1B-0x1F: invalid	RO	0x01
15:0	RL_ID	RL number	RO	0x6266

## BOND\_INFO

REGISTER ADDRESS : 0xBB010008

DEFAULT VALUE : 0x0

Specify the chip bonding information.

Bits	Field	Description	Type	Default
31:28	BOND_INFO_EN	Enable Bond Information display. 0xB: enable. Others: disable. Note: BOND_INFO only can be read when BOND_INFO_EN{3:0}=0xB, otherwise the read result will return 0x0.	RW	0x0
27:5	RESERVED			
4:0	BOND_CHIP_MODE	bound chip mode bit 0 - PAD_BOND_DMY_0 bit 1 - PAD_BOND_DMY_1 bit 2 - PAD_BOND_DMY_2 bit 3 - PAD_BOND_CHIP_MODE_0 bit 4 - PAD_BOND_CHIP_MODE_1	RO	0x0

## MISCELLANEOUS\_CONFIGURE0

REGISTER ADDRESS : 0xBB000084

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:10	RESERVED			
9	ADCKKI_FROM_PAD	select adckki function clock from pad or pll_125 from GPHY	RW	0x0
8	ADCKKI_EN	enable adckki function	RW	0x0
7:4	RESERVED			
3	OLT_ENABLE	enable olt mode	RW	0x0

Bits	Field	Description	Type	Default
2	DIS_PWRON_TABLE_INIT	disable power on table initial Bounding option	RW	0x0
1	DIS_PWRON_BIST	disable power on bist Bounding option	RW	0x0
0	EFUSE_EN	enable efuse 0:disable efuse 1:enable efuse Bonding option	RW	0x0

## FORCE\_P\_ABLTY

BASE ADDRESS : 0xBB000088

PORT INDEX : 0 - 6

PORT OFFSET : 0x4

DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Bits	Field	Description	Type	Default
31:12	RESERVED			
11	LPI_1000_ABLTY	LPI_1000	RW	0x0
10	LPI_100_ABLTY	LPI_100	RW	0x0
9	MST_FAULT_ABLTY	N-way fault	RW	0x0
8	MST_MOD_ABLTY	link on in master mode	RW	0x0
7	NWAY_ABLTY	Auto-Negotiation Ability	RW	0x0
6	TXPAUSE_ABLTY	transmit flow control 0:not flow control capable 1:flow control capable	RW	0x0
5	RXPAUSE_ABLTY	receive flow control capable 0:not flow control capable 1:flow control capable	RW	0x0
4	LINK_ABLTY	link status	RW	0x0
3	FIB1G_ABLTY	link at fiber 1g	RW	0x0
2	DUPLEX_ABLTY	full duplex capable 0=half duplex 1=full duplex	RW	0x0
1:0	SPEED_ABLTY	link speed . 00=10M 01=100M 10=1000M	RW	0x0

## MDX\_PHY\_REG1

REGISTER ADDRESS : 0xBB0000A4

DEFAULT VALUE : 0x1F

Bits	Field	Description	Type	Default
31:10	RESERVED			
9:5	PHY_BRD_MODE	SMI broadcast write enable	RW	0x0
4:0	BRD_PHYAD	SMI broadcast phyad	RW	0x1F

## UPS\_CTRL2

REGISTER ADDRESS : 0xBB0000A8

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	IGNOE_MAC5_LINK	ignore mac 5's link	RW	0x0
14:0	RESERVED			

## GATING\_CLK\_1

REGISTER ADDRESS : 0xBB0000AC

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	IGNOE_MAC6_LINK	ignore mac 6's link	RW	0x0

## ROUTER\_UPS\_CFG

REGISTER ADDRESS : 0xBB0000B0

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	SOFTSTART	0: System is cold start. 1: System is warm start ASIC will set this bit to 1 after first times DIS_PWR remove.	RO	0x0

## P\_ABLTY

BASE ADDRESS : 0xBB0000B4

PORT INDEX : 0 - 6

PORT OFFSET : 0x4



DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Bits	Field	Description	Type	Default
31:12	RESERVED			
11	LPI_1000	LPI_1000	RO	0x0
10	LPI_100	LPI_100	RO	0x0
9	P_NWAY_FAULT	N-way fault	RO	0x0
8	P_MSTR	link on in master mode	RO	0x0
7	P_NWAY_ABLTY	Auto-Negotiation Ability	RO	0x0
6	P_TX_FC	transmit flow control 0:not flow control capable 1:flow control capable	RO	0x0
5	P_RX_FC	receive flow control capable 0:not flow control capable 1:flow control capable	RO	0x0
4	P_LINK_STATUS	link status	RO	0x0
3	P_LINK_FIB1G	link at fiber 1g	RO	0x0
2	P_DUPLEX	full duplex capable 0=half duplex 1=full duplex	RO	0x0
1:0	P_LINK_SPD	link speed . 00=10M 01=100M 10=1000M	RO	0x0

## GPIO\_CTRL\_0

BASE ADDRESS : 0xBB0000D0

ARRAY INDEX : 0 - 71

ARRAY OFFSET : 1 bit

DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

Bits	Field	Description	Type	Default
0	CTRL_GPIO	control GPO pin 0 71 0:output 0 1:output 1	RW	0x0

## GPIO\_CTRL\_1

BASE ADDRESS : 0xBB0000DC

ARRAY INDEX : 0 - 71  
 ARRAY OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

Bits	Field	Description	Type	Default
0	STS_GPIO	status of GPI pin 0 71	RO	0x0

## GPIO\_CTRL\_2

BASE ADDRESS : 0xBB0000E8  
 ARRAY INDEX : 0 - 71  
 ARRAY OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

Bits	Field	Description	Type	Default
0	EN_GPIO	enable GPO function for GPO pin 0 71	RW	0x0

## GPIO\_CTRL\_3

BASE ADDRESS : 0xBB0000F4  
 ARRAY INDEX : 0 - 71  
 ARRAY OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

Bits	Field	Description	Type	Default
0	DUMMY		RW	0x0

## GPIO\_CTRL\_4

BASE ADDRESS : 0xBB000100  
 ARRAY INDEX : 0 - 71  
 ARRAY OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

Bits	Field	Description	Type	Default
0	SEL_GPIO	sel gpi/o mode 0:gpi 1:gpo note:chip_info sheet	RW	0x0

## RTL\_OUI\_CFG

REGISTER ADDRESS : 0xBB00010C  
DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:24	RESERVED			
23:0	OUI_CFG	Realtek OUI	RW	0x0

## REVISION\_CFG

REGISTER ADDRESS : 0xBB000110  
DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:4	RESERVED			
3:0	REVISOIN_CFG	Revision Number	RW	0x0

## MODEL\_CFG

REGISTER ADDRESS : 0xBB000114  
DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:0	MODEL_CFG	Model Number	RW	0x0

## WAKELPI\_SLOT\_PRD

REGISTER ADDRESS : 0xBB000118  
DEFAULT VALUE : 0x1F

Bits	Field	Description	Type	Default
31:5	RESERVED			
4:0	WAKE_LPI_SLOT_PRD	MAC EEE wake LPI time frame interval , time unit is us.	RW	0x1F

## WAKELPI\_SLOT

BASE ADDRESS : 0xBB00011C  
 PORT INDEX : 0 - 4  
 PORT OFFSET : 5 bits  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (5 bits per field)

Bits	Field	Description	Type	Default
4:0	WAKELPI_SLOT_PORT	MAC EEE wake LPI time slot number.	RW	0x0

## RGM\_EEE

REGISTER ADDRESS : 0xBB000120  
 DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:5	RESERVED			
4	EXT_PAD_STOP_EN	EXT_PAD_STOP_EN	RW	0x0
3:0	EXT_CYCLE_PAD	EXT_CYCLE_PAD	RW	0x0

## ABLTY\_FORCE\_MODE

REGISTER ADDRESS : 0xBB000124  
 DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:7	RESERVED			
6:0	ABLTY_FORCE_MODE		RW	0x0

## DEBUG\_SEL

REGISTER ADDRESS : 0xBB000128  
 DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:26	RESERVED			
25	DBGEN_BY_REG	debug selection by register	RW	0x0
24	DBG_BY_SPI	debug output on spi I/F	RW	0x0
23:22	DBG_BY_OEM	debug output on OE module I/F	RW	0x0
21	DBG_BY_SLIC	debug output on slic I/F	RW	0x0
20	DBG_BY_EXT	debug output on ext I/F	RW	0x0
19:16	CFG_DBGGO_SHIFT	switch the debug output for the case debug pin is not enough.	RW	0x0
15:0	DBGGO_SEL	selection for debug output	RW	0x0

## RST\_SYNC\_FIFO

REGISTER ADDRESS : 0xBB00012C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:4	RESERVED			
3	CFG_SYNC_FIFO_TX	extxf tx fifo link down reset enable	RW	0x0
2	CFG_SYNC_FIFO_RX	extxf rx fifo link down reset enable	RW	0x0
1	CFG_STOP_GLI_CLK_EN	MAC GLI clock gating enable as power saving mode	RW	0x0
0	CFG_STOP_CLK_PORT_EN	MAC system clock gating enable as power saving mode	RW	0x0

## SDS\_CFG

REGISTER ADDRESS : 0xBB000130

DEFAULT VALUE : 0x8

Bits	Field	Description	Type	Default
31:5	RESERVED			
4:0	CFG_SDS_MODE		RW	0x08

## MAC\_ACT\_CFG

REGISTER ADDRESS : 0xBB000134

DEFAULT VALUE : 0xFE00

Bits	Field	Description	Type	Default
31:17	RESERVED			

Bits	Field	Description	Type	Default
16:9	CFG_MAC_ACTIVE	Active MAC port mask	RW	0x7F
8	CFG_LINK_DOWN_TIME_EN	MAC minimum link down time enable	RW	0x0
7:0	CFG_LINK_DOWN_TIME	MAC minimum link down time in ms	RW	0x0

## BYPS\_ABLTY\_LOCK

REGISTER ADDRESS : 0xBB000138

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:7	RESERVED			
6:0	BYPS_ABLTY_LOCK	1: dont latch the ability from GPHY	RW	0x0

## FIFO\_ERR\_STS

REGISTER ADDRESS : 0xBB00013C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:7	RESERVED			
6	STS_SYNC_FIFO_TX_ERR	indicate that ext-port TX FIFO error detected.	RO	0x0
5:0	STS_SYNC_FIFO_RX_ERR	indicate that ext-port RX FIFO error detected.	RO	0x0

## SDS\_AN\_RX\_CFG

REGISTER ADDRESS : 0xBB000140

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	RX_CFG_REG_SDS		RO	0x0

## SDS\_FIB\_STATUS

REGISTER ADDRESS : 0xBB000144

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:17	RESERVED			
16:5	FIBER_ABLTY		RO	0x0
4	SDS_LINK_OK		RO	0x0
3	SDS_INTB		RO	0x0
2	SDS_ANFAULT		RO	0x0
1	FIB_ISO		RO	0x0
0	FIB100_DET		RO	0x0

## EXT\_STS

REGISTER ADDRESS : 0xBB000148

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	EXT_STS_EXTXF		RO	0x0

## AFE\_VER

REGISTER ADDRESS : 0xBB00014C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	AFE_VERSION		RO	0x0

## PON\_MODE\_CFG

REGISTER ADDRESS : 0xBB000150

DEFAULT VALUE : 0x1

PON MAC mode register

Bits	Field	Description	Type	Default
31:2	RESERVED			
1	EPON_EN	Enable EPON mode 0b0: disable 0b1: enable	RW	0x0
0	GPON_EN	Enable GPON mode 0b0: disable 0b1: enable	RW	0x1

## HTRAM\_DVS\_CFG

REGISTER ADDRESS : 0xBB023038

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	CFG_HTRAM_DVSE_3	Delay option enable signal	RW	0x0
14:12	CFG_HTRAM_DVS_3	Delay option control word, valid when DVSE==1	RW	0x0
11	CFG_HTRAM_DVSE_2	Delay option enable signal	RW	0x0
10:8	CFG_HTRAM_DVS_2	Delay option control word, valid when DVSE==1	RW	0x0
7	CFG_HTRAM_DVSE_1	Delay option enable signal	RW	0x0
6:4	CFG_HTRAM_DVS_1	Delay option control word, valid when DVSE==1	RW	0x0
3	CFG_HTRAM_DVSE_0	Delay option enable signal	RW	0x0
2:0	CFG_HTRAM_DVS_0	Delay option control word, valid when DVSE==1	RW	0x0

## HWPKT\_GEN\_STA

REGISTER ADDRESS : 0xBB02303C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:8	HWPKT_GEN_SUS		RWAC	0x0
7:0	HWPKT_GEN_STATUS		RO	0x0

## ALL\_PORT\_LKDN\_TIME

REGISTER ADDRESS : 0xBB000154

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	DUMMY		RW	0x0

## MODE\_EXT

REGISTER ADDRESS : 0xBB000158

DEFAULT VALUE : 0x0



Bits	Field	Description	Type	Default
31:4	RESERVED			
3:0	MODE_EXT	0000:Disable 0001:EXT MAC with RGMII 0010:EXT MAC with MII MAC mode 0011:EXT MAC with MII PHY mode 0100:EXT MAC with TMII MAC mode 0101:EXT MAC with TMII PHY mode 0110:EXT MAC with GMII 0111:EXT MAC with RMII MAC mode 1000:EXT MAC with RMII PHY mode	RW	0x0

## GPHY\_AFE\_DBG\_CFG

REGISTER ADDRESS : 0xBB00015C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:2	REG_ANA	analog debug control	RW	0x0
1	EN_RTT2	enable GPHY AFE debug pad RTT2	RW	0x0
0	EN_RTT1	enable GPHY AFE debug pad RTT1	RW	0x0

## AD5\_CTRL

REGISTER ADDRESS : 0xBB000160

DEFAULT VALUE : 0x136

ADC control

Bits	Field	Description	Type	Default
31:10	RESERVED			
9:7	ISSET_AD5	ADC SHA/CMP bias current selection	RW	0x2
6:4	AVSET_AD5	SHA gain selection	RW	0x3
3:1	VICM_AD5	Input VCM selection	RW	0x3
0	VINSEL_AD5	0 - VIN1 1 1.5V 1 - VIN2 3 4.6V	RW	0x0

## PWM\_CTRL1

REGISTER ADDRESS : 0xBB000164

DEFAULT VALUE : 0x1AA8

PWM control 1

Bits	Field	Description	Type	Default
31:14	RESERVED			
13	BYPASS_PWM	0 - determined by PWM_L 1 - close SR and D	RW	0x0
12	ENCS_PWM	0 - turn off current limit 1 - turn on current limit	RW	0x1
11	ENSS_PWM	0 - turn off soft start 1 - turn on soft start	RW	0x1
10	EN_PWM	0 - disable 1 - enable	RW	0x0
9:7	FCK_PWM		RW	0x5
6:5	IB20UTO5U_PWM	00 - IB5u 01 - IB10u 10 - IB15u 11 - IB20u	RW	0x1
4	IOS_PWM	0 - turn off 1 - turn on	RW	0x0
3	LATCH_PWM	0 - 90% latch 1 - 95% latch	RW	0x1
2:0	OCPT_PWM	over current protection trigger count = (N+1)x2	RW	0x0

## PWM\_CTRL2

REGISTER ADDRESS : 0xBB000168

DEFAULT VALUE : 0x564A83A

PWM control 2

Bits	Field	Description	Type	Default
31:30	RESERVED			
29:27	OVPT_PWM	over voltage protection trigger count = (N+1)x2	RW	0x0
26	OOS_PWM	0 - turn off 1 - turn on	RW	0x1
25:24	OSC_PWM	00 - 4.5pF 01 - 5.8pF 10 - 5.8pF 11 - 7.1pF	RW	0x1
23:22	OVPWIN_PWM	OVP threshold 00 - 2.5V 01 - 5V 10 - 7.5V 11 - 10V	RW	0x1
21	PWM	0 - D F.F. 1 - SR latch	RW	0x1
20:17	SAWFREQ_PWM	3+cfg_sawfreq_pwm (u)	RW	0x2
16	SELOS_PWM	0 - turn on OOS 1 - turn on IOS	RW	0x0
15:13	SSCLK_PWM	0X0 - C=3, 0X1 - C=4, 10X - C=5, 11X - C=6 softstart time =CLK*64*2power(C)	RW	0x5
12:10	VCMOCP_PWM	0.75V + 0.025V x cfg_vcmocp_pwm	RW	0x2
9:7	VREF09_PWM	determined by VREF09 as ENSS_H=0	RW	0x0
6:3	VREFOCP_PWM	4.125K + cfg_vrefocp_pwm x 0.125K	RW	0x7
2:0	VREFOVP_PWM	Output voltage setting	RW	0x2

## TM\_DLY

REGISTER ADDRESS : 0xBB00016C

DEFAULT VALUE : 0xFA57E4

Thermal delay setting

Bits	Field	Description	Type	Default
31:16	CMPDLY_TM	comparison delay , recommended time is 2us	RW	0x00FA
15:0	PONDLY_TM	power-on delay , recommended time is 180us	RW	0x57E4

## TM\_CTRL

REGISTER ADDRESS : 0xBB000170

DEFAULT VALUE : 0x0

Thermal control

Bits	Field	Description	Type	Default
31:18	RESERVED			
17	ENABLE_TM	enable thermal sensor	RW	0x0
16	REVERSE_TM	reverse compared result	RW	0x0
15:0	SMPDLY_TM	sampling delay = ( cfg_sample_tm + 1 ) x comparison delay	RW	0x0

## TM\_STS

REGISTER ADDRESS : 0xBB000174

DEFAULT VALUE : 0x0

Thermal status

Bits	Field	Description	Type	Default
31:7	RESERVED			
6	DATAVLD_TM	thermal data valid status	RO	0x0
5:0	DATAOUT_TM	thermal data	RO	0x0

## AD5\_ALARM

REGISTER ADDRESS : 0xBB000178

DEFAULT VALUE : 0x0

AD5 alarm

Bits	Field	Description	Type	Default
31:5	RESERVED			

Bits	Field	Description	Type	Default
4:0	AD5_ALARM_TH	battery low voltage alarm threshold	RW	0x0

## AD5\_DATA

REGISTER ADDRESS : 0xBB00017C

DEFAULT VALUE : 0x0

AD5 data

Bits	Field	Description	Type	Default
31:5	RESERVED			
4:0	AD5_DATAOUT	AD5 read data	RO	0x0

## TM\_ALARM

REGISTER ADDRESS : 0xBB000180

DEFAULT VALUE : 0x0

TM alarm

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:0	TM_ALARM_TH	over temperature alarm threshold	RW	0x0

## CHIP\_INF\_SEL

REGISTER ADDRESS : 0xBB000184

DEFAULT VALUE : 0x0

Chip interface select

Bits	Field	Description	Type	Default
31:2	RESERVED			
1	PHY4_EN	use PHY4, higher priority than gpon/epon	RW	0x0

## SLIC\_INSEL\_CTRL

REGISTER ADDRESS : 0xBB000188

DEFAULT VALUE : 0x0

slic interface select

Bits	Field	Description	Type	Default
31:3	RESERVED			
2	SLIC_EN	SLIC interface enable	RW	0x0
1:0	SLIC_INFSEL	00 - none 01 - SPI 10 - ZSI 11 - ISI	RW	0x0

## SYS\_PKT\_BUF\_CTRL

REGISTER ADDRESS : 0xBB00018C

DEFAULT VALUE : 0x1

system packet buffer config

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	PB_3M	0 - 2Mbits packet buffer 1 - 3.5Mbits packet buffer	RW	0x1

## DYNGASP\_CTRL

REGISTER ADDRESS : 0xBB000190

DEFAULT VALUE : 0x7F0

DYNGASP control

Bits	Field	Description	Type	Default
31:12	RESERVED			
11	DYNGASP_EN	enable dying gasp	RW	0x0
10:4	DYNGASP_IDX	qid selection for dying gasp	RW	0x7F
3	DYNGASP_CMP_INV	dyinggasp comparison result polarity inversion	RW	0x0
2	DYNGASP_OUT_INV	dyinggasp output pin polarity inversion	RW	0x0
1	DYNGASP_OUT_EN	dyinggasp output pin driving enable	RW	0x0
0	DYNGASP_OUT_PULL	dyinggasp output pin pull polarity	RO	0x0

## BOND\_STRAP\_STS0

REGISTER ADDRESS : 0xBB000194

DEFAULT VALUE : 0x0

bonding and straping status

Bits	Field	Description	Type	Default
31:0	BOND_STRAP_STS0	bonding option and pin straping status	RO	0x0

## BOND\_STRAP\_STS1

REGISTER ADDRESS : 0xBB000198

DEFAULT VALUE : 0x0

bonding and straping status

Bits	Field	Description	Type	Default
31:0	BOND_STRAP_STS1	bonding option and pin straping status	RO	0x0

## BOND\_STRAP\_STS2

REGISTER ADDRESS : 0xBB00019C

DEFAULT VALUE : 0x0

bonding and straping status

Bits	Field	Description	Type	Default
31:0	BOND_STRAP_STS2	bonding option and pin straping status	RO	0x0

## MISCELLANEOUS\_BONDING

REGISTER ADDRESS : 0xBB0001A0

DEFAULT VALUE : 0xC000

Bits	Field	Description	Type	Default
31	IN_EXT_CLK_CLK_LX	external clock 5 input ext_clk_lx	RO	0x0
30	IN_EXT_CLK_CLK_M90	external clock 3 input ext_clk_m90	RO	0x0
29	IN_EXT_CLK_CLK_M	external clock 3 input ext_clk_m	RO	0x0
28	IN_EXT_CLK_OCP2	external clock 2 input ext_clk_ocp2	RO	0x0
27	IN_EXT_CLK_OCP1	external clock 1 input ext_clk_ocp1	RO	0x0
26	IN_EXT_CLK_SW	external clock 0 input ext_clk_sw	RO	0x0

Bits	Field	Description	Type	Default
25	BOND_PHY_EN	Enable / Disable all PHY, include GPHY, USB, SATA, PCIE 0: Disable 1: Enable	RO	0x0
24	BOND_DUMMY2	Dummy	RO	0x0
23	BOND_DUMMY1	Dummy	RO	0x0
22	BOND_DUMMY0	Dummy	RO	0x0
21	BOND_CKSELB	If bond_cksel_en=1, the input clock is select by bond_cksel 0:25MHz clock input 1:40MHz clock input	RO	0x0
20	BOND_CKSEL_ENB	The input clock select by bonding option bond_cksel, bypass strapping pin SYS_CLK_SEL clock selection. 0: Enable 1: Disable	RO	0x0
19:18	BOND_DDR_FREQ_DIV	DDR PLL Freq. div 00: 1 01: 1/2 10: 1/4 11: 1/8	RO	0x0
17:14	BOND_DDR_PLL_FREQ	DDR PLL Freq. selection. 0000: 0001: 0010: 0011: 0100:	RO	0x3
13:12	BOND_VOIP_MODE	Select VOIP mode 00: model 0 01: model 1 10: model 2 11: model 3	RO	0x0
11	BOND_AFE_POR_EN	Enable AFE power on reset 0: Disable AFE Power on reset 1: Enable AFE Power on reset	RO	0x0
10	EXT_CLK_LX	When the PAD_DBG_EN=1, Bypass lynx clock ext_clk_lx, input clock from external clock input pin ext_clk_lx 0: normal 1: bypass ext_clk_lx	RO	0x0
9	EXT_CLK_M90	When the PAD_DBG_EN=1, Bypass DDR lag clock ext_clk_m90, input clock from external clock input pin ext_clk_m90 0: normal 1: bypass ext_clk_m90	RO	0x0
8	EXT_CLK_M	When the PAD_DBG_EN=1, Bypass DDR clock ext_clk_m, input clock from external clock input pin ext_clk_m 0: normal 1: bypass ext_clk_m	RW	0x0
7	EXT_CLK_OCP2	When the PAD_DBG_EN=1, Bypass OCP2 clock ext_clk_ocr2, input clock from external clock input pin ext_clk_ocr2 ( PAD_TOD) 0: normal 1: bypass ext_clk_ocr2	RO	0x0

Bits	Field	Description	Type	Default
6	EXT_CLK_OCP1	When the PAD_DBG_EN=1, Bypass OCP1 clock ext_clk_ocp1, input clock from external clock input pin ext_clk_ocp1 (PAD_TX_SD) 0: normal 1: bypass ext_clk_ocp1	RO	0x0
5	EXT_CLK_SW	When the PAD_DBG_EN=1, Bypass switch clock ext_clk_sw, input clock from external clock input pin ext_clk_sw (PAD_GTXC) 0: normal 1: bypass ext_clk_sw	RO	0x0
4	PAD_BOND_BISR_REMAP_EN	1: BISR remap 0: hold BISR remap	RO	0x0
3	PAD_BOND_NFBI_ENB	Not used. NFBI has been removed from LXB. 0:Enable 1: Disable	RO	0x0
2	PAD_BOND_NF_MUX_SEL	NAND flash I/O group selection 0: SPI flash 1: External	RO	0x0
1	PAD_BOND_TEST_EN	Enable / Disable DFT mode 0: Disable DFT mode 1: Enable DFT mode	RO	0x0
0	PAD_DBG_EN	Debug package 0: NOT Debug package 1: Debug package	RO	0x0

## MISCELLANEOUS\_STRAPPING1

REGISTER ADDRESS : 0xBB0001A4

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:6	RESERVED			
5	BOND_PON_BIST_EN	Enable / Disable Power on BIST 0: Disable 1: Enable	RO	0x0
4	BOND_EFUSE_ENB	Enable/Disable EFUSE patch by CPU 0: Enable EFUSE patch. 1: Disable EFUSE patch.	RO	0x0
3	BOND_NAT_ENB	Enable/Disable NAT 0: Enable NAT, 1: Disable NAT	RO	0x0
2:1	BOND_PON_SEL	PON mode selection 00: Disable 01:Enable GPON. 10:Enable EPON 11:Enable GPON & EPON	RO	0x0
0	BOND_PON_TAB_INIT_EN	Enable / Disable Table init 0: Disable 1: Enable	RO	0x0



## MISCELLANEOUS\_STRAPPING0

REGISTER ADDRESS : 0xBB0001A8

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:12	RESERVED			
11	EN_SMI_SLAVE	Enable/Disable SMI slave mode 1: Disable, 0: SMI_Slave (PON_LED[1:0} Register control)	RO	0x0
10	SYS_CLK_SEL	System clock selection 0:25MHz clock input 1:40MHz clock input	RO	0x0
9	DIS_JTAG	Enable / Disable JTAG interface 0: Enable JTAG 1: Disable JTAG	RW	0x0
8	SPIF4BEN	SPI flash address byte number 0: 3 Bytes 1: 4 Bytes	RO	0x0
7	NAFC_RC	NAND flash read command cycles 0: 1 cycles 1: 2 cycles	RO	0x0
6	NAF_AC1	NAND flash address command cycles 00: 3 cycles 01: 4 cycles 10: 5 cycles 11: reference naf_ac0	RO	0x0
5	NAF_AC0	NAND flash address command cycles 00: 3 cycles 01: 4 cycles 10: 5 cycles 11: reference naf_ac1	RO	0x0
4	BTUP_TYP1	Boot up type selection (NFBI/SPI/NAND) 00: NFBI 01: PCIE 10: SPI 11: NAND reference btup TYP0	RO	0x0
3	BTUP_TYP0	Boot up type selection (NFBI/SPI/NAND) 00: NFBI 01: PCIE 10: SPI 11: NAND reference btup TYP1	RO	0x0
2	DRAM_TYP1	DDR type selection (DDR1/2/3) 00: SDR 01: DDR1 10: DDR2 11: DDR3 reference DRAM TYP0	RO	0x0

Bits	Field	Description	Type	Default
1	DRAM_TYPO	DDR type selection (DDR1/2/3) 00: SDR 01: DDR1 10: DDR2 11: DDR3 reference DRAM TYP1	RO	0x0
0	EN_CPU	Enable / Disable CPU, 0:Disable CPU 1: Enable CPU	RO	0x0

## MAC\_DLYLNK

REGISTER ADDRESS : 0xBB0001AC

DEFAULT VALUE : 0x26

SWCORE MAC delay link

Bits	Field	Description	Type	Default
31:6	RESERVED			
5	MACRX_DUPDET_EN		RW	0x1
4	MAC_LNKUP_DELAY_EN	Enable MAC delay link up	RW	0x0
3:2	GE_100M_LNKUP_DELAY	2'b00 - disable delay link for giga and 100M 2'b01 - delay link for 10ms 2'b10 - delay link for 20ms 2'b11 - delay link for 30ms	RW	0x1
1:0	LNKUP_10M_DELAY	2'b00 - delay link for 50ms 2'b01 - delay link for 150ms 2'b10 - delay link for 250ms 2'b11 - delay link for 350ms	RW	0x2

## PLL\_RGM\_CTRL1

REGISTER ADDRESS : 0xBB0001B0

DEFAULT VALUE : 0x8000000

RGMII PLL control 1

Bits	Field	Description	Type	Default
31:28	RESERVED			
27	PLL_RGM_PSEN		RW	0x1
26	PLL_RGM_OEB		RW	0x0
25	PLL_RGM_FUPDN		RW	0x0
24	PLL_RGM_PWRDN		RW	0x0
23:22	PLL_RGM_SSC_TMODE		RW	0x0
21:14	PLL_RGM_SSC_OFFS		RW	0x0
13:8	PLL_RGM_SSC_STEP		RW	0x0

Bits	Field	Description	Type	Default
7:1	PLL_RGM_SSC_PERIOD		RW	0x0
0	PLL_RGM_SSC_EN		RW	0x0

## PLL\_RGM\_CTRL2

REGISTER ADDRESS : 0xBB0001B4

DEFAULT VALUE : 0x7EA5B421

RGMII PLL control 2

Bits	Field	Description	Type	Default
31	PLL_RGM_PI_COMP_DLY_L		RW	0x0
30:29	PLL_RGM_PI_BIAS		RW	0x3
28:27	PLL_RGM_PI_RS		RW	0x3
26:25	PLL_RGM_PI_RL		RW	0x3
24	PLL_RGM_PSTST		RW	0x0
23:22	PLL_RGM_C3		RW	0x2
21:19	PLL_RGM_R3		RW	0x4
18:17	PLL_RGM_CP		RW	0x2
16:15	PLL_RGM_CS		RW	0x3
14:12	PLL_RGM_RS		RW	0x3
11:9	PLL_RGM_IP		RW	0x2
8:2	PLL_RGM_DIV		RW	0x08
1:0	PLL_RGM_LDO		RW	0x1

## PLL\_RGM\_CTRL3

REGISTER ADDRESS : 0xBB0001B8

DEFAULT VALUE : 0xF0FFE0

RGMII PLL control 3

Bits	Field	Description	Type	Default
31:24	RESERVED			
23:18	PLL_RGM_RSVD		RW	0x3C
17:16	PLL_RGM_WDMODE		RW	0x0
15	PLL_RGM_EN_PI16		RW	0x1
14:13	PLL_RGM_PI16_BIAS		RW	0x3
12:11	PLL_RGM_PI16_RS		RW	0x3
10:9	PLL_RGM_PI16_RL		RW	0x3
8:5	PLL_RGM_REG_CK0		RW	0xF
4:1	PLL_RGM_PHS_H		RW	0x0

Bits	Field	Description	Type	Default
0	PLL_RGM_PI_COMP_DLY_H		RW	0x0

## CHAPTER 2

# MAC & PHY

The chapter describes features related to MAC & PHY

### SECTION 2.1

## MAC CONTROL

The module contains MAC polling configuration, Indirect PHY access and generic MAC control functions.

### FPGA\_VER\_MAC

REGISTER ADDRESS : 0xBB023040

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	FPGA_VER_MAC	fpga version	RO	0x0

### MAC\_CPU\_TAG\_CTRL

REGISTER ADDRESS : 0xBB023044

DEFAULT VALUE : 0x100

CPU tag control register

Bits	Field	Description	Type	Default
31:9	RESERVED			
8	TRAP_TAGET_INSERT_EN	insert CPU tag for trap port 0b0: disable 0b1: enable	RW	0x1
7:1	RESERVED			
0	TAG_FORMAT	CPU tag format usage 0b0: Apollo mode 0b1: 4-bytes mode	RW	0x0

### MAC\_CPU\_TAG\_AWARE\_CTRL

BASE ADDRESS : 0xBB023048

PORT INDEX : 0 - 6  
 PORT OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

CPU tag ingress aware control register

Bits	Field	Description	Type	Default
0	EN	CPU tag ingress parsing aware port 0b1:enable	RW	

## ACCEPT\_MAX\_LEN\_CTRL

BASE ADDRESS : 0xBB01100C  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Accepted max length control register

Bits	Field	Description	Type	Default
31:2	RESERVED			
1	MAX_LENGTH_GIGA	Per-Port max accepted frame length in speed Gpbs 0b0: reference ACCEPT_MAX_LENGTH_CFG0 configuration 0b1: reference ACCEPT_MAX_LENGTH_CFG1 configuration	RW	0x0
0	MAX_LENGTH_10_100	Per-Port max accepted frame length in speed 10/100 0b0: reference ACCEPT_MAX_LENGTH_CFG0 configuration 0b1: reference ACCEPT_MAX_LENGTH_CFG1 configuration	RW	0x0

## MAX\_LENGTH\_CFG1

REGISTER ADDRESS : 0xBB011028  
 DEFAULT VALUE : 0x3FF0

Bits	Field	Description	Type	Default
31:14	RESERVED			
13:0	ACCEPT_MAX_LENGTH_CFG1	max length cfiguration 1 The register value specify the limit rate This value can't exceed ACCEPT_MAX_LENGTH_CFG0.	RW AC-	0x3FF0

Bits	Field	Description	Type	Default
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## MAX\_LENGTH\_CFG0

REGISTER ADDRESS : 0xBB02304C

DEFAULT VALUE : 0x3FF0

Bits	Field	Description	Type	Default
31:14	RESERVED			
13:0	ACCEPT_MAX_LENGTH_CFG0	max length configuration 0 The register value specify the limit rate the max value is 0x3FF0, should not be configure exceed 0x3FF0.	RW	0x3FF0

## MAX\_LENGTH\_LIMIT\_IPG

REGISTER ADDRESS : 0xBB023050

DEFAULT VALUE : 0x3F87

Bits	Field	Description	Type	Default
31:14	RESERVED			
13:6	PAGES_BEFORE_FCDROP	Page threshold as egress flowctrl enable	RW	0xFE
5	CHECK_MIN_IPG_RXDV	Disable check min. limit in ipg/rxdv 0:Enable 1:Disable	RW	0x0
4:0	LIMIT_IPG_CFG	Limit ipg+preamble size for RX, Min. value is 7. Default : 7 byte-time	RW	0x07

## IOL\_RXDROP\_CFG

REGISTER ADDRESS : 0xBB023054

DEFAULT VALUE : 0x14

Bits	Field	Description	Type	Default
31:9	RESERVED			
8	RX_IOL_MAX_LENGTH_CFG	max-bc is 1518 or 1522 bytes 0:disable 1:enable	RW	0x0
7	RX_IOL_ERROR_LENGTH_CFG	eth_len != pktdata_len -> discard	RW	0x0
6	RX_NODROP_PAUSE_CFG	no drop rx pause 0:disable 1:enable	RW	0x0
5:0	RX_DV_CNT_CFG	Min. limit in pktlen, default: 20 bytes	RW	0x14

## CFG\_BACKPRESSURE

REGISTER ADDRESS : 0xBB023058

DEFAULT VALUE : 0x2

Bits	Field	Description	Type	Default
31:4	RESERVED			
3	LONGTXE	carrierbased back-pressure 0:collision based back-pressure 1:carrier based back-pressure, defer mode with 2K bytes TX_EN	RW	0x0
2	EN_BYPASS_ERROR	bypass crc error packet 0: disable 1:enable	RW	0x0
1	EN_BACKPRESSURE	Enable backpressure 0: disable 1:enable	RW	0x1
0	EN_48_PASS_1	Enable 48-pass-1 0: disable 1:enable	RW	0x0

## CFG\_UNHIOL

REGISTER ADDRESS : 0xBB02305C

DEFAULT VALUE : 0xA8

Bits	Field	Description	Type	Default
31:10	RESERVED			
9	DIS_ITFSP_OP	1: disable itfsp	RW	0x0
8	DIS_SKIP_FP	dis skip fp	RW	0x0
7:5	ITFSP_REG	select tx ipg 00:0byte 01:1byte 10:2byte	RW	0x5
4	IOL_16DROP	iol drop, drop packet after 16 collisions	RW	0x0
3	IOL_BACKOFF	the iol mode backoff, using full 10-bits	RW	0x1
2	BACKOFF_RANDOM_TIME	only using 3-bits for backoff random timer	RW	0x0
1	DISABLE_BACK_OFF	Dont do back off priority : disbkoff > spdbkoff > unhbckoff > normal bkoff(9 bits)	RW	0x0
0	IPG_COMPENSATION	0:90ppm TX IPG compensation 1:65ppm TX IPG compensation	RW	0x0

## SWITCH\_MAC

REGISTER ADDRESS : 0xBB023060

DEFAULT VALUE : 0x0



Bits	Field	Description	Type	Default
63:48	RESERVED			
47:40	SWITCH_MAC5	switch mac{47:40}	RW	0x0
39:32	SWITCH_MAC4	switch mac{39:32}	RW	0x0
31:24	SWITCH_MAC3	switch mac{31:24}	RW	0x0
23:16	SWITCH_MAC2	switch mac{23:16}	RW	0x0
15:8	SWITCH_MAC1	switch mac{15:8}	RW	0x0
7:0	SWITCH_MAC0	switch mac{7:0}	RW	0x0

## SWITCH\_CTRL

REGISTER ADDRESS : 0xBB023068

DEFAULT VALUE : 0x3

Bits	Field	Description	Type	Default
31:2	RESERVED			
1	SHORT_IPG	cfg_ifgsel can be used	RW	0x1
0	PAUSE_MAX128	0:Maximum of 128 consecutive pause frames 1:Infinite pause frame count	RW	0x1

## INBW\_BOUND

REGISTER ADDRESS : 0xBB02306C

DEFAULT VALUE : 0xED

Bits	Field	Description	Type	Default
31:8	RESERVED			
7:4	HBOUND	Ingress Flow Control High Threshold Configuration. Ingress flow control high threshold = ((INBW_HBOUND « 16 Bytes)   0xFFF00000). If RX ports used space greater than and equal to ingress flow threshold, system will turn on flow control mechanism.	RW	0xE
3:0	LBOUND	Ingress Flow Control Low Threshold Configuration. Ingress flow control low threshold = ((INBW_LBOUND « 16 Bytes)   0xFFF00000). If RX ports used space less ingress flow threshold, system will turn off flow control mechanism.	RW	0xD

## MAX\_FIFO\_SIZE

REGISTER ADDRESS : 0xBB023070

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:4	RESERVED			
3:0	MAX_FIFO_SIZE	maximum packet drop command for ctrlckt from ale queued in drop fifo	RO	0x0

## P\_TX\_ERR\_CNT

BASE ADDRESS : 0xBB020000  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 0x400  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Bits	Field	Description	Type	Default
31:3	RESERVED			
2:0	TX_ERR_CNT	TX error packet counter. Re-calculate the CRC and compare to the original CRC. If mismatched, this counter+1	RO	0x0

## P\_CGSTTIMER

BASE ADDRESS : 0xBB020004  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 0x400  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	RX_DMA_ERR_FLAG	RX DMA Error Flag	RO	0x0

## P\_MISC

BASE ADDRESS : 0xBB020008  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 0x400  
 DEFAULT VALUE : 0x20

This is a One-Dimension Port Register Array.

Bits	Field	Description	Type	Default
31:6	RESERVED			
5	LATE_COL	0: late collision boundary is at 64 bytes. 1: late collision boundary is at 72 bytes.	RW	0x1
4	SMALL_TAG_IPG	Small IPG for tag insertion. 0b0 : No small IPG for tag insertion. 0b1 : IPG is reduced by 4 bytes if egress packet length is increased due to tag insertion.	RW	0x0
3	TX_ITFSP_MODE	TX itfsp monitor source selection between crs and rxdv. 0b0 : itfsp monitor source is crs. 0b1 : itfsp monitor source is rxdv.	RW	0x0
2	RX_SPC	enable received special packet which packet length is smaller than 64 bytes, or received packet is not byte alignment and L2 CRC errored packet 0b0:disable 0b1:enable	RW	0x0
1	CRC_SKIP	skip L2CRC check 0b0:disable 0b1:enable	RW	0x0
0	MAC_LOOPBACK	enable loopback from Tx to Rx in MAC 0b0:Disable mac loop-back function 0b1:enable mac loop-back function	RW	0x0

## P\_CFG\_FRC\_RATE

BASE ADDRESS : 0xBB02000C  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 0x400  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Bits	Field	Description	Type	Default
31:0	P_FORCE_RATE	force the current rate for rx ingress bandwidth control	RW	0x0

## P\_CUR\_RATE

BASE ADDRESS : 0xBB020010  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 0x400  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Bits	Field	Description	Type	Default
31:0	P_CURRENT_RATE	the current rate for rx ingress bandwidth control	RO	0x0

## UTP\_FIBER\_AUTODET

REGISTER ADDRESS : 0xBB0001BC

DEFAULT VALUE : 0x0

UTP and fiber auto detection

Bits	Field	Description	Type	Default
31:9	RESERVED			
8	PHY4_SDET	PHY4 signal detect	RO	0x0
7	FIB_SDET	fiber signal detect	RO	0x0
6	PHY4_DIS_RX	PHY4 disable RX	RW	0x0
5	PHY4_FRC_LKDN	PHY4 forced link down	RW	0x0
4	SDS_PWR_GATING	serdes power gating	RW	0x0
3	SDS_RX_DISABLE	serdes RX disable	RW	0x0
2	SDS_TX_DISABLE	serdes TX disable	RW	0x0
1	SDS_FRC_LD	serdes forced link down	RW	0x0
0	CKGPHY_SEL	0 - gphy PLL is not synced with serdes. 1 - gphy PLL is synced with serdes.	RW	0x0

### SECTION 2.2

## PHY & SERDES

PHY & Serdes module

## WSDS\_ANA\_00

REGISTER ADDRESS : 0xBB022000

DEFAULT VALUE : 0x5026

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:14	REG_BG		RW	0x1
13:12	REG_SPDSEL		RW	0x1
11	REG_RX_SD_POR_SEL		RW	0x0
10	REG_CDR_BYPASS_SDM_I NT		RW	0x0

Bits	Field	Description	Type	Default
9	REG_CDR_EN_LPF_MANUAL		RW	0x0
8	REG_LOOPBACK_EN		RW	0x0
7:5	REG_TX_EMP		RW	0x1
4	REG_CDR_RESET_MANUAL		RW	0x0
3	REG_CDR_RESET_SEL		RW	0x0
2	REG_RX_SEL_CDR_AFEN		RW	0x1
1	REG_CMU_BIG_KVCO_RX		RW	0x1
0	REG_CMU_BYPASS_PI_RX		RW	0x0

### WSDS\_ANA\_01

REGISTER ADDRESS : 0xBB022004

DEFAULT VALUE : 0x3

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:2	REG_CDR_INT_INIT		RW	0x0
1	REG_CMU_BYPASS_R2		RW	0x1
0	REG_CDR_KD		RW	0x1

### WSDS\_ANA\_02

REGISTER ADDRESS : 0xBB022008

DEFAULT VALUE : 0x2D18

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:13	REG_CDR_KI		RW	0x1
12:9	REG_EN_M_VALUE		RW	0x6
8:4	REG_ST_M_VALUE		RW	0x11
3:1	REG_CDR_KP1		RW	0x4
0	RESERVED			

### WSDS\_ANA\_03

REGISTER ADDRESS : 0xBB02200C

DEFAULT VALUE : 0x6001

Bits	Field	Description	Type	Default
31:16	RESERVED			

Bits	Field	Description	Type	Default
15	REG_PI_M_MODE		RW	0x0
14	REG_SQU_TRI		RW	0x1
13:12	REG_CDR_SEL_TESTOUT		RW	0x2
11:7	RESERVED			
6:4	REG_CDR_KP2		RW	0x0
3:1	RESERVED			
0	REG_CMU_EN_CKOOBS_RX		RW	0x1

## WSDS\_ANA\_04

REGISTER ADDRESS : 0xBB022010

DEFAULT VALUE : 0x7C

Bits	Field	Description	Type	Default
31:8	RESERVED			
7	REG_BG_OFF		RW	0x0
6	REG_BG_POW		RW	0x1
5	REG_CKDEGLITCH		RW	0x1
4	REG_CKOOBS_AUX		RW	0x1
3	REG_CMU_CP_NEW_CP_RX		RW	0x1
2	REG_CMU_LDO_EN_RX		RW	0x1
1	REG_CMU_VC_DLY_RX		RW	0x0
0	RESERVED			

## WSDS\_ANA\_05

REGISTER ADDRESS : 0xBB022014

DEFAULT VALUE : 0x4003

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	REG_ACC2_MANUAL		RW	0x0
14:5	REG_ACC2_PERIOD		RW	0x200
4:3	RESERVED			
2:0	REG_CMU_PI_I_SEL_RX		RW	0x3

## WSDS\_ANA\_06

REGISTER ADDRESS : 0xBB022018

DEFAULT VALUE : 0xFF

Bits	Field	Description	Type	Default
31:8	RESERVED			
7:4	REG_CMU_SEL_CP_I_RX_40M		RW	0xF
3:0	REG_CMU_SEL_CP_I_RX_25M		RW	0xF

## WSDS\_ANA\_07

REGISTER ADDRESS : 0xBB02201C

DEFAULT VALUE : 0x2490

Bits	Field	Description	Type	Default
31:15	RESERVED			
14:12	REG_CMU_SEL_R1_RX_40 M		RW	0x2
11:9	REG_CMU_SEL_R1_RX_25 M		RW	0x2
8	REG_CMU_SEL_DIV4_RX		RW	0x0
7	REG_CMU_SEL_FREF		RW	0x1
6:5	REG_CMU_SEL_PREDIV_R X		RW	0x0
4	REG_CMU_SEL_VCO_RX		RW	0x1
3:2	RESERVED			
1:0	REG_TX_SWING		RW	0x0

## WSDS\_ANA\_08

REGISTER ADDRESS : 0xBB022020

DEFAULT VALUE : 0x1B7

Bits	Field	Description	Type	Default
31:9	RESERVED			
8:6	REG_CMU_VSEL_LDO_A_R X		RW	0x6
5:3	REG_CMU_VSEL_LDO_D		RW	0x6
2	REG_COMINIT		RW	0x1
1	REG_COMWAKE		RW	0x1
0	REG_EN_CLKREQ		RW	0x1

## WSDS\_ANA\_09

REGISTER ADDRESS : 0xBB022024

DEFAULT VALUE : 0x5

Bits	Field	Description	Type	Default
31:4	RESERVED			
3	REG_EN_SATA		RW	0x0
2	REG_FORCE_RCVDDET		RW	0x1
1:0	REG_IBRXSEL		RW	0x1

## WSDS\_ANA\_0A

REGISTER ADDRESS : 0xBB022028

DEFAULT VALUE : 0x730C

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:14	REG_IBTXSEL		RW	0x1
13:12	REG_OOBS_CALI		RW	0x3
11	REG_OOBS_CALSEL		RW	0x0
10	REG_OOBS_CKSEL		RW	0x0
9	REG_OOBS_FORCECAL		RW	0x1
8	REG_OOBS_FREQSEL		RW	0x1
7	REG_OOBS_ISEL		RW	0x0
6	REG_OOBS_NSQDLY		RW	0x0
5	REG_OOBS_RXIDLE_MANU AL		RW	0x0
4	REG_OOBS_SEL		RW	0x0
3:0	REG_OOBS_SEN		RW	0xC

## WSDS\_ANA\_0B

REGISTER ADDRESS : 0xBB02202C

DEFAULT VALUE : 0x10C9

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:14	REG_RX_DBG_SEL		RW	0x0
13	REG_RX_DCVS_SEL		RW	0x0
12	REG_RX_EN_KOFFSET		RW	0x1
11	REG_RX_EN_SELF		RW	0x0
10	REG_RX_EN_TEST		RW	0x0
9	REG_RX_EQ_EN_SLICER		RW	0x0
8:7	REG_RX_EQ_GAIN		RW	0x1
6	REG_RX_EQ_HOLD		RW	0x1
5	REG_RX_EQ_SELREG		RW	0x0
4:3	REG_RX_EQ2SEL		RW	0x1



Bits	Field	Description	Type	Default
2	REG_RX_FORCERUN		RW	0x0
1	REG_RX_IDLE_SPD		RW	0x0
0	REG_RX_IQDSEL		RW	0x1

## WSDS\_ANA\_0C

REGISTER ADDRESS : 0xBB022030

DEFAULT VALUE : 0xE511

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:9	REG_RX_EQ_IN		RW	0x72
8:5	REG_RX_OFFSET_ADJR		RW	0x8
4	REG_RX_OFFSET_AUTO_K		RW	0x1
3:2	REG_RX_OFFSET_RANGE		RW	0x0
1	REG_RX_PIENSEL		RW	0x0
0	REG_RX_PS_AFE		RW	0x1

## WSDS\_ANA\_0D

REGISTER ADDRESS : 0xBB022034

DEFAULT VALUE : 0x828

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	REG_RX_PSAVE_SEL		RW	0x0
14	REG_RX_SEL_RXIDLE		RW	0x0
13:9	REG_RX_TIMER_BER		RW	0x04
8:4	REG_RX_TIMER_EQ		RW	0x02
3:2	REG_RXDSEL		RW	0x2
1:0	REG_SERDES_MODE		RW	0x0

## WSDS\_ANA\_0E

REGISTER ADDRESS : 0xBB022038

DEFAULT VALUE : 0x1566

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:11	REG_RX_TIMER_LPF		RW	0x02

Bits	Field	Description	Type	Default
10:8	REG_TX_AMP		RW	0x5
7:5	REG_TX_BAMP		RW	0x3
4	REG_TX_BEAEEN		RW	0x0
3:2	REG_TX_DLY		RW	0x1
1	REG_TX_EN_EMPHAS		RW	0x1
0	REG_TX_EN_TEST		RW	0x0

## WSDS\_ANA\_0F

REGISTER ADDRESS : 0xBB02203C

DEFAULT VALUE : 0x9

Bits	Field	Description	Type	Default
31:4	RESERVED			
3	REG_TX_EN_VCM_RES		RW	0x1
2	REG_TX_SEL_CKRD_DUTY		RW	0x0
1:0	REG_TX_SEL_VCM		RW	0x1

## WSDS\_ANA\_10

REGISTER ADDRESS : 0xBB022040

DEFAULT VALUE : 0x1185

Bits	Field	Description	Type	Default
31:13	RESERVED			
12:9	REG_Z0_NADJR		RW	0x8
8	REG_Z0_NAUTO_K		RW	0x1
7:3	REG_Z0_PADJR		RW	0x10
2	REG_Z0_PAUTO_K		RW	0x1
1	REG_Z0_TEST		RW	0x0
0	REG_Z0_TUNE		RW	0x1

## WSDS\_ANA\_11

REGISTER ADDRESS : 0xBB022044

DEFAULT VALUE : 0x4F80

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	REG_CMU_SEL_CP_RX		RW	0x0

Bits	Field	Description	Type	Default
14:10	REG_OOBS_SEN_VAR		RW	0x13
9	REG_SEL_IBLPF		RW	0x1
8	REG_RX50_LINK		RW	0x1
7	REG_TX_50_EN		RW	0x1
6:0	RESERVED			

## WSDS\_ANA\_12

REGISTER ADDRESS : 0xBB022048  
DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	DMY0		RW	0x0

## WSDS\_ANA\_13

REGISTER ADDRESS : 0xBB02204C  
DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	DMY1		RW	0x0

## WSDS\_ANA\_14

REGISTER ADDRESS : 0xBB022050  
DEFAULT VALUE : 0x265D

Bits	Field	Description	Type	Default
31:14	RESERVED			
13	REG_CMU_CP_NEW_EN_TX		RW	0x1
12:9	REG_CMU_SEL_CP_I_TX		RW	0x3
8	REG_CMU_SEL_CP_TX		RW	0x0
7:5	REG_CMU_SEL_RS_TX		RW	0x2
4	REG_CMU_BIG_KVCO_TX		RW	0x1
3	REG_CMU_SEL_VCO_TX		RW	0x1
2	REG_CMU_LDO_EN_TX		RW	0x1
1	REG_CMU_VC_DLY_TX		RW	0x0
0	REG_CMU_BYPASS_PL_TX		RW	0x1

## WSDS\_ANA\_15

REGISTER ADDRESS : 0xBB022054

DEFAULT VALUE : 0x3072

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	REG_CMU_EN_GPHY		RW	0x0
14:12	REG_CMU_PI_I_SEL_TX		RW	0x3
11	REG_PREDIV_BYPASS_TX		RW	0x0
10:8	RESERVED			
7:5	REG_CMU_LDO_VREFSEL_TX		RW	0x3
4:0	REG_CMU_PREDIV_TX		RW	0x12

## WSDS\_ANA\_16

REGISTER ADDRESS : 0xBB022058

DEFAULT VALUE : 0x2000

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:13	REG_CMU_PREDIV_GPHY		RW	0x1
12:2	RESERVED			
1:0	REG_CMU_SEL_CP_GPHY		RW	0x0

## WSDS\_ANA\_17

REGISTER ADDRESS : 0xBB02205C

DEFAULT VALUE : 0x66

Bits	Field	Description	Type	Default
31:10	RESERVED			
9:5	REG_CMU_POSTDIV_GPHY_40M		RW	0x03
4:0	REG_CMU_POSTDIV_GPHY_25M		RW	0x06

## WSDS\_ANA\_18

REGISTER ADDRESS : 0xBB022060

DEFAULT VALUE : 0xA8C2

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:13	REG_BEN_SWING		RW	0x5
12	REG_BEN_SEL_CML		RW	0x0
11:10	REG_BEN_V20_SEL		RW	0x2
9	REG_RX_EN_I_SAMPLER		RW	0x0
8	RESERVED			
7	REG_CMU_TX_OFF		RW	0x1
6:4	REG_RX_KP1_2		RW	0x4
3:2	REG_RX_KP_DIV		RW	0x0
1:0	REG_TX_CLK_SEL		RW	0x2

## WSDS\_ANA\_19

REGISTER ADDRESS : 0xBB022064

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:14	RESERVED			
13	TX_DISABLE_OPTIC	0: TX_DISABLE_OPTIC PAD is external pull down 1: TX_DISABLE_OPTIC PAD is external pull up	RO	0x0
12	CKRDY_GPHY	0: rx clock from analog not stable 1: rx clock from analog stable	RO	0x0
11	BER_NOTIFY	0: analog cdr no lock 1: analog cdr lock	RO	0x0
10:4	REG_RX_EQ_FILTER_OUT		RO	0x0
3:0	REG_RX_OFFSET_CODE		RO	0x0

## WSDS\_ANA\_1A

REGISTER ADDRESS : 0xBB022068

DEFAULT VALUE : 0xDDE0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	REG_RX_SEL_SD		RW	0x1
14:13	REG_TX_V20_SEL		RW	0x2
12:5	REG_DIVN_GPHY_REF		RW	0xEF
4	REG_RX_ACC2_MANUAL_2		RW	0x0
3	REG_RX_SQU_TRI_2		RW	0x0
2:0	REG_RX_KP2_2		RW	0x0

## WSDS\_ANA\_1B

REGISTER ADDRESS : 0xBB02206C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:10	RESERVED			
9:0	REG_RX_ACC2_PERIOD_2		RW	0x0

## WSDS\_ANA\_1C

REGISTER ADDRESS : 0xBB022070

DEFAULT VALUE : 0x8

Bits	Field	Description	Type	Default
31:8	RESERVED			
7:0	REG_RX_FILT_CONFIG		RW	0x08

## WSDS\_ANA\_1D

REGISTER ADDRESS : 0xBB022074

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:14	RESERVED			
13:0	REG_RX_INT_INIT_2		RW	0x0

## WSDS\_ANA\_1E

REGISTER ADDRESS : 0xBB022078

DEFAULT VALUE : 0x5450

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:13	REG_CMU_AD_P_TIME_GPHY		RW	0x2
12	REG_CMU_AUTO_K_GPHY		RW	0x1
11:9	REG_CMU_CALIB_TIME_GPHY		RW	0x2
8:6	REG_CMU_CP_TIME_GPHY		RW	0x1
5:0	REG_CMU_DIVIDE_NUM_GPHY		RW	0x10

Bits	Field	Description	Type	Default
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## WSDS\_ANA\_1F

REGISTER ADDRESS : 0xBB02207C

DEFAULT VALUE : 0xC970

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	REG_CMU_FLD_DSEL_GPHY		RW	0x1
14:11	REG_CMU_ICP_SEL_GPHY		RW	0x9
10:8	REG_CMU_INIT_TIME_GPHY		RW	0x1
7:6	REG_CMU_ISTANK_SEL_GPHY		RW	0x1
5	REG_CMU_LCBIAS_LPF_EN_GPHY		RW	0x1
4:0	REG_CMU_LCVCO_TR_GPHY		RW	0x10

## WSDS\_ANA\_20

REGISTER ADDRESS : 0xBB022080

DEFAULT VALUE : 0x267

Bits	Field	Description	Type	Default
31:10	RESERVED			
9:0	REG_CMU_LOCK_DN_LIMIT_GPHY		RW	0x267

## WSDS\_ANA\_21

REGISTER ADDRESS : 0xBB022084

DEFAULT VALUE : 0x27B

Bits	Field	Description	Type	Default
31:10	RESERVED			
9:0	REG_CMU_LOCK_UP_LIMIT_GPHY		RW	0x27B

## WSDS\_ANA\_22

REGISTER ADDRESS : 0xBB022088  
DEFAULT VALUE : 0x5D80

Bits	Field	Description	Type	Default
31:15	RESERVED			
14:10	REG_CMU_N_PLL_GPHY		RW	0x17
9:2	REG_CMU_N_PLL_TX		RW	0x60
1:0	RESERVED			

## WSDS\_ANA\_23

REGISTER ADDRESS : 0xBB02208C  
DEFAULT VALUE : 0x608

Bits	Field	Description	Type	Default
31:12	RESERVED			
11:9	REG_CMU_SEL_R_GPHY		RW	0x3
8:4	RESERVED			
3:1	REG_CMU_VSEL_LREG_GPHY		RW	0x4
0	REG_SEL_IBN		RW	0x0

## WSDS\_ANA\_24

REGISTER ADDRESS : 0xBB022090  
DEFAULT VALUE : 0x3C0

Bits	Field	Description	Type	Default
31:14	RESERVED			
13:12	REG_FREF_SEL_GPHY		RW	0x0
11:10	REG_TTL_DRI_SEL		RW	0x0
9	REG_BEN_TTL_OUT		RW	0x1
8	REG_CMU_AUTO_MODE_GPHY		RW	0x1
7	REG_CMU_CALIB_LATE_GPHY		RW	0x1
6	REG_CMU_CALIB_MANUAL_GPHY		RW	0x1
5	REG_CMU_CP_ADJ_EN_GPHY		RW	0x0
4	REG_CMU_CP_EN_MANUAL_GPHY		RW	0x0
3	REG_CMU_EN_TX		RW	0x0
2	REG_CMU_START_EN_GPHY_MANUAL		RW	0x0



Bits	Field	Description	Type	Default
1	REG_CMU_WD_ENABLE_GPHY		RW	0x0
0	REG_TX_DBG_SEL		RW	0x0

## WSDS\_ANA\_25

REGISTER ADDRESS : 0xBB022094

DEFAULT VALUE : 0x1240

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:14	REG_CMU_F390K_GPHY		RW	0x0
13:12	REG_CMU_LC_BUF_SEL_GPHY		RW	0x1
11:9	REG_CMU_TIME0_CK_GPHY		RW	0x1
8:7	REG_CMU_TIME2_RST_WIDTH_GPHY		RW	0x0
6:5	REG_CMU_TIME_RDY_CKOUT_GPHY		RW	0x2
4:0	REG_CMU_VCO_COARSE_GPHY		RW	0x0

## WSDS\_DIG\_00

REGISTER ADDRESS : 0xBB022098

DEFAULT VALUE : 0xF30

Bits	Field	Description	Type	Default
31:12	RESERVED			
11	CFG_SFT_RSB_ANA	0: software reset sds analog 1: no software reset sds analog	RW	0x1
10	CFG_SFT_RSTB_GPON	0: software reset gpon mac 1: no software reset gpon_mac	RW	0x1
9	CFG_SFT_RSTB_EPON	0: software reset epon mac 1: no software reset epon_mac	RW	0x1
8	CFG_SFT_RSTB	0: software reset all wrap_sds 1: no software reset all wrap_sds	RW	0x1
7	CFG_FRCV_155M_EN		RW	0x0
6	CFG_FRC_155M_EN		RW	0x0
5	CFG_FRCV_125M_EN		RW	0x1
4	CFG_FRC_125M_EN		RW	0x1
3	CFG_FRCV_GMIICK_EN		RW	0x0
2	CFG_FRC_GMIICK_EN		RW	0x0
1	CFG_TXDIS_SEL		RW	0x0

Bits	Field	Description	Type	Default
0	CFG_STOP_CLK	0: no stop clock to swcore 1: stop clock to swcore	RW	0x0

## WSDS\_DIG\_01

REGISTER ADDRESS : 0xBB02209C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:14	CFG_FRC_CMUEN		RW	0x0
13:12	CFG_FRC_CMUEN_TX		RW	0x0
11:10	CFG_FRC_RX_OOBS_EN		RW	0x0
9:8	CFG_FRC_V2ANALOG		RW	0x0
7:6	CFG_FRC_PDOWN		RW	0x0
5:4	CFG_FRC_RX_EN		RW	0x0
3:2	CFG_FRC_NOTIFY		RW	0x0
1:0	CFG_FRC_RXIDLE		RW	0x0

## WSDS\_DIG\_02

REGISTER ADDRESS : 0xBB0220A0

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:10	RESERVED			
9	CFG_FRCV_SEL_FX100		RW	0x0
8	CFG_FRC_SEL_FX100		RW	0x0
7	CFG_SDS_PHY_MODE		RW	0x0
6	FRC_REG4_EN		RW	0x0
5	FRC_REG4_FIB100		RW	0x0
4	CFG_LPI_GMII_SEL		RW	0x0
3:0	CFG_CMD_STOP_GLI_CLK		RW	0x0

## WSDS\_DIG\_03

REGISTER ADDRESS : 0xBB0220A4

DEFAULT VALUE : 0x40

Bits	Field	Description	Type	Default
31:7	RESERVED			

Bits	Field	Description	Type	Default
6:4	CFG_TXDIS_SEL_DLY		RW	0x4
3:0	CFG_D2ANLOG_SEL		RW	0x0

## WSDS\_DIG\_04

REGISTER ADDRESS : 0xBB0220A8

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:3	RESERVED			
2	CFG_AFE_LPK_EN		RW	0x0
1	CFG_DIG_LPK_EN		RW	0x0
0	CFG_RMT_LPK_EN		RW	0x0

## WSDS\_DIG\_05

REGISTER ADDRESS : 0xBB0220AC

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	CFG_DMY0		RW	0x0

## WSDS\_DIG\_06

REGISTER ADDRESS : 0xBB0220B0

DEFAULT VALUE : 0xFF

Bits	Field	Description	Type	Default
31:0	CFG_DMY1		RW	0x000000FF

## WSDS\_DIG\_07

REGISTER ADDRESS : 0xBB0220B4

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	CFG_DBG_TRAN_SEL		RW	0x0

## WSDS\_DIG\_08

REGISTER ADDRESS : 0xBB0220B8

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:8	RESERVED			
7	CFG_BYPASS_PI_RX		RW	0x0
6	RESERVED			
5	CFG_EN_CENTER_IN_RX		RW	0x0
4	RESERVED			
3	CFG_EN_SSC_RX		RW	0x0
2	RESERVED			
1	CFG_ORDER_RX		RW	0x0
0	RESERVED			

## WSDS\_DIG\_09

REGISTER ADDRESS : 0xBB0220BC

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	CFG_SEL_MODE_RX		RW	0x0
14	RESERVED			
13:11	CFG_WTG_SEL_RX		RW	0x0
10:8	RESERVED			
7	CFG_FRC_POW_SSCD_RX		RW	0x0
6	RESERVED			
5	CFG_FRC_N_PLL_RX		RW	0x0
4	RESERVED			
3	CFG_FRC_PH_SEL_RX		RW	0x0
2	RESERVED			
1	CFG_FRCV_POW_SSCD_RX		RW	0x0
0	RESERVED			

## WSDS\_DIG\_0A

REGISTER ADDRESS : 0xBB0220C0

DEFAULT VALUE : 0x886

Bits	Field	Description	Type	Default
31:12	RESERVED			

Bits	Field	Description	Type	Default
11:0	CFG_F_CODE_RX_25M		RW	0x886

## WSDS\_DIG\_0B

REGISTER ADDRESS : 0xBB0220C4

DEFAULT VALUE : 0x353

Bits	Field	Description	Type	Default
31:12	RESERVED			
11:0	CFG_F_CODE_RX_40M		RW	0x353

## WSDS\_DIG\_0C

REGISTER ADDRESS : 0xBB0220C8

DEFAULT VALUE : 0x5F

Bits	Field	Description	Type	Default
31:9	RESERVED			
8:0	CFG_N_CODE_RX_25M		RW	0x05F

## WSDS\_DIG\_0D

REGISTER ADDRESS : 0xBB0220CC

DEFAULT VALUE : 0x3A

Bits	Field	Description	Type	Default
31:9	RESERVED			
8:0	CFG_N_CODE_RX_40M		RW	0x03A

## WSDS\_DIG\_0E

REGISTER ADDRESS : 0xBB0220D0

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:13	RESERVED			
12:0	CFG_STEP_IN_RX		RW	0x0

**WSDS\_DIG\_0F**

REGISTER ADDRESS : 0xBB0220D4

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:12	RESERVED			
11:0	CFG_TBASE_RX		RW	0x0

**WSDS\_DIG\_10**

REGISTER ADDRESS : 0xBB0220D8

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:9	RESERVED			
8:0	CFG_FRCV_N_PLL_RX		RW	0x0

**WSDS\_DIG\_11**

REGISTER ADDRESS : 0xBB0220DC

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	CFG_FRCV_PH_SEL_RX		RW	0x0

**WSDS\_DIG\_12**

REGISTER ADDRESS : 0xBB0220E0

DEFAULT VALUE : 0x1E4

Bits	Field	Description	Type	Default
31:12	RESERVED			
11	CFG_WD_ENABLE_RX		RW	0x0
10	CFG_WD_ENABLE_TX		RW	0x0
9	RESERVED			
8:7	CFG_F390K_RX		RW	0x3
6:5	CFG_F390K_TX		RW	0x3
4:3	RESERVED			
2:0	CFG_TIME0_CK_RX		RW	0x4

Bits	Field	Description	Type	Default
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## WSDS\_DIG\_13

REGISTER ADDRESS : 0xBB0220E4

DEFAULT VALUE : 0x2000

Bits	Field	Description	Type	Default
31:14	RESERVED			
13:11	CFG_TIME0_CK_TX		RW	0x4
10:8	RESERVED			
7:6	CFG_T_RDY_CKOUT_RX		RW	0x0
5:4	CFG_T_RDY_CKOUT_TX		RW	0x0
3:2	RESERVED			
1:0	CFG_T2_RST_WIDTH_RX		RW	0x0

## WSDS\_DIG\_14

REGISTER ADDRESS : 0xBB0220E8

DEFAULT VALUE : 0x186

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:14	CFG_T2_RST_WIDTH_TX		RW	0x0
13:12	RESERVED			
11	CFG_FRC_CKRDY_RX		RW	0x0
10	CFG_FRC_CKRDY_TX		RW	0x0
9	RESERVED			
8	CFG_FRCV_CKRDY_RX		RW	0x1
7	CFG_FRCV_CKRDY_TX		RW	0x1
6	RESERVED			
5	CFG_FRC_N911_B_RX		RW	0x0
4	CFG_FRC_N911_B_TX		RW	0x0
3	RESERVED			
2	CFG_FRCV_N911_B_RX		RW	0x1
1	CFG_FRCV_N911_B_TX		RW	0x1
0	RESERVED			

## WSDS\_DIG\_15

REGISTER ADDRESS : 0xBB0220EC

DEFAULT VALUE : 0x2

Bits	Field	Description	Type	Default
31:4	RESERVED			
3	CFG_CLKREQB		RW	0x0
2	CFG_RCV_DETECT		RW	0x0
1	CFG_RXIDLE_D		RW	0x1
0	CFG_TXBEACON		RW	0x0

## WSDS\_DIG\_16

REGISTER ADDRESS : 0xBB0220F0  
DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	CFG_WRAP_SDS_DBG_SEL		RW	0x0

## WSDS\_DIG\_17

REGISTER ADDRESS : 0xBB0220F4  
DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:2	RESERVED			
1:0	CFG_FRC_BYP_EPMC		RW	0x0

## WSDS\_DIG\_18

REGISTER ADDRESS : 0xBB0220F8  
DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:13	RESERVED			
12	BEN_OE		RW	0x0
11	TX_DISABLE_OPTIC_OE		RW	0x0
10	CFG_FRC_OPTIC_LOS_IN V		RW	0x0
9	CFG_FRC_CDR_LOS_INV		RW	0x0
8	CFG_FRC_TX_DISABLE_O PTIC_INV		RW	0x0
7:6	CFG_FRC_TX_DISABLE_O PTIC		RW	0x0
5	CFG_FRC_TX_OPTIC_SD_ INV		RW	0x0



Bits	Field	Description	Type	Default
4:3	CFG_FRC_TX_OPTIC_SD		RW	0x0
2	CFG_FRC_BEN_INV		RW	0x0
1:0	CFG_FRC_BEN		RW	0x0

## WSDS\_DIG\_19

REGISTER ADDRESS : 0xBB0220FC

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	CFG_PRBS_TYPE_SEL		RW	0x0

## WSDS\_DIG\_1A

REGISTER ADDRESS : 0xBB022100

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	CFG_PRBS_EN		RW	0x0

## WSDS\_DIG\_1B

REGISTER ADDRESS : 0xBB022104

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	CFG_PRBS_ERRORS		RO	0x0

## WSDS\_DIG\_1C

REGISTER ADDRESS : 0xBB022108

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	CFG_PRBS_STATUS		RO	0x0

Bits	Field	Description	Type	Default
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## WSDS\_DIG\_1D

REGISTER ADDRESS : 0xBB02210C

DEFAULT VALUE : 0x4000

Bits	Field	Description	Type	Default
31:15	RESERVED			
14	CFG_SFT_RSTB_INF		RW	0x1
13	CFG_FRC_CLK_EN		RW	0x0
12	CFG_FRCV_CLK_EN		RW	0x0
11:9	CFG_TX_WRPT_DN_SEL		RW	0x0
8:6	CFG_RX_WRPT_DN_SEL		RW	0x0
5	CFG_BEN_INV		RW	0x0
4	CFG_HAM_PTR		RW	0x0
3	CFG_ERRHAM_EN		RW	0x0
2:0	CFG_FREE_CNT_SEL		RW	0x0

## WSDS\_DIG\_1E

REGISTER ADDRESS : 0xBB022110

DEFAULT VALUE : 0x82

Bits	Field	Description	Type	Default
31:11	RESERVED			
10	CFG_A2D16_INV		RW	0x0
9	CFG_D2A16_INV		RW	0x0
8	CFG_RSTB_BITERR_INV		RW	0x0
7	CFG_FRCV_RSTB_BITERR		RW	0x1
6	CFG_FRC_RSTB_BITERR		RW	0x0
5	CFG_ANALOG2D_SEL		RW	0x0
4	CFG_D2ANLOG_INF_SEL		RW	0x0
3:0	CFG_622_START_SEL		RW	0x2

## WSDS\_DIG\_1F

REGISTER ADDRESS : 0xBB022114

DEFAULT VALUE : 0x37256E5

Bits	Field	Description	Type	Default
31:26	RESERVED			

Bits	Field	Description	Type	Default
25	CFG_CLR_T1_FULL		RW	0x1
24	CFG_CLR_T0_FULL		RW	0x1
23:18	CFG_T1_DIF_MIN		RW	0x1C
17:12	CFG_T1_DIF_MAX		RW	0x25
11:6	CFG_T0_DIF_MIN		RW	0x1B
5:0	CFG_T0_DIF_MAX		RW	0x25

## WSDS\_DIG\_20

REGISTER ADDRESS : 0xBB022118

DEFAULT VALUE : 0x182A

Bits	Field	Description	Type	Default
31:13	RESERVED			
12	CFG_CLR_R0_FULL		RW	0x1
11:6	CFG_R0_DIF_MIN		RW	0x20
5:0	CFG_R0_DIF_MAX		RW	0x2A

## WSDS\_DIG\_21

REGISTER ADDRESS : 0xBB02211C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:26	RESERVED			
25	T1_FULL		RO	0x0
24	T0_FULL		RO	0x0
23:18	T1_DIF_MIN		RO	0x0
17:12	T1_DIF_MAX		RO	0x0
11:6	T0_DIF_MIN		RO	0x0
5:0	T0_DIF_MAX		RO	0x0

## WSDS\_DIG\_22

REGISTER ADDRESS : 0xBB022120

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:13	RESERVED			
12	R0_FULL		RO	0x0

Bits	Field	Description	Type	Default
11:6	R0_DIF_MIN		RO	0x0
5:0	R0_DIF_MAX		RO	0x0

### WSDS\_DIG\_23

REGISTER ADDRESS : 0xBB022124

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	CFG_SDSINF_DMYRD_0		RO	0x0

### WSDS\_DIG\_24

REGISTER ADDRESS : 0xBB022128

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	CFG_WRAP_DMYRD_0		RO	0x0

### WSDS\_DIG\_25

REGISTER ADDRESS : 0xBB02212C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	CFG_WRAP_DMYRD_1		RO	0x0

### WSDS\_DIG\_26

REGISTER ADDRESS : 0xBB022130

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	CFG_WRAP_DMYRD_2		RO	0x0

### WSDS\_DIG\_27

REGISTER ADDRESS : 0xBB022134

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	CFG_WRAP_DMYRD_3		RO	0x0

## WSDS\_DIG\_28

REGISTER ADDRESS : 0xBB022138

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	CFG_WRAP_DMYRD_4		RO	0x0

## WSDS\_DIG\_29

REGISTER ADDRESS : 0xBB02213C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	CFG_WRAP_DMY_0		RW	0x0

## WSDS\_DIG\_2A

REGISTER ADDRESS : 0xBB022140

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	CFG_WRAP_DMY_1		RW	0x0

## WSDS\_DIG\_2B

REGISTER ADDRESS : 0xBB022144

DEFAULT VALUE : 0xFFFF

Bits	Field	Description	Type	Default
31:0	CFG_WRAP_DMY_2		RW	0x0000FFFF

## WSDS\_DIG\_2C

REGISTER ADDRESS : 0xBB022148

DEFAULT VALUE : 0xFFFF

Bits	Field	Description	Type	Default
31:0	CFG_WRAP_DMY_3		RW	0x0000FFFF

## SDS\_REG0

REGISTER ADDRESS : 0xBB022800

DEFAULT VALUE : 0x403

Bits	Field	Description	Type	Default
31:15	RESERVED			
14	DUMMY_00	dummy_00	RW	0x0
13	BYP_8B10B	bypass the 8b10b encode/decode 0: normal 1: bypass the 8b10b encode/decode	RW	0x0
12	CDET	dynamic comma detect function enable when alignment is done cdet[0] = 1'b0: auto mode cdet[0] = 1'b1: force mode, the force value is cdet[1]	RW	0x0
11	DIS_TMR_CMA	disable comma timeout monitor function 0: enable comma timeout monitor 1: disable comma timeout monitor	RW	0x0
10	DUMMY_01	dummy_01	RW	0x1
9	INV_HSI	invert the serdes input 20-bit data (polarity change manually) 0: normal 1: invert the input 20-bit data	RW	0x0
8	INV_HSO	invert the serdes output 20-bit data (polarity change manually) 0: normal 1: invert the output 20-bit data	RW	0x0
7:6	SDS_SDET_DEG	sds_sdet input deglitch or not 00: disable the deglitch function 01: tolerant 4 cycle glitch 10: tolerant 8 cycle glitch 11: tolerant 16 cycle glitch	RW	0x0
5	CODEC_LPK	digital codec loopback, loopback after the 8b10b encode in 10b domain	RW	0x0
4	AFE_LPK	digital afe loopback, loopback just behind the analog AFE	RW	0x0
3	REMOTE_LPK	analog remote loopback, loopback just come into the digital circuit	RW	0x0
2	SDS_TX_DOWN	serdes TX down, the d2analog 20-bit data will be zero	RW	0x0
1	SDS_EN_RX	serdes enable RX	RW	0x1
0	SDS_EN_TX	serdes enable TX	RW	0x1

## SDS\_REG1

REGISTER ADDRESS : 0xBB022804

DEFAULT VALUE : 0xF00

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:12	DUMMY_02	dummy_02	RW	0x0
11:8	SDS_FRC_RX	serdes force RX for 4-port 0: disable N-way (force RX) 1: enable N-way	RW	0xF
7:4	DUMMY_03	dummy_03	RW	0x0
3:0	SDS_FRC_TX	serdes force TX for 4-port 0: normal 1: force TX, even if not receive any signal	RW	0x0

## SDS\_REG2

REGISTER ADDRESS : 0xBB022808

DEFAULT VALUE : 0x7000

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:14	FRC_PRAMBLE	force insert preamble for solving the lose preamble issue frc_preamble[0] = 1'b0: auto mode frc_preamble[0] = 1'b1: force mode, the force value is frc_preamble[1]	RW	0x1
13:12	FRC_IPG	force insert IPG for solving the lose preamble issue frc_ipg[0] = 1'b0: auto mode frc_ipg[0] = 1'b1: force mode, the force value is frc_ipg[1]	RW	0x3
11:10	FRC_CGGOOD	force code-group good frc_cggo0{0} = 1'b0: auto mode frc_cggood{0} = 1'b1: force mode, the force value is frc_cggood{1}	RW	0x0
9:8	SDS_FRC_AN	serdes force N-way enable/disable sds_frc_an{0} = 1'b0: auto mode sds_frc_an{0} = 1'b1: force mode, the force value is sds_frc_an{1}	RW	0x0
7:4	DUMMY_04	cfg_dummy_04	RW	0x0
3:0	SDS_RESATRT_AN	serdes restart N-way for 4-port 0: normal 1: restart N-way	RW	0x0

## SDS\_REG3

REGISTER ADDRESS : 0xBB02280C

DEFAULT VALUE : 0x7106

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	WR_COFT_RSTB	write software soft-reset 0: normal 1: write soft-reset, write 8 times then trigger software soft-reset	RW	0x0
14	USE_25M_CLK	When CMU_EN = 1'b0, MAC gtxc/grxc will be zero, we can let gtxc/grxc be a free-run 25MHz clock 0: gtxc/grxc no clock when CMU_EN = 1'b0 1: gtxc/grxc is 25MHz when CMU_EN = 1'b0	RW	0x1
13	MARK_CARR_EXT	mark the carrier extend error issue, e2s_d0 = 10'h20f will be marked as 10'h00f	RW	0x1
12	SEL_DEG	select deglich circuit for e2s_ck and s2e_ck 0: without deglich circuit 1: with deglich circuit	RW	0x1
11:8	REG_CALIB_OK_CNT	U55 serdes IP will not support "CALIB_OK" to indicate that the CLKWR is ready, so we generate "CALIB_OK" by ourself. The signal will be generated after negedge of "RXIDLE" X us. The X is defined as follows. 0: calib_ok always 1'b1 1 15: calib_ok is delay	RW	0x1
7	EXT_PWR_CTL	CMU_EN/PDOWN/ the power saving related control 0: will be affected by sds_frc_ld, sds_en_rx, sds_en_tx 1: will not be affected	RW	0x0
6	SOFT_RST	level software-reset 0: normal 1: do level software-reset	RW	0x0
5	CLR_SOFT_RSTB	clear software soft-reset, soft-reset need the write soft-reset counter to be 8 timer, clear soft-reset means to clear the soft-reset counter 0: normal 1: clear the soft-reset counter	RW	0x0
4:0	CMA_RQ	number of comma should be received for alignment	RW	0x06

## SDS\_REG4

REGISTER ADDRESS : 0xBB022810

DEFAULT VALUE : 0x749

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:13	CFG_FRC_SDS_MODE	force sds_mode enable 3'd3: fib1g 3'd5: fib100 3'd7: fib100/fib1g auto_det	RW	0x0



Bits	Field	Description	Type	Default
12	CFG_FRC_SDS_MODE_EN	force sds_mode enable	RW	0x0
11:8	CFG_UPD_RXD	control the sample point of crxd(from codec_8b10b) to grxd(gmii) 4'd3: sample crxd 24ns later (after crxd transiton)	RW	0x7
7:4	CFG_UPD_TXD	control the sample point of gtxd(gmii) to ctxd(to codec_8b10b) 4'd4: sample gtxd 32ns later (after gtxd transiton)	RW	0x4
3	CFG_UPD_RXD_DYN	1'b1: rate_adpt update rxd dynamic 1'b0: rate_adpt update rxd according to cfg_upd_rxd	RW	0x1
2	CFG_EN_LINK_FIB1G	fix one_giga disable N-way linkon issue	RW	0x0
1	DUMMY_05	fix one_giga disable N-way linkon issue	RW	0x0
0	DUMMY_06	modify sgmi clock select	RW	0x1

## SDS\_REG5

REGISTER ADDRESS : 0xBB022814

DEFAULT VALUE : 0x8E80

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	LPI_TRANSMIT_STYLE	EEE lpi command transmit when changed	RW	0x1
14:12	DUMMY_07	dummy_07	RW	0x0
11	DUMMY_08	dummy_08	RW	0x1
10	DUMMY_09	dummy_09	RW	0x1
9	DUMMY_0A	dummy_0A	RW	0x1
8	DUMMY_0B	dummy_0B	RW	0x0
7:4	DUMMY_0C	dummy_0C	RW	0x8
3:0	DUMMY_0D	dummy_0D	RW	0x0

## SDS\_REG6

REGISTER ADDRESS : 0xBB022818

DEFAULT VALUE : 0x8F0F

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:12	DUMMY_0E	dummy_0E	RW	0x8
11:8	RX_BYPSR	Scrambler RX bypass, 4-bit for {ch3, ch2, ch1, ch0} 0: RX enable scrambler 1: RX disable scrambler	RW	0xF
7:4	DUMMY_0F	dummy_0F	RW	0x0

Bits	Field	Description	Type	Default
3:0	TX_BYPSCR	Scrambler TX bypass, 4-bit for {ch3, ch2, ch1, ch0} 0: TX enable scrambler 1: TX disable scrambler	RW	0xF

## SDS\_REG7

REGISTER ADDRESS : 0xBB02281C

DEFAULT VALUE : 0x5359

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:11	DUMMY_10	dummy_10	RW	0x0A
10	CFG_LPI_CMD_MII	lpi command support mii interface	RW	0x0
9	CFG_MARK_RXSCR_ERR	mark the carrier error when enable scrambler 0: disable "mark the carrier error" 1: enable "mark the carrier error"	RW	0x1
8	CFG_MARK_TXSCR_ERR	mark the carrier error when enable scrambler 0: disable "mark the carrier error" 1: enable "mark the carrier error"	RW	0x1
7:4	BYP_START	Scrambler bypass start, which is to generate the scrambler mask, (this function is done for being compatible with old serdes architecture) 0 9: to mask the bit position 0 9	RW	0x5
3:0	BYP_END	Scrambler bypass end, which is to generate the scrambler mask, (this function is done for being compatible with old serdes architecture) 0 9: to mask the bit position 0 9	RW	0x9

## SDS\_REG8

REGISTER ADDRESS : 0xBB022820

DEFAULT VALUE : 0x524B

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	DUMMY_11	dummy_11	RW	0x0
14	DUMMY_12	dummy_12	RW	0x1
13:11	DUMMY_13	dummy_13	RW	0x2
10:8	DUMMY_14	dummy_14	RW	0x2
7:5	DUMMY_15	dummy_15	RW	0x2
4:2	DUMMY_16	dummy_16	RW	0x2
1	DUMMY_17	dummy_17	RW	0x1
0	DUMMY_18	dummy_18	RW	0x1

## SDS\_REG9

REGISTER ADDRESS : 0xBB022824

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	CFG_EEE_PROGRAM_0	force mode of lpi control signal	RW	0x0

## SDS\_REG10

REGISTER ADDRESS : 0xBB022828

DEFAULT VALUE : 0x8CA4

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	DUMMY_19	dummy_19	RW	0x8CA4

## SDS\_REG11

REGISTER ADDRESS : 0xBB02282C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	DUMMY_1C	dummy_1c	RO	0x0

## SDS\_REG12

REGISTER ADDRESS : 0xBB022830

DEFAULT VALUE : 0x8E4

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:8	DUMMY_1D	dummy_1d	RW	0x08
7:4	ABLITY	serdes ability = {5G, 2.5G, 1.25G} ability{0} = 1'b0: auto mode ability{0} = 1'b1: force mode, the force value is ability{3:1}	RW	0xE
3	DUMMY_1E	dummy_1e	RW	0x0
2	DUMMY_1F	dummy_1f	RW	0x1

Bits	Field	Description	Type	Default
1	DUMMY_20	dummy_20	RW	0x0
0	SEND_NP_ON	send next page on, the next page of serdes N-way 0: serdes N-way will only send base page register 1: serdes N-way will send next page register after base page register	RW	0x0

### SDS\_REG13

REGISTER ADDRESS : 0xBB022834

DEFAULT VALUE : 0x4664

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:8	DUMMY_21	dummy_21	RW	0x46
7:0	DUMMY_22	dummy_22	RW	0x64

### SDS\_REG14

REGISTER ADDRESS : 0xBB022838

DEFAULT VALUE : 0x2053

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	CGF_SPDUP	when asserted high, the timer inside sds_port will be put into speed-up mode (for simulation usage)	RW	0x0
14:10	DUMMY_23	dummy_23	RW	0x08
9	CFG_SEL_ODD_BIT	select cma_det operating on half_rate mode	RW	0x0
8	CFG_FRC_LD_VALUE	sds_frc_ld value in force mode 1'b1: sds_frc_ld high 1'b0: sds_frc_ld low	RW	0x0
7	CFG_FRC_LD	select sds_frc_ld control in force mode 1'b0: sds_frc_ld driven by input 1'b1: sds_frc_ld driven by cfg_frc_ld_value	RW	0x0
6	DUMMY_24	dummy_24	RW	0x1
5:3	DUMMY_25	dummy_25	RW	0x2
2:0	CFG_LINK_TMR_NORM_SE L	select link_timer_done (not SGMII) 3'd0: 8ms 3'd1: 9ms 3'd2: 10ms 3'd3: 11ms 3'd4: 12ms 3'd5: 13ms 3'd6: 14ms 3'd7: 16ms	RW	0x3

**SDS\_REG15**

REGISTER ADDRESS : 0xBB02283C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	DUMMY_26	dummy_26	RW	0x0

**SDS\_REG16**

REGISTER ADDRESS : 0xBB022840

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	DUMMY_27	dummy_27	RW	0x0

**SDS\_REG17**

REGISTER ADDRESS : 0xBB022844

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:14	RESERVED			
13:0	DUMMY_28	dummy_28	RW	0x0

**SDS\_REG18**

REGISTER ADDRESS : 0xBB022848

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	DUMMY_29	dummy_29	RW	0x0

**SDS\_REG19**

REGISTER ADDRESS : 0xBB02284C

DEFAULT VALUE : 0x4001

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	DUMMY_2A	dummy_2a	RW	0x4001

## SDS\_REG20

REGISTER ADDRESS : 0xBB022850

DEFAULT VALUE : 0x1

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	DUMMY_2B	dummy_2b	RW	0x0001

## SDS\_REG21

REGISTER ADDRESS : 0xBB022854

DEFAULT VALUE : 0x4001

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	DUMMY_2C	dummy_2c	RW	0x4001

## SDS\_REG22

REGISTER ADDRESS : 0xBB022858

DEFAULT VALUE : 0x9800

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	DUMMY_2D	dummy_2d	RW	0x9800

## SDS\_REG23

REGISTER ADDRESS : 0xBB02285C

DEFAULT VALUE : 0x9800

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	DUMMY_2E	dummy_2e	RW	0x9800

**SDS\_REG24**

REGISTER ADDRESS : 0xBB022860

DEFAULT VALUE : 0x1C

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	DUMMY_2F	dummy_2f	RW	0x001C

**SDS\_REG25**

REGISTER ADDRESS : 0xBB022864

DEFAULT VALUE : 0x1C

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	DUMMY_30	dummy_30	RW	0x001C

**SDS\_REG26**

REGISTER ADDRESS : 0xBB022868

DEFAULT VALUE : 0x3810

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	CFG_DNG_OUT_ECO0	debug bus of sds_mode and ip_version	RO	0x3810

**SDS\_REG27**

REGISTER ADDRESS : 0xBB02286C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	CFG_DNG_OUT_ECO1	debug bus reserved for ECO	RO	0x0

**SDS\_REG28**

REGISTER ADDRESS : 0xBB022870

DEFAULT VALUE : 0xC040

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:12	DUMMY_31	dummy_31	RW	0xC
11	DUMMY_32	dummy_32	RW	0x0
10	DUMMY_33	dummy_33	RW	0x0
9:0	CFG_SDS_DBG_SEL	select signal for debug mux	RW	0x040

## SDS\_REG29

REGISTER ADDRESS : 0xBB022874

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	CFG_SDS_DBG_OUT	debug bus[31:0] from debug mux	RO	0x0

## SDS\_EXT\_REG0

REGISTER ADDRESS : 0xBB022A00

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	SDS_EXT_CFG0	serdes analog parameter register	RW	0x0

## SDS\_EXT\_REG1

REGISTER ADDRESS : 0xBB022A04

DEFAULT VALUE : 0xC000

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	SDS_EXT_CFG1	serdes analog parameter register	RW	0xC000

## SDS\_EXT\_REG2

REGISTER ADDRESS : 0xBB022A08

DEFAULT VALUE : 0x0



Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	SDS_EXT_CFG2	serdes analog parameter register	RW	0x0

### SDS\_EXT\_REG3

REGISTER ADDRESS : 0xBB022A0C

DEFAULT VALUE : 0xA170

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	SDS_EXT_CFG3	serdes analog parameter register	RW	0xA170

### SDS\_EXT\_REG4

REGISTER ADDRESS : 0xBB022A10

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	SDS_EXT_CFG4	serdes analog parameter register	RW	0x0

### SDS\_EXT\_REG5

REGISTER ADDRESS : 0xBB022A14

DEFAULT VALUE : 0xF000

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	SDS_EXT_CFG5	serdes analog parameter register	RW	0xF000

### SDS\_EXT\_REG6

REGISTER ADDRESS : 0xBB022A18

DEFAULT VALUE : 0x6E1B

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	SDS_EXT_CFG6	serdes analog parameter register	RW	0x6E1B

## SDS\_EXT\_REG7

REGISTER ADDRESS : 0xBB022A1C

DEFAULT VALUE : 0x858B

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	SDS_EXT_CFG7	serdes analog parameter register	RW	0x858B

## SDS\_EXT\_REG8

REGISTER ADDRESS : 0xBB022A20

DEFAULT VALUE : 0x850

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	SDS_EXT_CFG8	serdes analog parameter register	RW	0x0850

## SDS\_EXT\_REG9

REGISTER ADDRESS : 0xBB022A24

DEFAULT VALUE : 0x24A3

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	SDS_EXT_CFG9	serdes analog parameter register	RW	0x24A3

## SDS\_EXT\_REG10

REGISTER ADDRESS : 0xBB022A28

DEFAULT VALUE : 0x6D2C

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	SDS_EXT_CFG10	serdes analog parameter register	RW	0x6D2C

## SDS\_EXT\_REG11

REGISTER ADDRESS : 0xBB022A2C

DEFAULT VALUE : 0x2BE8

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	SDS_EXT_CFG11	serdes analog parameter register	RW	0x2BE8

## SDS\_EXT\_REG12

REGISTER ADDRESS : 0xBB022A30

DEFAULT VALUE : 0xEA14

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	SDS_EXT_CFG12	serdes analog parameter register	RW	0xEA14

## SDS\_EXT\_REG13

REGISTER ADDRESS : 0xBB022A34

DEFAULT VALUE : 0x304F

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	SDS_EXT_CFG13	serdes analog parameter register	RW	0x304F

## SDS\_EXT\_REG14

REGISTER ADDRESS : 0xBB022A38

DEFAULT VALUE : 0xA84C

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	SDS_EXT_CFG14	serdes analog parameter register	RW	0xA84C

## SDS\_EXT\_REG15

REGISTER ADDRESS : 0xBB022A3C

DEFAULT VALUE : 0xAA12

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	SDS_EXT_CFG15	serdes analog parameter register	RW	0xAA12

## SDS\_EXT\_REG16

REGISTER ADDRESS : 0xBB022A40

DEFAULT VALUE : 0x3292

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	SDS_EXT_CFG16	serdes analog parameter register	RW	0x3292

## SDS\_EXT\_REG24

REGISTER ADDRESS : 0xBB022A44

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:3	CFG_RG24X153	cfg_rg24x153	RW	0x0
2:0	CFG_SYMBOLERR_CNT	select symbol error count of different channel 3'd0: channel0 3'd1: channel1 3'd2: channel2 3'd2: channel2	RW	0x0

## SDS\_EXT\_REG25

REGISTER ADDRESS : 0xBB022A48

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:8	ALL_SYMBOLERR_CNT	total symbol error count (sum of each channel's error)	RO	0x0
7:0	MUX_SYMBOLERR_CNT	symbol error count of single channel	RO	0x0

## SDS\_EXT\_REG26

REGISTER ADDRESS : 0xBB022A4C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:12	P3_LONKDOWN_CNT	link down counter of channel 3	RO	0x0

Bits	Field	Description	Type	Default
11:8	P2_LONKDOWN_CNT	link down counter of channel 2	RO	0x0
7:4	P1_LONKDOWN_CNT	link down counter of channel 1	RO	0x0
3:0	P0_LONKDOWN_CNT	link down counter of channel 0	RO	0x0

## SDS\_EXT\_REG27

REGISTER ADDRESS : 0xBB022A50

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	CFG_DBG_STATUS_ECO_0	debug bus for eco	RO	0x0

## SDS\_EXT\_REG28

REGISTER ADDRESS : 0xBB022A54

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	CFG_DBG_STATUS_ECO_1	debug bus for eco	RO	0x0

## SDS\_EXT\_REG29

REGISTER ADDRESS : 0xBB022A58

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:9	CFG_DBG_STATUS_ECO_2	debug bus for eco	RO	0x0
8	SIGNOK_LAT	sds_sdet for debug	RO	0x0
7:4	LINKOK_LAT	an_ok for debug	RO	0x0
3:0	SYNCOK_LAT	sync_ok for debug	RO	0x0

## SDS\_EXT\_REG30

REGISTER ADDRESS : 0xBB022A5C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:9	CFG_DBG_STATUS_ECO_3	debug bus for eco	RO	0x0
8	SIGNOKLAT	sds_sdet for debug (latch version)	RO	0x0
7:4	LINKOKLAT	an_ok for debug (latch version)	RO	0x0
3:0	SYNCKLAT	sync_ok for debug (latch version)	RO	0x0

## FIB\_REG0

REGISTER ADDRESS : 0xBB022C00

DEFAULT VALUE : 0x1140

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	CFG_FIB_RST	cfg_fib_rst	RWAC	0x0
14	CFG_FIB_LPK	cfg_fib_lpk	RW	0x0
13	CFG_FIB_SPD_RD_0	cfg_fib_spd_rd(0)	RO	0x0
12	CFG_FIB_ANEN	cfg_fib_anen	RW	0x1
11	CFG_FIB_PDOWN	cfg_fib_pdown	RW	0x0
10	CFG_FIB_ISO	cfg_fib_iso	RW	0x0
9	CFG_FIB_RESTART	cfg_fib_restart	RWAC	0x0
8	CFG_FIB_FULLDUP	cfg_fib_fulldup	RW	0x1
7	RESERVED			
6	CFG_FIB_SPD_RD_1	cfg_fib_spd_rd(1)	RO	0x1
5	CFG_FIB_FRCTX	cfg_fib_frctx	RW	0x0
4:0	RESERVED			

## FIB\_REG1

REGISTER ADDRESS : 0xBB022C04

DEFAULT VALUE : 0x6109

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:6	CAPBILITY	capbility	RO	0x184
5	AN_COMPLETE	an_complete	RO	0x0
4	R_FAULT	r_fault	RO	0x0
3	NWAY_ABILITY	nway_ability	RO	0x1
2	LINK_STATUS	link_status	RO	0x0
1	JABBER_DETECT	jabber_detect	RO	0x0
0	EXTENDED_CAPBILITY	extended_capbility	RO	0x1

Bits	Field	Description	Type	Default
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## FIB\_REG2

REGISTER ADDRESS : 0xBB022C08

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:10	REALTEK_OUI	realtek_oui	RO	0x0
9:4	MODEL_NO	model_no	RO	0x0
3:0	REVISION_NO	revision_no	RO	0x0

## FIB\_REG4

REGISTER ADDRESS : 0xBB022C0C

DEFAULT VALUE : 0x1A0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	TX_CFG_REG	tx_cfg_reg	RO	0x01A0

## FIB\_REG5

REGISTER ADDRESS : 0xBB022C10

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	RX_CFG_REG	rx_cfg_reg	RO	0x0

## FIB\_REG6

REGISTER ADDRESS : 0xBB022C14

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:3	RESERVED			
2	FIB_NP_EN	fib_np_en	RO	0x0
1	RXPAGE	rxpage	RO	0x0

Bits	Field	Description	Type	Default
0	RESERVED			

## FIB\_REG7

REGISTER ADDRESS : 0xBB022C18

DEFAULT VALUE : 0x4

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	MR_NP_TX	mr_np_tx	RW	0x0004

## FIB\_REG8

REGISTER ADDRESS : 0xBB022C1C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	MR_NP_TX	mr_np_rx	RO	0x0

## FIB\_REG13

REGISTER ADDRESS : 0xBB022C30

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:14	INDR_FUNC	indr_func	RW	0x0
13:5	DUMMY	dummy_620d	RW	0x0
4:0	INDR_DEVAD	indr_devad	RW	0x0

## FIB\_REG14

REGISTER ADDRESS : 0xBB022C34

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	MMDRDBUS	mmdrdbus	RO	0x0



Bits	Field	Description	Type	Default
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## FIB\_REG16

REGISTER ADDRESS : 0xBB022C3C

DEFAULT VALUE : 0x83

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	ANA_RG2X	serdes analog parameter register	RW	0x0083

## FIB\_REG17

REGISTER ADDRESS : 0xBB022C40

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	ANA_RG3X	serdes analog parameter register	RW	0x0

## FIB\_REG18

REGISTER ADDRESS : 0xBB022C44

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	ANA_RG4X	serdes analog parameter register	RW	0x0

## FIB\_REG19

REGISTER ADDRESS : 0xBB022C48

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	ANA_RG5X	serdes analog parameter register	RW	0x0

## FIB\_REG20

REGISTER ADDRESS : 0xBB022C4C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	ANA_RG6X	serdes analog parameter register	RW	0x0

## FIB\_REG21

REGISTER ADDRESS : 0xBB022C50

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	ANA_RG7X	serdes analog parameter register	RW	0x0

## FIB\_REG22

REGISTER ADDRESS : 0xBB022C54

DEFAULT VALUE : 0x1

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	ANA_RG8X	serdes analog parameter register	RW	0x0001

## FIB\_REG23

REGISTER ADDRESS : 0xBB022C58

DEFAULT VALUE : 0x4001

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	ANA_RG9X	serdes analog parameter register	RW	0x4001

## FIB\_REG28

REGISTER ADDRESS : 0xBB022C5C

DEFAULT VALUE : 0x33FA

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:12	CFG_CONS1_MAX	maxmuim num for concecutive eyes to be accepted (auto_det parameter)	RW	0x3
11:8	CFG_CONS0_MAX	maxmuim num for concecutive eyes to be accepted (auto_det parameter)	RW	0x3
7:0	CFG_CNT_MIN	lower bound for difference between eyes (auto_det parameter)	RW	0xFA

## FIB\_REG29

REGISTER ADDRESS : 0xBB022C60

DEFAULT VALUE : 0xE46A

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	CFG_AUTO_DET_ON	auto_det enable	RW	0x1
14:9	CFG_TOUT_MAX	maxuim num for rule violation (auto_det parameter)	RW	0x32
8:5	CFG_STATE_TMR	maxmuim time between eyes (auto_det parameter)	RW	0x3
4:0	CFG_TEST_TMR	time interval for valid fib100 data (auto_det parameter)	RW	0x0A

## FIB\_REG30

REGISTER ADDRESS : 0xBB022C64

DEFAULT VALUE : 0x71E

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:8	CFG_RG30X1508	Reserved	RW	0x07
7:0	CFG_LNK_ON_TMR	auto_det timer to wait fib100 lnkup (auto_det parameter)	RW	0x1E

## FIB\_EXT\_REG0

REGISTER ADDRESS : 0xBB022E00

DEFAULT VALUE : 0x1140

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	CFG_FIB_RST	cfg_fib_rst	RWAC	0x0

Bits	Field	Description	Type	Default
14	CFG_FIB_LPK	cfg_fib_lpk	RW	0x0
13	CFG_FIB_SPD_RD_0	cfg_fib_spd_rd(0)	RW	0x0
12	CFG_FIB_ANEN	cfg_fib_anen	RW	0x1
11	CFG_FIB_PDOWN	cfg_fib_pdown	RW	0x0
10	CFG_FIB_ISO	cfg_fib_iso	RW	0x0
9	CFG_FIB_RESTART	cfg_fib_restart	RWAC	0x0
8	CFG_FIB_FULLDUP	cfg_fib_fulldup	RW	0x1
7	RESERVED			
6	CFG_FIB_SPD_RD_1	cfg_fib_spd_rd(1)	RW	0x1
5	CFG_FIB_FRCTX	cfg_fib_frctx	RW	0x0
4:0	RESERVED			

## FIB\_EXT\_REG1

REGISTER ADDRESS : 0xBB022E04

DEFAULT VALUE : 0x6109

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:6	CAPBILITY	capbility	RO	0x184
5	AN_COMPLETE	an_complete	RO	0x0
4	R_FAULT	r_fault	RO	0x0
3	NWAY_ABILITY	nway_ability	RO	0x1
2	LINK_STATUS	link_status	RO	0x0
1	JABBER_DETECT	jabber_detect	RO	0x0
0	EXTENDED_CAPBILITY	extended_capability	RO	0x1

## FIB\_EXT\_REG2

REGISTER ADDRESS : 0xBB022E08

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:10	REALTEK_OUI	ext_realtek_oui	RO	0x0
9:4	MODEL_NO	ext_model_no	RO	0x0
3:0	REVISION_NO	ext_revision_no	RO	0x0

## FIB\_EXT\_REG4

REGISTER ADDRESS : 0xBB022E0C  
DEFAULT VALUE : 0x1A0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	TX_CFG_REG	ext_tx_cfg_reg	RO	0x01A0

## FIB\_EXT\_REG5

REGISTER ADDRESS : 0xBB022E10  
DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	RX_CFG_REG	ext_rx_cfg_reg	RO	0x0

## FIB\_EXT\_REG6

REGISTER ADDRESS : 0xBB022E14  
DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:3	RESERVED			
2	FIB_NP_EN	ext_fib_np_en	RO	0x0
1	RXPAGE	ext_rxpage	RO	0x0
0	RESERVED			

## FIB\_EXT\_REG7

REGISTER ADDRESS : 0xBB022E18  
DEFAULT VALUE : 0x4

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	MR_NP_TX	ext_mr_np_tx	RW	0x0004

## FIB\_EXT\_REG8

REGISTER ADDRESS : 0xBB022E1C  
DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	MR_NP_TX	ext_mr_np_rx	RO	0x0

### FIB\_EXT\_REG13

REGISTER ADDRESS : 0xBB022E30

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:14	INDR_FUNC	ext_indr_func	RW	0x0
13:5	DUMMY	ext_dummy_630d	RW	0x0
4:0	INDR_DEVAD	ext_indr_devad	RW	0x0

### FIB\_EXT\_REG14

REGISTER ADDRESS : 0xBB022E34

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	MMDRDBUS	ext_mmdrdbus	RO	0x0

### FIB\_EXT\_REG16

REGISTER ADDRESS : 0xBB022E3C

DEFAULT VALUE : 0x416

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	ANA_RG2X	serdes analog parameter register	RW	0x0416

### FIB\_EXT\_REG17

REGISTER ADDRESS : 0xBB022E40

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	ANA_RG3X	serdes analog parameter register	RW	0x0

## FIB\_EXT\_REG18

REGISTER ADDRESS : 0xBB022E44

DEFAULT VALUE : 0x124

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	ANA_RG4X	serdes analog parameter register	RW	0x0124

## FIB\_EXT\_REG19

REGISTER ADDRESS : 0xBB022E48

DEFAULT VALUE : 0x31B

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	ANA_RG5X	serdes analog parameter register	RW	0x031B

## FIB\_EXT\_REG20

REGISTER ADDRESS : 0xBB022E4C

DEFAULT VALUE : 0x1F33

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	ANA_RG6X	serdes analog parameter register	RW	0x1F33

## FIB\_EXT\_REG21

REGISTER ADDRESS : 0xBB022E50

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			

Bits	Field	Description	Type	Default
15:13	FIB_STS_0	fib_sts_0	RO	0x0
12:4	ANA_RG7X	ext_ana_rg7x	RW	0x0
3:0	FIB_STS_1	serdes analog parameter register	RO	0x0

## FIB\_EXT\_REG22

REGISTER ADDRESS : 0xBB022E54

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:2	ANA_RG8X	ext_ana_rg8x	RW	0x0
1:0	FIB_STS_2	serdes analog parameter register	RO	0x0

## FIB\_EXT\_REG23

REGISTER ADDRESS : 0xBB022E58

DEFAULT VALUE : 0x1408

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	ANA_RG9X	serdes analog parameter register	RW	0x1408

## FIB\_EXT\_REG24

REGISTER ADDRESS : 0xBB022E5C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	ANA_RG10X	serdes analog parameter register	RO	0x0

## FIB\_EXT\_REG25

REGISTER ADDRESS : 0xBB022E60

DEFAULT VALUE : 0x0



Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	ANA_RG11	serdes analog parameter register	RO	0x0

## FIB\_EXT\_REG26

REGISTER ADDRESS : 0xBB022E64

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	ANA_RG12	serdes analog parameter register	RO	0x0

## FIB\_EXT\_REG27

REGISTER ADDRESS : 0xBB022E68

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	ANA_RG13	serdes analog parameter register	RO	0x0

## FIB\_EXT\_REG28

REGISTER ADDRESS : 0xBB022E6C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	ANA_RG14	serdes analog parameter register	RO	0x0

## FIB\_EXT\_REG29

REGISTER ADDRESS : 0xBB022E70

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			

Bits	Field	Description	Type	Default
15:0	DBG_STS_OUT	serdes debug counter output, selected by SDS_REG4{14:12} 0: p0syberrcnt {15:0} 1: p1syberrcnt {15:0} 2: p2syberrcnt{15:0} 3: p3syberrcnt{15:0} 4: {p1lnkdowncnt{7:0}, p0lnkdowncnt{7:0}} 5: {p3lnkdowncnt{7:0}, p2lnkdowncnt{7:0}} 6: {c2_c0_cnt{3:0}, c0_c2_	RO	0x0

## FIB\_EXT\_REG30

REGISTER ADDRESS : 0xBB022E74

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:9	RESERVED			
8	SIGNSTAT	signal status, latch-low and read-clear 0: RX signal loss occurs 1: RX signal is always OK	RO	0x0
7:4	LINKSTAT	link status for 4-port, latch-low and read-clear	RO	0x0
3:0	SYNCSTAT	sync status for 4-port, latch-low and read-clear, sync means digital circuit has detected the comma and finish the alignment process	RO	0x0

### SECTION 2.3

## RTCT

RTCT module

### SECTION 2.4

## POWER SAVING

Power Saving(Green Ethernet/EEE/EEE+) module

## EEE\_TX\_SEL\_CTRL

REGISTER ADDRESS : 0xBB0001C0

DEFAULT VALUE : 0x0

Configure EEE TX wake up decision selection, TX LPI decision selection.

Bits	Field	Description	Type	Default
31:0	DUMMY		RW	0x0

## EEE\_EEEP\_PORT\_CFG

BASE ADDRESS : 0xBB020014  
 PORT INDEX : 0 - 4  
 PORT OFFSET : 0x400  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

EEEE per port configuration.

Bits	Field	Description	Type	Default
31:4	RESERVED			
3	EEE_EEEP_TX_STS	Indicate the per port EEE or EEEP TX LPI status (read to clear)  0b0: the port TX is in normal state. 0b1: the port TX is in LPI state.	RC	0x0
2	EEE_EEEP_RX_STS	Indicate the per port EEE or EEEP RX LPI status (read to clear)  0b0: the port RX is in normal state. 0b1: the port RX is in LPI state.	RC	0x0
1:0	RESERVED			

## P\_EEECFG

BASE ADDRESS : 0xBB020018  
 PORT INDEX : 0 - 4  
 PORT OFFSET : 0x400  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Bits	Field	Description	Type	Default
31:11	RESERVED			
10	EEE_FORCE	for force mode eee	RW	0x0
9	EEE_100M	mac enable eee in 100M	RW	0x0
8	EEE_GIGA	mac enable eee in giga	RW	0x0
7	EEE_TX	enable mac eee tx	RW	0x0
6	EEE_RX	enable mac eee rx	RW	0x0
5	RESERVED			
4	EEE_DSP_RX	consider dsp rx convergence in eee lpi wakeup	RW	0x0
3	EEE_LPI	eee status	RO	0x0
2	EEE_PAUSE_INDICATOR	eee pause flag ( latch high and read clear )	RO	0x0
1	EEE_WAKE_REQ	eee+ wake request ( latch high and read clear )	RO	0x0

Bits	Field	Description	Type	Default
0	EEE_SLEEP_REQ	eee+ sleep request ( latch high and read clear )	RO	0x0

## P\_EEETXMTR

BASE ADDRESS : 0xBB02001C  
 PORT INDEX : 0 - 4  
 PORT OFFSET : 0x400  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Bits	Field	Description	Type	Default
31:0	P_EEETXMTR	eee tx meter to calculate the time for tx in lpi status	RO	0x0

## P\_EEERXMTR

BASE ADDRESS : 0xBB020020  
 PORT INDEX : 0 - 4  
 PORT OFFSET : 0x400  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Bits	Field	Description	Type	Default
31:0	P_EEERXMTR	eee rx meter to calculate the time for rx in lpi status	RO	0x0

## EEE\_TX\_THR\_GIGA

REGISTER ADDRESS : 0xBB023074  
 DEFAULT VALUE : 0xD

Bits	Field	Description	Type	Default
31:16	RESERVED			

Bits	Field	Description	Type	Default
15:0	TX_RATE_EEE_GIGA	EEE_TX_THR_FE Set the TX threshold in EEE function. Unit is Byte; $EEE\_TX\_THR = \text{Round} \{ (T\_tx\_rateRate) / 8 \}$ . If you set $T\_tx\_rate = 10\text{usRate} = 10\text{Mbps}$ , so set $EEE\_TX\_THR = 0xD$ (13 bytes). Default value is 0xD. EEPROM and register configurable.	RW	0x000D

## EEE\_TX\_THR\_FE

REGISTER ADDRESS : 0xBB023078

DEFAULT VALUE : 0xD

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	TX_RATE_EEE_100M	Set the TX threshold in EEE function. Unit is Byte; $EEE\_TX\_THR = \text{Round} \{ (T\_tx\_rateRate) / 8 \}$ . If you set $T\_tx\_rate = 10\text{usRate} = 10\text{Mbps}$ , so set $EEE\_TX\_THR = 0xD$ (13 bytes). Default value is 0xD. EEPROM and register configurable.	RW	0x000D

## EEE\_RX\_FC\_REG

REGISTER ADDRESS : 0xBB02307C

DEFAULT VALUE : 0x120

Bits	Field	Description	Type	Default
31:11	RESERVED			
10	EEE_HALF_DUP_EN	Enable EEE in half duplex 1:Enable 0:Disable	RW	0x0
9:0	RX_PGCNT	reserving page number for incoming packet before flowctrl dropping	RW	0x120

## EEE\_MISC

REGISTER ADDRESS : 0xBB023080

DEFAULT VALUE : 0x50

Bits	Field	Description	Type	Default
31:8	RESERVED			

Bits	Field	Description	Type	Default
7	EEE_REQ_SET1	Enable LPI TX request queue empty decision maker for EEE; 1: enable; 0: disable.	RW	0x0
6	EEE_REQ_SET0	Enable LPI TX request Rate decision maker for EEE; 1: enable; 0: disable.	RW	0x1
5	EEE_WAKE_SET1	Enable LPI TX transmit wakeup decision maker for EEE; 1: enable; 0: disable.	RW	0x0
4	EEE_WAKE_SET0	Enable LPI TX request RX pause on frame decision maker for EEE; 1: enable; 0: disable.	RW	0x1
3:2	EEE_TU_GIGA	Set the unit for timer T_tx_rate and T_wakeup in EEE function. 00: 1us; 01: 16us; 10: 128us; 11: 1024us.	RW	0x0
1:0	EEE_TU_100M	Set the unit for timer T_tx_rate and T_wakeup in EEE function. 00: 1us; 01: 16us; 10: 128us; 11: 1024us.	RW	0x0

## EEE\_GIGA\_CTRL0

REGISTER ADDRESS : 0xBB023084

DEFAULT VALUE : 0x14140A

Bits	Field	Description	Type	Default
31:24	RESERVED			
23:16	EEE_TW_500M	Timer value in EEE function for T_wakeup. Value from 0 256. Unit: See register EEE_Timer_Unit_Giga. Default value is 20 us. EEPROM and register configurable.	RW	0x14
15:8	EEE_TW_GIGA	Timer value in EEE function for T_wakeup. Value from 0 256. Unit: See register EEE_Timer_Unit_Giga. Default value is 20 us. EEPROM and register configurable.	RW	0x14
7:0	EEE_TR_GIGA	Timer value in EEE function for T_tx_rate. Unit: See register EEE_Timer_Unit_Giga. Default value is 10 us. EEPROM and register configurable.	RW	0x0A

## EEE\_GIGA\_CTRL1

REGISTER ADDRESS : 0xBB023088

DEFAULT VALUE : 0xC80A

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:8	EEE_TD_GIGA	Timer value in EEE function for QoS based LPI decision maker T_tx_delay. Unit: See register EEE_Timer_Unit_Giga. Default value is 200 us. EEPROM and register configurable.	RW	0xC8
7:0	EEE_TP_GIGA	Timer value in EEE function for TX decision maker T_pause. Unit: See register EEE_Timer_Unit_Giga. Default value is 10 us. EEPROM and register configurable.	RW	0x0A

## EEE\_100M\_CTRL0

REGISTER ADDRESS : 0xBB02308C

DEFAULT VALUE : 0x240A

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:8	EEE_TW_100M	Timer value in EEE function for T_wakeup. Value from 0 256. Unit: See register EEE_Timer_Unit_FE. Default value is 36 us. EEPROM and register configurable.	RW	0x24
7:0	EEE_TR_100M	Timer value in EEE function for T_tx_rate. Unit: See register EEE_Timer_Unit_FE. Default value is 10 us. EEPROM and register configurable.	RW	0x0A

## EEE\_100M\_CTRL1

REGISTER ADDRESS : 0xBB023090

DEFAULT VALUE : 0xC80A

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:8	EEE_TD_100M	Timer value in EEE function for QoS based LPI decision maker T_tx_delay. Unit: See register EEE_Timer_Unit_FE. Default value is 200 us. EEPROM and register configurable.	RW	0xC8

Bits	Field	Description	Type	Default
7:0	EEE_TP_100M	Timer value in EEE function for TX decision maker T_pause. Unit: See register EEE_Timer_Unit_FE. Default value is 10 us. EEPROM and register configurable.	RW	0x0A

## EEE\_BURSTSIZE

REGISTER ADDRESS : 0xBB023094

DEFAULT VALUE : 0x1000

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	EEE_BURSTSIZE	EEE leaky bucket burst size in bytes.	RW	0x1000

## EEE\_IFG\_CFG

REGISTER ADDRESS : 0xBB023098

DEFAULT VALUE : 0x1

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	EEE_INC_IFG	EEE leaky bucket include ifg ( 20 bytes ) .	RW	0x1

## EEE\_RXIDLE

REGISTER ADDRESS : 0xBB02309C

DEFAULT VALUE : 0x101

monitor rxdv for specific time to decide if enter TX LPI

Bits	Field	Description	Type	Default
31:18	RESERVED			
17	WAIT_RX_IDLE_GELITE	control if TX LPI decision must consider rxdv idle time for 500M	RW	0x0
16	WAIT_RX_IDLE_GE	control if TX LPI decision must consider rxdv idle time for giga	RW	0x0
15:8	WAIT_RX_IDLE_TIMER_GELITE	min rxdv idle time for 500M TX LPI enter condition	RW	0x01
7:0	WAIT_RX_IDLE_TIMER_G E	min rxdv idle time for giga TX LPI enter condition	RW	0x01



## EEE\_DECISION\_WINDOW

REGISTER ADDRESS : 0xBB0230A0

DEFAULT VALUE : 0x2D1010

EEE TX LPI decision window for txpla and MAC\_EEE

Bits	Field	Description	Type	Default
31:24	RESERVED			
23:16	EEE_DECISION_WINDOW_100M	EEE LPI decision window for 100M , time unit is system clock cycle time	RW	0x2D
15:8	EEE_DECISION_WINDOW_500M	EEE LPI decision window for 500M , time unit is system clock cycle time	RW	0x10
7:0	EEE_DECISION_WINDOW_GE	EEE LPI decision window for giga , time unit is system clock cycle time	RW	0x10

## PS\_LINKID\_GATCLK\_CTRL

REGISTER ADDRESS : 0xBB0230A4

DEFAULT VALUE : 0x0

Specify link idle gating clock and link idle time control register.

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:4	LINKID_TIME	When enable Link Idle Gating Clock Control Register and link idle time exceed LINKID_TIME, will trigger clock gating power saving mode. 0x0: 100 ms 0x1: 200 ms 0x2: 300 ms 0x3: 30 sec	RW	0x0
3:0	RESERVED			

## P\_EEEP\_CFG

BASE ADDRESS : 0xBB020024

PORT INDEX : 0 - 4

PORT OFFSET : 0x400

DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Bits	Field	Description	Type	Default
31:2	RESERVED			
1	EEEP_TX_EN	enable eep tx	RW	0x0
0	EEEP_RX_EN	enable_eep_rx	RW	0x0

## EEEP\_CFG

REGISTER ADDRESS : 0xBB0230A8

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:4	RESERVED			
3	EEEP_SLAVE_EN	0:Not support EEEP slave mode.Only Giga/500M master mode can enter EEEP LPI. 1:support EEEP slave mode. Giga/500M Master and slave mode can enter EEEP LPI.	RW	0x0
2	EEEP_100M	Enable/Disable 100M speed EEEP function.	RW	0x0
1	EEEP_500M	Enable/Disable 500M speed EEEP function.	RW	0x0
0	EEEP_GIGA	Enable/Disable GIGA speed EEEP function.	RW	0x0

## EEEP\_TIMER\_UNIT\_CTRL

REGISTER ADDRESS : 0xBB0230AC

DEFAULT VALUE : 0x15

Configure the timer unit for EEEP RX and TX of 100M and GIGA port.

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:4	TIMER_UNIT_GIGA	Set the unit for timer in EEEP function for port link at 100M speed. 0x0:1us 0x1:16us 0x2:128us 0x3:1024us	RW	0x1
3:2	TIMER_UNIT_500M	Set the unit for timer in EEEP function for port link at 500M speed. 00: 200ns; 01: 500ns; 10: 1us; 11: 16us. EEPROM and register configurable.	RW	0x1

Bits	Field	Description	Type	Default
1:0	TIMER_UNIT_100M	Set the unit for timer in EEEP function for port link at GIGA speed. 0x0:1us 0x1:16us 0x2:128us 0x3:1024us	RW	0x1

## EEEP\_TX\_TIMER\_GIGA\_CTRL

REGISTER ADDRESS : 0xBB0230B0

DEFAULT VALUE : 0x404

Configure the timer unit for EEEP GIGA speed

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:8	TX_IDLE_TIMER_GIGA	Used to fast enter LPI when there is no traffic need to be transmitted. Unit is decided by TIMER_UNIT_GIGA.	RW	0x04
7:0	TX_WAKE_TIMER_GIGA	Timer value in EEEP function for TX wake time at GIGA speed Default Unit: 500ns Default value is 2us. EEPROM and register configurable.	RW	0x04

## EEEP\_TX\_TIMER\_500M\_CTRL

REGISTER ADDRESS : 0xBB0230B4

DEFAULT VALUE : 0x404

Configure the timer unit for EEEP 500M speed

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:8	TX_IDLE_TIMER_500M	Used to fast enter LPI when there is no traffic need to be transmitted. Unit is decided by TIMER_UNIT_500M.	RW	0x04
7:0	TX_WAKE_TIMER_500M	Timer value in EEEP function for TX wake time at 500M speed Default Unit: 500ns Default value is 2us. EEPROM and register configurable.	RW	0x04

## EEEP\_TX\_TIMER\_100M\_CTRL

REGISTER ADDRESS : 0xBB0230B8

DEFAULT VALUE : 0x404

Configure the timer unit for EEEP 100M speed

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:8	TX_IDLE_TIMER_100M	Used to fast enter LPI when there is no traffic need to be transmitted. Unit is decided by TIMER_UNIT_100M.	RW	0x04
7:0	TX_WAKE_TIMER_100M	Timer value in EEEP function for TX wake time at 100M speed Default Unit: 500ns Default value is 2us. EEPROM and register configurable.	RW	0x04

## EEEP\_TX\_GIGA\_CTRL

REGISTER ADDRESS : 0xBB0230BC

DEFAULT VALUE : 0x1411

Configure EEEP TX parameters including TX rate caculation enable state, TX rate calculation interval timer and TX packet length threshold for port link at GIGA.

Bits	Field	Description	Type	Default
31:25	RESERVED			
24:9	TX_RATE_THR_GIGA	Set the TX packet length threshold in EEEP function for port link at GIGA speed. Unit is Byte. $TX\_RATE\_THR\_GIGA = Round\{(TX\_RATE\_TIMER\_GIGA * Rate) / 8\}$ . If you set $TX\_RATE\_TIMER\_GIGA = 192us$ , $Rate = 10Mbps$ , so set $TX\_RATE\_THR\_GIGA = 0xF0$ (240 bytes).	RW	0x000A
8:1	TX_RATE_TIMER_GIGA	Timer interval for EEEP TX rate detection for port link at GIGA speed. Unit is decided by TIMER_UNIT_GIGA.	RW	0x08
0	TX_RATE_EN_GIGA	Enable TX rate calculation to decide if the port linked at GIGA speed could enter EEEP LPI mode. The TX packets would be counted in $TX\_RATE\_TIMER\_GIGA$ , if the total length of TX packets is lower than $TX\_RATE\_THR\_GIGA$ , the port could enter EEEP LPI mode. 0b0: Disable 0b1: Enable	RW	0x1

## EEEP\_TX\_500M\_CTRL

REGISTER ADDRESS : 0xBB0230C0

DEFAULT VALUE : 0x1410

Configure EEEP TX parameters including TX rate caculation enable state, TX rate calculation interval timer and TX packet length threshold for port link at 100M.

Bits	Field	Description	Type	Default
31:25	RESERVED			
24:9	TX_RATE_THR_500M	cfg_tx_rate_eeep_500	RW	0x000A
8:1	TX_RATE_TIMER_500M	Timer for TX rate measuring when speed = 500M	RW	0x08
0	TX_RATE_EN_500M	Enable EEEP TX measuring rate and enter TX LPI	RW	0x0

## EEEP\_TX\_100M\_CTRL

REGISTER ADDRESS : 0xBB0230C4

DEFAULT VALUE : 0x1411

Configure EEEP TX parameters including TX rate caculation enable state, TX rate calculation interval timer and TX packet length threshold for port link at 100M.

Bits	Field	Description	Type	Default
31:25	RESERVED			
24:9	TX_RATE_THR_100M	Set the TX packet length threshold in EEEP function for port link at 100M speed. Unit is Byte. $TX\_RATE\_THR\_100M = Round\{(TX\_RATE\_TIMER\_100M * Rate) / 8\}$ . If you set $TX\_RATE\_TIMER\_100M = 192us$ , $Rate = 10Mbps$ , so set $TX\_RATE\_THR\_100M = 0xF0$ (240 bytes).	RW	0x000A
8:1	TX_RATE_TIMER_100M	Timer interval for EEEP TX rate detection for port link at 100M speed. Unit is decided by $TIMER\_UNIT\_100M$ .	RW	0x08
0	TX_RATE_EN_100M	Enable TX rate calculation to decide if the port linked at 100M speed could enter EEEP LPI mode. The TX packets would be counted in $TX\_RATE\_TIMER\_100M$ , if the total length of TX packets is lower than $TX\_RATE\_THR\_100M$ , the port could enter EEEP LPI mode. 0b0: Disable 0b1: Enable	RW	0x1

## EEEP\_RX\_RATE\_GIGA\_CTRL

REGISTER ADDRESS : 0xBB0230C8

DEFAULT VALUE : 0x1410

Configure EEEP RX rate calculation related parameters including RX rate calculation interval timer and RX packet length threshold for port link at GIGA.

Bits	Field	Description	Type	Default
31:24	RESERVED			

Bits	Field	Description	Type	Default
23:8	RX_RATE_THR_GIGA	Set the RX rate threshold in EEEP function. Unit is Byte; $RX\_RATE\_THR\_GIGA = \text{Round} \{ (RX\_RATE\_TIMER\_GIGA * Rate) / 8 \}.$ If you set $RX\_RATE\_TIMER\_GIGA = 192\mu s$ , $Rate = 10\text{Mbps}$ , so set $RX\_RATE\_THR\_GIGA = 0xF0$ (240 bytes).	RW	0x0014
7:0	RX_RATE_TIMER_GIGA	Timer for EEEP RX bit rate detection. The unit is decided by $TIMER\_UNIT\_100M$ .	RW	0x10

## EEEP\_RX\_RATE\_500M\_CTRL

REGISTER ADDRESS : 0xBB0230CC

DEFAULT VALUE : 0x1410

Configure EEEP RX rate calculation related parameters including RX rate calculation interval timer and RX packet length threshold for port link at GIGA.

Bits	Field	Description	Type	Default
31:24	RESERVED			
23:8	RX_RATE_THR_500M	cfg_rx_rate_eeep_500	RW	0x0014
7:0	RX_RATE_TIMER_500M	Timer value in EEEP function for $T_{rx\_rate}$ . Unit: 500ns Default value is 8 us. EEPROM and register configurable.	RW	0x10

## EEEP\_RX\_RATE\_100M\_CTRL

REGISTER ADDRESS : 0xBB0230D0

DEFAULT VALUE : 0x1410

Configure EEEP RX rate calculation related parameters including RX rate calculation interval timer and RX packet length threshold for port link at 100M.

Bits	Field	Description	Type	Default
31:24	RESERVED			
23:8	RX_RATE_THR_100M	Set the RX rate threshold in EEEP function. Unit is Byte; $RX\_RATE\_THR\_100M = \text{Round} \{ (RX\_RATE\_TIMER\_100M * Rate) / 8 \}.$ If you set $RX\_RATE\_TIMER\_100M = 192\mu s$ , $Rate = 10\text{Mbps}$ , so set $RX\_RATE\_THR\_100M = 0xF0$ (240 bytes).	RW	0x0014
7:0	RX_RATE_TIMER_100M	Timer for EEEP RX bit rate detection. The unit is decided by $TIMER\_UNIT\_100M$ .	RW	0x10

## EEEEP\_RX\_SLEEP\_STEP\_CTRL

REGISTER ADDRESS : 0xBB0230D4

DEFAULT VALUE : 0x1

Configure EEEP RX maximum sleep step and show the current sleep step of a specific port.

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:8	RX_SLEEP_STEP_CURRENT	Current EEEP sleep step (Read Only).	RO	0x0
7:0	RX_SLEEP_STEP_MAX	Maximum EEEP sleep step.	RW	0x01

## EEEEP\_RX\_WAKE\_TIMER\_GIGA\_CTRL

REGISTER ADDRESS : 0xBB0230D8

DEFAULT VALUE : 0x1414

Configure the timers for GIGA EEEP RX wake up delay time.

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:8	RX_WAKE_TIMER_GIGA_MASTER	Delay timer for a port leaving RX LPI. It is needed for MAC to wait PHY and other circuits to wake up. The unit is decided by TIMER_UNIT_GIGA.	RW	0x14
7:0	RX_WAKE_TIMER_GIGA_SLAVE	Delay timer for a port leaving RX LPI. It is needed for MAC to wait PHY and other circuits to wake up.	RW	0x14

## EEEEP\_RX\_TIMER\_GIGA\_CTRL

REGISTER ADDRESS : 0xBB0230DC

DEFAULT VALUE : 0x800FF0A

Configure the timers for GIGA EEEP RX including delay timer after sending PAUSE ON frame, sleep time for each sleep step, minimum sleep time for RX LPI awoken by TX request

Bits	Field	Description	Type	Default
31:24	RX_IDLE_TIMER_GIGA	Used to fast enter LPI when there is no traffic received. Unit is decided by TIMER_UNIT_GIGA	RW	0x08
23:16	RX_MIN_SLEEP_TIMER_GIGA	Min sleep time for a port in RX LPI mode and being awoken because the port has packets to TX. The unit is decided by TIMER_UNIT_GIGA. (This timer is used to make sure the minimum time a port in RX LPI mode can sleep)	RW	0x0
15:8	RX_SLEEP_TIMER_GIGA	Timer for a port RX falling sleep in LPI mode. The unit is decided by TIMER_UNIT_GIGA.	RW	0xFF

Bits	Field	Description	Type	Default
7:0	RX_PAUSE_ON_TIMER_GIGA	Delay timer for a port RX to fall to sleep after sending out Pause ON frame. The unit is decided by TIMER_UNIT_GIGA.	RW	0x0A

## EEEP\_RX\_WAKE\_TIMER\_500M\_CTRL

REGISTER ADDRESS : 0xBB0230E0

DEFAULT VALUE : 0x2828

Configure the timers for 500M EEEP RX wake up delay time.

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:8	RX_WAKE_TIMER_500M_MASTER	Timer value in EEEP function for T_rx_wait. Default Unit: 500ns Default value is 20 us. EEPROM and register configurable.	RW	0x28
7:0	RX_WAKE_TIMER_500M_SLAVE	Delay timer for a port leaving RX LPI. It is needed for MAC to wait PHY and other circuits to wake up.	RW	0x28

## EEEP\_RX\_TIMER\_500M\_CTRL

REGISTER ADDRESS : 0xBB0230E4

DEFAULT VALUE : 0x800FF0A

Configure the timers for 500M EEEP RX including delay timer after sending PAUSE ON frame, sleep time for each sleep step, minimum sleep time for RX LPI awoken by TX request

Bits	Field	Description	Type	Default
31:24	RX_IDLE_TIMER_500M	Used to fast enter LPI when there is no traffic received. Unit is decided by TIMER_UNIT_500M.	RW	0x08
23:16	RX_MIN_SLEEP_TIMER_500M	Min sleep time for a port in RX LPI mode and being awoken because the port has packets to TX. The unit is decided by TIMER_UNIT_500M. (This timer is used to make sure the minimum time a port in RX LPI mode can sleep)	RW	0x0
15:8	RX_SLEEP_TIMER_500M	value of Timer in EEEP function for T_rx_sleep. Unit: microsecond. Default value is 128 us. EEPROM and register configurable.	RW	0xFF
7:0	RX_PAUSE_ON_TIMER_500M	Delay timer for a port RX to fall to sleep after sending out Pause ON frame. The unit is decided by TIMER_UNIT_GIGA.	RW	0x0A



## EEEE\_RX\_WAKE\_TIMER\_100M\_CTRL

REGISTER ADDRESS : 0xBB0230E8

DEFAULT VALUE : 0x14

Configure the timers for 100M EEEP RX wake up delay time.

Bits	Field	Description	Type	Default
31:8	RESERVED			
7:0	RX_WAKE_TIMER_100M	Delay timer for a port leaving RX LPI. It is needed for MAC to wait PHY and other circuits to wake up. The unit is decided by TIMER_UNIT_100M.	RW	0x14

## EEEE\_RX\_TIMER\_100M\_CTRL

REGISTER ADDRESS : 0xBB0230EC

DEFAULT VALUE : 0x800FF0A

Configure the timers for 100M EEEP RX including delay timer after sending PAUSE ON frame, sleep time for each sleep step, minimum sleep time for RX LPI awoken by TX request

Bits	Field	Description	Type	Default
31:24	RX_IDLE_TIMER_100M	Used to fast enter LPI when there is no traffic received. Unit is decided by TIMER_UNIT_100M.	RW	0x08
23:16	RX_MIN_SLEEP_TIMER_100M	Min sleep time for a port in RX LPI mode and being awoken because the port has packets to TX. The unit is decided by TIMER_UNIT_100M. (This timer is used to make sure the minimum time a port in RX LPI mode can sleep)	RW	0x0
15:8	RX_SLEEP_TIMER_100M	Timer for a port RX falling sleep in LPI mode. The unit is decided by TIMER_UNIT_100M.	RW	0xFF
7:0	RX_PAUSE_ON_TIMER_100M	Delay timer for a port RX to fall to sleep after sending out Pause ON frame. The unit is decided by TIMER_UNIT_100M.	RW	0x0A

## P\_EEEPTXMTR

BASE ADDRESS : 0xBB020028

PORT INDEX : 0 - 4

PORT OFFSET : 0x400

DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Bits	Field	Description	Type	Default
31:0	P_EEEPTXMTR	eeep tx meter to calculate the time for tx in eeep-lpi status	RO	0x0

## P\_EEEPRXMTR

BASE ADDRESS : 0xBB02002C  
 PORT INDEX : 0 - 4  
 PORT OFFSET : 0x400  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Bits	Field	Description	Type	Default
31:0	P_EEEPRXMTR	eeep rx meter to calculate the time for rx in eeep-lpi status	RO	0x0

## SW\_PWRSV\_CTRL

REGISTER ADDRESS : 0xBB0001C4  
 DEFAULT VALUE : 0xF102

swcore power saving control

Bits	Field	Description	Type	Default
31:19	RESERVED			
18	SLOW_DOWN_PLL_EN	slow down PLL as swcore power saving	RW	0x0
17	SLOW_DOWN_CLK_EN	slow down swcore clock as swcore power saving	RW	0x0
16	FRC_MAC_ACTIVE	active MAC port force mode	RW	0x0
15:12	SLOW_CLK_TGL_RATE	dgckmx cks clock source	RW	0xF
11:2	GPHY_MDX_MDC_DIV	GPHY MDC freq division	RW	0x040
1	WAIT_FOR_AGREEMENT	swcore power saving need CPU agreement	RW	0x1
0	AGREE_SLEEP	agree swcore power saving	RW	0x0

### SECTION 2.5

## AUTO FALLBACK

Power Saving(Green Ethernet/EEE/EEE+) module

## FB\_CTRL

REGISTER ADDRESS : 0xBB01B000

DEFAULT VALUE : 0x0

Configure auto-fallback related parameters

Bits	Field	Description	Type	Default
31:17	RESERVED			
16	STOP_TMR	Stop per port timer	RW	0x0
15:13	ERR_TH	Error Packet Count(Threshold of Error Ratio) 0x0: 1(1/MAX_TH) 0x1: 2(2/MAX_TH) 0x2: 4(4/MAX_TH) 0x3: 8(8/MAX_TH) 0x4: 16(16/MAX_TH) 0x5: 32(32/MAX_TH) 0x6: 64(64/MAX_TH) 0x7: 128(128/MAX_TH)	RW	0x0
12:10	MAX_TH	Maximal Monitoring Count 0x0: 8K 0x1: 16K 0x2: 32K 0x3: 64K 0x4: 128K 0x5: 256K 0x6: 512K 0x7: 1M	RW	0x0
9	TO_IGNORE	Monitor timeout Ignore or Error Decision	RW	0x0
8:1	TO_TH	Monitor timeout threshold(unit 4ms)	RW	0x0
0	PL_DEC_EN	allow the power level can be reduced	RW	0x0

## FB\_PORT\_CFG

BASE ADDRESS : 0xBB01B004

PORT INDEX : 0 - 4

PORT OFFSET : 0x4

DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Configure port auto-fallback related parameters

Bits	Field	Description	Type	Default
31:4	RESERVED			
3	CPL	Current Power Level	RO	0x0
2	VALID_FLOW	Per port valid flow indicator	RO	0x0
1	RST_PL	1: restore to default value 0: clear to 0 when link up/down	RO	0x0
0	EN	per-port enable Power Saving Auto-Fallback 0: Disable 1: Enable	RW	0x0

**FB\_PORT\_ERR\_CNT**

BASE ADDRESS : 0xBB01B018  
PORT INDEX : 0 - 4  
PORT OFFSET : 8 bits  
DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (8 bits per field)

auto-fallback port error counter

Bits	Field	Description	Type	Default
7:0	CNT	per-port error counter	RO	0x0

**FB\_PORT\_MONITOR\_CNT**

BASE ADDRESS : 0xBB01B020  
PORT INDEX : 0 - 4  
PORT OFFSET : 28 bits  
DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (28 bits per field)

auto-fallback port monitor counter

Bits	Field	Description	Type	Default
27:0	CNT	per-port monitor counter	RO	0x0

## CHAPTER 3

# Layer 2

The chapter describes features related to layer 2

### SECTION 3.1

## ADDRESS TABLE LOOKUP

Address Table Lookup module

### LUT\_UNMATCHED\_SA\_CTRL

BASE ADDRESS : 0xBB01C000

PORT INDEX : 0 - 6

PORT OFFSET : 2 bits

DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (2 bits per field)

unmatched SA control register

Bits	Field	Description	Type	Default
1:0	ACT	Drop/Trap packet if SA is not from the same source port as L2 SPA 0b00: normal 0b01: drop packet & disable learning 0b10: trap to CPU 0b11: copy to CPU	RW	0x0

### LUT\_UNKN\_SA\_CTRL

BASE ADDRESS : 0xBB01C004

PORT INDEX : 0 - 6

PORT OFFSET : 2 bits

DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (2 bits per field)

unknown SA control register

Bits	Field	Description	Type	Default
1:0	ACT	Drop/Trap packet if SA is unknown 0b00: normal 0b01: drop packet & disable learning 0b10: trap to CPU 0b11: copy to CPU	RW	0x0

## LUT\_UNKN\_UC\_DA\_CTRL

BASE ADDRESS : 0xBB01C008  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 2 bits  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (2 bits per field)

unknown unicast DA control register

Bits	Field	Description	Type	Default
1:0	ACT	Drop/Trap packet if unicast DA is unknown 0b00: normal flooding 0b01: drop packet, exclude IGMP/MLD packets 0b10: trap to CPU, exclude IGMP/MLD packets 0b11: reserved	RW	0x0

## LUT\_LEARN\_OVER\_CTRL

BASE ADDRESS : 0xBB01C00C  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 2 bits  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (2 bits per field)

LUT learning over control register

Bits	Field	Description	Type	Default
1:0	ACT	Auto leaning number exceed behavior 0b00: normal flooding 0b01: drop packet 0b10: trap to CPU 0b11: copy to cpu	RW	0x0

## LUT\_CFG

REGISTER ADDRESS : 0xBB017000  
 DEFAULT VALUE : 0x600BB8

## LUT global control register

Bits	Field	Description	Type	Default
31:26	RESERVED			
25	LUT_IPMC_LOOKUP_OP	L3 lookup option for incoming IP multicast packet 1: using DIP+SIP hash when DIP is matched one of IPMC_GROUP_TABLE entry, otherwise use DIP+(SIP=0.0.0.0) hash 0: using DIP+(SIP=0.0.0.0) hash when DIP is matched one of IPMC_GROUP_TABLE entry, otherwise use DIP+SIP hash	RW	0x0
24:23	LUT_IPMC_HASH	Hash algorithm for incoming IP multicast packet to lookup forwarding decision 0b00:using {DMAC,FID} hash algorithm 0b01:using {DIP,SIP} hash algorithm 0b10:hash method {GIP, VID}	RW	0x0
22	LINKDOWN_AGEOUT	Link down port aging out setting 0b0:disable aging out 0b1:enable force aging out all L2 lookup entries belong to link down ports	RW	0x1
21	BCAM_DIS	Binary CAM usage setting 0b0:enable 0b1:disable	RW	0x1
20:0	AGE_SPD	L2 lookup table aging speed/period for each 2K entries, unit 0.1 sec	RW	0x000BB8

**LUT\_AGEOUT\_CTRL**

BASE ADDRESS : 0xBB017004  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 1 bit  
 DEFAULT VALUE : 0x1

This is a One-Dimension Register Field Array. (1 bit per field)

## LUT aging control register

Bits	Field	Description	Type	Default
0	AGEOUT_OUT	per port aging out enable/disable setting 0b0:disable aging out 0b1:enable aging out	RW	0x1

**LUT\_LRN\_LIMITNO**

BASE ADDRESS : 0xBB017008  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 12 bits  
 DEFAULT VALUE : 0xFFF

This is a One-Dimension Register Field Array. (12 bits per field)

L2 learning limitation entry number register

Bits	Field	Description	Type	Default
11:0	NUM	L2 learning limitation entry number. ASIC supports 2K LUT entries and L2 learning limitation is for auto-learning L2 entry number. Set register to value 0xFFFF for non-limitation	RW	0xFFFF

## L2\_LRN\_CNT

BASE ADDRESS : 0xBB017018  
PORT INDEX : 0 - 6  
PORT OFFSET : 12 bits  
DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (12 bits per field)

Number of SA learned register

Bits	Field	Description	Type	Default
11:0	L2_LRN_CNT	Number of SA learned on Port index 0-6:per-port counter	RO	0x0

## L2\_LRN\_OVER\_STS

BASE ADDRESS : 0xBB01D010  
PORT INDEX : 0 - 6  
PORT OFFSET : 1 bit  
DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

L2 per-port learning over event register

Bits	Field	Description	Type	Default
0	LRN_OVER_IND	L2 learning over ever occurs	RW1C	0x0

## LUT\_SYS\_LRN\_LIMITNO

REGISTER ADDRESS : 0xBB017028  
DEFAULT VALUE : 0xFFFF

L2 learning system-wised limitation entry number register



Bits	Field	Description	Type	Default
31:12	RESERVED			
11:0	SYS_LRN_LIMITNO	system learning limit number	RW	0xFFF

## L2\_SYS\_LRN\_OVER\_STS

REGISTER ADDRESS : 0xBB01D014

DEFAULT VALUE : 0x0

L2 system learning over event register

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	LRN_OVER_IND	L2 system learning over ever occurs	RW1C	0x0

## L2\_SYS\_LRN\_CNT

REGISTER ADDRESS : 0xBB01702C

DEFAULT VALUE : 0x0

System Number of SA learned register

Bits	Field	Description	Type	Default
31:12	RESERVED			
11:0	SYS_L2_LRN_CNT	Whole system number of SA learned counter	RO	0x0

## UNKN\_L2\_MC

BASE ADDRESS : 0xBB01C010

PORT INDEX : 0 - 6

PORT OFFSET : 2 bits

DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (2 bits per field)

unknown L2 multicast register

Bits	Field	Description	Type	Default
1:0	ACT	unknow L2 multicast frame behavior 0b00: normal flooding 0b01: drop packet 0b10: trap to CPU 0b11: drop packet exclude RMA	RW	0x0

Bits	Field	Description	Type	Default
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## UNKN\_IP4\_MC

BASE ADDRESS : 0xBB01C014  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 2 bits  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (2 bits per field)

unknown IPv4 multicast register

Bits	Field	Description	Type	Default
1:0	ACT	unknow IPv4 multicast frame behavior 0b00: normal flooding 0b01: drop packet, exclude IP 224.0.0.x and IGMP packets 0b10: trap to CPU, exclude IP 224.0.0.x and IGMP packets 0b11: reserved	RW	0x0

## UNKN\_IP6\_MC

BASE ADDRESS : 0xBB01C018  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 2 bits  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (2 bits per field)

unknown IPv6 multicast register

Bits	Field	Description	Type	Default
1:0	ACT	unknow IPv6 multicast frame behavior 0b00: normal flooding 0b01: drop packet, exclude IP [FFXX::/8] and MLD packets 0b10: trap to CPU, exclude IP [FFXX::/8] and MLD packets 0b11: reserved	RW	0x0

## UNKN\_MC\_PRI

REGISTER ADDRESS : 0xBB01C01C  
 DEFAULT VALUE : 0x0

LUT global control register

Bits	Field	Description	Type	Default
31:3	RESERVED			
2:0	UNKN_MC_PRI	Trap priority for unknown L2/Ipv4/IPv6 multicast	RW	0x0

## LUT\_BC\_FLOOD

BASE ADDRESS : 0xBB01C020  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 1 bit  
 DEFAULT VALUE : 0x1

This is a One-Dimension Register Field Array. (1 bit per field)

LUT broadcast flooding control register

Bits	Field	Description	Type	Default
0	EN	Egress port mask for broadcast(ff-ff-ff-ff-ff-ff) flooding packets 0b0: drop 0b1: normal flooding	RW	0x1

## LUT\_UNKN\_MC\_FLOOD

BASE ADDRESS : 0xBB01C024  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 1 bit  
 DEFAULT VALUE : 0x1

This is a One-Dimension Register Field Array. (1 bit per field)

LUT unknown multicast flooding control register

Bits	Field	Description	Type	Default
0	EN	Egress port mask for unknown multicast flooding packets 0b0: drop 0b1: normal flooding	RW	0x1

## LUT\_UNKN\_UC\_FLOOD

BASE ADDRESS : 0xBB01C028  
 PORT INDEX : 0 - 6

PORT OFFSET : 1 bit  
DEFAULT VALUE : 0x1

This is a One-Dimension Register Field Array. (1 bit per field)

LUT unknown unicast flooding control register

Bits	Field	Description	Type	Default
0	EN	Egress port mask for unknown unicast flooding packets 0b0: drop 0b1: normal flooding	RW	0x1

## L2\_EFID

BASE ADDRESS : 0xBB017030  
PORT INDEX : 0 - 6  
PORT OFFSET : 3 bits  
DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (3 bits per field)

per port Enhanced filtering database ID

Bits	Field	Description	Type	Default
2:0	EFID	per port EFID	RW	0x0

## LUT\_SYS\_LRN\_OVER\_CTRL

REGISTER ADDRESS : 0xBB017034  
DEFAULT VALUE : 0x0

LUT system learning over control register

Bits	Field	Description	Type	Default
31:2	RESERVED			
1:0	ACT	Auto leaning number exceed behavior 0b00: normal flooding 0b01: drop packet 0b10: trap to CPU 0b11: Copy to cPU	RW	0x0

### SECTION 3.2

## ADDRESS LEARNING & FLUSH

Address Learning & Flush module

## L2\_TBL\_FLUSH\_CTRL

REGISTER ADDRESS : 0xBB017038

DEFAULT VALUE : 0x0

L2 table flush control register. Specify the fid/vid and/or port to flush entries or replace the SLP field of L2 table.

Bits	Field	Description	Type	Default
31:21	RESERVED			
20:17	LUT_FLUSH_FID	L2 flushing FID	RW	0x0
16:5	LUT_FLUSH_VID	L2 flushing VID	RW	0x0
4	LUT_FLUSH_DYNAMIC	enable Force Flush dynamic entries	RW	0x0
3	LUT_FLUSH_STATIC	enable Force Flush static entries	RW	0x0
2:1	LUT_FLUSH_MODE	Force lut flush mode 0b00: Port based 0b01: Port + VLAN based 0b10: Port + FID/MSTI based 0b11: reserved.	RW	0x0
0	FLUSH_STATUS	Status of flush L2 table action. 0: non-busy 1: busy	RO	0x0

## L2\_TBL\_FLUSH\_EN

BASE ADDRESS : 0xBB01703C

PORT INDEX : 0 - 6

PORT OFFSET : 1 bit

DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

L2 table per-port flush enable register.

Bits	Field	Description	Type	Default
0	EN	Per-port L2 entries flush portmask	RWAC	0x0

### SECTION 3.3

## L2 & IP MULTICAST

L2 & IP Multicast module

## L2\_IPMC\_VLAN\_LEAKY

BASE ADDRESS : 0xBB01C02C

PORT INDEX : 0 - 6

PORT OFFSET : 1 bit

DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

L3 Multicast VLAN leaky function

Bits	Field	Description	Type	Default
0	EN	VLAN leaky for IPv4/IPv6 multicast packets 0b0:disable 0b1:enable	RW	0x0

## L2\_IPMC\_ISO\_LEAKY

BASE ADDRESS : 0xBB01C030

PORT INDEX : 0 - 6

PORT OFFSET : 1 bit

DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

L3 Multicast Port isolation leaky function

Bits	Field	Description	Type	Default
0	EN	Port isolation leaky for for IPv4/IPv6 multicast packets 0b0:disable 0b1:enable	RW	0x0

### SECTION 3.4

## (IEEE802.1Q) VLAN

(IEEE802.1Q VLAN) module

## VLAN\_PORT\_ACCEPT\_FRAME\_TYPE

BASE ADDRESS : 0xBB013000

PORT INDEX : 0 - 6

PORT OFFSET : 2 bits

DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (2 bits per field)

VLAN accept frame type configuration.

Bits	Field	Description	Type	Default
1:0	FRAME_TYPE	0b00: Admit All frames 0b01: Admit Only VLAN-tagged frames(VID 0-4094 and VID 4095 if VLAN_VID4095_TYPE = 1 and VLAN_VID0_TYPE = 1) 0b10: Admit Only Untagged and Priority-tagged frames.(Also VID 4095 if VLAN_VID4095_TYPE = 0) 0b11: Admit 1Q and 1P tagged frame(VID 0 4095)	RW	0x0

## VLAN\_INGRESS

BASE ADDRESS : 0xBB013004

PORT INDEX : 0 - 6

PORT OFFSET : 1 bit

DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

VLAN ingress function setting

Bits	Field	Description	Type	Default
0	INGRESS	VLAN per-Port enable VLAN ingress function setting 0b0:disable port vlan ingress filtering 0b1:enable	RW	0x0

## VLAN\_EGRESS\_TAG

BASE ADDRESS : 0xBB020030

PORT INDEX : 0 - 6

PORT OFFSET : 0x400

DEFAULT VALUE : 0x3

This is a One-Dimension Port Register Array.

VLAN tag egress format

Bits	Field	Description	Type	Default
31:2	RESERVED			
1:0	EGRESS_MODE	Per-port VLAN tag egress format 0b00: Original mode. Output frame will follow VLAN untag setting. 0b01: Keep format mode. Output frame will keep VLAN original format. 0b10: Priority tag mode. Output frame will be priority tag. 0b11: Keep format mode. Output frame will keep VLAN original format.(the same as 0b01)	RW	0x3

## VLAN\_MBR\_CFG

```

BASE ADDRESS :    0xBB013008
ARRAY INDEX :    0 - 31
ARRAY OFFSET :    0x8
DEFAULT VALUE :    0x0

```

This is a One-Dimension Common Register Array.

## VLAN memembr configuration

<b>Bits</b>	<b>Field</b>	<b>Description</b>	<b>Type</b>	<b>Default</b>
63:59	RESERVED			
58:46	EVID	Enhanced VID setting	RW	0x0
45:41	METERIDX	Policing share meter index	RW	0x0
40	ENVLANPOL	VLAN based policing 0b0:disable 0b1:enable	RW	0x0
39:37	VBPRI	VLAN based priority	RW	0x0
36	VBPEN	VLAN based priority decision source of VLAN member configuration index 0 0b0:disable 0b1:enable	RW	0x0
35:32	FID_MSTI	FID_MSTI	RW	0x0
31:29	RESERVED			
28:23	EXT_MBR	Extension forwardinf portmask, CPU and 5 extension ports. Per-entry default value as below: {0x0,0x0,0x0,0x0,0x0,0x0,0x0,0x0, 0x0,0x0,0x0,0x0,0x0,0x0,0x0,0x0, 0x0,0x0,0x0,0x0,0x0,0x0,0x0,0x0, 0x0,0x0,0x0,0x0,0x0,0x0,0x0,0x3F}	RW	0x0
22:7	RESERVED			
6:0	MBR	VLAN member. Per-entry default value as below: {0x0,0x0,0x0,0x0,0x0,0x0,0x0,0x0, 0x0,0x0,0x0,0x0,0x0,0x0,0x0,0x0, 0x0,0x0,0x0,0x0,0x0,0x0,0x0,0x0, 0x0,0x0,0x0,0x0,0x0,0x0,0x0,0x7F}	RW	0x0

## VLAN\_CTRL

REGISTER ADDRESS : 0xBB013108  
 DEFAULT VALUE : 0x0

VLAN global configuration.

Bits	Field	Description	Type	Default
31:5	RESERVED			



Bits	Field	Description	Type	Default
4	VID_4095_TYPE	0b0: treat VID 4095 as un-tagging frame 0b1: treat VID 4095 as tagging frame	RW	0x0
3	VID_0_TYPE	0b0: treat VID 0 as un-tagging frame 0b1: treat VID 0 as tagging frame	RW	0x0
2	CFI_KEEP	Keep ingress tag CFI 0b0: Always egress CFI=0 0b1: Keep ingress tag CFI value to egress tag	RW	0x0
1	TRANSPARENT_EN	Discard VLAN egress filtering if egress port in port-mask of VLAN_EGRESS_PORTn_VLAN_KEEP is configured in VLAN real keep mode	RW	0x0
0	VLAN_FILTERING	VLAN ingress and egress filtering enable setting 0b0:disable 0b1:enable	RW	0x0

## VLAN\_PB\_FID

BASE ADDRESS : 0xBB01310C  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 4 bits  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (4 bits per field)

Port-based FID configuration.

Bits	Field	Description	Type	Default
3:0	PBFID	Port Based FID	RW	0x0

## VLAN\_PB\_FIDEN

BASE ADDRESS : 0xBB013110  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

Port-based FID enable configuration.

Bits	Field	Description	Type	Default
0	PBFIDEN	Per port forced Port-based FID setting 0b0:disable, FID will be decided from 4K VLAN table or 32 VLAN member configuration 0b1:enable, forced using PORTn_PBFID for packets received from Port n	RW	0x0

## VLAN\_PB\_PRI

BASE ADDRESS : 0xBB01C034  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 3 bits  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (3 bits per field)

Port-based VLAN priority

Bits	Field	Description	Type	Default
2:0	PB_PRI	VLAN IQ Port based priority assignment	RW	0x0

## VLAN\_PB\_VIDX

BASE ADDRESS : 0xBB013114  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 5 bits  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (5 bits per field)

Port-based VLAN configuration.

Bits	Field	Description	Type	Default
4:0	VIDX	Port based CVLAN index to CVLAN member configuration	RW	0x0

## VLAN\_EGRESS\_KEEP

BASE ADDRESS : 0xBB01C038  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 7 bits  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (7 bits per field)

egress port 1 setting for VLAN mode Real keep reference by ingress port

Bits	Field	Description	Type	Default
6:0	MBR	Per egress port setting for VLAN mode Real keep reference by ingress port 0b0:packet from ingress port to egress port n will follow egress vlan mode setting by normal VLAN tag egress configuration 0b1:packet from ingress port to egress port n will be in VLAN real keep mode	RW	0x0

Bits	Field	Description	Type	Default
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## VLAN\_EXT\_VIDX

BASE ADDRESS : 0xBB01311C  
 ARRAY INDEX : 0 - 4  
 ARRAY OFFSET : 5 bits  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (5 bits per field)

EXT-based VLAN configuration.

Bits	Field	Description	Type	Default
4:0	VIDX	Extension port based CVLAN index to CVLAN member configuration	RW	0x0

### SECTION 3.5

## (IEEE802.1AD) PROVIDER BRIDGES/Q-IN-Q

(IEEE802.1ad) Provider Bridges/Q-in-Q module

## SVLAN\_UPLINK\_PMSK

BASE ADDRESS : 0xBB0230F0  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

SVLAN uplink port mask

Bits	Field	Description	Type	Default
0	EN	SVLAN uplink port enable configuration	RW	0x0

## SVLAN\_LOOK\_UP\_TYPE

REGISTER ADDRESS : 0xBB0230F4  
 DEFAULT VALUE : 0x0

SVLAN lookup type

Bits	Field	Description	Type	Default
31:7	RESERVED			

Bits	Field	Description	Type	Default
6:0	TYPE	0b0:SVLAN look up SVLAN 64 member configuration table 0b1:SVLAN look up CVLAN 4k table	RW	0x0

## SVLAN\_MC2S

BASE ADDRESS : 0xBB018000  
 ARRAY INDEX : 0 - 7  
 ARRAY OFFSET : 0xC  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

L2/L3 Multicast to SVLAN configuration

Bits	Field	Description	Type	Default
95:72	RESERVED			
71:66	SVIDX	SVLAN member configuration index of uplink port egressing packet which is L2 multicast or IPv4 multicast and destination mac/IP address is matched to MC2S configuration entry 0	RW	0x0
65	FORMAT	Compare data format of uplink port egressing packet which is L2 multicast or IPv4 multicast and destination mac/IP address is matched to MC2S configuration entry 0 0b0: compare data is DMAC{31:0} 0b1: compare data is IPv4 DIP	RW	0x0
64	VALID	Valid setting of MC2S configuration entry 0 0b0: not valid 0b1: valid	RW	0x0
63:32	DATA	Compare destination mac{31:0}/IP address	RW	0x0
31:0	MASK	Compare destination mac/IP address mask	RW	0x0

## SVLAN\_C2S

BASE ADDRESS : 0xBB014000  
 ARRAY INDEX : 0 - 127  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

CVLAN to SVLAN configuration

Bits	Field	Description	Type	Default
31:26	RESERVED			

Bits	Field	Description	Type	Default
25:13	EVID	Ingressing Enhanced VID of C2S configuration entry 0	RW	0x0
12:6	C2SENPMASK	Port member to assign egress SVID which packet ingress Enhanced VID is matched to C2S configuration entry 0	RW	0x0
5:0	SVIDX	SVLAN member configuration index of uplink port egressing packets which ingress Enhanced VID is matched to C2S configuration	RW	0x0

## SVLAN\_SP2C

BASE ADDRESS : 0xBB02A000  
 ARRAY INDEX : 0 - 127  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

Downstream SVLAN + Egress port to CVID configuration

Bits	Field	Description	Type	Default
31:22	RESERVED			
21:10	VID	Egressing CVID	RW	0x0
9:7	DST_PORT	Egressing customer port number of s-tag packet from uplink ports in SP2C configuration	RW	0x0
6:1	SVIDX	SVIDX of ingress s-tag packet from uplink ports in SP2C configuration	RW	0x0
0	VALID	Valid setting	RW	0x0

## SVLAN\_EP\_DMACK\_CTRL

BASE ADDRESS : 0xBB014200  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

egress Dmac CVID decision

Bits	Field	Description	Type	Default
0	EN	CVID decision from DMACK enable configuration	RW	0x0

## SVLAN\_P\_SVIDX

BASE ADDRESS : 0xBB014204  
PORT INDEX : 0 - 6  
PORT OFFSET : 6 bits  
DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (6 bits per field)

default egress SVLAN configuration

Bits	Field	Description	Type	Default
5:0	SVIDX	SVLAN configuration index	RW	0x0

## SVLAN\_CTRL

REGISTER ADDRESS : 0xBB01420C  
DEFAULT VALUE : 0x0

SVLAN related control register

Bits	Field	Description	Type	Default
31:23	RESERVED			
22	VS_SP2C_UNMAT	Ctagging action for downstream SP2C is un-matched 0b0:non C-tag 0b1:Ctagging	RW	0x0
21	VS_DEI_KEEP	Keep SVLAN ingress tag DEI 0b0: Always egress DEI=0 0b1: Keep ingress tag DEI value to egress tag	RW	0x0
20:18	VS_PRI	Trap priority for SVLAN trapping packets	RW	0x0
17:12	VS_UNTAG_SVIDX	Ingress SVLAN for un-stag packet from uplink port	RW	0x0
11:6	VS_UNMAT_SVIDX	Ingress SVLAN for unmatched SVID packet from uplink port	RW	0x0
5:4	VS_UNMAT	Unmatched SVID packet with trap to CPU action 0b00:drop 0b01: trap to CPU 0b10: assign ingress SVID as VS_UNMAT_SVIDX 0b11: assign ingress SVID as VS_UNMAT_SVIDX and keep original SVLAN format	RW	0x0
3:2	VS_UNTAG	un-stagged packet with trap to CPU action 0b00:drop 0b01: trap to CPU 0b10: assign ingress SVID as VS_UNTAG_SVIDX 0b11: reserved	RW	0x0

Bits	Field	Description	Type	Default
1:0	VS_SPRISEL	S-priority assignment of upstream packet setting 0b00: use internal priority 0b01: use 1Q tag priority 0b10: use VS_SPRI as S-Priority 0b11: using port based priority	RW	0x0

## SVLAN\_CFG

REGISTER ADDRESS : 0xBB0230F8

DEFAULT VALUE : 0x88A8

SVLAN TPID configuration control register

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	VS_TPID	VLAN Stacking Protocol Type	RW	0x88A8

## SVLAN\_MBRCFG

BASE ADDRESS : 0xBB014210

ARRAY INDEX : 0 - 63

ARRAY OFFSET : 0x8

DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

SVLAN member configuration

Bits	Field	Description	Type	Default
63:48	RESERVED			
47:45	EFID	EFID of received S-tag packet which SVID is the same as this configuration entry	RW	0x0
44	EFIDEN	Usage EFID setting of received S-tag packet which SVID is the same as this configuration entry	RW	0x0
43:32	SVID	SVID of received S-tag packet which SVID is the same as this configuration	RW	0x0
31:24	RESERVED			
23	FIDEN	Force FID from SVLAN	RW	0x0
22:20	SPR	SVLAN priority assignment of received S-tag packet which SVID is the same as this configuration entry 0	RW	0x0
19:16	FID_MSTI	Filtering Database/ Multiple Spanning Tree Instance for accepted S-VID	RW	0x0
15	RESERVED			
14:8	UNTAGSET	SVLAN untag set	RW	0x0

Bits	Field	Description	Type	Default
7	RESERVED			
6:0	MBR	Port member of received S-tag packet which SVID is the same as this configuration entry	RW	0x0

## SECTION 3.6

## (IEEE802.1V) PROTOCOL-BASED VLAN

(IEEE802.1v) Protocol-based VLAN module

### VLAN\_PPB\_VLAN\_VAL

BASE ADDRESS : 0xBB013120  
 ARRAY INDEX : 0 - 3  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

Specify IEEE 802.1v(Protocol-and-Port-based VLAN) configuration. Global eight protocol values are supported and each port can have different PPB VLAN for the same protocol value through VLAN\_PORT\_PPB\_VLAN.

Bits	Field	Description	Type	Default
31:18	RESERVED			
17:2	ETHER_TYPE	EtherType or DSAP/SSAP of protocol and port based vlan	RW	0x0
1:0	FRAME_TYPE	Frame format of protocol and port based vlan 0b00: Ethernet 0b01: LLC_Other 0b10: RFC1042 0b11:As usage disabled	RW	0x0

### VLAN\_PORT\_PPB\_VLAN

BASE ADDRESS : 0xBB013130  
 ARRAY INDEX1 : 0 - 6  
 ARRAY OFFSET1 : 0x10  
 ARRAY INDEX2 : 0 - 3  
 ARRAY OFFSET2 : 0x4  
 DEFAULT VALUE : 0x0

This is a Two-Dimension Common Register Array.

Per-port per-protocol specifies the Protocol-and-Port-based VLAN. A packet is given to the specified VID if its protocol value hit the PPB configuration.

Bits	Field	Description	Type	Default
31:16	RESERVED			



Bits	Field	Description	Type	Default
15:13	PPB_PRI	VLAN 1Q priority assignmnet for PPB VLAN	RW	0x0
12:6	RESERVED			
5:1	PPB_VIDX	Protocol-and-Port-based VLAN	RW	0x0
0	VALID	Valid bit.	RW	0x0

## SECTION 3.7

## LINK AGGREGATION

Link Aggregation module

### PORT\_TRUNK\_GROUP\_EN

BASE ADDRESS : 0xBB01C040  
 PORT INDEX : 0 - 3  
 PORT OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Port trunking aggregation UTP port enable register

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	EN	Port trunking aggregation UTP port enable setting	RW	0x0

### PORT\_TRUNK\_CTRL

REGISTER ADDRESS : 0xBB01C050  
 DEFAULT VALUE : 0x100

Port trunking configuration

Bits	Field	Description	Type	Default
31:10	RESERVED			
9	EN_FLOWCTRL_TG0	Egress port flow control for trunking group 0 0b0:disable 0b1:enable port trunking egress flow control	RW	0x0
8	PORT_TRUNK_DUMB	0: not dumb mode, 1: dumb mode	RW	0x1
7	PORT_TRUNK_FLOOD	Enable directly forwarding unknown (L2 lookup miss) packets to aggregation logic 1st port and normal forward other packets to other available trunking ports.	RW	0x0
6	DPORT_HASH	Port trunking hash algorithm selection with DPORT	RW	0x0

Bits	Field	Description	Type	Default
5	SPORT_HASH	Port trunking hash algorithm selection with SPORT	RW	0x0
4	DIP_HASH	Port trunking hash algorithm selection with DIP	RW	0x0
3	SIP_HASH	Port trunking hash algorithm selection with SIP	RW	0x0
2	DMAC_HASH	Port trunking hash algorithm selection with DMAC	RW	0x0
1	SMAC_HASH	Port trunking hash algorithm selection with SMAC	RW	0x0
0	SPA_HASH	Port trunking hash algorithm selection with SPA (source port)	RW	0x0

## PORT\_TRUNK\_HASH\_MAPPING

BASE ADDRESS : 0xBB01C054  
 ARRAY INDEX : 0 - 15  
 ARRAY OFFSET : 2 bits  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (2 bits per field)

Port number mapping to hash value

Bits	Field	Description	Type	Default
1:0	HASH	Port number mapping to hash value	RW	0x0

### SECTION 3.8

## SPANNING TREE

Spanning Tree module

## MSTI\_CTRL

BASE ADDRESS : 0xBB017040  
 ARRAY INDEX1 : 0 - 6  
 ARRAY OFFSET1 : 0x4  
 ARRAY INDEX2 : 0 - 15  
 ARRAY OFFSET2 : 2 bits  
 DEFAULT VALUE : 0x3

This is a Two-Dimension Register Field Array. (2 bits per field)

MSTP Port State register

Bits	Field	Description	Type	Default
1:0	STATE	Port status of multiple spanning tree 0b00: Disabled State 0b01: Blocking/Listening State 0b10: Learning State 0b11: Forwarding State	RW	0x3

## SECTION 3.9

## PORT ISOLATION

Port Isolation

### PISO\_P\_MODE0\_CTRL

BASE ADDRESS : 0xBB027000  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 13 bits  
 DEFAULT VALUE : 0x1FFF

This is a One-Dimension Register Field Array. (13 bits per field)

Port isolation configuration that each port can specify a port list to communicate with.

Bits	Field	Description	Type	Default
12:0	PORTMASK	The destination portmask of ingress port bit 6-0: port 6 port 0 bit 7: CPU port bit 12-8: extension port 4 0	RW	0x1FFF

### PISO\_P\_MODE1\_CTRL

BASE ADDRESS : 0xBB027010  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 13 bits  
 DEFAULT VALUE : 0x1FFF

This is a One-Dimension Register Field Array. (13 bits per field)

Port isolation configuration that each port can specify a port list to communicate with.

Bits	Field	Description	Type	Default
12:0	PORTMASK	The destination portmask of ingress port bit 6-0: port 6 port 0 bit 7: CPU port bit 12-8: extension port 4 0	RW	0x1FFF

## PISO\_EXT\_MODE0\_CTRL

BASE ADDRESS : 0xBB027020  
 ARRAY INDEX : 0 - 4  
 ARRAY OFFSET : 13 bits  
 DEFAULT VALUE : 0x1FFF

This is a One-Dimension Register Field Array. (13 bits per field)

Port isolation configuration that each extension port can specify a port list to communicate with.

Bits	Field	Description	Type	Default
12:0	PORTMASK	The destination portmask of ingress port bit 6-0: port 6 port 0 bit 7: CPU port bit 12-8: extension port 4 0	RW	0x1FFF

## PISO\_EXT\_MODE1\_CTRL

BASE ADDRESS : 0xBB02702C  
 ARRAY INDEX : 0 - 4  
 ARRAY OFFSET : 13 bits  
 DEFAULT VALUE : 0x1FFF

This is a One-Dimension Register Field Array. (13 bits per field)

Port isolation configuration that each extension port can specify a port list to communicate with.

Bits	Field	Description	Type	Default
12:0	PORTMASK	The destination portmask of ingress port bit 6-0: port 6 port 0 bit 7: CPU port bit 12-8: extension port 4 0	RW	0x1FFF

## PISO\_CTRL

REGISTER ADDRESS : 0xBB027038  
 DEFAULT VALUE : 0x0

Port isolation control

Bits	Field	Description	Type	Default
31:2	RESERVED			

Bits	Field	Description	Type	Default
1	CTAG_SEL	Isolation configuration selection for ingress Ctag packets 0b0: Using port or extension port isolation setting mode 0 0b1: Using port or extension port isolation setting mode 1	RW	0x0
0	L34_SEL	Isolation configuration selection for L34 packets (which L2trans hsb field is set) 0b0: Using port or extension port isolation setting mode 0 0b1: Using port or extension port isolation setting mode 1	RW	0x0

## SECTION 3.10

## RMA

RMA module

### RMA\_CTRL00

REGISTER ADDRESS : 0xBB01C058

DEFAULT VALUE : 0x0

Reserved Multicast Address control register for 01-80-C2-00-00-00

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:4	OPERATION	Operation setting for aware Reserved Multicast Address 0B00: forwarding 0B01: trap to CPU 0B10: drop 0B11: forward, but not trap to CPU	RW	0x0
3	DISCARD_STORM_FILTER	Discard packet flow counting in storm filtering control for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
2	KEEP_FORMAT	Keep packet C-tag format for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
1	VLAN_LEAKY	Bypass CVLAN egress filtering for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
0	PORTISO_LEAKY	Bypass port isolation function for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0

## RMA\_CTRL01

REGISTER ADDRESS : 0xBB01C05C

DEFAULT VALUE : 0x20

Reserved Multicast Address control register for 01-80-C2-00-00-01

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:4	OPERATION	Operation setting for aware Reserved Multicast Address 0B00: forwarding 0B01: trap to CPU 0B10: drop 0B11: forward, but not trap to CPU	RW	0x2
3	DISCARD_STORM_FILTER	Discard packet flow counting in storm filtering control for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
2	KEEP_FORMAT	Keep packet C-tag format for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
1	VLAN_LEAKY	Bypass CVLAN egress filtering for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
0	PORTISO_LEAKY	Bypass port isolation function for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0

## RMA\_CTRL02

REGISTER ADDRESS : 0xBB01C060

DEFAULT VALUE : 0x20

Reserved Multicast Address control register for 01-80-C2-00-00-02

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:4	OPERATION	Operation setting for aware Reserved Multicast Address 0B00: forwarding 0B01: trap to CPU 0B10: drop 0B11: forward, but not trap to CPU	RW	0x2
3	DISCARD_STORM_FILTER	Discard packet flow counting in storm filtering control for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0

Bits	Field	Description	Type	Default
2	KEEP_FORMAT	Keep packet C-tag format for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
1	VLAN_LEAKY	Bypass CVLAN egress filtering for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
0	PORTISO_LEAKY	Bypass port isolation function for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0

### RMA\_CTRL03

REGISTER ADDRESS : 0xBB01C064

DEFAULT VALUE : 0x0

Reserved Multicast Address control register for 01-80-C2-00-00-03

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:4	OPERATION	Operation setting for aware Reserved Multicast Address 0B00: forwarding 0B01: trap to CPU 0B10: drop 0B11: forward, but not trap to CPU	RW	0x0
3	DISCARD_STORM_FILTER	Discard packet flow counting in storm filtering control for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
2	KEEP_FORMAT	Keep packet C-tag format for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
1	VLAN_LEAKY	Bypass CVLAN egress filtering for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
0	PORTISO_LEAKY	Bypass port isolation function for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0

### RMA\_CTRL04

REGISTER ADDRESS : 0xBB01C068

DEFAULT VALUE : 0x0

Reserved Multicast Address control register for 01-80-C2-00-00-04,05,06,07,09,0A,0B,0C,0F

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:4	OPERATION	Operation setting for aware Reserved Multicast Address 0B00: forwarding 0B01: trap to CPU 0B10: drop 0B11: forward, but not trap to CPU	RW	0x0
3	DISCARD_STORM_FILTER	Discard packet flow counting in storm filtering control for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
2	KEEP_FORMAT	Keep packet C-tag format for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
1	VLAN_LEAKY	Bypass CVLAN egress filtering for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
0	PORTISO_LEAKY	Bypass port isolation function for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0

## RMA\_CTRL08

REGISTER ADDRESS : 0xBB01C06C

DEFAULT VALUE : 0x0

Reserved Multicast Address control register for 01-80-C2-00-00-08

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:4	OPERATION	Operation setting for aware Reserved Multicast Address 0B00: forwarding 0B01: trap to CPU 0B10: drop 0B11: forward, but not trap to CPU	RW	0x0
3	DISCARD_STORM_FILTER	Discard packet flow counting in storm filtering control for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
2	KEEP_FORMAT	Keep packet C-tag format for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0



Bits	Field	Description	Type	Default
1	VLAN_LEAKY	Bypass CVLAN egress filtering for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
0	PORTISO_LEAKY	Bypass port isolation function for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0

## RMA\_CTRL0D

REGISTER ADDRESS : 0xBB01C070

DEFAULT VALUE : 0x0

Reserved Multicast Address control register for 01-80-C2-00-00-0D

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:4	OPERATION	Operation setting for aware Reserved Multicast Address 0B00: forwarding 0B01: trap to CPU 0B10: drop 0B11: forward, but not trap to CPU	RW	0x0
3	DISCARD_STORM_FILTER	Discard packet flow counting in storm filtering control for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
2	KEEP_FORMAT	Keep packet C-tag format for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
1	VLAN_LEAKY	Bypass CVLAN egress filtering for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
0	PORTISO_LEAKY	Bypass port isolation function for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0

## RMA\_CTRL0E

REGISTER ADDRESS : 0xBB01C074

DEFAULT VALUE : 0x0

Reserved Multicast Address control register for 01-80-C2-00-00-0E

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:4	OPERATION	Operation setting for aware Reserved Multicast Address 0B00: forwarding 0B01: trap to CPU 0B10: drop 0B11: forward, but not trap to CPU	RW	0x0
3	DISCARD_STORM_FILTER	Discard packet flow counting in storm filtering control for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
2	KEEP_FORMAT	Keep packet C-tag format for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
1	VLAN_LEAKY	Bypass CVLAN egress filtering for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
0	PORTISO_LEAKY	Bypass port isolation function for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0

## RMA\_CTRL10

REGISTER ADDRESS : 0xBB01C078

DEFAULT VALUE : 0x0

Reserved Multicast Address control register for 01-80-C2-00-00-10

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:4	OPERATION	Operation setting for aware Reserved Multicast Address 0B00: forwarding 0B01: trap to CPU 0B10: drop 0B11: forward, but not trap to CPU	RW	0x0
3	DISCARD_STORM_FILTER	Discard packet flow counting in storm filtering control for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
2	KEEP_FORMAT	Keep packet C-tag format for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
1	VLAN_LEAKY	Bypass CVLAN egress filtering for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0

Bits	Field	Description	Type	Default
0	PORTISO_LEAKY	Bypass port isolation function for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0

## RMA\_CTRL11

REGISTER ADDRESS : 0xBB01C07C

DEFAULT VALUE : 0x0

Reserved Multicast Address control register for 01-80-C2-00-00-11

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:4	OPERATION	Operation setting for aware Reserved Multicast Address 0B00: forwarding 0B01: trap to CPU 0B10: drop 0B11: forward, but not trap to CPU	RW	0x0
3	DISCARD_STORM_FILTER	Discard packet flow counting in storm filtering control for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
2	KEEP_FORMAT	Keep packet C-tag format for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
1	VLAN_LEAKY	Bypass CVLAN egress filtering for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
0	PORTISO_LEAKY	Bypass port isolation function for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0

## RMA\_CTRL12

REGISTER ADDRESS : 0xBB01C080

DEFAULT VALUE : 0x0

Reserved Multicast Address control register for 01-80-C2-00-00-12

Bits	Field	Description	Type	Default
31:6	RESERVED			

Bits	Field	Description	Type	Default
5:4	OPERATION	Operation setting for aware Reserved Multicast Address 0B00: forwarding 0B01: trap to CPU 0B10: drop 0B11: forward, but not trap to CPU	RW	0x0
3	DISCARD_STORM_FILTER	Discard packet flow counting in storm filtering control for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
2	KEEP_FORMAT	Keep packet C-tag format for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
1	VLAN_LEAKY	Bypass CVLAN egress filtering for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
0	PORTISO_LEAKY	Bypass port isolation function for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0

## RMA\_CTRL13

REGISTER ADDRESS : 0xBB01C084

DEFAULT VALUE : 0x0

Reserved Multicast Address control register for 01-80-C2-00-00-13,14,15,16,17,19,1B,1C,1D,1E,1F

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:4	OPERATION	Operation setting for aware Reserved Multicast Address 0B00: forwarding 0B01: trap to CPU 0B10: drop 0B11: forward, but not trap to CPU	RW	0x0
3	DISCARD_STORM_FILTER	Discard packet flow counting in storm filtering control for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
2	KEEP_FORMAT	Keep packet C-tag format for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
1	VLAN_LEAKY	Bypass CVLAN egress filtering for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0

Bits	Field	Description	Type	Default
0	PORTISO_LEAKY	Bypass port isolation function for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0

## RMA\_CTRL18

REGISTER ADDRESS : 0xBB01C088

DEFAULT VALUE : 0x0

Reserved Multicast Address control register for 01-80-C2-00-00-18

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:4	OPERATION	Operation setting for aware Reserved Multicast Address 0B00: forwarding 0B01: trap to CPU 0B10: drop 0B11: forward, but not trap to CPU	RW	0x0
3	DISCARD_STORM_FILTER	Discard packet flow counting in storm filtering control for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
2	KEEP_FORMAT	Keep packet C-tag format for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
1	VLAN_LEAKY	Bypass CVLAN egress filtering for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
0	PORTISO_LEAKY	Bypass port isolation function for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0

## RMA\_CTRL1A

REGISTER ADDRESS : 0xBB01C08C

DEFAULT VALUE : 0x0

Reserved Multicast Address control register for 01-80-C2-00-00-1A

Bits	Field	Description	Type	Default
31:6	RESERVED			

Bits	Field	Description	Type	Default
5:4	OPERATION	Operation setting for aware Reserved Multicast Address 0B00: forwarding 0B01: trap to CPU 0B10: drop 0B11: forward, but not trap to CPU	RW	0x0
3	DISCARD_STORM_FILTER	Discard packet flow counting in storm filtering control for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
2	KEEP_FORMAT	Keep packet C-tag format for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
1	VLAN_LEAKY	Bypass CVLAN egress filtering for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
0	PORTISO_LEAKY	Bypass port isolation function for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0

## RMA\_CTRL20

REGISTER ADDRESS : 0xBB01C090

DEFAULT VALUE : 0x0

Reserved Multicast Address control register for 01-80-C2-00-00-20

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:4	OPERATION	Operation setting for aware Reserved Multicast Address 0B00: forwarding 0B01: trap to CPU 0B10: drop 0B11: forward, but not trap to CPU	RW	0x0
3	DISCARD_STORM_FILTER	Discard packet flow counting in storm filtering control for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
2	KEEP_FORMAT	Keep packet C-tag format for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
1	VLAN_LEAKY	Bypass CVLAN egress filtering for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0

Bits	Field	Description	Type	Default
0	PORTISO_LEAKY	Bypass port isolation function for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0

## RMA\_CTRL21

REGISTER ADDRESS : 0xBB01C094

DEFAULT VALUE : 0x0

Reserved Multicast Address control register for 01-80-C2-00-00-21

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:4	OPERATION	Operation setting for aware Reserved Multicast Address 0B00: forwarding 0B01: trap to CPU 0B10: drop 0B11: forward, but not trap to CPU	RW	0x0
3	DISCARD_STORM_FILTER	Discard packet flow counting in storm filtering control for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
2	KEEP_FORMAT	Keep packet C-tag format for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
1	VLAN_LEAKY	Bypass CVLAN egress filtering for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
0	PORTISO_LEAKY	Bypass port isolation function for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0

## RMA\_CTRL22

REGISTER ADDRESS : 0xBB01C098

DEFAULT VALUE : 0x0

Reserved Multicast Address control register for 01-80-C2-00-00-22 2F

Bits	Field	Description	Type	Default
31:6	RESERVED			

Bits	Field	Description	Type	Default
5:4	OPERATION	Operation setting for aware Reserved Multicast Address 0B00: forwarding 0B01: trap to CPU 0B10: drop 0B11: forward, but not trap to CPU	RW	0x0
3	DISCARD_STORM_FILTER	Discard packet flow counting in storm filtering control for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
2	KEEP_FORMAT	Keep packet C-tag format for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
1	VLAN_LEAKY	Bypass CVLAN egress filtering for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
0	PORTISO_LEAKY	Bypass port isolation function for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0

## RMA\_CTRL\_CDP

REGISTER ADDRESS : 0xBB01C09C

DEFAULT VALUE : 0x0

Cisco Discovery Protocol control register for 01-00-0C-CC-CC-CC

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:4	OPERATION	Operation setting for aware Reserved Multicast Address 0B00: forwarding 0B01: trap to CPU 0B10: drop 0B11: forward, but not trap to CPU	RW	0x0
3	DISCARD_STORM_FILTER	Discard packet flow counting in storm filtering control for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
2	KEEP_FORMAT	Keep packet C-tag format for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
1	VLAN_LEAKY	Bypass CVLAN egress filtering for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0



Bits	Field	Description	Type	Default
0	PORTISO_LEAKY	Bypass port isolation function for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0

## RMA\_CTRL\_SSTP

REGISTER ADDRESS : 0xBB01C0A0

DEFAULT VALUE : 0x0

Cisco Shared Spanning Tree Protocol control register for 01-00-0C-CC-CC-CD

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:4	OPERATION	Operation setting for aware Reserved Multicast Address 0B00: forwarding 0B01: trap to CPU 0B10: drop 0B11: forward, but not trap to CPU	RW	0x0
3	DISCARD_STORM_FILTER	Discard packet flow counting in storm filtering control for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
2	KEEP_FORMAT	Keep packet C-tag format for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
1	VLAN_LEAKY	Bypass CVLAN egress filtering for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0
0	PORTISO_LEAKY	Bypass port isolation function for aware Reserved Multicast Address 0B0: disable 0B1: enable	RW	0x0

## RMA\_CFG

REGISTER ADDRESS : 0xBB01C0A4

DEFAULT VALUE : 0x0

Reserved Multicast Address control configuration

Bits	Field	Description	Type	Default
31:3	RESERVED			
2:0	RMA_TRAP_PRIORITY	RMA trap priority assignment for frames be trapped to CPU port	RW	0x0

Bits	Field	Description	Type	Default
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## EEELDP\_CTRL\_0

REGISTER ADDRESS : 0xBB01C0A8

DEFAULT VALUE : 0x0

Reserved Multicast Address control configuration

Bits	Field	Description	Type	Default
31:10	RESERVED			
9	EN	Enable/Disable EEE LLDP function 0: Disable 1: Enable	RW	0x0
8	TRAP_EN	Enable/Disable trap EEE LLDP to CPU 0: Disable 1: Enable	RW	0x0
7:0	SUBTYPE	Subtype field of EEE LLDP	RW	0x0

## EEELDP\_CTRL\_1

REGISTER ADDRESS : 0xBB01C0AC

DEFAULT VALUE : 0x0

Reserved Multicast Address control configuration

Bits	Field	Description	Type	Default
31:3	RESERVED			
2:0	TRAP_PRI	Trap to CPU priority of EEE LLDP	RW	0x0

### SECTION 3.11

## L2 MISC.

L2 Misc. module

## L2\_SRC\_PORT\_PERMIT

BASE ADDRESS : 0xBB01C0B0

PORT INDEX : 0 - 6

PORT OFFSET : 1 bit

DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

per port block packet forwarding

Bits	Field	Description	Type	Default
0	EN	per port block packet forwarding which receiving from the same port 0b0:enable block 0b1:forward	RW	0x0

## L2\_SRC\_EXT\_PERMIT

BASE ADDRESS : 0xBB01C0B4

ARRAY INDEX : 0 - 4

ARRAY OFFSET : 1 bit

DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

per EXT port block packet forwarding

Bits	Field	Description	Type	Default
0	EN	per EXT port block packet forwarding which receiving from the same port 0b0:enable block 0b1:forward	RW	0x0



## CHAPTER 4

# NIC

The chapter describes features related to NIC interface

### SECTION 4.1

## NIC & DMA

NIC & DMA module

### NIC\_ID\_CTRL0

REGISTER ADDRESS : 0xBB710000

DEFAULT VALUE : 0x0

ID registers control 0

Bits	Field	Description	Type	Default
31:24	IDR3	ID Register 3	RW	0x0
23:16	IDR2	ID Register 2	RW	0x0
15:8	IDR1	ID Register 1	RW	0x0
7:0	IDR0	ID Register 0, The ID register0-5 are only permitted to write by 4-byte access. Read access can be byte, word, or double word access. The initial value is autoloading from Flash	RW	0x0

### NIC\_ID\_CTRL1

REGISTER ADDRESS : 0xBB710004

DEFAULT VALUE : 0x0

ID registers control 1

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:8	IDR5	ID Register 5	RW	0x0
7:0	IDR4	ID Register 4	RW	0x0

## NIC\_MC\_CRTL0

REGISTER ADDRESS : 0xBB710008

DEFAULT VALUE : 0x0

Multicast control 0

Bits	Field	Description	Type	Default
31:24	MAR3	ID Register 3	RW	0x0
23:16	MAR2	ID Register 2	RW	0x0
15:8	MAR1	ID Register 1	RW	0x0
7:0	MAR0	Multicast Register 0, The MAR register0-7 are only permitted to write by 4-byte access. Read access can be byte, word, or double word access. Driver is responsible for initializing these registers. The MAR7-0 define 64 bits which is a bit wise index of the multicast function of multicast addresses. The hash function of multicast address is the upper 6 MSBs of the CRC32 of the address (destination). The index then is the numerical representation of those 6 bits in hex format.	RW	0x0

## NIC\_MC\_CRTL1

REGISTER ADDRESS : 0xBB71000C

DEFAULT VALUE : 0x0

Multicast control 1

Bits	Field	Description	Type	Default
31:24	MAR7	ID Register 7	RW	0x0
23:16	MAR6	ID Register 6	RW	0x0
15:8	MAR5	ID Register 5	RW	0x0
7:0	MAR4	ID Register 4	RW	0x0

## NIC\_MIB0

REGISTER ADDRESS : 0xBB710010

DEFAULT VALUE : 0x0

MIB counter 0

Bits	Field	Description	Type	Default
31:16	RX_OK_CNT	counter of Tx DMA Ok packets	RO	0x0

Bits	Field	Description	Type	Default
15:0	TX_OK_CNT	counter of Rx Ok packets	RO	0x0

## NIC\_MIB1

REGISTER ADDRESS : 0xBB710014

DEFAULT VALUE : 0x0

MIB counter 1

Bits	Field	Description	Type	Default
31:16	RX_ERR_CNT	packet counter of Rx errors including CRC error packets (should be larger than 8 bytes) and missed packets	RO	0x0
15:0	TX_ERR_CNT	packet counter of Tx errors including Tx abort, carrier lost and out of window collision	RO	0x0

## NIC\_MIB2

REGISTER ADDRESS : 0xBB710018

DEFAULT VALUE : 0x0

MIB counter 2

Bits	Field	Description	Type	Default
31:16	FAE	counter of Frame Alignment Error packets (MII mode only)	RO	0x0
15:0	MISS_PKT	counter of missed packets resulting from Rx FIFO full.	RO	0x0

## NIC\_MIB3

REGISTER ADDRESS : 0xBB71001C

DEFAULT VALUE : 0x0

MIB counter 3

Bits	Field	Description	Type	Default
31:16	TX_MUL_COL	counter of those Tx Ok packets with more than 1, and less than 16 collisions happened before Tx Ok	RO	0x0
15:0	TX_1_COL	counter of those Tx Ok packets with only 1 collision happened before Tx Ok.	RO	0x0

**NIC\_MIB4**

REGISTER ADDRESS : 0xBB710020

DEFAULT VALUE : 0x0

MIB counter 4

Bits	Field	Description	Type	Default
31:16	RX_OK_BC	counter of all Rx Ok packets with broadcast destination ID.	RO	0x0
15:0	RX_OK_PHY	counter of all Rx Ok packets with physical address matched destination ID	RO	0x0

**NIC\_MIB5**

REGISTER ADDRESS : 0xBB710024

DEFAULT VALUE : 0x0

MIB counter 5

Bits	Field	Description	Type	Default
31:16	TX_ABORT	counter of Tx abort packets	RO	0x0
15:0	RX_OK_MC	counter of all Rx Ok packets with multicast destination	RO	0x0

**NIC\_MIB6**

REGISTER ADDRESS : 0xBB710028

DEFAULT VALUE : 0x0

MIB counter 6

Bits	Field	Description	Type	Default
31:16	RSV2A		RO	0x0
15:0	TX_UNDER_RUN	counter of Tx Underrun packets. Rolls over automatically. Write to clear. gmac only	RO	0x0

**NIC\_STS**

REGISTER ADDRESS : 0xBB710034

DEFAULT VALUE : 0x0



## Tx/Rx Status Register

Bits	Field	Description	Type	Default
31:3	RESERVED			
2	TX_UNDER	Transmit FIFO Underrun: Set to 1 if the Tx FIFO was exhausted during the transmission of a packet. The Ethernet module can re-transfer data if the Tx FIFO underruns and can also transmit the packet to the wire successfully even though the Tx FIFO underruns. That is, when TSD<TUN>=1, TSD<TOK>=0 and ISR<TOK>=1 (or ISR<TER>=1). Handle under-run transmit with care.	RO	0x0
1:0	RESERVED			

**NIC\_COM**

REGISTER ADDRESS : 0xBB710038

DEFAULT VALUE : 0x0

## Tx/Rx Status Register

Bits	Field	Description	Type	Default
31:4	RESERVED			
3	RX_JUMBO	1: support jumble packet receiving. The maximum packet size is 16384B(0x4000). 0: Does not support jumble packet receiving	RW	0x0
2	RX_VLAN	Receive VLAN de-tagging enable. 1: Enable. 0: Disable.	RW	0x0
1	RX_CHKSUM	Receive checksum offload enable. 1: Enable. 0: Disable.	RW	0x0
0	RST	Reset: Setting to 1 forces the Ethernet module to a software reset state which disables the transmitter and receiver, reinitializes the FIFOs, triggers interrupt Swint for RISC to reset the system buffer pointer to the initial value Tx/Rx FDP. The values of IDR0-5 and MAR0-7 will have no changes. This bit is 1 during the reset operation, and is cleared to 0 by the Ethernet Module when the reset operation is complete.	RW	0x0

**NIC\_INTR**

REGISTER ADDRESS : 0xBB71003C

DEFAULT VALUE : 0x0

## interrupt control

Bits	Field	Description	Type	Default
31	ISR_RDU6	Rx Descriptor Unavailable for RING6: When set, indicates Rx descriptor is unavailable.	RC	0x0
30	ISR_RDU5	Rx Descriptor Unavailable for RING5: When set, indicates Rx descriptor is unavailable.	RC	0x0
29	ISR_RDU4	Rx Descriptor Unavailable for RING4: When set, indicates Rx descriptor is unavailable.	RC	0x0
28	ISR_RDU3	Rx Descriptor Unavailable for RING3: When set, indicates Rx descriptor is unavailable.	RC	0x0
27	ISR_RDU2	Rx Descriptor Unavailable for RING2: When set, indicates Rx descriptor is unavailable.	RC	0x0
26	ISR_SW_INT	Software Interrupt pending: When set to 1 indicates a software interrupt was forced	RC	0x0
25	ISR_TDU	Tx Descriptor Unavailable: When set, indicates Tx descriptor is unavailable	RC	0x0
24	ISR_LINK_CHG	Link Change	RC	0x0
23	ISR_TER	Transmit (Tx) Error: Indicates that a packet transmission was aborted, due to excessive collisions, according to the TXRR's setting	RC	0x0
22	ISR_TOK_TI	Transmit Interrupt: Indicates that the DMA of the last descriptor of RxIntMitigation number of Tx packet has completed and the last descriptor has been closed.	RC	0x0
21	ISR_RDU	Rx Descriptor Unavailable for RING1: When set, indicates Rx descriptor is unavailable	RC	0x0
20	ISR_RER_OVF	Rx FIFO Overflow, caused by RBO/RDU, poor system bus (Lexra bus) performance, or overloaded Lexra bus traffic	RC	0x0
19	RESERVED			
18	ISR_RER_RUNT	Rx error caused by runt error characterized by the frame length in bytes being less than 64 bytes.	RC	0x0
17	RESERVED			
16	ISR_ROK	Receive (Rx) OK: This interrupt is set either when RxIntMitigation packet is met or RxPktTimer expires	RC	0x0
15	IMR_RDU6	Rx Descriptor Unavailable for RING6: When set, indicates Rx descriptor is unavailable.	RW	0x0
14	IMR_RDU5	Rx Descriptor Unavailable for RING5: When set, indicates Rx descriptor is unavailable.	RW	0x0
13	IMR_RDU4	Rx Descriptor Unavailable for RING4: When set, indicates Rx descriptor is unavailable.	RW	0x0
12	IMR_RDU3	Rx Descriptor Unavailable for RING3: When set, indicates Rx descriptor is unavailable.	RW	0x0
11	IMR_RDU2	Rx Descriptor Unavailable for RING2: When set, indicates Rx descriptor is unavailable.	RW	0x0
10	IMR_SW_INT	Software Interrupt pending: When set to 1 indicates a software interrupt was forced	RW	0x0
9	IMR_TDU	Tx Descriptor Unavailable: When set, indicates Tx descriptor is unavailable	RW	0x0
8	IMR_LINK_CHG	Link Change	RW	0x0

Bits	Field	Description	Type	Default
7	IMR_TER	Transmit (Tx) Error: Indicates that a packet transmission was aborted, due to excessive collisions, according to the TXRR's setting	RW	0x0
6	IMR_TOK_TI	Transmit Interrupt: Indicates that the DMA of the last descriptor of RxIntMitigation number of Tx packet has completed and the last descriptor has been closed.	RW	0x0
5	IMR_RDU	Rx Descriptor Unavailable for RING1: When set, indicates Rx descriptor is unavailable	RW	0x0
4	IMR_RER_OVF	Rx FIFO Overflow, caused by RBO/RDU, poor system bus (Lexra bus) performance, or overloaded Lexra bus traffic	RW	0x0
3	RESERVED			
2	IMR_RER_RUNT	Rx error caused by runt error characterized by the frame length in bytes being less than 64 bytes.	RW	0x0
1	RESERVED			
0	IMR_ROK	Receive (Rx) OK: This interrupt is set either when RxIntMitigation packet is met or RxPktTimer expires	RW	0x0

## NIC\_IMR0\_CFG

REGISTER ADDRESS : 0xBB710040

DEFAULT VALUE : 0x0

IMR0 configuration

Bits	Field	Description	Type	Default
31:29	RESERVED			
28	IMR0_TDU5		RW	0x0
27	IMR0_TDU4		RW	0x0
26	IMR0_TDU3		RW	0x0
25	IMR0_TDU2		RW	0x0
24	IMR0_TDU1		RO	0x0
23:21	RESERVED			
20	IMR0_TOK5		RW	0x0
19	IMR0_TOK4		RW	0x0
18	IMR0_TOK3		RW	0x0
17	IMR0_TOK2		RW	0x0
16	IMR0_TOK1		RO	0x0
15:6	RESERVED			
5	IMR0_ROK6		RW	0x0
4	IMR0_ROK5		RW	0x0
3	IMR0_ROK4		RW	0x0
2	IMR0_ROK3		RW	0x0
1	IMR0_ROK2		RW	0x0

Bits	Field	Description	Type	Default
0	IMR0_ROK1		RO	0x0

## NIC\_IMR1\_CFG

REGISTER ADDRESS : 0xBB710044

DEFAULT VALUE : 0x0

IMR1 configuration

Bits	Field	Description	Type	Default
31:29	RESERVED			
28	IMR1_TDU5		RW	0x0
27	IMR1_TDU4		RW	0x0
26	IMR1_TDU3		RW	0x0
25	IMR1_TDU2		RW	0x0
24	IMR0_TDU1		RO	0x0
23:21	RESERVED			
20	IMR1_TOK5		RW	0x0
19	IMR1_TOK4		RW	0x0
18	IMR1_TOK3		RW	0x0
17	IMR1_TOK2		RW	0x0
16	IMR1_TOK1		RO	0x0
15:14	RESERVED			
13	IMR1_RDU6		RW	0x0
12	IMR1_RDU5		RW	0x0
11	IMR1_RDU4		RW	0x0
10	IMR1_RDU3		RW	0x0
9	IMR1_RDU2		RW	0x0
8	IMR1_RDU1		RO	0x0
7:6	RESERVED			
5	IMR1_ROK6		RW	0x0
4	IMR1_ROK5		RW	0x0
3	IMR1_ROK4		RW	0x0
2	IMR1_ROK3		RW	0x0
1	IMR1_ROK2		RW	0x0
0	IMR1_ROK1		RO	0x0

## NIC\_ISR1\_CFG

REGISTER ADDRESS : 0xBB710048

DEFAULT VALUE : 0x0

## ISR1 configuration

Bits	Field	Description	Type	Default
31:29	RESERVED			
28	ISR1_TDU5		RW1C	0x0
27	ISR1_TDU4		RW1C	0x0
26	ISR1_TDU3		RW1C	0x0
25	ISR1_TDU2		RW1C	0x0
24	ISR1_TDU1		RO	0x0
23:21	RESERVED			
20	ISR1_TOK5		RW1C	0x0
19	ISR1_TOK4		RW1C	0x0
18	ISR1_TOK3		RW1C	0x0
17	ISR1_TOK2		RW1C	0x0
16	ISR1_TOK1		RO	0x0
15:6	RESERVED			
5	ISR1_ROK6		RW1C	0x0
4	ISR1_ROK5		RW1C	0x0
3	ISR1_ROK4		RW1C	0x0
2	ISR1_ROK3		RW1C	0x0
1	ISR1_ROK2		RW1C	0x0
0	ISR1_ROK1		RO	0x0

**NIC\_INT\_ROUTE**

REGISTER ADDRESS : 0xBB71004C

DEFAULT VALUE : 0x0

## Interrupt routing configuration

Bits	Field	Description	Type	Default
31:25	RESERVED			
24	TR5_INT_ROUTING	0: routing tx ring5 relative interrupt to int_gmac 1: routing tx ring5 relative interrupt to int1_gmac	RW	0x0
23	RESERVED			
22	TR4_INT_ROUTING	0: routing tx ring4 relative interrupt to int_gmac 1: routing tx ring4 relative interrupt to int1_gmac	RW	0x0
21	RESERVED			
20	TR3_INT_ROUTING	0: routing tx ring3 relative interrupt to int_gmac 1: routing tx ring3 relative interrupt to int1_gmac	RW	0x0
19	RESERVED			
18	TR2_INT_ROUTING	0: routing tx ring2 relative interrupt to int_gmac 1: routing tx ring2 relative interrupt to int1_gmac	RW	0x0
17	RESERVED			

Bits	Field	Description	Type	Default
16	TR1_INT_ROUTING	0: routing tx ring1 relative interrupt to int_gmac 1: routing tx ring1 relative interrupt to int1_gmac	RW	0x0
15:11	RESERVED			
10	RR6_INT_ROUTING	0: routing rx ring6 relative interrupt to int_gmac 1: routing rx ring6 relative interrupt to int1_gmac	RW	0x0
9	RESERVED			
8	RR5_INT_ROUTING	0: routing rx ring5 relative interrupt to int_gmac 1: routing rx ring5 relative interrupt to int1_gmac	RW	0x0
7	RESERVED			
6	RR4_INT_ROUTING	0: routing rx ring4 relative interrupt to int_gmac 1: routing rx ring4 relative interrupt to int1_gmac	RW	0x0
5	RESERVED			
4	RR3_INT_ROUTING	0: routing rx ring3 relative interrupt to int_gmac 1: routing rx ring3 relative interrupt to int1_gmac	RW	0x0
3	RESERVED			
2	RR2_INT_ROUTING	0: routing rx ring2 relative interrupt to int_gmac 1: routing rx ring2 relative interrupt to int1_gmac	RW	0x0
1	RESERVED			
0	RR1_INT_ROUTING	0: routing rx ring1 relative interrupt to int_gmac 1: routing rx ring1 relative interrupt to int1_gmac	RW	0x0

## NIC\_TC

REGISTER ADDRESS : 0xBB710050

DEFAULT VALUE : 0x0

Transmit Configuration Register

Bits	Field	Description	Type	Default
31:13	RESERVED			
12:10	IFG2_0	InterFrameGap Time: This field allows the user to adjust the interframe gap time longer than the standard: 9.6 us for 10Mbps, 960 ns for 100Mbps. The time can be programmed from 9.6 us to 14.4 us (10Mbps) and 960ns to 1440ns (100Mbps).	RW	0x0

Bits	Field	Description	Type	Default
9:8	LBK1_0	Loopback test. There will be no packet on the TX+/- lines under the Loopback test condition. The loopback function must be independent of the link state. 00 : normal operation 01 : Loopback mode_R2T(lbkmode_r2t) : Lbk methld: no SW requirement. 1. receive ingress data. 2. assign rxd to txd (txd). 3. egress pkt. 10 : Reserved 11 : Loopback mode(lbk_mode). Lbk method: 1. rx fet descriptor. 2. tx fet descriptor and data 3. put data in txfifo 4. assign txd to rxd.(lbk) 5. gmac mv data to lxb.	RW	0x0
7:0	RESERVED			

## NIC\_RC

REGISTER ADDRESS : 0xBB710054

DEFAULT VALUE : 0x0

Receive Configuration Register

Bits	Field	Description	Type	Default
31:8	RESERVED			
7	HOME_PNA	HomePNA mode: When set to 1, will use crs pin doing tx deferring	RW	0x0
6	AFLOW	Accept flow control : When set to 1, flow control packet will also be received & DMA to rx buffer for debug. Default is 0	RW	0x0
5	AER	Accept Error Packet: When set to 1, all packets with CRC error, alignment error, and/or collided fragments will be accepted. When set to 0, all packets with CRC error, alignment error, and/or collided fragments will be rejected	RW	0x0
4	AR	Accept Runt: This bit allows the receiver to accept packets that are smaller than 64 bytes. The packet must be at least 8 bytes long to be accepted as a runt. Set to 1 to accept runt packets	RW	0x0
3	AB	Set to 1 to accept broadcast packets, 0 to reject.	RW	0x0
2	AM	Set to 1 to accept multicast packets, 0 to reject.	RW	0x0
1	APM	Set to 1 to accept physical match packets, 0 to reject.	RW	0x0
0	AAP	Set to 1 to accept all packets with physical destination address, 0 to reject	RW	0x0

## NIC\_CPUTAG

REGISTER ADDRESS : 0xBB710058

DEFAULT VALUE : 0x0

### CPU tag Configuration Register

Bits	Field	Description	Type	Default
31	CTEN_RX	Enable parsing ingress packet with cputag format.	RW	0x0
30:27	CT_TSIZE	Cputag size in egress pkt. CTT_size: 4h0: 0 Byte 4h1: 4 Byte 4h2: 8Byte 4h3: 10Byte	RW	0x0
26:25	CT_RSIZE_3_2	After r18681 (including), this field is only for ingress pkt. CTR_size: 4h0: 0 Byte 4h1: 4 Byte 4h2: 8Byte For Apollo cputag with PTP timestamp, set CT_RSIZE to 4h2	RW	0x0
24	CT_DSLRN	In rtl8370s, Setting of Disable Learning field in tx cputag. Setting of Disable Learning field in RTL8368 or DSLRN field in RTL8307h tx cputag when short_dsc_format = 0.	RW	0x0
23	CT_NORMK	Setting of NORMK field in RTL8307h tx cputag when short_dsc_format = 0	RW	0x0
22	CT_ASPRI	In RTL8307h, setting ASPRI field in tx cputag when short_dsc_format = 0. In RTL8370S, setting priority select field in tx cputag when short_dsc_format = 0	RW	0x0
21:18	CT_SWITCH	Support cputag format of switch 0: no cputag support 1: 8368 2: 8306 3: 8307 4: 8370 5: gmac in 8681. 6: gmac in Apollo	RW	0x0
17:16	CT_RSIZE_1_0		RW	0x0
15:8	CTPM	CPU tag protocol mask. 8306:0xf0 8368:0xe0 8370:0xff 8307h:0xff	RW	0x0
7:0	CTPV	CPU tag protocol value. 8306:0x90 8368:0xa0 or 0xb0 8370:0x04 8307h:0x04	RW	0x0



## NIC\_CONFIG

REGISTER ADDRESS : 0xBB71005C

DEFAULT VALUE : 0x20000000

CONFIGURATION Register

Bits	Field	Description	Type	Default
31	EN_INT_ROUTE	0: disable interrupt route, IMR0_reg, IMR1_reg 1: enable interrupt route, IMR0_reg, IMR1_reg	RW	0x0
30	EN_INT_SPLIT	When EN_INT_ROUTE = 0, 0: only init.tdu, tok, rok present 1: IMR0_reg, IMR1_reg and ISR1_reg present.  When EN_INT_ROUTE = 1 this field is 1	RW	0x0
29:28	RFF_SIZE_SEL	Set gmac_rxfifo size. 2b00: 1KB 2b01: 1664B 2b10: 2KB	RW	0x2
27	TSO_ID_SEL	Uses to choose LSO(TCP) IP.identification value 0: keep. 1: incremental.	RW	0x0
26:0	RESERVED			

## NIC\_CPUTAG1

REGISTER ADDRESS : 0xBB710060

DEFAULT VALUE : 0x0

CPUTAG1 Register

Bits	Field	Description	Type	Default
31:7	RESERVED			
6:4	SPA_DSL	The ingress cputag.SPA=DSL field. Used in Apollo cputag.	RW	0x0
3	RESERVED			
2:0	SPA_PON	The ingress cputag.SPA=PON field. Used in Apollo cputag.	RW	0x0

## NIC\_MS

REGISTER ADDRESS : 0xBB710068

DEFAULT VALUE : 0x0

Media Status Register

Bits	Field	Description	Type	Default
31	FORCE_TRXFCE	Force Tx/RX Flow Control: 1 = enabled Flow control in the absence of NWAY. 0 = disables Flow control in the absence of NWAY. Version effect: rl6166(ECO) and after.	RW	0x0
30	RXFCE	RX Flow control Enable: The flow control is enabled in full-duplex mode only. Packets are dropped if buffer is exhausted. Default is 0. 1 = Rx Flow Control Enabled. 0 = Rx Flow Control Disabled	RW	0x0
29	TXFCE	Tx Flow Control Enable: 1 = tx flow control enabled. 0 = tx flow control disabled. ACCEPT ERROR MUST NOT BE ENABLED	RW	0x0
28	SPEED_1000	{SPEED_1000, SPEED_10} 10: 1000Mbps, 11: not allowed	RO	0x0
27	SPEED_10	{SPEED_1000, SPEED_10} 00: 100Mbps, 01: 10Mbps	RO	0x0
26	LINKB	Inverse of Link status. 0 = Link OK. 1 = Link Fail	RO	0x0
25	TXPF	Tx Pause frame: 1 = Ethernet module has sent a pause packet. 0 = the Ethernet module has sent a timer done packet	RO	0x0
24	RXPF	Pause Flag: 1 = Ethernet module is in backoff state because a pause packet received. 0 = pause state is clear	RO	0x0
23	SEL_RGMII	gmac_sel_rgmii	RO	0x0
22	FULLDUPREG	Indicates Full duplex mode in gmac	RO	0x0
21	NWCOMPLETE	Nway complete	RO	0x0
20	SEL_MII	indicates in mii mode	RO	0x0
19	FORCEDFULLDUP	force gmac operates at full duplex mode. 1b1: force gmac in full duplex mode. 1b0: duplex status is from MDIO auto-polling. Not means gmac is in half duplex mode.	RW	0x0
18	FORCELINK	force gmac in link ok mode. This bit is Write only in RLE0315. This bit is R/W in RLE0390 (RL6166). 1b1: force gmac in linkok. 1b0: link status is from MDIO auto-polling	RW	0x0
17:16	FORCE_SPD	Force gmac in 10/100/GIGA mode. 2b00: 100M 2b01: 10M 2b10: GIGA 2b11: not force mode. These bits are Write only in RLE0390 (RL6166). The current speed status of gmac can be checked in MSR_reg.{speed1000, speed_10}. In force mode, SW can set gmac operates in 100M, FD and Link ok(for example) and SW can not set gmac operates in 100M, HD and Link ok. When FORCEDFULLDUP is 1b0, the duplex status is from MDIO auto-polling, therefore, it is not controlled by SW.	RW	0x0
15	SEL_PHYIF_0	1: phy interface 0.works. 0: phy interface 1 works	RO	0x0

Bits	Field	Description	Type	Default
14	RESERVED			
13	PHY_MODE	1: in phy mode. 0: not in phy mode	RO	0x0
12	RGMII_RX_STS	0: Does not support rgmii in band status(link status, speed and duplex mode of the PHY) by decoding rxd. 1: Supports rgmii in band status(link status, speed and duplex mode of the PHY) by decoding rxd.	RW	0x0
11	RGMII_TX_STS	This field is valid only in phy mode. 0: Does not support rgmii in band status(link status, speed and duplex mode of the PHY) by encoding txd. 1: Supports rgmii in band status(link status, speed and duplex mode of the PHY) by encoding txd.	RW	0x0
10	FORCE_SPD_MODE	1: gmac is in force speed mode. The real speed in force mode is set in MS_REG.FORCE_SPD. 0: gmac speed status is from md operation.	RW	0x0
9:0	RESERVED			

## NIC\_MIIA

REGISTER ADDRESS : 0xBB71006C

DEFAULT VALUE : 0x0

### MII Access Register

Bits	Field	Description	Type	Default
31	FLAG	Flag bit, used to identify access to MII register: 1: Write data to MII register. Turns to 0 automatically upon completion of MAC writing to the specified MII register. 0: Read data from MII register. Turns to 1 automatically upon completion of MAC reading the specified MII register. Read write turn around time is about 64 us.	RW	0x0
30:26	PHY_ADDR	Defines the Phy address for the MII	RW	0x0
25:23	RESERVED			
22	DIS_AUTO_POLLING	Disable auto polling feature of mdio operation. 0: HW auto polling PCS status. 1: HW does not auto polling PCS status	RW	0x0
21	POLLING_EEE	polling PCS EEE advertisement register (7.60). If driver wants to access another register in MMD register mapping table, MIIAR.polling_eee_reg should be disabled first. In rl6166(rl60315) and before: this bit is not supported. In rl60390: In in-direct method, gmac had to access PCS register by multiples R/W of reg13 and 14. It is OK for PCS to be aborted in the middle of indirect method. In rl60371: HW will complete current indirect access to PCS then stop in-direct method	RW	0x0

Bits	Field	Description	Type	Default
20:16	REG_ADDR_4_0	Defines 5-bit MII register address	RW	0x0
15:0	DATA_15_0	Defines 16 bit MII register data	RW	0x0

## NIC\_SWINT

REGISTER ADDRESS : 0xBB710070

DEFAULT VALUE : 0x0

software interrupt Register

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	SWINT	Write 1 will force ISR register bit 10 set to 1	RW	0x0

## NIC\_VLAN

REGISTER ADDRESS : 0xBB710074

DEFAULT VALUE : 0x0

VLAN Register

Bits	Field	Description	Type	Default
31:16	STAG_PID	Set the s-tag protocol identifier. This field is valid only when COM_REG.TDSC_VLAN_TYPE is high	RW	0x0
15	TDSC_VLAN_TYPE	1: tx command descriptor.tx_vlan_action is for s-tag. 0: tx command descriptor.tx_vlan_action is for c-tag.	RW	0x0
14:0	RESERVED			

## NIC\_LED\_CR

REGISTER ADDRESS : 0xBB710080

DEFAULT VALUE : 0x0

led control Register

Bits	Field	Description	Type	Default
31:20	RESERVED			
19	EEE_EN_LED	Enable/disable lpi led.	RW	0x0

Bits	Field	Description	Type	Default
18	CUSTOM_LED	Custom led mode.	RW	0x0
17:16	LED_SEL	Non custom led select. Following EEE spec, combine the Link signal and LPI signal in the same LED pin. While entering LPI state, LED will blink with 2000ms cycle, of which the first 1670ms LED light is turned off, after 334ms is turned on	RW	0x0
15:12	LED_SEL3	Custom led3 select	RW	0x0
11:8	LED_SEL2	Custom led2 select	RW	0x0
7:4	LED_SEL1	Custom led1 select	RW	0x0
3:0	LED_SEL0	Custom led0 select	RW	0x0

## NIC\_TXFDP1

REGISTER ADDRESS : 0xBB720000

DEFAULT VALUE : 0x0

TxFDP1 register

Bits	Field	Description	Type	Default
31:0	TXFDP1	Tx First Descriptor Pointer (FDP) for 1st priority queue	RW	0x0

## NIC\_TXCDO1

REGISTER ADDRESS : 0xBB720004

DEFAULT VALUE : 0x0

TxCDO1 register

Bits	Field	Description	Type	Default
31:12	RESERVED			
11:0	TXCDO1	Tx 1st priority Current Descriptor Offset: FDP+CDO = current descriptor pointer. CDO increments by 16 bytes each time	RO	0x0

## NIC\_TXFDP2

REGISTER ADDRESS : 0xBB720010

DEFAULT VALUE : 0x0

TxFDP2 register

Bits	Field	Description	Type	Default
31:0	TXFDP2	Tx 2nd priority Descriptor Pointer to the Tx Ring	RW	0x0

## NIC\_TXCDO2

REGISTER ADDRESS : 0xBB720014

DEFAULT VALUE : 0x0

TxCDO2 register

Bits	Field	Description	Type	Default
31:12	RESERVED			
11:0	TXCDO2	Tx 2nd priority Current Descriptor Offset: FDP+CDO = current descriptor pointer. CDO increments by 16 bytes each time.	RO	0x0

## NIC\_TXFDP3

REGISTER ADDRESS : 0xBB720020

DEFAULT VALUE : 0x0

TxFDP3 register

Bits	Field	Description	Type	Default
31:0	TXFDP3	Tx 3rd priority Descriptor Pointer to the Tx Ring	RW	0x0

## NIC\_TXCDO3

REGISTER ADDRESS : 0xBB720024

DEFAULT VALUE : 0x0

TxCDO3 register

Bits	Field	Description	Type	Default
31:12	RESERVED			
11:0	TXCDO3	Tx 3rd priority Current Descriptor Offset: FDP+CDO = current descriptor pointer. CDO increments by 16 bytes each time	RO	0x0

**NIC\_TXFDP4**

REGISTER ADDRESS : 0xBB720030

DEFAULT VALUE : 0x0

TxFDP4 register

Bits	Field	Description	Type	Default
31:0	TXFDP4	Tx 4th priority Descriptor Pointer to the Tx Ring	RW	0x0

**NIC\_TXCDO4**

REGISTER ADDRESS : 0xBB720034

DEFAULT VALUE : 0x0

TxCDO4 register

Bits	Field	Description	Type	Default
31:12	RESERVED			
11:0	TXCDO4	Tx 4th priority Current Descriptor Offset: FDP+CDO = current descriptor pointer. CDO increments by 16 bytes each time	RO	0x0

**NIC\_TXFDP5**

REGISTER ADDRESS : 0xBB720040

DEFAULT VALUE : 0x0

TxFDP5 register

Bits	Field	Description	Type	Default
31:0	TXFDP5	Tx 5th priority Descriptor Pointer to the Tx Ring	RW	0x0

**NIC\_TXCDO5**

REGISTER ADDRESS : 0xBB720044

DEFAULT VALUE : 0x0

TxCDO5 register

Bits	Field	Description	Type	Default
31:12	RESERVED			
11:0	TXCDO5	Tx 5th priority Current Descriptor Offset: FDP+CDO = current descriptor pointer. CDO increments by 16 bytes each time	RO	0x0

## NIC\_RRING\_ROUTING1

REGISTER ADDRESS : 0xBB720070

DEFAULT VALUE : 0x0

RRING\_ROUNDING1 register

Bits	Field	Description	Type	Default
31	RESERVED			
30:28	PRI_7_ROUTE	Cputag.priority = 7 rout select.	RW	0x0
27	RESERVED			
26:24	PRI_6_ROUTE	Cputag.priority = 6 rout select.	RW	0x0
23	RESERVED			
22:20	PRI_5_ROUTE	Cputag.priority = 5 rout select.	RW	0x0
19	RESERVED			
18:16	PRI_4_ROUTE	Cputag.priority = 4 rout select.	RW	0x0
15	RESERVED			
14:12	PRI_3_ROUTE	Cputag.priority = 3 rout select.	RW	0x0
11	RESERVED			
10:8	PRI_2_ROUTE	Cputag.priority = 2 rout select.	RW	0x0
7	RESERVED			
6:4	PRI_1_ROUTE	Cputag.priority = 1 rout select.	RW	0x0
3	RESERVED			
2:0	PRI_0_ROUTE	Cputag.priority = 0 rout select.	RW	0x0

## NIC\_RRING\_ROUTING2

REGISTER ADDRESS : 0xBB720074

DEFAULT VALUE : 0x0

RRING\_ROUNDING2 register

Bits	Field	Description	Type	Default
31	RESERVED			
30:28	PRI_7_ROUTE	Cputag.priority = 7 rout select.	RW	0x0
27	RESERVED			



Bits	Field	Description	Type	Default
26:24	PRI_6_ROUTE	Cputag.priority = 6 rout select.	RW	0x0
23	RESERVED			
22:20	PRI_5_ROUTE	Cputag.priority = 5 rout select.	RW	0x0
19	RESERVED			
18:16	PRI_4_ROUTE	Cputag.priority = 4 rout select.	RW	0x0
15	RESERVED			
14:12	PRI_3_ROUTE	Cputag.priority = 3 rout select.	RW	0x0
11	RESERVED			
10:8	PRI_2_ROUTE	Cputag.priority = 2 rout select.	RW	0x0
7	RESERVED			
6:4	PRI_1_ROUTE	Cputag.priority = 1 rout select.	RW	0x0
3	RESERVED			
2:0	PRI_0_ROUTE	Cputag.priority = 0 rout select.	RW	0x0

### NIC\_RRING\_ROUTING3

REGISTER ADDRESS : 0xBB720078

DEFAULT VALUE : 0x0

RRING\_ROUTING3 register

Bits	Field	Description	Type	Default
31	RESERVED			
30:28	PRI_7_ROUTE	Cputag.priority = 7 rout select.	RW	0x0
27	RESERVED			
26:24	PRI_6_ROUTE	Cputag.priority = 6 rout select.	RW	0x0
23	RESERVED			
22:20	PRI_5_ROUTE	Cputag.priority = 5 rout select.	RW	0x0
19	RESERVED			
18:16	PRI_4_ROUTE	Cputag.priority = 4 rout select.	RW	0x0
15	RESERVED			
14:12	PRI_3_ROUTE	Cputag.priority = 3 rout select.	RW	0x0
11	RESERVED			
10:8	PRI_2_ROUTE	Cputag.priority = 2 rout select.	RW	0x0
7	RESERVED			
6:4	PRI_1_ROUTE	Cputag.priority = 1 rout select.	RW	0x0
3	RESERVED			
2:0	PRI_0_ROUTE	Cputag.priority = 0 rout select.	RW	0x0

## NIC\_RRING\_ROUTING4

REGISTER ADDRESS : 0xBB72007C

DEFAULT VALUE : 0x0

RRING\_ROUNDING4 register

Bits	Field	Description	Type	Default
31	RESERVED			
30:28	PRI_7_ROUTE	Cputag.priority = 7 rout select.	RW	0x0
27	RESERVED			
26:24	PRI_6_ROUTE	Cputag.priority = 6 rout select.	RW	0x0
23	RESERVED			
22:20	PRI_5_ROUTE	Cputag.priority = 5 rout select.	RW	0x0
19	RESERVED			
18:16	PRI_4_ROUTE	Cputag.priority = 4 rout select.	RW	0x0
15	RESERVED			
14:12	PRI_3_ROUTE	Cputag.priority = 3 rout select.	RW	0x0
11	RESERVED			
10:8	PRI_2_ROUTE	Cputag.priority = 2 rout select.	RW	0x0
7	RESERVED			
6:4	PRI_1_ROUTE	Cputag.priority = 1 rout select.	RW	0x0
3	RESERVED			
2:0	PRI_0_ROUTE	Cputag.priority = 0 rout select.	RW	0x0

## NIC\_RRING\_ROUTING5

REGISTER ADDRESS : 0xBB720080

DEFAULT VALUE : 0x0

RRING\_ROUNDING5 register

Bits	Field	Description	Type	Default
31	RESERVED			
30:28	PRI_7_ROUTE	Cputag.priority = 7 rout select.	RW	0x0
27	RESERVED			
26:24	PRI_6_ROUTE	Cputag.priority = 6 rout select.	RW	0x0
23	RESERVED			
22:20	PRI_5_ROUTE	Cputag.priority = 5 rout select.	RW	0x0
19	RESERVED			
18:16	PRI_4_ROUTE	Cputag.priority = 4 rout select.	RW	0x0
15	RESERVED			
14:12	PRI_3_ROUTE	Cputag.priority = 3 rout select.	RW	0x0

Bits	Field	Description	Type	Default
11	RESERVED			
10:8	PRI_2_ROUTE	Cputag.priority = 2 rout select.	RW	0x0
7	RESERVED			
6:4	PRI_1_ROUTE	Cputag.priority = 1 rout select.	RW	0x0
3	RESERVED			
2:0	PRI_0_ROUTE	Cputag.priority = 0 rout select.	RW	0x0

## NIC\_RRING\_ROUTING6

REGISTER ADDRESS : 0xBB720084

DEFAULT VALUE : 0x0

RRING\_ROUTING6 register

Bits	Field	Description	Type	Default
31	RESERVED			
30:28	PRI_7_ROUTE	Cputag.priority = 7 rout select.	RW	0x0
27	RESERVED			
26:24	PRI_6_ROUTE	Cputag.priority = 6 rout select.	RW	0x0
23	RESERVED			
22:20	PRI_5_ROUTE	Cputag.priority = 5 rout select.	RW	0x0
19	RESERVED			
18:16	PRI_4_ROUTE	Cputag.priority = 4 rout select.	RW	0x0
15	RESERVED			
14:12	PRI_3_ROUTE	Cputag.priority = 3 rout select.	RW	0x0
11	RESERVED			
10:8	PRI_2_ROUTE	Cputag.priority = 2 rout select.	RW	0x0
7	RESERVED			
6:4	PRI_1_ROUTE	Cputag.priority = 1 rout select.	RW	0x0
3	RESERVED			
2:0	PRI_0_ROUTE	Cputag.priority = 0 rout select.	RW	0x0

## NIC\_RXFDP2

REGISTER ADDRESS : 0xBB720090

DEFAULT VALUE : 0x0

RxFDP2 register

Bits	Field	Description	Type	Default
31:0	RXFDP	Rx #2 queue Descriptor Pointer to the Rx Ring	RW	0x0

## NIC\_RXCDORINGRS2

REGISTER ADDRESS : 0xBB720094

DEFAULT VALUE : 0x0

RxCDO2 register and Rx Ring Size 2

Bits	Field	Description	Type	Default
31:28	RESERVED			
27:16	RXRINGSIZE	The total number of descriptors in the Rx descriptor rings of #2 queue. Act as bit mask, eg. RxRingSize {11:0}: 0000_0000_1111: 16 descriptors 0000_0001_1111: 32 descriptors 0000_0011_1111: 64 descriptors 0000_0111_1111: 128 descriptors 0000_1111_1111: 256 descriptors 0001_1111_1111: 512 descriptors 0011_1111_1111: 1024 descriptors 0111_1111_1111: 2048 descriptors 1111_1111_1111: 4096 descriptors Any other value in this register yields undefined results	RW	0x0
15:12	RESERVED			
11:0	RXCDO	Rx Current Descriptor Offset of #2 queue: Rx FDP + Rx CDO = current descriptor pointer. CDO increments by 16 each time (each increment is one byte)	RO	0x0

## NIC\_RX\_CPU\_DESN2

REGISTER ADDRESS : 0xBB720098

DEFAULT VALUE : 0x0

RX\_CPU\_DESN2 register

Bits	Field	Description	Type	Default
31:12	RESERVED			
11:0	CPU_DES_NUM	Indicate the number of descriptor of #2 queue, which has been finished Rx process and returned to IO by CPU. After ending Rx process, CPU needs to update this field.	RW	0x0

## NIC\_RX\_DES\_THRES2

REGISTER ADDRESS : 0xBB72009C

DEFAULT VALUE : 0x0

RX\_DES\_THRES2 register

Bits	Field	Description	Type	Default
31:28	RESERVED			
27:16	DES_ON_TH	Specifies the difference between EthrnetRx-CPU_Des_Num2 and the descriptor #2of #2 queue currently in use by Ethernet Module in which flow control will be assert	RW	0x0
15:12	RESERVED			
11:0	DES_OFF_TH	Specifies the difference between EthrnetRx-CPU_Des_Num2 and the descriptor #2 of 2#2queue currently in use by Ethernet Module in which flow control will be de-assert	RW	0x0

## NIC\_RXFDP3

REGISTER ADDRESS : 0xBB7200A0

DEFAULT VALUE : 0x0

RxFDP3 register

Bits	Field	Description	Type	Default
31:0	RXFDP	Rx # 3 queue Descriptor Pointer to the Rx Ring	RW	0x0

## NIC\_RXCDORINGRS3

REGISTER ADDRESS : 0xBB7200A4

DEFAULT VALUE : 0x0

RxCDO3 register and Rx Ring Size 3

Bits	Field	Description	Type	Default
31:28	RESERVED			
27:16	RXRINGSIZE	The total number of descriptors in the Rx descriptor rings of #3 queue.	RW	0x0
15:12	RESERVED			
11:0	RXCDO	Rx Current Descriptor Offset of #3 queue: Rx FDP+Rx CDO = current descriptor pointer. CDO increments by 16 each time (each increment is one byte)	RO	0x0

## NIC\_RX\_CPU\_DESN3

REGISTER ADDRESS : 0xBB7200A8

DEFAULT VALUE : 0x0

RX\_CPU\_DESN3 register

Bits	Field	Description	Type	Default
31:12	RESERVED			
11:0	CPU_DES_NO	Indicate the number of descriptor of #3 queue, which has been finished Rx process and returned to IO by CPU. After ending Rx process, CPU needs to update this field.	RW	0x0

## NIC\_RX\_DES\_THRES3

REGISTER ADDRESS : 0xBB7200AC

DEFAULT VALUE : 0x0

RX\_DES\_THRES3 register

Bits	Field	Description	Type	Default
31:28	RESERVED			
27:16	DES_ON_TH	Specifies the difference between EthrnetRx-CPU_Des_Num3 and the descriptor #3 of #3 queue currently in use by Ethernet Module in which flow control will be assert	RW	0x0
15:12	RESERVED			
11:0	DES_OFF_TH	Specifies the difference between EthrnetRx-CPU_Des_Num3 and the descriptor #3of #3 queue currently in use by Ethernet Module in which flow control will be de-assert	RW	0x0

## NIC\_RXFDP4

REGISTER ADDRESS : 0xBB7200B0

DEFAULT VALUE : 0x0

RxFDP4 register

Bits	Field	Description	Type	Default
31:0	RXFDP4	Rx 4 queue Descriptor Pointer to the Rx Ring	RW	0x0

## NIC\_RXCDORINGRS4

REGISTER ADDRESS : 0xBB7200B4

DEFAULT VALUE : 0x0

RxCDO4 register and Rx Ring Size 4

Bits	Field	Description	Type	Default
31:28	RESERVED			
27:16	RXRINGSIZE	The total number of descriptors in the Rx descriptor rings of #4 queue.	RW	0x0
15:12	RESERVED			
11:0	RXCDO	Rx Current Descriptor Offset of #4 queue: Rx FDP+Rx CDO = current descriptor pointer. CDO increments by 16 each time (each increment is one byte)	RO	0x0

## NIC\_RX\_CPU\_DESN4

REGISTER ADDRESS : 0xBB7200B8

DEFAULT VALUE : 0x0

RX\_CPU\_DESN4 register

Bits	Field	Description	Type	Default
31:12	RESERVED			
11:0	CPU_DES_NO	Indicate the number of descriptor of #4 queue, which has been finished Rx process and returned to IO by CPU. After ending Rx process, CPU needs to update this field.	RW	0x0

## NIC\_RX\_DES\_THRES4

REGISTER ADDRESS : 0xBB7200BC

DEFAULT VALUE : 0x0

RX\_DES\_THRES4 register

Bits	Field	Description	Type	Default
31:28	RESERVED			
27:16	DES_ON_TH	Specifies the difference between EthernetRx-CPU_Des_Num4 and the descriptor #4 of #4 queue currently in use by Ethernet Module in which flow control will be assert	RW	0x0
15:12	RESERVED			

Bits	Field	Description	Type	Default
11:0	DES_OFF_TH	Specifies the difference between EthrnetRx-CPU_Des_Num4 and the descriptor #4of #4 queue currently in use by Ethernet Module in which flow control will be de-assert	RW	0x0

## NIC\_RXFDP5

REGISTER ADDRESS : 0xBB7200C0

DEFAULT VALUE : 0x0

RxFDP5 register

Bits	Field	Description	Type	Default
31:0	RXFDP5	Rx 5 queue Descriptor Pointer to the Rx Ring	RW	0x0

## NIC\_RXCDORINGRS5

REGISTER ADDRESS : 0xBB7200C4

DEFAULT VALUE : 0x0

RxCDO5 register and Rx Ring Size 5

Bits	Field	Description	Type	Default
31:28	RESERVED			
27:16	RXRINGSIZE	The total number of descriptors in the Rx descriptor rings of #5 queue.	RW	0x0
15:12	RESERVED			
11:0	RXCDO	Rx Current Descriptor Offset of #5 queue: RxFDP+RxCDO = current descriptor pointer. CDO increments by 16 each time (each increment is one byte)	RO	0x0

## NIC\_RX\_CPU\_DESN5

REGISTER ADDRESS : 0xBB7200C8

DEFAULT VALUE : 0x0

RX\_CPU\_DESN5 register

Bits	Field	Description	Type	Default
31:12	RESERVED			



Bits	Field	Description	Type	Default
11:0	CPU_DES_NO	Indicate the number of descriptor of #5 queue, which has been finished Rx process and returned to IO by CPU. After ending Rx process, CPU needs to update this field.	RW	0x0

## NIC\_RX\_DES\_THRES5

REGISTER ADDRESS : 0xBB7200CC

DEFAULT VALUE : 0x0

RX\_DES\_THRES5 register

Bits	Field	Description	Type	Default
31:28	RESERVED			
27:16	DES_ON_TH	Specifies the difference between EthrnetRx-CPU_Des_Num5 and the descriptor #5 of #5 queue currently in use by Ethernet Module in which flow control will be assert	RW	0x0
15:12	RESERVED			
11:0	DES_OFF_TH	Specifies the difference between EthrnetRx-CPU_Des_Num5 and the descriptor #5 of #5 queue currently in use by Ethernet Module in which flow control will be de-assert	RW	0x0

## NIC\_RXFDP6

REGISTER ADDRESS : 0xBB7200D0

DEFAULT VALUE : 0x0

RxFDP6 register

Bits	Field	Description	Type	Default
31:0	RXFDP6	Rx 6 queue Descriptor Pointer to the Rx Ring	RW	0x0

## NIC\_RXCDORINGRS6

REGISTER ADDRESS : 0xBB7200D4

DEFAULT VALUE : 0x0

RxCDO6 register and Rx Ring Size 6

Bits	Field	Description	Type	Default
31:28	RESERVED			
27:16	RXRINGSIZE	The total number of descriptors in the Rx descriptor rings of #6 queue.	RW	0x0
15:12	RESERVED			
11:0	RXCDO	Rx Current Descriptor Offset of #6 queue: $RxFDP + RxCDO$ = current descriptor pointer. CDO increments by 16 each time (each increment is one byte)	RO	0x0

## NIC\_RX\_CPU\_DESN6

REGISTER ADDRESS : 0xBB7200D8

DEFAULT VALUE : 0x0

RX\_CPU\_DESN6 register

Bits	Field	Description	Type	Default
31:12	RESERVED			
11:0	CPU_DES_NO	Indicate the number of descriptor of #6 queue, which has been finished Rx process and returned to IO by CPU. After ending Rx process, CPU needs to update this field.	RW	0x0

## NIC\_RX\_DES\_THRES6

REGISTER ADDRESS : 0xBB7200DC

DEFAULT VALUE : 0x0

RX\_DES\_THRES6 register

Bits	Field	Description	Type	Default
31:28	RESERVED			
27:16	DES_ON_TH	Specifies the difference between EthernetRx-CPU_Des_Num6 and the descriptor #6 of #6 queue currently in use by Ethernet Module in which flow control will be assert	RW	0x0
15:12	RESERVED			
11:0	DES_OFF_TH	Specifies the difference between EthernetRx-CPU_Des_Num6 and the descriptor #6 of #6 queue currently in use by Ethernet Module in which flow control will be de-assert	RW	0x0

## NIC\_RXFDP1

REGISTER ADDRESS : 0xBB7200F0

DEFAULT VALUE : 0x0

RxFDP1 register

Bits	Field	Description	Type	Default
31:0	RXFDP1	Rx 1st queue Descriptor Pointer to the Rx Ring	RW	0x0

## NIC\_RXCDORINGRS1

REGISTER ADDRESS : 0xBB7200F4

DEFAULT VALUE : 0x0

RxCDO1 register and Rx Ring Size 1

Bits	Field	Description	Type	Default
31:28	RESERVED			
27:16	RXRINGSIZE	This is the total number of descriptors in the Rx descriptor rings of 1st queue	RW	0x0
15:12	RESERVED			
11:0	RXCDO	Rx Current Descriptor Offset of 1st queue: Rx FDP+Rx CDO = current descriptor pointer. CDO increments by 16 each time (each increment is one byte).	RO	0x0

## NIC\_SMSA

REGISTER ADDRESS : 0xBB7200FC

DEFAULT VALUE : 0x0

SMSA register

Bits	Field	Description	Type	Default
31:0	SMSA	SRAM mapping start address for header mapping to sram	RW	0x0

## NIC\_PROBE\_SELECT

REGISTER ADDRESS : 0xBB720100

DEFAULT VALUE : 0x0

RxCDO1 register and Rx Ring Size 1

Bits	Field	Description	Type	Default
31:26	RESERVED			
25:24	PROB_SEL	This MAC IP will have 16 probe signal output for debug. These 2 bit choose between 4 sets of internal signal being probed. 000 - { wintf, bt, tx, nojamtx, tok, jam, col, underjam, txabt, tfetdma, tdesdma, tclodma, tfetact, masrdact, tcloact, tfifofull } 001 - { entfctrl, enrftctrl, entfp0en, entfp0, entfp1, tflowp0, tflowp1, txpf, wintf, bt, tx, nojamtx, tok, jam, col, underjam } 010 - { rstag1, rstag2, rok1, rfail, rxdv, receive, rxd (3:0), enflowpkt, rfetact, maswract, rclact, rfifofull, rbufffull } 011 - { 1b0, rxdp(7:0), pincol, fulldup, mdc, md, enmdo_n, mdo, linkok } 100 - { gmii_rxdvp, gmii_rxdp(3:0), gmii_txenp, gmii_txdp(3:0), dbg_txc_out, dbg_sram_rxc, dbg_sram_txc, dbg_txc_in, dbg_rxc_in, 1b0 } 101 - { 1b0, tsh(1:0), en_early_tx, dbg_extend_lsmrend, pgtxcom, txunder, dbg_tfp44q(8:0) } 110 - { dbg_txrdoe, dbg_entldcnt, dbg_tldcnt(1:0), dbg_realtbcqeq0, dbg_tfw(8:0) }	RW	0x0
23:9	RESERVED			

## NIC\_DIAGNOSE1

REGISTER ADDRESS : 0xBB720104

DEFAULT VALUE : 0x0

DIAGNOSE1 register

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:3	RXMRING		RO	0x0
2:0	LSO_STS		RO	0x0

## NIC\_RX\_PSE1\_TXC\_OUT\_SEL1

REGISTER ADDRESS : 0xBB72012C

DEFAULT VALUE : 0x0

Rx\_Pse\_Des\_Thres\_1\_h and TXC\_OUT\_PH\_SEL\_1

Bits	Field	Description	Type	Default
31:30	RESERVED			
29	SET_D_TXC	Add delay to gmii_txc_out. Used in clk250M. Rgmii_1000: add 2nS delay. Rgmii_100: add 4nS delay. Rgmii_10: add 4nS delay.	RW	0x0

Bits	Field	Description	Type	Default
28:24	TXC_OUT_PH_SEL	32-tap delay chain for txc_out. Used in clk125M mode.	RW	0x0
23:4	RESERVED			
3:0	RX_TH_OFF_1	This is the Rx_Pse_Des_Thres_off1{11:8}.	RW	0x0

## NIC\_ETNRXCPU1

REGISTER ADDRESS : 0xBB720130

DEFAULT VALUE : 0x0

EhtrntRxCPU\_Des\_Num1

Bits	Field	Description	Type	Default
31:30	CPU_DES_NUM_7_0	Indicate the number of descriptor of 1st queue, which has been finished Rx process and returned to IO by CPU. After ending Rx process, CPU needs to update this field.	RW	0x0
29	DES_ON_TH_7_0	Specifies the difference between EthrntRx-CPU_Des_Num1 and the descriptor # of 1st queue currently in use by Ethernet Module in which flow control will be assert.	RW	0x0
28:24	DES_OFF_TH	Specifies the difference between EthrntRx-CPU_Des_Num1 and the descriptor # of 1st queue currently in use by Ethernet Module in which flow control will be de-assert.	RW	0x0

## NIC\_ETN\_IO\_CMD

REGISTER ADDRESS : 0xBB720134

DEFAULT VALUE : 0x0

Ethernet\_IO\_CMD

Bits	Field	Description	Type	Default
31	MAX_DMA_SEL_0	Select the dma burst size on bus(memory controller should assert continuous btrdy). 00:16 DW(1DW=4B) 01:32 DW 10:64 DW	RW	0x0
30	SHORT_DES_FMT	Short descriptor format. Set 1 tx/rx descriptor will use old format - 4x32bit each item, set 0 use new format to support sram mapping.	RW	0x0
29	MAX_DMA_SEL_1		RW	0x0
28	EN_EARLY_TX	0: disable, 1: enable. Disable early tx by GAMC while tx command descriptor.IPCS, UDPCS or TCPCS are set to high	RW	0x0

Bits	Field	Description	Type	Default
27:24	TX_PKT_TMR	Timer to trigger TxOK interrupt after receipt of Tx-IntMitigation pkts. 0000 no timer set 0001 1111 : the timer interval defining a multiple of TU ex: 0011 = timer interval set to 3 x4 =12TU Once TxOK is asserted the timer mechanism is reinitialized	RW	0x0
23	TX_INT_MITIG_3		RW	0x0
22	RX_PKT_TMR_3		RW	0x0
21	RX_INT_MITIG_3		RW	0x0
20:19	TSH	Tx Threshold: Specifies the threshold level in the Tx FIFO to begin the transmission. When the byte count of the data in the Tx FIFO reaches this level, (or the FIFO contains at least one complete packet or the end of a packet) the Ethernet module will transmit this packet. 00:128B. 01:256B. 10:512B. 11:1024B.	RW	0x0
18:16	TX_INT_MITIG_2_0	This sets the number of packets received before TxOK interrupt is triggered. 0000- 1 pkt 0001- 4 pkts 0010- 8 pkts 0011- 12 pkts 0100- 16 pkts 0101- 20 pkts 0110- 24 pkts 0111- 28 pkts	RW	0x0
15:13	RX_PKT_TMR_2_0	Timer to trigger RxOK interrupt after receipt of RxIntMitigation pkts. 0000 no timer set 0001 1111 : the timer interval defining a multiple of TU ex: 011 = timer interval set to 3 x4 =12TU This only applies to packets of size larger than 128 bytes. Once RxOK is asserted the timer mechanism is reinitialized. For ingress pkt which is short than 128B, RxOK interrupt asserts after DMA completes.	RW	0x0
12:11	RXFTH	Rx Threshold: Specifies the threshold level in the Rx FIFO to begin the transmission. When the byte count of the data in the Rx FIFO reaches this level, (or the FIFO contains at least one complete packet or the end of a packet) the Ethernet module will transmit this packet. 00 256 bytes 10 64 bytes 11 128 bytes	RW	0x0

Bits	Field	Description	Type	Default
10:8	RX_INT_MITIG_2_0	This sets the number of packets received before RxOK interrupt is triggered. 0000- 1 pkt 0001- 4 pkts 0010- 8 pkts 0011- 12pkts 0100- 16 pkts 0101- 20 pkts 0110- 24 pkts 0111- 28 pkts	RW	0x0
7:6	REG_INI_TMR_SEL	RXPktTimer, TXPktTimer Unit. (TU)	RW	0x0
5	RE	MII Rx Enable	RW	0x0
4	TE	MII Tx Enable	RW	0x0
3	TXFN4	4th Priority DMA-Ethernet Transmit enable. 1: Enable. 0: Disable	RW	0x0
2	TXFN3	3rd Priority DMA-Ethernet Transmit enable. 1: Enable. 0: Disable	RW	0x0
1	TXFN2	2nd Priority DMA-Ethernet Transmit enable. 1: Enable. 0: Disable	RW	0x0
0	TXFN1	1st Priority DMA-Ethernet Transmit enable. 1: Enable. 0: Disable	RW	0x0

## NIC\_ETN\_IO\_CMD1

REGISTER ADDRESS : 0xBB720138

DEFAULT VALUE : 0x0

Ethernet\_IO\_CMD1

Bits	Field	Description	Type	Default
31	RESERVED			
30:28	DSC_FMT_EXTRA	Extra descriptor format. Dsc_format_extra{0} used to indicate the lso format in tx descriptor. In rle0437, bit28 is lso_des_format and is write only.	RW	0x0
27	RESERVED			
26	RXOKINT_MSK_128B	1: For ingress pkt which is short than 128B, RxOK interrupt asserts after DMA completes(compatible issue). 0: For ingress pkt which is short than 128B, RxOK interrupt does not assert after DMA completes.	RW	0x0
25	EN_RX_MRING	Enable rx multiple rings. 1: rx using multiple rings. max: 6rings (ring1 to ring6). 0. rx using single ring.	RW	0x0

Bits	Field	Description	Type	Default
24	EN_1GB	1: support 1GB addressing in lx master bus. For gmac used in rl0371 and after. 0: no support. For project used in rle0390 and before	RW	0x0
23:22	RESERVED			
21	RXRING6	Ethernet-DMA Receive Ring6 enable. 1: Enable. 0: Disable	RW	0x0
20	RXRING5	Ethernet-DMA Receive Ring5 enable	RW	0x0
19	RXRING4	Ethernet-DMA Receive Ring4 enable	RW	0x0
18	RXRING3	Ethernet-DMA Receive Ring3 enable	RW	0x0
17	RXRING2	Ethernet-DMA Receive Ring2 enable	RW	0x0
16	RXRING1	Ethernet-DMA Receive Ring1 enable	RW	0x0
15:14	TX_HL_PRI_SEL	2b00: TX ring uses strict priority. 2b01: TX ring uses high and low queue priority. Inside high queue, tx ring is round robin. Inside low queue, tx ring is round robin. Strict priority is used for high and low queue selection. 2b10 and 2b11: reserved.	RW	0x0
13:9	RESERVED			
8	TX_FN5	5th Priority DMA-Ethernet Transmit enable. 1: Enable. 0: Disable. After IO_CMD.TE is set high, TxFN5th is writable.	RW	0x0
7:5	RESERVED			
4	TXQ5_H	1: TxFN5th is a high queue. 0: TxFN5th is a low queue	RW	0x0
3	TXQ4_H	1: TxFN4th is a high queue. 0: TxFN4th is a low queue	RW	0x0
2	TXQ3_H	1: TxFN3rd is a high queue. 0: TxFN3rd is a low queue	RW	0x0
1	TXQ2_H	1: TxFN2nd is a high queue. 0: TxFN2nd is a low queue	RW	0x0
0	TXQ1_H	1: TxFN1st is a high queue. 0: TxFN1st is a low queue	RW	0x0

## NIC\_WOL

REGISTER ADDRESS : 0xBB72013C

DEFAULT VALUE : 0x0

## 70 WOL

Bits	Field	Description	Type	Default
31:3	RESERVED			



Bits	Field	Description	Type	Default
2	WOL_PME	<p>HW asserts pme when</p> <p>a. HW entered wol idle state and</p> <p>b. received magic ingress pkt.</p> <p>HW asserts pme to wake up system.</p> <p>Wol_pme indicates:</p> <p>0: No magic pkt receives.</p> <p>1: HW had received one magic pkt and system should wake up</p>	RO	0x0
1	WOL_STS	<p>HW enters wol idle state when</p> <p>a. SW issues wol_cmd state and</p> <p>b. HW tx/rx function enter idle state.</p> <p>Wol_sts indicates:</p> <p>0: HW is not in wol idle state.</p> <p>1: HW is in wol idle state.</p>	RO	0x0
0	WOL_CMD	Issue wol command by SW	RW	0x0



## CHAPTER 5

# Traffic Suppression

The chapter describes features related to traffic suppression

### SECTION 5.1

## STORM CONTROL (B/M/UM/DLF)

Storm Control (B/M/UM/DLF) module

### STORM\_CTRL\_UM\_CTRL

BASE ADDRESS : 0xBB01705C

PORT INDEX : 0 - 6

PORT OFFSET : 1 bit

DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

Storm control global configuration for unknown multicast

Bits	Field	Description	Type	Default
0	EN	Per port unknown multicasting storm filtering setting 0b0:disable unknown multicasting storm filtering 0b1:enable unknown multicasting storm filtering	RW	0x0

### STORM\_CTRL\_UC\_CTRL

BASE ADDRESS : 0xBB017060

PORT INDEX : 0 - 6

PORT OFFSET : 1 bit

DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

Storm control global configuration for unknown unicast

Bits	Field	Description	Type	Default
0	EN	Per port unknown unicasting storm filtering setting 0b0:disable unknown unicasting storm filtering 0b1:enable unknown unicasting storm filtering	RW	0x0

## STORM\_CTRL\_MC\_CTRL

BASE ADDRESS : 0xBB017064  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

Storm control global configuration for multicast

Bits	Field	Description	Type	Default
0	EN	Per port multicasting storm filtering setting 0b0:disable multicasting storm filtering 0b1:enable multicasting storm filtering	RW	0x0

## STORM\_CTRL\_BC\_CTRL

BASE ADDRESS : 0xBB017068  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

Storm control global configuration for broadcast.

Bits	Field	Description	Type	Default
0	EN	Per port broadcasting storm filtering setting 0b0:disable broadcasting storm filtering 0b1:enable broadcasting storm filtering	RW	0x0

## STORM\_CTRL\_UM\_METER\_IDX

BASE ADDRESS : 0xBB01706C  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 5 bits  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (5 bits per field)

Storm control meter index for unknown multicast

Bits	Field	Description	Type	Default
4:0	IDX	unknown multicast storm meter index	RW	0x0

**STORM\_CTRL\_UC\_METER\_IDX**

BASE ADDRESS : 0xBB017074  
PORT INDEX : 0 - 6  
PORT OFFSET : 5 bits  
DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (5 bits per field)

Storm control meter index for unknown unicast

Bits	Field	Description	Type	Default
4:0	IDX	unknown unicast storm meter index	RW	0x0

**STORM\_CTRL\_MC\_METER\_IDX**

BASE ADDRESS : 0xBB01707C  
PORT INDEX : 0 - 6  
PORT OFFSET : 5 bits  
DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (5 bits per field)

Storm control meter index formulticast

Bits	Field	Description	Type	Default
4:0	IDX	multicast storm meter index	RW	0x0

**STORM\_CTRL\_BC\_METER\_IDX**

BASE ADDRESS : 0xBB017084  
PORT INDEX : 0 - 6  
PORT OFFSET : 5 bits  
DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (5 bits per field)

Storm control meter index for broadcast

Bits	Field	Description	Type	Default
4:0	IDX	broadcast storm meter index	RW	0x0

**STORM\_CTRL\_ALT\_TYPE\_SEL**

REGISTER ADDRESS : 0xBB01708C

DEFAULT VALUE : 0x0

Storm control alternative type selection

Bits	Field	Description	Type	Default
31:8	RESERVED			
7:6	UNMC_TYPE	Unknown multicast storm alternative type selection. 0b00:Unknown multicast storm 0b01:ARP storm 0b10:DHCP storm 0b11:IGMP/MLD storm	RW	0x0
5:4	UNDA_TYPE	Unknown unicast storm alternative type selection. 0b00:Unknown unicast storm 0b01:ARP storm 0b10:DHCP storm 0b11:IGMP/MLD storm	RW	0x0
3:2	MC_TYPE	Multicast storm alternative type selection. 0b00:Multicast storm 0b01:ARP storm 0b10:DHCP storm 0b11:IGMP/MLD storm	RW	0x0
1:0	BC_TYPE	Broadcast storm alternative type selection. 0b00:Broadcast storm 0b01:ARP storm 0b10:DHCP storm 0b11:IGMP/MLD storm	RW	0x0

## SECTION 5.2

## BANDWIDTH CONTROL (INGRESS/EGRESS)

Bandwidth Control (Ingress/Egress) module

### IGR\_BWCTRL\_P\_CTRL

BASE ADDRESS : 0xBB020034

PORT INDEX : 0 - 6

PORT OFFSET : 0x400

DEFAULT VALUE : 0x7FFFC

This is a One-Dimension Port Register Array.

Ingress bandwidth control per-port control register.

Bits	Field	Description	Type	Default
31:19	RESERVED			
18:2	RATE	Ingress Bandwidth Control, unit: 8Kbps (K=1024) 17'h1ffff : BW= full rate (line rate) N : BW=N*8Kbps	RW	0x1FFFF
1	MODE	Flow control setting while input rate is over input bandwidth 0: disable, drop packet 1: enable flow control	RW	0x0

Bits	Field	Description	Type	Default
0	IFG	Bandwidth Control Include/exclude Preamble & IFG (20bytes) 0: exclude, 1: include	RW	0x0

## IGR\_BWCTRL\_GLB\_CTRL

REGISTER ADDRESS : 0xBB01C0B8

DEFAULT VALUE : 0x0

Ingress bandwidth control global control register.

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	BYPASS_EN	Enable DMAC=01-80-C2-00-00-xx, IGMP/MLD control packet and ether type 8899 frames bypass ingress flow control	RW	0x0

### SECTION 5.3

## METER MARKER

Meter Marker (Dual Leaky Bucket/srTCM/trTCM) module

## METER\_TB\_CTRL

REGISTER ADDRESS : 0xBB025000

DEFAULT VALUE : 0x11A1D

Specify the tick time of the leaky bucket for a meter block. Unit: clock.

Bits	Field	Description	Type	Default
31:17	RESERVED			
16	METER_OP	0b0: Can't consume token exceed requirement 0b1: consume token exceed requirement, and return to 0.	RW	0x1
15:8	TICK_PERIOD	Meter bucket refresh timing tick, uint 1/system clock frequency. Default value should be set with different chip mode.	RW	0x1A
7:0	TKN	Refresh bytes counter of shared meter. The shared meter TICK and COUNTER should be assigned to matched refresh speed as 8kbps. Default value should be set with different chip mode.	RW	0x1D

## METER\_GLB\_CTRL

BASE ADDRESS : 0xBB025004  
 ARRAY INDEX : 0 - 31  
 ARRAY OFFSET : 0x8  
 DEFAULT VALUE : 0x258

This is a One-Dimension Common Register Array.

Share meter global control register

Bits	Field	Description	Type	Default
63:49	RESERVED			
48:32	RATE	Meter rate,unit: 8Kbps (K=1024) 17'h1ffff : BW= full rate (line rate) N : BW=N*8Kbps	RW	0x0
31:17	RESERVED			
16:1	BUCKET_SIZE	Bucket size of shared meter	RW	0x012C
0	IFG	Share meter rate calculation with 20 bytes IPG	RW	0x0

## METER\_LB\_EXCEED\_STS

BASE ADDRESS : 0xBB025104  
 ARRAY INDEX : 0 - 31  
 ARRAY OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

meter leaky buckets exceeding status. A bit would be set to 1 for a meter if it satisfies "drop packet" or "color packet red". It is write 1 to clear.

Bits	Field	Description	Type	Default
0	LB_EXCEED	1 bit flag per meter entry to show if the meter entry ever drops a packet or color a packet to red. Write 1 to clear. 0b0: no packet is dropped or colored red by this meter 0b1: some packets are ever dropped or colored red by this meter	RW1C	0x0

## PON\_TB\_CTRL

REGISTER ADDRESS : 0xBB025108  
 DEFAULT VALUE : 0x13042

Specify the tick time in PON MAC. Unit: clock.



Bits	Field	Description	Type	Default
31:17	RESERVED			
16	METER_OP	0b0: Can't consume token exceed requirement 0b1: consume token exceed requirement, and return to 0.	RW	0x1
15:8	TICK_PERIOD	Meter bucket refresh timing tick for PON port, uint 1/system clock frequency. Default value should be set with different chip mode.	RW	0x30
7:0	TKN	Refresh bytes counter of shared meter for PON port. The shared meter TICK and COUNTER should be assigned to matched refresh speed as 64kbps. Default value should be set with different chip mode.	RW	0x42

## METER\_PKT\_RATE

REGISTER ADDRESS : 0xBB02510C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:0	SHMTR_PKT_RATE	Share meter mode for calculating packet rate	RW	0x0



## CHAPTER 6

# Security

The chapter describes features related to security

### SECTION 6.1

## 802.1X

802.1X

### DOT1X\_CFG\_0

REGISTER ADDRESS : 0xBB01C0BC

DEFAULT VALUE : 0x0

802.1x function control register

Bits	Field	Description	Type	Default
31:3	RESERVED			
2:0	DOT1X_PRIORITY	Trap priority for 802.1X trapping packets	RW	0x0

### DOT1X\_CFG\_1

REGISTER ADDRESS : 0xBB017090

DEFAULT VALUE : 0x0

802.1x function control register

Bits	Field	Description	Type	Default
31:7	RESERVED			
6	DOT1X_GVOPDIR	Operation direction setting for unauthorized packet belong to guest VLAN 0: SA belongs to Guest VLAN is disallowed to talk to authorized DA 1: SA belongs to Guest VLAN is allowed to talk to authorized DA	RW	0x0
5	DOT1X_MAC_OPDIR	802.1X Mac-based operation direction setting 0b0:BOTH, don't RX unauthorized SA frame and don't TX unauthorized DA frame 0b1:IN , don't RX unauthorized SA frame only.	RW	0x0

Bits	Field	Description	Type	Default
4:0	DOT1X_GVIDX	Guest VLAN member index for unauthorized packets	RW	0x0

## DOT1X\_P\_CTRL

BASE ADDRESS : 0xBB017094  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

802.1X control register

Bits	Field	Description	Type	Default
31:6	RESERVED			
5	PB_EN	Per port 802.1X port-based function enable/disable setting. 0b0:disable 0b1:enable	RW	0x0
4	MAC_EN	Per port 802.1X MAC-based function enable/disable setting. 0b0:disable 0b1:enable	RW	0x0
3	PB_AUTH	Per port 802.1X port-based authentication setting. 0b0:unauthorized 0b1:authorized	RW	0x0
2	PB_DIR	Per port 802.1X port-based operation direction setting while port-based authentication setting is unauthorized 0b0:BOTH, unauthorized port can not TX/RX. 0b1:IN , unauthorized port can TX only.	RW	0x0
1:0	UNAUTH_ACT	unauthorized behavior for both Port and MAC Access Control 0b00: Drop unauthorized frames 0b01: Trap unauthorized frames to CPU 0b10: Guest VLAN 0b11: Reserved	RW	0x0

### SECTION 6.2

## DENIAL-OF-SERVICE ATTACK PREVENTION

Denial-of-service attack prevention module

## DOS\_EN

BASE ADDRESS : 0xBB026000  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 1 bit

DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

per-Port DOS function enable register

Bits	Field	Description	Type	Default
0	EN	Enable per-port DOS function	RW	0x0

## DOS\_CFG

REGISTER ADDRESS : 0xBB026004

DEFAULT VALUE : 0x0

DOS function configuration register

Bits	Field	Description	Type	Default
31	DOS_ICMPFLOOD_ACT	0b0:Drop while ICMP packets number is over threshold 0b1:Trap ICMP packets	RW	0x0
30	DOS_FINFLOOD_ACT	0b0:Drop while TCP FIN packets number is over threshold 0b1:Trap TCP FIN packets	RW	0x0
29	DOS_SYNFLOOD_ACT	0b0:Drop while TCP SYN packets number is over threshold 0b1:Trap TCP SYN packets	RW	0x0
28	DOS_SYNWITHDATA_ACT	Treating type for packets match DOS_SYNWITHDATA 0b0:Drop 0b1:Trap	RW	0x0
27	DOS_UDPBOMB_ACT	Treating type for packets match DOS_UDPBOMB 0b0:Drop 0b1:Trap	RW	0x0
26	DOS_PINGOFDEATH_ACT	Treating type for packets match DOS_PINGOFDEATH 0b0:Drop 0b1:Trap	RW	0x0
25	DOS_ICMPFRAGMENT_ACT	Treating type for packets match DOS_ICMPFRAGMENT 0b0:Drop 0b1:Trap	RW	0x0
24	DOS_TCPFRAGERROR_ACT	Treating type for packets match DOS_TCPFRAGERROR 0b0:Drop 0b1:Trap	RW	0x0
23	DOS_TCPSHORTHDR_ACT	Treating type for packets match DOS_TCPSHORTHDR 0b0:Drop 0b1:Trap	RW	0x0
22	DOS_SYN1024_ACT	Treating type for packets match DOS_SYN1024 0b0:Drop 0b1:Trap	RW	0x0

Bits	Field	Description	Type	Default
21	DOS_NULLSCAN_ACT	Treating type for packets match DOS_NULLSCAN 0b0:Drop 0b1:Trap	RW	0x0
20	DOS_XMASCAN_ACT	Treating type for packets match DOS_XMASCAN 0b0:Drop 0b1:Trap	RW	0x0
19	DOS_SYNFINSCAN_ACT	Treating type for packets match DOS_SYNFINSCAN 0b0:Drop 0b1:Trap	RW	0x0
18	DOS_BLATATTACKS_ACT	Treating type for packets match DOS_BLATATTACKS 0b0:Drop 0b1:Trap	RW	0x0
17	DOS_LANDATTACKS_ACT	Treating type for packets match DOS_LANDATTACKS 0b0:Drop 0b1:Trap	RW	0x0
16	DOS_DAEQSA_ACT	Treating type for packets match DOS_DAEQSA 0b0:Drop 0b1:Trap	RW	0x0
15	DOS_ICMPFLOOD	Receiving ICMP packet number is over threshold, unit per 1ms	RW	0x0
14	DOS_FINFLOOD	Receiving TCP FIN packet number is over thresh- old, unit per 1ms	RW	0x0
13	DOS_SYNFLOOD	Receiving TCP SYN packet number is over thresh- old, unit per 1ms	RW	0x0
12	DOS_SYNWITHDATA	1.IP length > IP header + TCP header length while SYN flag is set 1 2. IP More Fragment and Offset > 0 while SYN is set to 1	RW	0x0
11	DOS_UDPBOMB	UDP length > IP payload length	RW	0x0
10	DOS_PINGOFDEATH	IP packet size > 65535 bytes, ((IP offset *8) + (IP length) (IPIHL*4))>65535	RW	0x0
9	DOS_ICMPFRAGMENT	ICMPv4/ICMPv6 data unit carried in a fragmented IP datagram	RW	0x0
8	DOS_TCPFRAGERROR	the Frangment_Offset=1 in anyfragment of a frag- mented IP datagram carrying part of TCP data	RW	0x0
7	DOS_TCPSHORTHDR	the length of a TCP header carried in an unfrag- mented IP(IPv4 and IPv6) datagram or the first fragment of a fragmented IP(IPv4) datagram is less than MIN_TCP_Header_Size(20 bytes)	RW	0x0
6	DOS_SYN1024	TCP SYN packets with source port less than 1024	RW	0x0
5	DOS_NULLSCAN	TCP packets while sequence number is zero and all contorl bits are zeros.	RW	0x0
4	DOS_XMASCAN	TCP packets while sequence number is zero and FIN,URG,PSH bits are set	RW	0x0
3	DOS_SYNFINSCAN	TCP packets while SYN and FIN bits are set	RW	0x0
2	DOS_BLATATTACKS	packets while the TCP/UDP SPORT is the same as DPORT destination TCP/UDP port	RW	0x0

Bits	Field	Description	Type	Default
1	DOS_LANDATTACKS	packets while SIP is the same as DIP(support IPv4 only)	RW	0x0
0	DOS_DAEQSA	packets while SMAC is the same as DMAC	RW	0x0

## DOS\_SYN\_FLOOD\_TH

REGISTER ADDRESS : 0xBB026008

DEFAULT VALUE : 0x0

system-based SYN flood threshold register

Bits	Field	Description	Type	Default
31:8	RESERVED			
7:0	TH	System-based SYN flood threshold, time unit 1ms	RW	0x0

## DOS\_FIN\_FLOOD\_TH

REGISTER ADDRESS : 0xBB02600C

DEFAULT VALUE : 0x0

system-based FIN flood threshold register

Bits	Field	Description	Type	Default
31:8	RESERVED			
7:0	TH	System-based FIN flood threshold, time unit 1ms	RW	0x0

## DOS\_ICMP\_FLOOD\_TH

REGISTER ADDRESS : 0xBB026010

DEFAULT VALUE : 0x0

system-based ICMP flood threshold register

Bits	Field	Description	Type	Default
31:8	RESERVED			
7:0	TH	System-based ICMP flood threshold, time unit 1ms	RW	0x0





## CHAPTER 7

# Network Monitoring

The chapter describes features related to network monitoring

### SECTION 7.1

## MIRRORING

Mirroring module

### MIR\_CTRL

REGISTER ADDRESS : 0xBB0230FC

DEFAULT VALUE : 0x0

Mirror control register

Bits	Field	Description	Type	Default
31:13	RESERVED			
12:6	MIR_SRC_PMSK	Mirror Source Port Mask	RW	0x0
5	MIR_ISO	Enable the traffic isolation on monitor port. 0b0 Normal operation. 0b1 The monitor port will accept only the packets from the source port.	RW	0x0
4	MIR_TX	Enable the mirror function on TX of the source port. 0b0 Disable. 0b1 Enable.	RW	0x0
3	MIR_RX	Enable the mirror function on RX of the source port. 0b0 Disable. 0b1 Enable.	RW	0x0
2:0	MIR_MONITOR_PORT	Select the monitor port to be mirroring	RW	0x0

### SECTION 7.2

## SFLOW

sFlow module

## SECTION 7.3

## STATISTIC COUNTERS

Statistic Counters module

### STAT\_PRIVATE\_REASON

BASE ADDRESS : 0xBB01C0C0  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 10 bits  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (10 bits per field)

Specify per-port packet debug information

Bits	Field	Description	Type	Default
9:0	PKT_INFO	port index 0 6:per-port the newest packet trap/drop reason	RO	0x0

### STAT\_ACL\_REASON

BASE ADDRESS : 0xBB01C0CC  
 ARRAY INDEX : 0 - 5  
 ARRAY OFFSET : 8 bits  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (8 bits per field)

Specify ACL hit reason

Bits	Field	Description	Type	Default
7:0	ACL_HIT_INFO	ACLhit rule reason	RO	0x0

### STAT\_CF\_REASON

BASE ADDRESS : 0xBB01C0D4  
 ARRAY INDEX : 0 - 1  
 ARRAY OFFSET : 10 bits  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (10 bits per field)

Specify Classification hit reason

Bits	Field	Description	Type	Default
9:0	CF_HIT_INFO	Classification hit reason	RO	0x0

Bits	Field	Description	Type	Default
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## STAT\_PORT\_TX\_MIB

BASE ADDRESS : 0xBB032000  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 0x80  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Per port stanadard TX MIB counters.

Bits	Field	Description	Type	Default
1023:992	tx_etherStatsMulticastPkts	The total number of good packets received that were directed to a multicast address. Note that this number does not include packets directed to the broadcast address.	RO	0x0
991:960	tx_etherStatsBroadcastPkts	The total number of good packets received that were directed to the broadcast address. Note that this does not include multicast packets.	RO	0x0
959:928	tx_etherStatsUndersizePkts	The total number of packets received that were less than 64 octets long (excluding framing bits, but including FCS octets) and were otherwise well formed. Note: count w/wo tag length depends on TX_CNT_TAG	RO	0x0
927:896	tx_etherStatsOversizePkts	The total number of packets received that were longer than 1518 octets (excluding framing bits, but including FCS octets) and were otherwise well formed. Note: count w/wo tag length depends on RX_CNT_TAG	RO	0x0
895:864	tx_etherStatsPkts64Octets	The total number of packets (including bad packets) received that were 64 octets in length (excluding framing bits but including FCS octets). Note: count w/wo tag length depends on TX_CNT_TAG	RO	0x0
863:832	tx_etherStatsPkts65to127Octets	The total number of packets (including bad packets) received that were between 65 and 127 octets in length inclusive (excluding framing bits but including FCS octets). Note: count w/wo tag length depends on TX_CNT_TAG	RO	0x0
831:800	tx_etherStatsPkts128to255Octets	The total number of packets (including bad packets) received that were between 128 and 255 octets in length inclusive (excluding framing bits but including FCS octets). Note: count w/wo tag length depends on TX_CNT_TAG	RO	0x0

Bits	Field	Description	Type	Default
799:768	tx_etherStatsPkts256 to511Octets	The total number of packets (including bad packets) received that were between 256 and 511 octets in length inclusive (excluding framing bits but including FCS octets). Note: count w/wo tag length depends on TX_CNT_TAG	RO	0x0
767:736	tx_etherStatsPkts512 to1023Octets	The total number of packets (including bad packets) received that were between 512 and 1023 octets in length inclusive (excluding framing bits but including FCS octets). Note: count w/wo tag length depends on TX_CNT_TAG	RO	0x0
735:704	tx_etherStatsPkts1024 to1518Octets	The total number of packets (including bad packets) received that were between 1024 and 1518 octets in length inclusive (excluding framing bits but including FCS octets). Note: count w/wo tag length depends on TX_CNT_TAG	RO	0x0
703:672	ifOutOctets_L	ifOutOctets: 32 bits counter. The total number of octets transmitted out of the interface, including framing characters.  ifHCOctets: 64 bits counter. Same as ifOutOctets. Note: count with tag length	RO	0x0
671:640	ifOutOctets_H	ifOutOctets: 32 bits counter. The total number of octets transmitted out of the interface, including framing characters.  ifHCOctets: 64 bits counter. Same as ifOutOctets. Note: count with tag length	RO	0x0
639:608	dot3StatsSingleCollisionFrames	A count of frames that are involved in a single collision, and are subsequently transmitted successfully.	RO	0x0
607:576	dot3StatsMultipleCollisionFrames	A count of frames that are involved in more than one collision and are subsequently transmitted successfully.	RO	0x0
575:544	dot3StatsDeferredTransmissions	A count of frames for which the first transmission attempt on a particular interface is delayed because the medium is busy. Note: in half-duplex mode. The the counter does not include frames involved in collisions.	RO	0x0
543:512	dot3StatsLateCollisions	The number of times that a collision is detected on a particular interface later than one slotTime into the transmission of a packet.	RO	0x0
511:480	etherStatsCollisions	The best estimate of the total number of collisions on this Ethernet segment	RO	0x0
479:448	dot3StatsExcessiveCollisions	A count of frames for which transmission on a particular interface fails due to excessive collisions.	RO	0x0
447:416	dot3OutPauseFrames	A count of MAC Control frames transmitted on this interface with an opcode indicating the PAUSE operation.	RO	0x0

Bits	Field	Description	Type	Default
415:384	ifOutDiscards	The number of outbound packets which were chosen to be discarded even though no errors had been detected to prevent their being transmitted. One possible reason for discarding such a packet could be to free up buffer space.	RO	0x0
383:352	tx_etherStatsPkts1519toMaxOctets	The total number of packets (including bad packets) received that were between 1519 and Max octets in length inclusive (excluding framing bits but including FCS octets). Note: count w/wo tag length depends on TX_CNT_TAG	RO	0x0
351:320	RESERVED			
319:288	dot1dTpPortInDiscards	Count of valid frames received which were discarded (i.e., filtered) by the Forwarding Process. Note: drop in ALE	RO	0x0
287:256	ifOutUcastPkts	The total number of packets that higher-level protocols requested be transmitted, and which were not addressed to a multicast or broadcast address at this sub-layer, including those that were discarded or not sent. Note: discarded or not sent packets are count in.	RO	0x0
255:224	ifOutMulticastPkts	The total number of packets that higher-level protocols requested be transmitted, and which were addressed to a multicast address at this sub-layer, including those that were discarded or not sent. Note: discarded or not sent packets are count in.	RO	0x0
223:192	ifOutBroadcastPkts	The total number of packets that higher-level protocols requested be transmitted, and which were addressed to a broadcast address at this sub-layer, including those that were discarded or not sent. Note: discarded or not sent packets are count in.	RO	0x0
191:0	RESERVED			

## STAT\_PORT\_RX\_MIB

BASE ADDRESS : 0xBB032400  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 0x80  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Per port stanadard RX MIB counters.

Bits	Field	Description	Type	Default
1023:992	ifInOctets_L	ifInOctets: 32 bits counter. The total number of octets received on the interface, including framing characters.  ifHCInOctets: 64 bits counter. Same as ifInOctets. Note: count with tag length	RO	0x0

Bits	Field	Description	Type	Default
991:960	ifInOctets_H	ifInOctets: 32 bits counter. The total number of octets received on the interface, including framing characters.  ifHCInOctets: 64 bits counter. Same as ifInOctets. Note: count with tag length	RO	0x0
959:928	etherStatsCRCAlignErrors	The total number of packets received that had a length (excluding framing bits, but including FCS octets) of between 64 and 1518 octets, inclusive, but had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error). Note: count w/wo tag length depends on RX_CNT_TAG	RO	0x0
927:896	dot3StatsSymbolErrors	For an interface operating at 100 Mb/s, the number of times there was an invalid data symbol when a valid carrier was present.	RO	0x0
895:864	dot3InPauseFrames	A count of MAC Control frames received on this interface with an opcode indicating the PAUSE operation.	RO	0x0
863:832	dot3ControlInUnknownOpCodes	A count of MAC Control frames received on this interface that contain an opcode that is not supported by this device. Note: ether type = 8808 and opcode != 0001 in non-PON/0001 to 0006 in PON	RO	0x0
831:800	etherStatsFragments	The total number of packets received that were less than 64 octets in length (excluding framing bits but including FCS octets) and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error) Note: count w/wo tag length depends on RX_CNT_TAG	RO	0x0
799:768	etherStatsJabbers	The total number of packets received that were longer than 1518 octets (excluding framing bits, but including FCS octets), and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error). Note: count w/wo tag length depends on RX_CNT_TAG	RO	0x0
767:736	ifInUcastPkts	The number of packets, delivered by this sub-layer to a higher (sub-)layer, which were not addressed to a multicast or broadcast address at this sub-layer. Note: only count valid frame.	RO	0x0
735:704	etherStatsDropEvents	The total number of events in which packets were dropped by the probe due to lack of resources. Note that this number is not necessarily the number of packets dropped; it is just the number of times this condition has been detected. Note: drop before ALE due to lack of resources, ex. no system packet buffer, receiving packets after sending pause ON frame.	RO	0x0

Bits	Field	Description	Type	Default
703:672	ifInMulticastPkts	The number of packets, delivered by this sub-layer to a higher (sub-)layer, which were addressed to a multicast address at this sub-layer (Number of received valid multicast packets). Note: only count valid frame.	RO	0x0
671:640	ifInBroadcastPkts	The number of packets, delivered by this sub-layer to a higher (sub-)layer, which were addressed to a broadcast address at this sub-layer (Number of received valid broadcast packets). Note: only count valid frame.	RO	0x0
639:608	rx_etherStatsPkts1519toMax-Octets	The total number of packets (including bad packets) received that were between 1519 and Max octets in length inclusive (excluding framing bits but including FCS octets). Note: count w/wo tag length depends on RX_CNT_TAG	RO	0x0
607:576	rx_etherStatsUndersizeDropPkts	Private counter. The total number of packets received that were less than 64 octets long (excluding framing bits, but including FCS octets) and were otherwise well formed. Note: count w/wo tag length depends on RX_CNT_TAG Note: under size and drop only	RO	0x0
575:544	rx_etherStatsUndersizePkts	The total number of packets received that were less than 64 octets long (excluding framing bits, but including FCS octets) and were otherwise well formed. Note: count w/wo tag length depends on RX_CNT_TAG Note: under size including drop or forward	RO	0x0
543:512	rx_etherStatsOversizePkts	The total number of packets received that were longer than 1518 octets (excluding framing bits, but including FCS octets) and were otherwise well formed. Note: count w/wo tag length depends on RX_CNT_TAG	RO	0x0
511:480	rx_etherStatsPkts64Octets	The total number of packets (including bad packets) received that were 64 octets in length (excluding framing bits but including FCS octets). Note: count w/wo tag length depends on RX_CNT_TAG	RO	0x0
479:448	rx_etherStatsPkts65to127Octets	The total number of packets (including bad packets) received that were between 65 and 127 octets in length inclusive (excluding framing bits but including FCS octets). Note: count w/wo tag length depends on RX_CNT_TAG	RO	0x0
447:416	rx_etherStatsPkts128to255Octets	The total number of packets (including bad packets) received that were between 128 and 255 octets in length inclusive (excluding framing bits but including FCS octets). Note: count w/wo tag length depends on RX_CNT_TAG	RO	0x0

Bits	Field	Description	Type	Default
415:384	rx_etherStatsPkts256to511Octets	The total number of packets (including bad packets) received that were between 256 and 511 octets in length inclusive (excluding framing bits but including FCS octets). Note: count w/wo tag length depends on RX_CNT_TAG	RO	0x0
383:352	rx_etherStatsPkts512to1023Octets	The total number of packets (including bad packets) received that were between 512 and 1023 octets in length inclusive (excluding framing bits but including FCS octets). Note: count w/wo tag length depends on RX_CNT_TAG	RO	0x0
351:320	rx_etherStatsPkts1024to1518Octets	The total number of packets (including bad packets) received that were between 1024 and 1518 octets in length inclusive (excluding framing bits but including FCS octets). Note: count w/wo tag length depends on RX_CNT_TAG	RO	0x0
319:0	RESERVED			

## STAT\_PORT\_OAM\_MIB

BASE ADDRESS : 0xBB032800  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 0x8  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Per port stanadard OAM MIB counters.

Bits	Field	Description	Type	Default
63:32	OutOampduPkts	A count of OAMPDUs transmitted on this interface	RO	0x0
31:0	InOampduPkts	Number of received OAMPDUs.	RO	0x0

## STAT\_BRIDGE\_DOT1DTPLEARNEDENTRYDISCARDS

REGISTER ADDRESS : 0xBB032840  
 DEFAULT VALUE : 0x0

dot1dTpLearnedEntryDiscards MIB counter in RFC 1493/2674.

Bits	Field	Description	Type	Default
31:0	dot1dTpLearnedEntryDiscards	Learning miss. The total number of Forwarding Database entries, which have been or would have been learnt, but have been discarded due to lack of space to store them in the Forwarding Database.	RO	0x0



Bits	Field	Description	Type	Default
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## STAT\_ACL\_CNT

BASE ADDRESS : 0xBB032880  
 ARRAY INDEX : 0 - 31  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

ACL logging counter

Bits	Field	Description	Type	Default
31:0	loggingcounter	Logging counter for ACL action	RO	0x0

## STAT\_CTRL

REGISTER ADDRESS : 0xBB034000  
 DEFAULT VALUE : 0xC

MIB control register

Bits	Field	Description	Type	Default
31:13	RESERVED			
12	SYNC_STATUS	MIB stop sync status 0b0:Busy 0b1:Done	RO	0x0
11:4	LATCH_TIMER	MIB latch timer, unit 1 second. Clear by asic after reach latch time	RWAC	0x0
3	TX_CNT_CTAG	Count tag length in TX packet length include C-tag or not MIB counter 0b1: enable 0b0: disable	RW	0x1
2	RX_CNT_CTAG	Count tag length in RX packet length include C-tag or not MIB counter 0b1: enable 0b0: disable	RW	0x1
1	SYNC_MODE	MIB register data update mode 0b0: stop sync 0b1: normal free run sync	RW	0x0
0	CNTING_MODE	MIB data update mode 0b00: normal free run counting 0b01: counting and latch all MIBs by MIB_TIMER control	RW	0x0

## STAT\_ACL\_CNT\_MODE

BASE ADDRESS : 0xBB034004  
 ARRAY INDEX : 0 - 15  
 ARRAY OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

ACL logging counter mode

Bits	Field	Description	Type	Default
0	MODE	ACL logging counter m(0,2,4,...30) mode 0b0:32bits mode 0b1:64bits mode	RW	0x0

## STAT\_ACL\_CNT\_TYPE

BASE ADDRESS : 0xBB034008  
 ARRAY INDEX : 0 - 15  
 ARRAY OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

ACL logging counter type

Bits	Field	Description	Type	Default
0	TYPE	ACL logging counter byte/packet count 0b0:Packet count 0b1:Byte count	RW	0x0

## STAT\_ACL\_CNT\_RST

BASE ADDRESS : 0xBB03400C  
 ARRAY INDEX : 0 - 31  
 ARRAY OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

ACL logging counter reset

Bits	Field	Description	Type	Default
0	EN	Reset ACL logging counter 0b0:disable 0b1:enable resetting	RW	0x0

## STAT\_PORT\_RST

BASE ADDRESS : 0xBB034010  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

Reset all of MIB counter for a specified port.

Bits	Field	Description	Type	Default
0	RST_PORT_MIB	Reset MIB counters for a port. Write 1 to clear MIB counters. After resetting, the value is reset to 0	RW	0x0

## STAT\_RST

REGISTER ADDRESS : 0xBB034014  
 DEFAULT VALUE : 0x0

MIB reset configurations

Bits	Field	Description	Type	Default
31:4	RESERVED			
3	RST_STAT	ASIC is resetting MIB	RO	0x0
2	RST_MIB_VAL	Reset MIB counter(except private debug counter ) to 0 or all 1 0b1: reset counter to all '1' 0b0: reset counter to 0	RW	0x0
1	RESERVED			
0	RST_GLOBAL_MIB	Reset global MIB counters. Write 1 to clear MIB counters. After resetting, the value is reset to 0	RW	0x0

## OMCI\_DROP\_PKT\_CNT

REGISTER ADDRESS : 0xBB032900  
 DEFAULT VALUE : 0x0

OMCI drop packet counter

Bits	Field	Description	Type	Default
31:0	omciDropPktCnt	OMCI Drop packet counter	RO	0x0

**OMCI\_TX\_PKT\_CNT**

REGISTER ADDRESS : 0xBB032904

DEFAULT VALUE : 0x0

OMCI TX packet counter

Bits	Field	Description	Type	Default
31:0	omciTxPktCnt	OMCI TX packet counter	RO	0x0

**OMCI\_RX\_PKT\_CNT**

REGISTER ADDRESS : 0xBB032908

DEFAULT VALUE : 0x0

OMCI RX packet counter

Bits	Field	Description	Type	Default
31:0	omciRxPktCnt	OMCI RX packet counter	RO	0x0

**OMCI\_TX\_BYTE\_CNT**

REGISTER ADDRESS : 0xBB03290C

DEFAULT VALUE : 0x0

OMCI TX byte counter

Bits	Field	Description	Type	Default
31:0	omciTxByteCnt	OMCI TX byte counter	RO	0x0

**OMCI\_RX\_BYTE\_CNT**

REGISTER ADDRESS : 0xBB032910

DEFAULT VALUE : 0x0

OMCI RX byte counter

Bits	Field	Description	Type	Default
31:0	omciRxByteCnt	OMCI RX byte counter	RO	0x0

## OMCI\_CRC\_ERROR\_PKT\_CNT

REGISTER ADDRESS : 0xBB032914

DEFAULT VALUE : 0x0

OMCI CRC Error counter

Bits	Field	Description	Type	Default
31:0	omciCRCErrorPktCnt	OMCI CRC Error packet counter	RO	0x0

## EPON\_STAT\_RST

REGISTER ADDRESS : 0xBB034018

DEFAULT VALUE : 0x0

EPON MIB reset configurations.

Bits	Field	Description	Type	Default
31:7	RESERVED			
6	BUSY_STAT	ASIC is accessing MIB	RO	0x0
5	RST_CMD	Reset MIB(Global, port, ACL) counter, clear by ASIC	RWAC	0x0
4:2	RST_LLID_IDX	Reset LLID idx	RW	0x0
1	RST_LLID	Reset LLID MPCP counter MIB and LLID relative counters including dot3ExtPkgStatTxFramesQueue, clear by ASIC	RW	0x0
0	RST_ALL_MIB	Reset all EPON MIB counters. Write 1 to clear MIB counters. After resetting, the value is reset to 0	RW	0x0

## DOT3\_Q\_TX\_FRAMES

BASE ADDRESS : 0xBB032918

ARRAY INDEX : 0 - 127

ARRAY OFFSET : 0x4

DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

dot3ExtPkgStatTxFramesQueue

Bits	Field	Description	Type	Default
31:0	dot3ExtPkgStatTxFramesQueue	A count of the number of times a frame transmission occurs from the corresponding 'Queue'. Increment the counter by one for each frame transmitted, which is an output of the 'Queue'.	RO	0x0

Bits	Field	Description	Type	Default
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## DOT3\_MPCP\_RX\_DISC

REGISTER ADDRESS : 0xBB032B18

DEFAULT VALUE : 0x0

dot3MpcpRxDiscoveryGate

Bits	Field	Description	Type	Default
31:0	dot3MpcpRxDiscoveryGate	rx discovery gate number.	RO	0x0

## DOT3\_EPON\_FEC\_CORRECTED\_BLOCKS

REGISTER ADDRESS : 0xBB032B1C

DEFAULT VALUE : 0x0

dot3EponFecCorrectedBlocks

Bits	Field	Description	Type	Default
31:0	dot3EponFecCorrected Blocks	it is a count of correctable FEC blocks.	RO	0x0

## DOT3\_EPON\_FEC\_UNCORRECTED\_BLOCKS

REGISTER ADDRESS : 0xBB032B20

DEFAULT VALUE : 0x0

dot3EponFecUncorrectableBlocks

Bits	Field	Description	Type	Default
31:0	dot3EponFecUncorrectable Blocks	For 10PASS-TS, 2BASE-TL, and 1000BASE-PX PHYs, it is a count of uncorrectable FEC blocks. This counter will not increment for other PHY Types. Increment the counter by one for each FEC block that is determined to be uncorrectable by the FEC function in the PHY.	RO	0x0

## DOT3\_EPON\_FEC\_CODING\_VIO

REGISTER ADDRESS : 0xBB032B24

DEFAULT VALUE : 0x0

dot3EponFecPCSCodingViolation

Bits	Field	Description	Type	Default
31:0	FecPCSCodingViolatio n	For a 1000 Mbps operation, it is a count of the number of times an invalid codegroup is received.	RO	0x0

## DOT3\_NOT\_BROADCAST\_BIT\_NOT\_ONU\_LLID

REGISTER ADDRESS : 0xBB032B28

DEFAULT VALUE : 0x0

dot3OmpEmulationNotBroadcastBitNotOnuLlid

Bits	Field	Description	Type	Default
31:0	NotBroadcastBitNotOn uLlid	A count of frames received that contain a valid SLD field, pass the CRC-8 check, and do not contain the ONU's LLID (Mode is unicast but LLID not local ONU's LLID ) this kind of packet will be dropped	RO	0x0

## DOT3\_BROADCAST\_BIT\_PLUS\_ONU\_LLID

REGISTER ADDRESS : 0xBB032B2C

DEFAULT VALUE : 0x0

dot3OmpEmulationBroadcastBitPlusOnuLlid

Bits	Field	Description	Type	Default
31:0	BroadcastBitPlusOnuL lid	A count of frames received that contain a valid SLD field, pass the CRC-8 check, and contain the broadcast bit in the LLID and match the ONU's LLID (frame reflected) (mode is broadcast, but LLID not equal to 0x7FFF and ONU's LLID)this kind of packet wii be dropped	RO	0x0

## DOT3\_BROADCAST\_NOT\_ONUID

REGISTER ADDRESS : 0xBB032B30

DEFAULT VALUE : 0x0

dot3OmpEmulationBroadcastBitNotOnuLlid

Bits	Field	Description	Type	Default
31:0	BroadcastBitNotOnuLl id	A count of frames received that contain a valid SLD field, pass the CRC-8 check, contain the broadcast bit in the LLID and not the ONUs LLID	RO	0x0

## DOT3\_CRC8\_ERRORS

REGISTER ADDRESS : 0xBB032B34

DEFAULT VALUE : 0x0

dot3OmpEmulationCRC8Errors

Bits	Field	Description	Type	Default
31:0	CRC8Errors	A count of frames received that contain a valid SLD field, but do not pass the CRC-8 check. (valid SLD field but CRC-8 check fail)	RO	0x0

## DOT3\_LLID\_RX\_BROADCAST\_DROP\_FRAMES

REGISTER ADDRESS : 0xBB032B38

DEFAULT VALUE : 0x0

dot3LLIDRxBroadcastFramesDrop

Bits	Field	Description	Type	Default
31:0	dot3LLIDRxBroadcastFramesDrop	A count of the number of times a frame drop occurs by egress for all SBC frames.	RO	0x0

## DOT3\_MPCP\_TX\_REPORT

BASE ADDRESS : 0xBB032B3C

ARRAY INDEX : 0 - 7

ARRAY OFFSET : 0x4

DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

dot3MpcpTxReport counter

Bits	Field	Description	Type	Default
31:0	dot3MpcpTxReport	A count of the number of times a REPORT MPCP frame transmission occurs.	RO	0x0



## DOT3\_MPCP\_EX\_GATE

BASE ADDRESS : 0xBB032B5C  
 ARRAY INDEX : 0 - 7  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

dot3MpcpRxGate counter

Bits	Field	Description	Type	Default
31:0	dot3MpcpRxGate	A count of the number of times a GATE MPCP frame reception occurs. (exclude discovery gate)	RO	0x0

## DOT3\_ONUID\_NOT\_BROADCAST

BASE ADDRESS : 0xBB032B7C  
 ARRAY INDEX : 0 - 7  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

dot3OmpEmulationOnuLLIDNotBroadcast

Bits	Field	Description	Type	Default
31:0	OnuLLIDNotBroadcast	A count of frames received that contain a valid SLD field, pass the CRC-8 check, and contain the ONU's LLID.	RO	0x0

## STAT\_DOT3\_LLIDRXFRAMESDROP

BASE ADDRESS : 0xBB032B9C  
 ARRAY INDEX : 0 - 7  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

dot3LLIDRxFramesDrop

Bits	Field	Description	Type	Default
31:0	dot3LLIDRxFramesDrop	A count of the number of times a frame drop occurs by ALE egress for this LLID.	RO	0x0

**DOT3\_MPCP\_TX\_REG\_REQ**

REGISTER ADDRESS : 0xBB032BBC

DEFAULT VALUE : 0x0

dot3MpcpTxRegRequest

Bits	Field	Description	Type	Default
31:0	dot3MpcpTxRegRequest	A count of the number of times a REGISTER_REQ MPCP frame transmission occurs.	RO	0x0

## CHAPTER 8

# Buffer Management

The chapter describes features related to buffer management

### SECTION 8.1

## FLOWCONTROL & BACKPRESSURE THRESHOLD

Flowcontrol & Backpressure Threshold module

### FC\_CTRL

REGISTER ADDRESS : 0xBB023100

DEFAULT VALUE : 0xB

Flow control related configuration

Bits	Field	Description	Type	Default
31:4	RESERVED			
3:2	FC_JUMBO_SIZE	Size of Jumbo frame for flow control usage 0x0: 3Kbytes 0x1: 4Kbytes 0x2: 6Kbytes 0x3: max packet length > (bytes per page) * 70. In Apollo, 64 bytes per page	RW	0x2
1	FC_JUMBO_MODE	Using jumbo threshold to check if ingress port is in congest state	RW	0x1
0	FC_TYPE	Flow control enable setting 0b0:using egress flow control 0b1:using ingress flow control	RW	0x1

### FC\_DROP\_ALL\_TH

REGISTER ADDRESS : 0xBB023104

DEFAULT VALUE : 0x1B58

Specify flow control drop all threshold register.

Bits	Field	Description	Type	Default
31:13	RESERVED			

Bits	Field	Description	Type	Default
12:0	TH	Flow control force drop(run-out) threshold. ASIC will force drop incoming packet while total page used counter is over this setting unit page	RW	0x1B58

## FC\_PAUSE\_ALL\_TH

REGISTER ADDRESS : 0xBB023108

DEFAULT VALUE : 0x1A86

Specify flow control pause all threshold register.

Bits	Field	Description	Type	Default
31:13	RESERVED			
12:0	TH	Threshold of system page usage number is over this one and egress flow control is enabled, ASIC will force sending pause ON frame to all ports until page using number is under this threshold, unit page	RW	0x1A86

## FC\_GLB\_FCOFF\_HI\_TH

REGISTER ADDRESS : 0xBB02310C

DEFAULT VALUE : 0xCDA0C94

Specify global high on/off threshold when flow ctrl off.

Bits	Field	Description	Type	Default
31:29	RESERVED			
28:16	ON_TH	System based threshold for starting to drop packet	RW	0x0CDA
15:13	RESERVED			
12:0	OFF_TH	System based threshold for stopping to drop packet	RW	0x0C94

## FC\_GLB\_FCOFF\_LO\_TH

REGISTER ADDRESS : 0xBB023110

DEFAULT VALUE : 0xC080BC2

Specify global low on/off threshold when flow ctrl off.

Bits	Field	Description	Type	Default
31:29	RESERVED			

Bits	Field	Description	Type	Default
28:16	ON_TH	Shared based threshold for starting to drop packet	RW	0x0C08
15:13	RESERVED			
12:0	OFF_TH	Shared based threshold for stopping to drop packet	RW	0x0BC2

## FC\_GLB\_HI\_TH

REGISTER ADDRESS : 0xBB023114

DEFAULT VALUE : 0xCDA0C94

Specify global high on/off threshold when flow ctrl on.

Bits	Field	Description	Type	Default
31:29	RESERVED			
28:16	ON_TH	System based threshold for turn on flow control	RW	0x0CDA
15:13	RESERVED			
12:0	OFF_TH	System based threshold for turn off flow control	RW	0x0C94

## FC\_GLB\_LO\_TH

REGISTER ADDRESS : 0xBB023118

DEFAULT VALUE : 0xC080BC2

Specify global low on/off threshold when flow ctrl on.

Bits	Field	Description	Type	Default
31:29	RESERVED			
28:16	ON_TH	Shared based threshold for turn on flow control	RW	0x0C08
15:13	RESERVED			
12:0	OFF_TH	Shared based threshold for turn off flow control	RW	0x0BC2

## FC\_P\_HI\_TH

REGISTER ADDRESS : 0xBB02311C

DEFAULT VALUE : 0x54004EC

Specify per port high on/off threshold when flow control on.

Bits	Field	Description	Type	Default
31:29	RESERVED			

Bits	Field	Description	Type	Default
28:16	ON_TH	port based threshold for turn on flow control	RW	0x0540
15:13	RESERVED			
12:0	OFF_TH	Port based threshold for turn off flow control	RW	0x04EC

## FC\_P\_LO\_TH

REGISTER ADDRESS : 0xBB023120

DEFAULT VALUE : 0xE00054

Specify per port low on/off threshold when flow control on.

Bits	Field	Description	Type	Default
31:29	RESERVED			
28:16	ON_TH	Port based reserved threshold for turn on flow control	RW	0x00E0
15:13	RESERVED			
12:0	OFF_TH	Port based reserved threshold for turn off flow control	RW	0x0054

## FC\_P\_FCOFF\_HI\_TH

REGISTER ADDRESS : 0xBB023124

DEFAULT VALUE : 0x54004EC

Specify per port high on/off threshold when flow control off

Bits	Field	Description	Type	Default
31:29	RESERVED			
28:16	ON_TH	port based threshold for turn on flow control	RW	0x0540
15:13	RESERVED			
12:0	OFF_TH	Port based threshold for turn off flow control	RW	0x04EC

## FC\_P\_FCOFF\_LO\_TH

REGISTER ADDRESS : 0xBB023128

DEFAULT VALUE : 0xE00054

Specify per port low on/off threshold when flow control off

Bits	Field	Description	Type	Default
31:29	RESERVED			
28:16	ON_TH	Port based reserved threshold for turn on flow control	RW	0x00E0
15:13	RESERVED			
12:0	OFF_TH	Port based reserved threshold for turn off flow control	RW	0x0054

## FC\_JUMBO\_GLB\_HI\_TH

REGISTER ADDRESS : 0xBB02312C

DEFAULT VALUE : 0x173E02BC

Specify jumbo mode global high on/off threshold when flow control on.

Bits	Field	Description	Type	Default
31:29	RESERVED			
28:16	ON_TH	Jumbo System based threshold for turn on flow control	RW	0x173E
15:13	RESERVED			
12:0	OFF_TH	Jumbo System based threshold for turn off flow control	RW	0x02BC

## FC\_JUMBO\_GLB\_LO\_TH

REGISTER ADDRESS : 0xBB023130

DEFAULT VALUE : 0x0

Specify jumbo mode global low on/off threshold when flow control on.

Bits	Field	Description	Type	Default
31:29	RESERVED			
28:16	ON_TH	Jumbo Shared based threshold for turn on flow control	RW	0x0
15:13	RESERVED			
12:0	OFF_TH	Jumbo Shared based threshold for turn off flow control	RW	0x0

## FC\_JUMBO\_P\_HI\_TH

REGISTER ADDRESS : 0xBB023134

DEFAULT VALUE : 0x41A0348

Specify jumbo mode per port high on/off threshold when flow control on.

Bits	Field	Description	Type	Default
31:29	RESERVED			
28:16	ON_TH	Jumbo port based threshold for turn on flow control	RW	0x041A
15:13	RESERVED			
12:0	OFF_TH	Jumbo Port based threshold for turn off flow control	RW	0x0348

## FC\_JUMBO\_P\_LO\_TH

REGISTER ADDRESS : 0xBB023138

DEFAULT VALUE : 0x39C0150

Specify jumbo mode per port low on/off threshold when flow control on.

Bits	Field	Description	Type	Default
31:29	RESERVED			
28:16	ON_TH	Jumbo Port based reserved threshold for turn on flow control	RW	0x039C
15:13	RESERVED			
12:0	OFF_TH	Jumbo Port based reserved threshold for turn off flow control	RW	0x0150

## FC\_Q\_EGR\_DROP\_TH

BASE ADDRESS : 0xBB02D000

ARRAY INDEX : 0 - 7

ARRAY OFFSET : 13 bits

DEFAULT VALUE : 0x2BC

This is a One-Dimension Register Field Array. (13 bits per field)

Specify per queue egress drop threshold

Bits	Field	Description	Type	Default
12:0	TH	The threshold of per queue egress drop	RW	0x02BC

## FC\_P\_EGR\_DROP\_TH

BASE ADDRESS : 0xBB02D010

PORT INDEX : 0 - 6

PORT OFFSET : 13 bits



DEFAULT VALUE : 0x1B58

This is a One-Dimension Register Field Array. (13 bits per field)

Specify per port egress drop threshold

Bits	Field	Description	Type	Default
12:0	TH	The threshold of per port egress drop.	RW	0x1B58

## FC\_Q\_EGR\_GAP\_TH

REGISTER ADDRESS : 0xBB02D020

DEFAULT VALUE : 0xA8

Specify per queue egress drop off threshold

Bits	Field	Description	Type	Default
31:13	RESERVED			
12:0	TH	Egress flow control turn off packet gap counter. If egress queue flow control is turn on, ASIC will turn off flow control only while pages using of QUEUE n value is low than (Q_EGR_DROP_TH-Q_EGR_GAP_TH)	RW	0x00A8

## FC\_P\_EGR\_GAP\_TH

REGISTER ADDRESS : 0xBB02D024

DEFAULT VALUE : 0x15E

Specify per port egress drop off threshold

Bits	Field	Description	Type	Default
31:13	RESERVED			
12:0	TH	Egress flow control turn off packet gap counter. If egress port flow control is turn on, ASIC will turn off flow control only while pages using of PORT n value is low than (P_EGR_DROP_TH-P_EGR_GAP_TH)	RW	0x015E

## FC\_P\_Q\_EGR\_DROP\_EN

BASE ADDRESS : 0xBB01C0D8

ARRAY INDEX1 : 0 - 6

ARRAY OFFSET1 : 0x4

ARRAY INDEX2 : 0 - 7

ARRAY OFFSET2 : 1 bit

DEFAULT VALUE : 0x1

This is a Two-Dimension Register Field Array. (1 bit per field)

Specify per port per queue egress drop enable.

Bits	Field	Description	Type	Default
0	TH	Per queue egress drop enable of port. 0b0: enable 0b1: disable	RW	0x1

## FC\_DBG\_CTRL

REGISTER ADDRESS : 0xBB02D028

DEFAULT VALUE : 0x0

Flow control tuning debug control

Bits	Field	Description	Type	Default
31:14	RESERVED			
13:10	PORT_NO	Port number of flow control debugging information latching register address from ????	RW	0x0
9	CLR_TOTAL_PKT CNT		RWAC	0x0
8	CLR_PE_MAX_PAGE_CNT	Clear maximum egress port latch page value	RWAC	0x0
7:0	CLR_Q_MAX_PAGE_CNT	Clear maximum egress queue latch page value	RWAC	0x0

## CLR\_MAX\_USED\_PAGE\_CNT

REGISTER ADDRESS : 0xBB02313C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	CLR_MAX_USED_PAGE_CNT	Clear maximum latch page value	RWAC	0x0

## FC\_TOTAL\_PAGE\_CNT

REGISTER ADDRESS : 0xBB02D02C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	TOTAL_PAGE_CNT		RO	0x0

## FC\_PE\_USED\_PAGE\_CNT

BASE ADDRESS : 0xBB02D030  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Specify per egress port used page count include maximum and dynamic used page count.

Bits	Field	Description	Type	Default
31:29	RESERVED			
28:16	PE_MAX_USED_PAGE_CNT	This register can latch the maximum used page count of egress port.	RO	0x0
15:13	RESERVED			
12:0	PE_USED_PAGE_CNT	This register can indicate dynamic used page count of egress port.	RO	0x0

## FC\_Q\_USED\_PAGE\_CNT

BASE ADDRESS : 0xBB02D04C  
 ARRAY INDEX1 : 0 - 5  
 ARRAY OFFSET1 : 0x20  
 ARRAY INDEX2 : 0 - 7  
 ARRAY OFFSET2 : 0x4  
 DEFAULT VALUE : 0x0

This is a Two-Dimension Common Register Array.

Specify the output queue used page count include maximum and dynamic used page count.

Port array index

0-3:UTP

4:EXT MAC

5:CPU MAC

Bits	Field	Description	Type	Default
31:29	RESERVED			
28:16	Q_MAX_USED_PAGE_CNT	maximum used page counts for output queue on each port.	RO	0x0
15:13	RESERVED			
12:0	Q_USED_PAGE_CNT	Dynamic used page counts for output queue on each port.	RO	0x0

## FC\_TL\_USED\_PAGE\_CNT

REGISTER ADDRESS : 0xBB023140

DEFAULT VALUE : 0x0

Specify total used page count include maximum and dynamic used page count.

Bits	Field	Description	Type	Default
31:29	RESERVED			
28:16	TL_MAX_USED_PAGE_CNT	This register can latch the maximum total used page count.	RC	0x0
15:13	RESERVED			
12:0	TL_USED_PAGE_CNT	This register can indicate the total used page count dynamic.	RO	0x0

## FC\_PUB\_USED\_PAGE\_CNT

REGISTER ADDRESS : 0xBB023144

DEFAULT VALUE : 0x0

Specify public used page count include maximum and dynamic used page count.

Bits	Field	Description	Type	Default
31:29	RESERVED			
28:16	PUB_MAX_USED_PAGE_CNT	This register can latch the maximum public used page count.	RC	0x0
15:13	RESERVED			
12:0	PUB_USED_PAGE_CNT	This register can indicate the public used page count dynamic.	RO	0x0

## FC\_PUB\_FCOFF\_USED\_PAGE\_CNT

REGISTER ADDRESS : 0xBB023148

DEFAULT VALUE : 0x0

Specify public used page count include maximum and dynamic used page count when flow control off.

Bits	Field	Description	Type	Default
31:29	RESERVED			
28:16	PUB_FCOFF_MAX_USED_PAGE_CNT	This register can latch the maximum public used page count in dropping mode	RC	0x0
15:13	RESERVED			
12:0	PUB_FCOFF_USED_PAGE_CNT	This register can indicate the public used page count dynamic in dropping mode	RO	0x0

Bits	Field	Description	Type	Default
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## FC\_PUB\_JUMBO\_USED\_PAGE\_CNT

REGISTER ADDRESS : 0xBB02314C

DEFAULT VALUE : 0x0

Specify public used page count include maximum and dynamic used page count in jumbo mode

Bits	Field	Description	Type	Default
31:29	RESERVED			
28:16	PUB_JUMBO_MAX_USED_PAGE_CNT	This register can latch the maximum public used page count in jumbo mode	RC	0x0
15:13	RESERVED			
12:0	PUB_JUMBO_USED_PAGE_CNT	This register can indicate the public used page count dynamic in jumbo mode	RO	0x0

## FC\_P\_USED\_PAGE\_CNT

BASE ADDRESS : 0xBB023150

PORT INDEX : 0 - 6

PORT OFFSET : 0x4

DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Specify per ingress port used page count include maximum and dynamic used page count.

Bits	Field	Description	Type	Default
31:29	RESERVED			
28:16	P_MAX_USED_PAGE_CNT	This register can latch the maximum used page count of ingress port.	RC	0x0
15:13	RESERVED			
12:0	P_USED_PAGE_CNT	This register can indicate dynamic used page count of ingress port.	RO	0x0

## FC\_P\_DBG\_PKT\_PAGE\_CNT

BASE ADDRESS : 0xBB020038

PORT INDEX : 0 - 6

PORT OFFSET : 0x400

DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Page counter for the newest receiving packet

Bits	Field	Description	Type	Default
31:13	RESERVED			
12:0	PKT_PAGE_CNT	used page count of this receiving packet	RO	0x0

## FC\_PON\_GLB\_HI\_TH

REGISTER ADDRESS : 0xBB02316C

DEFAULT VALUE : 0x7780746

Specify PON MAC global high on/off threshold when flow ctrl on.

Bits	Field	Description	Type	Default
31:29	RESERVED			
28:16	ON_TH	PON MAC System based threshold for turn on flow control	RW	0x0778
15:13	RESERVED			
12:0	OFF_TH	PON MAC System based threshold for turn off flow control	RW	0x0746

## FC\_PON\_GLB\_LO\_TH

REGISTER ADDRESS : 0xBB023170

DEFAULT VALUE : 0x3520320

Specify PON MAC global low on/off threshold when flow ctrl on.

Bits	Field	Description	Type	Default
31:29	RESERVED			
28:16	ON_TH	PON MAC Shared based threshold for turn on flow control	RW	0x0352
15:13	RESERVED			
12:0	OFF_TH	PON MAC Shared based threshold for turn off flow control	RW	0x0320

## FC\_PON\_P\_HI\_TH

REGISTER ADDRESS : 0xBB023174

DEFAULT VALUE : 0x12C00FA

Specify PON MAC per port high on/off threshold when flow control on.

Bits	Field	Description	Type	Default
31:29	RESERVED			
28:16	ON_TH	PON MAC port based threshold for turn on flow control	RW	0x012C
15:13	RESERVED			
12:0	OFF_TH	PON MAC Port based threshold for turn off flow control	RW	0x00FA

## FC\_PON\_P\_LO\_TH

REGISTER ADDRESS : 0xBB023178

DEFAULT VALUE : 0x140014

Specify PON MAC per port low on/off threshold when flow control on.

Bits	Field	Description	Type	Default
31:29	RESERVED			
28:16	ON_TH	PON MAC Port based reserved threshold for turn on flow control	RW	0x0014
15:13	RESERVED			
12:0	OFF_TH	PON MAC Port based reserved threshold for turn off flow control	RW	0x0014

## FC\_PON\_Q\_EGR\_DROP\_IDX

BASE ADDRESS : 0xBB02317C

ARRAY INDEX : 0 - 127

ARRAY OFFSET : 3 bits

DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (3 bits per field)

Specify PON queue egress threshold referenece threshold index

Bits	Field	Description	Type	Default
2:0	IDX	Threshold usage index for PON queue	RW	0x0

## FC\_PON\_Q\_EGR\_DROP\_TH

BASE ADDRESS : 0xBB0231B0

ARRAY INDEX : 0 - 7

ARRAY OFFSET : 13 bits

DEFAULT VALUE : 0xF0

This is a One-Dimension Register Field Array. (13 bits per field)

Specify PON MAC per queue egress drop threshold

Bits	Field	Description	Type	Default
12:0	TH	The threshold of per queue egress drop	RW	0x00F0

## FC\_PON\_Q\_EGR\_GAP\_TH

REGISTER ADDRESS : 0xBB0231C0

DEFAULT VALUE : 0x18

Specify PON MAC per queue egress drop off threshold

Bits	Field	Description	Type	Default
31:13	RESERVED			
12:0	TH	Egress flow control turn off packet gap counter. If egress queue flow control is turn on.	RW	0x0018

## FC\_PON\_Q\_USED\_PAGE\_CTRL

REGISTER ADDRESS : 0xBB0231C4

DEFAULT VALUE : 0x0

Specify control register for PON MAC output queue used page count include maximum and dynamic used page count.

Bits	Field	Description	Type	Default
31:8	RESERVED			
7	CLR_MAX_PAGE_CNT	Clear max. counter	RWAC	0x0
6:0	QID	queue index for queue counter access	RW	0x0

## FC\_PON\_Q\_USED\_PAGE\_CNT

REGISTER ADDRESS : 0xBB0231C8

DEFAULT VALUE : 0x0

Specify the output queue used page count include maximum and dynamic used page count.



Bits	Field	Description	Type	Default
31:29	RESERVED			
28:16	Q_MAX_USED_PAGE_CNT	maximum used page counts for output queue on each port.	RO	0x0
15:13	RESERVED			
12:0	Q_USED_PAGE_CNT	Dynamic used page counts for output queue on each port.	RO	0x0

## TH\_TX\_PREFET

REGISTER ADDRESS : 0xBB02D10C

DEFAULT VALUE : 0x2

Bits	Field	Description	Type	Default
31:8	RESERVED			
7:0	CFG_TH_TX_PREFET	MAC TX prefect page threshold	RW	0x02

## LOW\_QUEUE\_TH

REGISTER ADDRESS : 0xBB02D110

DEFAULT VALUE : 0x1

Bits	Field	Description	Type	Default
31:13	RESERVED			
12:0	LOW_QUEUE_TH	Low queue over threshold for EEE usage	RW	0x0001

## HIGH\_QUEUE\_MSK

BASE ADDRESS : 0xBB02D114

PORT INDEX : 0 - 6

PORT OFFSET : 8 bits

DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (8 bits per field)

Per port high queue mask

Bits	Field	Description	Type	Default
7:0	HIGH_QUEUE_MSK	Per port high queue mask	RW	0x0

## SECTION 8.2

## CONGESTION AVOIDANCE

Congestion Avoidance (include WRED & Egress Drop) module

### SC\_P\_CTRL\_0

BASE ADDRESS : 0xBB02003C  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 0x400  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Specify congestion timer control register.

Bits	Field	Description	Type	Default
31:24	RESERVED			
23:20	CGST_TMR_H	Half duplex Congest timer, unit in seconds	RO	0x0
19:16	CGST_SUST_TMR_LMT_H	Half duplex Congest sustain timer limit, unit in seconds. If CNGST_TMR_H >= CNGST_SUST_TMR_LMT_H, this port will enter special congest state. If CNGST_SUST_TMR_LMT_H!=0, this function is enabled.	RW	0x0
15:8	RESERVED			
7:4	CGST_TMR	Congest timer, unit in seconds.	RO	0x0
3:0	CGST_SUST_TMR_LMT	Congest sustain timer limited, unit in seconds. If CGST_TMR >= CGST_SUST_TMR_LMT, this port will enter Special Congest State. When CGST_SUST_TMR_LMT!=0, special congest function is enabled.	RW	0x0

### SC\_P\_CTRL\_1

REGISTER ADDRESS : 0xBB01D018  
 DEFAULT VALUE : 0x0

Specify congestion timer control register.

Bits	Field	Description	Type	Default
31:7	RESERVED			
6:0	CGST_IND	TX special congest ever occurs	RW1C	0x0

## SECTION 8.3

**PACKET AGING**

Packet Aging module



## CHAPTER 9

# Quality of Service

The chapter describes features related to QoS

### SECTION 9.1

## (IEEE802.1P) PRIORITY

(IEEE802.1p) Priority module

### SECTION 9.2

## QUEUE MANAGEMENT

Queue Management module

### QOS\_INTPRI\_TO\_QID

BASE ADDRESS : 0xBB01C0F4  
 ARRAY INDEX1 : 0 - 3  
 ARRAY OFFSET1 : 0x4  
 ARRAY INDEX2 : 0 - 7  
 ARRAY OFFSET2 : 3 bits  
 DEFAULT VALUE : 0x0

This is a Two-Dimension Register Field Array. (3 bits per field)

Specify valid queue ID to each internal-priority in different QID mapping table of output queue.

Bits	Field	Description	Type	Default
2:0	PRI_TO_QID	Internal priority mapping to queue ID 0x0 0x7: queue ID 0 7	RW	
The default value is: {0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x0, 0x1, 0x1, 0x1, 0x1, 0x0, 0x0, 0x1, 0x1, 0x2, 0x2, 0x3, 0x3, 0x0, 0x1, 0x2, 0x3, 0x4, 0x5, 0x6, 0x7}				

### QOS\_PORT\_QMAP\_CTRL

BASE ADDRESS : 0xBB01C104  
 PORT INDEX : 0 - 6

PORT OFFSET : 2 bits  
DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (2 bits per field)

Specify output queue number 1 8 to a port.

Bits	Field	Description	Type	Default
1:0	IDX	The index of QID mapping table	RW	0x0

## QOS\_PRI\_REMAP\_IN\_CPU

BASE ADDRESS : 0xBB01C108  
ARRAY INDEX : 0 - 7  
ARRAY OFFSET : 3 bits  
DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (3 bits per field)

Specify internal-priority to packets that normal forwarded to CPU port.

Bits	Field	Description	Type	Default
2:0	PRI	Internal priority mapping to the packets that normal forwarded to CPU.	RW	

### SECTION 9.3

## INGRESS PRIORITY DECISION

Ingress Priority Decision module

## QOS\_1Q\_PRI\_REMAP

BASE ADDRESS : 0xBB01C10C  
ARRAY INDEX : 0 - 7  
ARRAY OFFSET : 3 bits  
DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (3 bits per field)

Specify a 3-bit internal priority for 1Q priority.

Bits	Field	Description	Type	Default
2:0	INTPRI_1Q	802.1Q priority remapping	RW	

## QOS\_DSCP\_REMAP

BASE ADDRESS : 0xBB01C110  
 ARRAY INDEX : 0 - 63  
 ARRAY OFFSET : 3 bits  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (3 bits per field)

Specify a 3-bit internal priority for a DSCP value.

Bits	Field	Description	Type	Default
2:0	INTPRI_DSCP	Remap DSCP to internal priority.	RW	0x0

## QOS\_PB\_PRI

BASE ADDRESS : 0xBB01C12C  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 3 bits  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (3 bits per field)

Specify a 3-bit internal priority for a port.

Bits	Field	Description	Type	Default
2:0	INTPRI_PB	Port-based internal priority.	RW	0x0

## PRI\_SEL\_TBL\_CTRL

REGISTER ADDRESS : 0xBB01C130  
 DEFAULT VALUE : 0x0

Configure priority decision weight values register.

Bits	Field	Description	Type	Default
31:28	SVLAN_WEIGHT	Internal priority decision weight configuration of SVLAN based priority source	RW	0x0
27:24	SA_WEIGHT	Internal priority decision weight configuration of source MAC based priority source	RW	0x0
23:20	LUTFWD_WEIGHT	Internal priority decision weight configuration of Lookup Forward based priority source	RW	0x0
19:16	CVLAN_WEIGHT	Internal priority decision weight configuration of CVLAN based priority source	RW	0x0
15:12	ACL_WEIGHT	Internal priority decision weight configuration of ACL priority source	RW	0x0
11:8	DSCP_WEIGHT	Internal priority decision weight configuration of DSCP based priority source	RW	0x0

Bits	Field	Description	Type	Default
7:4	DOT1Q_WEIGHT	Internal priority decision weight configuration of 802.1Q based priority source	RW	0x0
3:0	PORT_WEIGHT	Internal priority decision weight configuration of port based priority source	RW	0x0

## PRI\_SEL\_TBL\_CTRL2

REGISTER ADDRESS : 0xBB01C134

DEFAULT VALUE : 0x0

Configure priority decision weight values register.

Bits	Field	Description	Type	Default
31:4	RESERVED			
3:0	L4_WEIGHT	Weighted value for L4 Priority Assignment	RW	0x0

### SECTION 9.4

## REMARKING

Remarking module

## RMK\_DOT1Q\_RMK\_EN\_CTRL

BASE ADDRESS : 0xBB020040

PORT INDEX : 0 - 6

PORT OFFSET : 0x400

DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Specify dot1q remarking abilities register.

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	EN	Enable/Disable 1Q remarking for a port. 0b0: disable 0b1: enable	RW	0x0

## RMK\_1Q\_CTRL

BASE ADDRESS : 0xBB0231CC

ARRAY INDEX : 0 - 7

ARRAY OFFSET : 3 bits



DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (3 bits per field)

Configure inner-priority remarking table. Original inner-priority or internal priority can be selected to be table index controlled by IPRI\_RMK\_SRC.

Bits	Field	Description	Type	Default
2:0	INTPRI_1Q	New inner-priority for a inner-priority or a internal priority.	RW	0x0

## RMK\_DSCP\_RMK\_EN\_CTRL

BASE ADDRESS : 0xBB0231D0

PORT INDEX : 0 - 6

PORT OFFSET : 0x4

DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Specify dscp remarking abilities register.

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	EN	Enable/Disable DSCP remarking for egress port. 0b0: disable 0b1: enable	RW	0x0

## RMK\_DSCP\_CTRL

BASE ADDRESS : 0xBB01102C

ARRAY INDEX : 0 - 63

ARRAY OFFSET : 6 bits

DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (6 bits per field)

Configure DSCP remarking table  
must move to file\_Remarking

Bits	Field	Description	Type	Default
5:0	INTPRI_DSCP	New DSCP value for a DSCP value . If RMK_DSCP_CFG.SEL=1.	RW	0x0

## RMK\_DSCP\_INT\_PRI\_CTRL

BASE ADDRESS : 0xBB011060  
 ARRAY INDEX : 0 - 7  
 ARRAY OFFSET : 6 bits  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (6 bits per field)

Configure internal priority to DSCP remarking value table

Bits	Field	Description	Type	Default
5:0	INTPRI_DSCP	New DSCP value for a internal priority. If RMK_DSCP_CFG.SEL=0.	RW	0x0

## RMK\_P\_DSCP\_SEL

BASE ADDRESS : 0xBB02A200  
 ARRAY INDEX : 0 - 6  
 ARRAY OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

Configure DSCP remarking configuration

Bits	Field	Description	Type	Default
0	SEL	DSCP remarking source selection for egress port 0b0:from internal priority 0b1:from original DSCP	RW	0x0

## SECTION 9.5

# SCHEDULING

Scheduling (SP, WRR, WFQ) module

## WFQ\_CTRL

REGISTER ADDRESS : 0xBB02D800  
 DEFAULT VALUE : 0x3FFF

Specify the WFQ related setting

Bits	Field	Description	Type	Default
31:17	RESERVED			
16	WFQ_IFG	Rate calculation include IFG(Inter Frame Gap) setting in WFQ leaky bucket 0b0:exclude IPG 0b1:include IPG	RW	0x0

Bits	Field	Description	Type	Default
15:0	WFQ_BURSTSIZE	Bucket size (high threshold) of WFQ Leaky Bucket, unit bytes	RW	0x3FFF

## EGR\_BWCTRL\_P\_CTRL

BASE ADDRESS : 0xBB02D804

PORT INDEX : 0 - 6

PORT OFFSET : 0x4

DEFAULT VALUE : 0x3FFFE

This is a One-Dimension Port Register Array.

egress bandwidth control per-port control register.

Bits	Field	Description	Type	Default
31:18	RESERVED			
17:1	RATE	Egress Bandwidth Control, unit: 8Kbps (K=1024) 17'h1ffff : BW= full rate (line rate) N : BW=N*8Kbps	RW	0x1FFFF
0	IFG	Bandwidth Control Include/Exclude Preamble & IFG (20 bytes) 0: exclude 1: Include	RW	0x0

## LINE\_RATE\_1G

REGISTER ADDRESS : 0xBB02D820

DEFAULT VALUE : 0x1FFFF

Line rate for 1Gbps

Bits	Field	Description	Type	Default
31:17	RESERVED			
16:0	RATE	Giga line rate control, unit: 8Kbps (K=1024) N : BW=N*8Kbps	RW	0x1FFFF

## LINE\_RATE\_500M

REGISTER ADDRESS : 0xBB02D824

DEFAULT VALUE : 0x0

Line rate for 500M

Bits	Field	Description	Type	Default
31:17	RESERVED			
16:0	RATE	500Mbps line rate control, unit: 8Kbps (K=1024) N : BW=N*8Kbps	RW	0x0

## LINE\_RATE\_100M

REGISTER ADDRESS : 0xBB02D828

DEFAULT VALUE : 0x3333

Line rate for 100M

Bits	Field	Description	Type	Default
31:17	RESERVED			
16:0	RATE	100Mbps line rate control, unit: 8Kbps (K=1024) N : BW=N*8Kbps	RW	0x03333

## LINE\_RATE\_10M

REGISTER ADDRESS : 0xBB02D82C

DEFAULT VALUE : 0x51E

Line rate for 10M

Bits	Field	Description	Type	Default
31:17	RESERVED			
16:0	RATE	10Mbps line rate control, unit: 8Kbps (K=1024) N : BW=N*8Kbps	RW	0x0051E

## OUTPUT\_DROP\_CFG

REGISTER ADDRESS : 0xBB011068

DEFAULT VALUE : 0x6

Output drop configuration

Bits	Field	Description	Type	Default
31:3	RESERVED			
2	OD_BC_SEL	Select broadcast packet type for output drop control 1: select 0: not select	RW	0x1

Bits	Field	Description	Type	Default
1	OD_MC_SEL	Select multicast packet type for output drop control 1: select 0: not select	RW	0x1
0	OD_UC_SEL	Select unknown unicast packet type for output drop control 1: select 0: not select	RW	0x0

## OUTPUT\_DROP\_EN

BASE ADDRESS : 0xBB01106C

PORT INDEX : 0 - 6

PORT OFFSET : 1 bit

DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

Output drop enable configuration

Bits	Field	Description	Type	Default
0	EN	Enable Port output mode 1: Enabled 0 Disabled	RW	0x0

## WFQ\_PORT\_CFG0

BASE ADDRESS : 0xBB02D830

PORT INDEX : 0 - 6

PORT OFFSET : 16 bits

DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (16 bits per field)

WFQ related configuration

Bits	Field	Description	Type	Default
15:0	WEIGHT0	Weight of WFQ0	RW	0x0

## WFQ\_PORT\_CFG1\_7

BASE ADDRESS : 0xBB02D840

ARRAY INDEX1 : 0 - 6

ARRAY OFFSET1 : 0xC

ARRAY INDEX2 : 1 - 7

ARRAY OFFSET2 : 10 bits  
DEFAULT VALUE : 0x0

This is a Two-Dimension Register Field Array. (10 bits per field)

WFQ related configuration

Bits	Field	Description	Type	Default
9:0	WEIGHT1_7	Weight of WFQ1 WFQ7	RW	0x0

## WFQ\_TYPE\_PORT\_CFG

BASE ADDRESS : 0xBB02D894  
ARRAY INDEX1 : 0 - 6  
ARRAY OFFSET1 : 0x4  
ARRAY INDEX2 : 0 - 7  
ARRAY OFFSET2 : 1 bit  
DEFAULT VALUE : 0x0

This is a Two-Dimension Register Field Array. (1 bit per field)

Queue scheduling type

Bits	Field	Description	Type	Default
0	QUEUE_TYPE	WFQ or strict queue type setting 0b0:strict queue type 0b1:WFQ queue type	RW	0x0

## APR\_EN\_PORT\_CFG

BASE ADDRESS : 0xBB02D8B0  
ARRAY INDEX1 : 0 - 6  
ARRAY OFFSET1 : 0x4  
ARRAY INDEX2 : 0 - 7  
ARRAY OFFSET2 : 1 bit  
DEFAULT VALUE : 0x0

This is a Two-Dimension Register Field Array. (1 bit per field)

APR enable configuration

Bits	Field	Description	Type	Default
0	EN	APR leaky bucket functionenable setting 0b0:disable 0b1:enable	RW	0x0

## CPU\_PORT\_RATE\_CFG

REGISTER ADDRESS : 0xBB02D8CC

DEFAULT VALUE : 0x0

bypass PHY line rate limit

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	BYPASS_LINE_RATE	force mode enable of CPU port egress rate	RW	0x0

## APR\_METER\_PORT\_CFG

BASE ADDRESS : 0xBB02D8D0

ARRAY INDEX1 : 0 - 6

ARRAY OFFSET1 : 0x4

ARRAY INDEX2 : 0 - 7

ARRAY OFFSET2 : 3 bits

DEFAULT VALUE : 0x0

This is a Two-Dimension Register Field Array. (3 bits per field)

APR meter index configuration

Bits	Field	Description	Type	Default
2:0	IDX	APR meter index	RW	0x0

## P\_QUEUE\_EMPTY

REGISTER ADDRESS : 0xBB02D11C

DEFAULT VALUE : 0x0

per-port queue FIFO empty status

Bits	Field	Description	Type	Default
31:7	RESERVED			
6:0	EMPTY	Egress port mask which output ports' queue FIFO is empty.	RO	0x0

## MOCIR\_TH\_H

REGISTER ADDRESS : 0xBB02D8EC

DEFAULT VALUE : 0x20E

high threshold for determining total cir satisfied

Bits	Field	Description	Type	Default
31:17	RESERVED			
16:0	MOCIR_TH_H	high threshold for determining total cir satisfied	RW	0x0020E

## MOCIR\_TH\_L

REGISTER ADDRESS : 0xBB02D8F0

DEFAULT VALUE : 0x1F0

low threshold for determining total cir satisfied

Bits	Field	Description	Type	Default
31:17	RESERVED			
16:0	MOCIR_TH_L	low threshold for determining total cir satisfied	RW	0x001F0

## MOCIR\_BPT

REGISTER ADDRESS : 0xBB02D8F4

DEFAULT VALUE : 0x42

bytes per tkn for mocir meter

Bits	Field	Description	Type	Default
31:8	RESERVED			
7:0	MOCIR_BPT	bytes per tkn for mocir meter	RW	0x42

## MOCIR\_FRC\_MD

REGISTER ADDRESS : 0xBB02D8F8

DEFAULT VALUE : 0x0

force mode for determining cir satisfied

Bits	Field	Description	Type	Default
31:0	MOCIR_FRC_MD	force mode for determining cir satisfied	RW	0x0



**MOCIR\_FRC\_VAL**

REGISTER ADDRESS : 0xBB02D8FC

DEFAULT VALUE : 0x0

force value for determining cir satisfied

Bits	Field	Description	Type	Default
31:0	MOCIR_FRC_VAL	force value for determining cir satisfied	RW	0x0

**DBG\_HSA\_EP**

REGISTER ADDRESS : 0xBB02A204

DEFAULT VALUE : 0x0

select which port to store has bus of the last pkt

Bits	Field	Description	Type	Default
31:3	RESERVED			
2:0	DBG_HSA_EP	select which port to store has bus of the last pkt	RW	0x0



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## CHAPTER 10

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# Packet Inspection Engine

The chapter describes features related to PIE

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### SECTION 10.1

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## PIE TEMPLATE

PIE Template module

### ACL\_TEMPLATE\_CTRL

BASE ADDRESS : 0xBB015000  
ARRAY INDEX1 : 0 - 3  
ARRAY OFFSET1 : 0x8  
ARRAY INDEX2 : 0 - 7  
ARRAY OFFSET2 : 7 bits  
DEFAULT VALUE : 0x0

This is a Two-Dimension Register Field Array. (7 bits per field)

ACL template configuration

Bits	Field	Description	Type	Default
6:0	FIELD	Type of field	RW	0x0

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### SECTION 10.2

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## FLOW CLASSIFICATION (FLOW TABLE)

Flow Classification (Flow Table) module

### CF\_OP\_DS

BASE ADDRESS : 0xBB015020  
ARRAY INDEX : 0 - 511  
ARRAY OFFSET : 1 bit  
DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

Classification operation control

Bits	Field	Description	Type	Default
0	NOT_DS	Not operation config for downstream classification rule	RW	0x0

## CF\_OP\_US

BASE ADDRESS : 0xBB015060  
 ARRAY INDEX : 0 - 511  
 ARRAY OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

Classification operation control

Bits	Field	Description	Type	Default
0	NOT_US	Not operation config for upstream classification rule	RW	0x0

## CF\_VALID

BASE ADDRESS : 0xBB0150A0  
 ARRAY INDEX : 0 - 511  
 ARRAY OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

Classification valid control

Bits	Field	Description	Type	Default
0	VALID	Classification valid control	RW	0x0

## CF\_CFG

REGISTER ADDRESS : 0xBB0150E0  
 DEFAULT VALUE : 0x0

Classification function configuration

Bits	Field	Description	Type	Default
31:4	RESERVED			
3	CF_SEL_RGMII_EN	Classification function of RGMII. 0b0: disalbe 0b1: enalbe	RW	0x0

Bits	Field	Description	Type	Default
2	CF_SEL_PON_EN	Classification function of PON 0b0: disable. 0b1: enable	RW	0x0
1:0	CF_US_PERMIT	Permit packet which unmatch upstream classification rules  0b00: permit as normal forward 0b01: permit without PON port forwarding 0b10: drop	RW	0x0

## RMK\_DSCP\_CF\_PRI\_CTRL

BASE ADDRESS : 0xBB0150E4  
 ARRAY INDEX : 0 - 7  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

DCSP Remarking value for classification

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:0	CFPRI_DSCP	New DSCP value for classification priority	RW	0x0

### SECTION 10.3

## INGRESS ACL

The section describes registers related to Ingress ACL

## ACL\_EN

BASE ADDRESS : 0xBB015104  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

ACL block lookup enable configuration.

Bits	Field	Description	Type	Default
0	EN	Per port ACL function enable setting 0b0:disable 0b1:enable	RW	0x0

## ACL\_PERMIT

BASE ADDRESS : 0xBB015108  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

ACL block lookup enable configuration.

Bits	Field	Description	Type	Default
0	PERMIT	Per port permit ACL unmatched packet setting 0b0:drop 0b1:permit	RW	0x0

## ACL\_ACTION

BASE ADDRESS : 0xBB01510C  
 ARRAY INDEX : 0 - 127  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x7F

This is a One-Dimension Common Register Array.

ACL action configuration

Bits	Field	Description	Type	Default
31:8	RESERVED			
7	VALID	Valid configuration bit for each rule 0b0:in-vlaid 0b1:valid and will check rule hit bit	RW	0x0
6	NOT	NOT operation of ACL	RW	0x1
5	INT_CF	Interrupt and classification control	RW	0x1
4	FWD	Forwarding action control	RW	0x1
3	POLICING	Policing action control	RW	0x1
2	PRI	Priority action control	RW	0x1
1	SVLAN	SVLAN action control	RW	0x1
0	CVLAN	CVLAN action control	RW	0x1

## ACL\_CFG

REGISTER ADDRESS : 0xBB01530C  
 DEFAULT VALUE : 0x0

ACL function configuration

Bits	Field	Description	Type	Default
31:9	RESERVED			
8:1	CFHITLATCH	Latch hit ACL index for classification check pattern	RO	0x0
0	MODE	ACL rule format 0b0:144bits with 8 fields template mode 0b1: 80bits with 4 fields + 64 bits with 3 fields template mode	RW	0x0

## SECTION 10.4

## RANGE CHECK (PORT/VLAN/IP/L4PORT)

Range Check (port/vlan/ip/L4port) module

### RNG\_CHK\_VID\_RNG

BASE ADDRESS : 0xBB015310  
 ARRAY INDEX : 0 - 7  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

VID range check configuration

Bits	Field	Description	Type	Default
31:26	RESERVED			
25:24	TYPE	Range checking data type 0x0:non-valid 0x1:CVLAN VID range check 0x2:SVLAN VID range check 0x3:reserved	RW	0x0
23:12	VID_UPPER	VID range upper bound	RW	0x0
11:0	VID_LOWER	VID range lower bound	RW	0x0

### RNG\_CHK\_IP\_RNG

BASE ADDRESS : 0xBB015330  
 ARRAY INDEX : 0 - 7  
 ARRAY OFFSET : 0xC  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

IP range check configuration

Bits	Field	Description	Type	Default
95:67	RESERVED			
66:64	TYPE	Range checking data type 0:non-valid 1:IPv4 SIP range check 2:IPv4 DIP range check 3:IPv6 SIP{31:0} range check 4:IPv6 DIP{31:0} range check 5 7:reserved	RW	0x0
63:32	IP_UPPER	IP range check upper bound IP	RW	0x0
31:0	IP_LOWER	IP range check lower bound IP	RW	0x0

## RNG\_CHK\_L4PORT\_RNG

BASE ADDRESS : 0xBB015390  
 ARRAY INDEX : 0 - 15  
 ARRAY OFFSET : 0x8  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

L4 port range check configuration.

Bits	Field	Description	Type	Default
63:34	RESERVED			
33:32	TYPE	Range checking data type 0x0:non-valid 0x1:soruce port range check 0x2:destination range check 0x3:reserved	RW	0x0
31:16	L4PORT_UPPER	TCP/UDP port upper bound.	RW	0x0
15:0	L4PORT_LOWER	TCP/UDP port lower bound.	RW	0x0

## RNG\_CHK\_PKTLEN\_RNG

BASE ADDRESS : 0xBB015410  
 ARRAY INDEX : 0 - 7  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

L4 packet length range check configuration.

Bits	Field	Description	Type	Default
31:29	RESERVED			



Bits	Field	Description	Type	Default
28	TYPE	Range checking data type 0x0:don't revise the compare result 0x1:revise the compare result	RW	0x0
27:14	PKTLEN_UPPER	Packet length upper bound.	RW	0x0
13:0	PKTLEN_LOWER	Packet length lower bound.	RW	0x0

## RNG\_CHK\_IP\_RNG\_CF

BASE ADDRESS : 0xBB015430  
 ARRAY INDEX : 0 - 7  
 ARRAY OFFSET : 0xC  
 DEFAULT VALUE : 0xFFFFFFFF

This is a One-Dimension Common Register Array.

IP range check configuration for classification

Bits	Field	Description	Type	Default
95:65	RESERVED			
64	TYPE	Range checking data type 0x0:IPv4 SIP range check 0x1:IPv4 DIP range check	RW	0x0
63:32	IP_UPPER	IP range check upper bound IP	RW	0x0
31:0	IP_LOWER	IP range check lower bound IP	RW	0xFFFFFFFF

## RNG\_CHK\_L4PORT\_RNG\_CF

BASE ADDRESS : 0xBB015490  
 ARRAY INDEX : 0 - 7  
 ARRAY OFFSET : 0x8  
 DEFAULT VALUE : 0xFFFF

This is a One-Dimension Common Register Array.

L4 port range check configuration for classification.

Bits	Field	Description	Type	Default
63:33	RESERVED			
32	TYPE	Range checking data type 0x0:soruce port range check 0x1:destination range check	RW	0x0
31:16	L4PORT_UPPER	TCP/UDP port upper bound.	RW	0x0
15:0	L4PORT_LOWER	TCP/UDP port lower bound.	RW	0xFFFF



## CHAPTER 11

# Management

The chapter describes features related to management

### SECTION 11.1

## OAM

OAM module

### OAM\_P\_CTRL\_0

BASE ADDRESS : 0xBB0170B0  
PORT INDEX : 0 - 6  
PORT OFFSET : 2 bits  
DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (2 bits per field)

OAM per-port control register

Bits	Field	Description	Type	Default
1:0	OAM_PARSER	OAM layer PARSER(receiving parsing function) action. 0b00-FWD(default) -Normal process -Forwarding non-OAMPDUs 0b01-LB(loopback) -Looping back non-OAMPDUs -drop CRC and receiving FAILED packets -trap OAMPDUs to CPU 0b10-DISCARD	RW	0x0

### OAM\_P\_CTRL\_1

BASE ADDRESS : 0xBB0170B4  
PORT INDEX : 0 - 6  
PORT OFFSET : 2 bits  
DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (2 bits per field)

OAM per-port control register

Bits	Field	Description	Type	Default
1:0	OAM_MULTIPLEXER	AM MULTIPLEXER(transmitting multiplexing function) action. 0b00 FWD(default) -Normal process -Forwarding non-OAMPDUs 0b01-DISCARD -Discarding non-OAMPDUs 0b10-CPUONLY - Transmitting PDUs from CPU only. 0b11-reserved(as FWD)	RW	0x0

## OAM\_CTRL\_0

REGISTER ADDRESS : 0xBB01C138

DEFAULT VALUE : 0x0

OAM system control register

Bits	Field	Description	Type	Default
31:3	RESERVED			
2:0	OAM_PRIORITY	Trap priority for OAM trapping packets	RW	0x0

## OAM\_CTRL\_1

REGISTER ADDRESS : 0xBB0170B8

DEFAULT VALUE : 0x0

OAM system control register

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	OAM_ENABLE	OAM function enable setting 0b0: disable 0b1: enable OAM function and will trap OAM packet to CPU	RW	0x0

### SECTION 11.2

## UDLD

UDLD module

## SECTION 11.3

**RLDP & RLPP**

RLDP &amp; RLPP module

**RLDP\_CTRL\_0**

REGISTER ADDRESS : 0xBB0231EC

DEFAULT VALUE : 0x0

RLDP protocol control

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	ACT_RUNOUTDSC	RLDP action while descriptors run-out state 1: Not drop RLDP packet besides DSC run out. 0: Drop RLDP packet when DSC run out.	RW	0x0

**RLDP\_CTRL\_1**

REGISTER ADDRESS : 0xBB01A000

DEFAULT VALUE : 0x2

RLDP protocol control

Bits	Field	Description	Type	Default
31:6	RESERVED			
5	TRIG_MODE	RLDP trigger mode 0:SA moving mode 1:Periodically	RW	0x0
4	RESERVED			
3	GEN_RNDM	Request of generating new random number, cleared by hardware	RWAC	0x0
2	CMP_TYPE	Comparing identifier when identifying a loop detection packet 0: Compare SA+ magic number 1: Compare SA+ magic number + identifier	RW	0x0
1	CPU_HANDLE	Loop Detection Protocol is handled by CPU or ASIC 0: Loop Detection Protocol is handled by CPU 1: Loop Detection Protocol is handled by ASIC	RW	0x1
0	EN	Enable/Disable RLDP 0b0: Disable 0b1: Enable	RW	0x0

**RLDP\_CHK\_STS\_CTRL**

REGISTER ADDRESS : 0xBB01A004

DEFAULT VALUE : 0x0

RLDP config in check state

Bits	Field	Description	Type	Default
31:24	RESERVED			
23:8	PERIOD	Interval between two retries in checking state(Unit: ms)	RW	0x0
7:0	CNT	Number of re-send Loop Detection Packet in checking state	RW	0x0

## RLDP\_LP\_STS\_CTRL

REGISTER ADDRESS : 0xBB01A008

DEFAULT VALUE : 0x0

RLDP config in looped state

Bits	Field	Description	Type	Default
31:24	RESERVED			
23:8	PERIOD	Interval between two retries in looped state(Unit: ms)	RW	0x0
7:0	CNT	Number of re-send Loop Detection Packet in looped state	RW	0x0

## RLDP\_RNDM\_NUM

REGISTER ADDRESS : 0xBB01A00C

DEFAULT VALUE : 0x0

RLDP random number config

Bits	Field	Description	Type	Default
63:48	RESERVED			
47:32	NUM_47_32	RLDP random number bits{47:32}	RO	0x0
31:0	NUM_31_0	RLDP random number bits{31:0}	RO	0x0

## RLDP\_MAGIC\_NUM

REGISTER ADDRESS : 0xBB01A014

DEFAULT VALUE : 0x0

RLDP magic number config

Bits	Field	Description	Type	Default
63:48	RESERVED			
47:32	NUM_47_32	RLDP magic number bits{47:32}	RW	0x0
31:0	NUM_31_0	RLDP magic number bits{31:0}	RW	0x0

## RLDP\_PORT\_TX\_EN

BASE ADDRESS : 0xBB01A01C  
 PORT INDEX : 0 - 5  
 PORT OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

RLDP packet transmit control of port 0-4

Bits	Field	Description	Type	Default
0	EN	per-port enable/disable TX RLDP packets 0b0: Disable 0b1: Enable	RW	0x0

## RLDP\_PORT\_LP\_ENTER\_STS

BASE ADDRESS : 0xBB01A020  
 PORT INDEX : 0 - 5  
 PORT OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

RLDP enter looped state of port 0-4

Bits	Field	Description	Type	Default
0	STS	Port status enter looped, write 1 to clear	RW1C	0x0

## RLDP\_PORT\_LP\_LEAVE\_STS

BASE ADDRESS : 0xBB01A024  
 PORT INDEX : 0 - 5  
 PORT OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

RLDP leave looped state of port 0-4

Bits	Field	Description	Type	Default
0	STS	Port status leave looped, write 1 to clear	RW1C	0x0

## RLDP\_PORT\_LP\_STS

BASE ADDRESS : 0xBB01A028

PORT INDEX : 0 - 5

PORT OFFSET : 1 bit

DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

RLDP looping state of port 0-4

Bits	Field	Description	Type	Default
0	STS	Port status in looping	RO	0x0

## RLDP\_PORT\_CPU\_LP\_STS

BASE ADDRESS : 0xBB01A02C

PORT INDEX : 0 - 5

PORT OFFSET : 1 bit

DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

RLDP forced looping state by CPU control of port 0-4

Bits	Field	Description	Type	Default
0	STS	Loop status port mask configuration by CPU 0n0: Non-looping 0b1:Looping	RW	0x0

## RLDP\_PORT\_LP\_PNUM

BASE ADDRESS : 0xBB01A030

PORT INDEX : 0 - 5

PORT OFFSET : 3 bits

DEFAULT VALUE : 0x0



This is a One-Dimension Register Field Array. (3 bits per field)

RLDP looped port number of port 0-4

Bits	Field	Description	Type	Default
2:0	P_NUM	per-port looped port number	RO	0x0

## RLPP\_CTRL

REGISTER ADDRESS : 0xBB01A034

DEFAULT VALUE : 0x0

RLPP protocol control

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	TRAP_EN	Trap Loop Prevention Protocol to CPU 0: Disable 1: Enable	RW	0x0

SECTION 11.4

## CODE PROTECTION

Code Protection module



## CHAPTER 12

# Private

The chapter describes features used internally

### SECTION 12.1

## PARSER HSB

Parser HSB module

### HSB\_CTRL

REGISTER ADDRESS : 0xBB028000

DEFAULT VALUE : 0x0

Control register to access HSB data

Bits	Field	Description	Type	Default
31:5	RESERVED			
4:2	LATCH_MODE	HSB_DATA latched method 0x0: all latch 0x1: non-latch 0x2: latch first Drop 0x3: latch first Pass 0x4: latch first trap to CPU 0x5: latch drop pkt 0x6: latch trap to CPU 0x7: latch for ACL action	RW	0x0
1	SEL	0x0 indicate HSB derive from RX parser 0x1 indicate HSB derive from HSB_DATA0 HSB_DATA18	RW	0x0
0	VALID	0x1 indicates send HSB_DATA0 HSB_DATA18 to ALE	RWAC	0x0

### HSB\_DATA

BASE ADDRESS : 0xBB028040

ARRAY INDEX : 0 - 19

ARRAY OFFSET : 0x4

DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

Control register to access HSB data

Bits	Field	Description	Type	Default
31:0	DATA	HSB access data	RW	0x0

## HSB\_DATA\_TABLE

TABLE TYPE : 0x0

TABLE INDEX : 0 - 0

HSB access data

Bits	Field	Description
588:586	SPA	Source Port ID
585:570	USER_FIELD_15	user define field 15
569:554	USER_FIELD_14	user define field 14
553:538	USER_FIELD_13	user define field 13
537:522	USER_FIELD_12	user define field 12
521:506	USER_FIELD_11	user define field 11
505:490	USER_FIELD_10	user define field 10
489:474	USER_FIELD_9	user define field 9
473:458	USER_FIELD_8	user define field 8
457:442	USER_FIELD_7	user define field 7
441:426	USER_FIELD_6	user define field 6
425:410	USER_FIELD_5	user define field 5
409:394	USER_FIELD_4	user define field 4
393:378	USER_FIELD_3	user define field 3
377:362	USER_FIELD_2	user define field 2
361:346	USER_FIELD_1	user define field 1
345:330	USER_FIELD_0	user define field 0
329:314	USER_VALID	valid user field mask
313	IP6_HN_RG	IP6 with routing/hop-by-hop next header
312	CKS_OK_L4	L4 checksum is ok
311	CKS_OK_L3	IP checksum is ok
310	TTL_GT1	TTL > 1
309	TTL_GT5	TTL >5
308	GRE_IF	Is GRE
307	ICMP_IF	Is ICMP
306	UDP_IF	Is UDP
305	TCP_IF	Is TCP
304:289	PPPOE_SESSION	PPPoE section id
288:257	DIP	DIP
256:225	SIP	SIP

Bits	Field	Description
224:217	TOS_DSCP	TOS or DSCP
216:215	IP_TYPE	IP type 0b00: not IP packet 0b01: IPv4 packet 0b10: IPv6 packet 0b11: IPv6 Multicast packet
214	PTP_IF	Has PTP header
213	OMAPDU	OAM control frame
212	RLPP_IF	Is RLPP
211	RLDP_IF	Is RLDP
210	LLC_OTHER	Is LLC others
209	PPPOE_IF	Has PPPoE header
208	SNAP_IF	Has snap
207:192	ETHER_TYPE	Ether type
191:176	CTAG	C-tag field
175	CTAG_IF	Has C-Tag
174:159	STAG	S-tag field
158	STAG_IF	Has S-Tag
157	CPUTAG_L3C	Need L3 checksum egress re-calculation
156	CPUTAG_L4C	Need L4 checksum egress re-calculation
155:150	CPUTAG_TXPMSK	Forced forwarding portmask
149	CPUTAG_EFID_EN	enable EFID
148:146	CPUTAG_EFID	EFID
145	CPUTAG_PRISEL	enable CPU-tag priority decision
144:142	CPUTAG_PRI	CPU-tag priority
141	CPUTAG_KEEP	Keep egress packet as payload
140	CPUTAG_VSEL	Forwarding VLAN decision
139	CPUTAG_DISLRN	Disable L2 learning
138	CPUTAG_PSEL	enable forced PON SID assign
137:136	RESERVED	
135	L34KEEP	
134	RESERVED2	
133:131	CPUTAG_EXTSPA	Extension port source address
130:129	CPUTAG_PPPOE_ACT	PPPoE action
128:126	CPUTAG_PPPOE_IDX	PPPoE reference index
125	CPUTAG_L2BR	L2 bridge
124:118	CPUTAG_PON_SID	PON stream ID
117	CPUTAG_IF	Has CPU Tag
116:69	SA	Source MAC address
68:21	DA	Destination MAC address
20:14	PON_IDX	GPON GemPortId or EPON LLID
13:0	PKT_LEN	Packet length (Include CRC)

## SECTION 12.2

## HSM

HSM module

## SECTION 12.3

## MODIFIER HSA

Modifier HSA module

### HSA\_DATA

BASE ADDRESS : 0xBB0280C0  
 ARRAY INDEX : 0 - 12  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

Control register to access HSA data

Bits	Field	Description	Type	Default
31:0	DATA	HSA access data	RW	0x0

### HSA\_DATA\_NAT

TABLE TYPE : 0x0  
 TABLE INDEX : 0 - 0

HSA access data

Bits	Field	Description
390:378	RNG_NHSAB_ENDSC	
377:365	RNG_NHSAB_BGDSC	
364:340	RNG_NHSAB_QID	
339:312	RNG_NHSAB_RESERVE	
311:309	RNG_NHSAB_CPUPRI	
308:301	RNG_NHSAB_FWDRSN	
300:294	RNG_NHSAB_PON_SID	
293:288	RNG_NHSAB_EXT_MASK	
287:274	RNG_NHSAB_DPM	
273:271	RNG_NHSAB_SPA	
270:257	RNG_NHSAB_PKTLEN	
256:250	RNG_NHSAC_UNTAGSET	
249:246	RNG_NHSAC_CTAG_ACT	
245	RNG_NHSAC_VIDZERO	

Bits	Field	Description
244	RNG_NHSAC_PRITAG_IF	
243	RNG_NHSAC_CTAG_IF	
242:231	RNG_NHSAC_VID	
230	RNG_NHSAC_CFI	
229:227	RNG_NHSAC_PRI	
226	RNG_NHSAS_STAG_IF	
225	RNG_NHSAS_STAG_TYPE	
224	RNG_NHSAS_SP2S	
223	RNG_NHSAS_DEI	
222	RNG_NHSAS_VIDSEL	
221	RNG_NHSAS_FRCTAG	
220	RNG_NHSAS_FRCTAG_IF	
219:208	RNG_NHSAS_SVID	
207:202	RNG_NHSAS_SVIDX	
201:199	RNG_NHSAS_PKT_SPRI	
198:196	RNG_NHSAS_SPRI	
195:175	RNG_NHSAM_USER_PRI	
174:172	RNG_NHSAM_1P_REM	
171	RNG_NHSAM_1P_REM_EN	
170:165	RNG_NHSAM_DSCP_REM	
164	RNG_NHSAM_DSCP_REM_EN	
163	RNG_NHSAF_REGEN_CRC	
162	RNG_NHSAF_CPUKEEP	
161	RNG_NHSAF_KEEP	
160	RNG_NHSAF_PTP	
159	RNG_NHSAF_TCP	
158	RNG_NHSAF_UDP	
157	RNG_NHSAF_IPV4	
156	RNG_NHSAF_IPV6	
155	RNG_NHSAF_RFC1042	
154	RNG_NHSAF_PPPOE_IF	
153	RNG_NHSAN_L3R	
152	RNG_NHSAN_ORG	
151	RNG_NHSAN_IPMC	
150	RNG_NHSAN_L2TRANS	
149	RNG_NHSAN_L34TRANS	
148	RNG_NHSAN_SRC_MOD	1: Modify SIP/SPORT, 0: Modify DIP/DPORT
147:145	RNG_NHSAN_PPPOE_IDX	lookup from ale34 about pppoe session to tx, out 16bits session ID
144:143	RNG_NHSAN_PPPOE_ACT	0: Intact, 1: insert, 2: remove, 3: modify
142:140	RNG_NHSAN_SMAC_IDX	lookup from ale34 about source mac to tx, out 48bits mac
139:124	RNG_NHSAN_L3CKSUM	
123:108	RNG_NHSAN_L4CKSUM	
107:76	RNG_NHSAN_NEWIP	

Bits	Field	Description
75:60	RNG_NHSAN_NEWPORT	
59:12	RNG_NHSAN_NEWDMAC	when SID==127, means OMCI packet, then bit7 0 mean packet type, and bit23 8 means the packet length in OMCI header
11:7	RNG_NHSAN_TTLM1_EXTM ASK	
6:0	RNG_NHSAN_TTLM1_PMAS K	

## HSA\_DATA\_TABLE

TABLE TYPE : 0x0

TABLE INDEX : 0 - 0

HSA access data

Bits	Field	Description
390:378	RNG_NHSAB_ENDSC	
377:365	RNG_NHSAB_BGDSC	
364:340	RNG_NHSAB_QID	
339:312	RNG_NHSAB_RESERVE	
311:309	RNG_NHSAB_CPUPRI	
308:301	RNG_NHSAB_FWDRSN	
300:294	RNG_NHSAB_PON_SID	
293:288	RNG_NHSAB_EXT_MASK	
287:274	RNG_NHSAB_DPM	
273:271	RNG_NHSAB_SPA	
270:257	RNG_NHSAB_PKTLEN	
256:250	RNG_NHSAC_UNTAGSET	
249:246	RNG_NHSAC_CTAG_ACT	
245	RNG_NHSAC_VIDZERO	
244	RNG_NHSAC_PRITAG_IF	
243	RNG_NHSAC_CTAG_IF	
242:231	RNG_NHSAC_VID	
230	RNG_NHSAC_CFI	
229:227	RNG_NHSAC_PRI	
226	RNG_NHSAS_STAG_IF	
225	RNG_NHSAS_STAG_TYPE	
224	RNG_NHSAS_SP2S	
223	RNG_NHSAS_DEI	
222	RNG_NHSAS_VIDSEL	
221	RNG_NHSAS_FRCTAG	
220	RNG_NHSAS_FRCTAG_IF	
219:208	RNG_NHSAS_SVID	
207:202	RNG_NHSAS_SVIDX	



Bits	Field	Description
201:199	RNG_NHSAS_PKT_SPRI	
198:196	RNG_NHSAS_SPRI	
195:175	RNG_NHSAM_USER_PRI	
174:172	RNG_NHSAM_IP_REM	
171	RNG_NHSAM_IP_REM_EN	
170:165	RNG_NHSAM_DSCP_REM	
164	RNG_NHSAM_DSCP_REM_EN	
163	RNG_NHSAF_REGEN_CRC	
162	RNG_NHSAF_CPUKEEP	
161	RNG_NHSAF_KEEP	
160	RNG_NHSAF_PTP	
159	RNG_NHSAF_TCP	
158	RNG_NHSAF_UDP	
157	RNG_NHSAF_IPV4	
156	RNG_NHSAF_IPV6	
155	RNG_NHSAF_RFC1042	
154	RNG_NHSAF_PPPOE_IF	
153:89	RNG_NHSAP_PTP_RESV	
88:82	RNG_NHSAP_PTP_ID	
81:80	RNG_NHSAP_PTP_ACT	0: No action, 1: Latch Timestamp(set PTP_P_TX_TIME_VALID to 1), 2: Latch Timestamp and TX mirror to CPU(set PTP_P_TX_TIME_VALID to 1), 3: Modify Correlation field
79:32	RNG_NHSAP_PTP_SEC	
31:0	RNG_NHSAP_PTP_NSEC	

#### SECTION 12.4

### DEBUGGING (ALE, LOOPBACK, DROP MECHANISM, FC AND QM)

Debugging (ALE, Loopback, Drop Mechanism, FC and QM) module

#### DBG\_BLK\_SEL

REGISTER ADDRESS : 0xBB0001C8

DEFAULT VALUE : 0x0

Debug block select

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	DBG_BLK_SEL	debug block select	RW	0x0

## PORT\_VM\_EN

BASE ADDRESS : 0xBB020044  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 0x400  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

enable port gmii like function (virtual MAC function)

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	PORT_VM_EN	enable port gmii like function	RW	0x0

## PORT\_VM\_RX

BASE ADDRESS : 0xBB020048  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 0x400  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

rx clk toggle once when PORT\_VM\_RX is write (virtual MAC function)

Bits	Field	Description	Type	Default
31:9	RESERVED			
8	PORT_VM_RXDV	gmii rxdv	RW	0x0
7:0	PORT_VM_RXD	gmii rxd	RW	0x0

## PORT\_VM\_TX

BASE ADDRESS : 0xBB02004C  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 0x400  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

tx clk toggle once when PORT\_VM\_TX is read (virtual MAC function)

Bits	Field	Description	Type	Default
31:9	RESERVED			
8	PORT_VM_TXEN	gmii txen	RO	0x0
7:0	PORT_VM_TXD	gmii txd	RO	0x0

Bits	Field	Description	Type	Default
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## SECTION 12.5

## SMART PACKET GENERATOR

Smart Packet Generator module

### SPG\_GLB\_CTRL

REGISTER ADDRESS : 0xBB0231F0

DEFAULT VALUE : 0xFFFF0000

Global smart packet generator control.

Bits	Field	Description	Type	Default
31:16	PAUSE_TIME	To set the pause timer which will affect the pause frame	RW	0xFFFF
15:3	RESERVED			
2	BYPASS_FC_MODE	Packet generator bypass flow control 0b0: Disable 0b1: Enable	RW	0x0
1	CMD_STOP	Stop the smart packet generator function for whole system. 0b0: Disable 0b1: Enable	RW	0x0
0	CMD_START	Start the smart packet generator function for whole system. 0b0: Disable 0b1: Enable	RW	0x0

### SPG\_PORT\_TX\_GRP\_CTRL

BASE ADDRESS : 0xBB020050

PORT INDEX : 0 - 6

PORT OFFSET : 0x400

DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Smart packet generator per-port tx enable control.

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	GRP_TX_PORT	Port mask for TX group.  0b0: Disable 0b1: Enable	RW	0x0

## SPG\_PORT\_STS

BASE ADDRESS : 0xBB020054  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 0x400  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Smart packet generator per-port tx done status.

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	TX_DONE_PORT	TX ports transmits finish flag. 0b0: normal 0b1: TX finished. (Only for TO-TAL_PKT_COUNT!=0)	RC	0x0

## SPG\_P\_TX\_GRP\_CTRL

BASE ADDRESS : 0xBB020058  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 0x400  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Smart packet generator per-port tx enable control.

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	TX_FIRST	Packet generator priority is higher than normal packet. 0b0 : Normal packet first. 0b1 : Packet generator first.	RW	0x0
14	STS_GEN	Port Packet Gen Status	RO	0x0
13	STS_BUSY	Packet generator busy status.	RO	0x0
12	CMD_SUSPEND	Suspend packet genertor	RWAC	0x0
11	MODE_LEN_SEL	Packet Generator length field as P_TX_LEN 0b0:Payload 0b1:Packet Length	RW	0x0
10	MODE_RANDOM_LEN	Enable sending random length of packets between BYTE_LENGTH and MAX_LENGTH while PKG in continue mode.	RW	0x0
9	RESERVED			
8	MODE_BCINC	0b0: Fixed byte count. 0b1: Enable incremental or random byte count	RW	0x0
7	MODE_SAINC	0b0: Disable incremental SA. 0b1: Enable incremental SA.	RW	0x0

Bits	Field	Description	Type	Default
6	MODE_DAINC	0b0: Disable incremental DA. 0b1: Enable incremental DA.	RW	0x0
5	MODE_RANDOM	0b0: Fixed data. 0b1: Random data.	RW	0x0
4	MODE_CRC	0b0: Transmit packets with CRC error. 0b1: Transmit packets without CRC error.	RW	0x0
3	CMD_STOP	Stop packet generator, write 1 to stop and clear to 0 by asic.	RWAC	0x0
2	MODE_CONTINUE	0b0: disable continues transmit 0b1: enable continues transmit	RW	0x0
1	MODE_PAUSE	0b0: pause off packet flag. 0b1: pause on packet flag.	RW	0x0
0	CMD_START	Start packet generator, write 1 to start and clear to 0 by asic.	RWAC	0x0

## SPG\_P\_LEN\_CTRL

BASE ADDRESS : 0xBB02005C  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 0x400  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Smart packet generator per-port tx length control.

Bits	Field	Description	Type	Default
31:30	RESERVED			
29:16	MAX_LEN	Max packet size for transmitting out	RW	0x0
15:14	RESERVED			
13:0	BYTE_LEN	Transmit length in byte (minimum packet size)	RW	0x0

## SPG\_P\_TX\_CNT

BASE ADDRESS : 0xBB020060  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 0x400  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Smart packet generator per-port tx counter

Bits	Field	Description	Type	Default
31:24	RESERVED			

Bits	Field	Description	Type	Default
23:0	CNT	Transmit packet counter	RW	0x0

## SPG\_P\_SA

BASE ADDRESS : 0xBB020064  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 0x400  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Smart packet generator per-port transmit SA

Bits	Field	Description	Type	Default
63:48	RESERVED			
47:32	MAC_47_32	Initial SA{47:32}	RW	0x0
31:0	MAC_31_0	Initial SA{31:0}	RW	0x0

## SPG\_P\_DA

BASE ADDRESS : 0xBB02006C  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 0x400  
 DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Smart packet generator per-port transmit DA

Bits	Field	Description	Type	Default
63:48	RESERVED			
47:32	MAC_47_32	Initial DA{47:32}	RW	0x0
31:0	MAC_31_0	Initial DA{31:0}	RW	0x0

## SPG\_PAYLOAD

BASE ADDRESS : 0xBB0231F4  
 ARRAY INDEX : 0 - 47  
 ARRAY OFFSET : 8 bits  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (8 bits per field)

Smart packet generator user define payload

Bits	Field	Description	Type	Default
7:0	PAYLOAD	User define payload for smart packet generation. If payload of packet is over 48 bytes, PKG will turn-around to fill defined payload	RW	0x0

## SPG\_PORT\_USER\_PKT

BASE ADDRESS : 0xBB020074  
PORT INDEX : 0 - 6  
PORT OFFSET : 0x400  
DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

Smart packet generator per-port user packets latch function enable control.

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	EN	Latch user defined packet in queue 7 setting. 0b0: Disable 0b1: Enable	RW	0x0





## CHAPTER 13

# Layer 3

The chapter describes features related to layer 3

### SECTION 13.1

## L3 ROUTING

L3 unicast routing module

### SECTION 13.2

## IGMP SNOOPING

IGMP snooping module

### IGMP\_MC\_GROUP

BASE ADDRESS : 0xBB01C13C  
ARRAY INDEX : 0 - 63  
ARRAY OFFSET : 0x8  
DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

Specify IP multicast group IP

Bits	Field	Description	Type	Default
63:45	RESERVED			
44:39	EXT_PMSK	Forwarding extension portmask	RW	0x0
38:32	PMSK	Forwarding portmask	RW	0x0
31:28	RESERVED			
27:0	GIP	GIP for IGMP snooping entry	RW	0x0

### IGMP\_GLB\_CTRL

REGISTER ADDRESS : 0xBB011070  
DEFAULT VALUE : 0x0

IGMP snooping global control

Bits	Field	Description	Type	Default
31:8	RESERVED			
7:5	TRAP_PRIORITY	Specify the priority of trapped IGMP/MLD packets	RW	0x0
4	PISO_LEAKY	Port isolation leaky for IGMP/MLD packets 1: Enable Leaky 0: Disable Leaky	RW	0x0
3	VLAN_LEAKY	VLAN leaky for IGMP/MLD packets 1: Enable Leaky 0: Disable Leaky	RW	0x0
2	DISC_STORM_FILTER	Discard packet flow counting in storm filtering control for IGMP/MLD packets 1: Discard storm counting 0: Enable Storm counting	RW	0x0
1:0	CKS_ERR_OP	Checksum error option 0b00: Forward 0b01: Drop 0b10: Trap to CPU 0b11: Reserved	RW	0x0

## IGMP\_P\_CTRL

BASE ADDRESS : 0xBB011074  
 PORT INDEX : 0 - 6  
 PORT OFFSET : 0x4  
 DEFAULT VALUE : 0x400

This is a One-Dimension Port Register Array.

IGMP snooping per-port control

Bits	Field	Description	Type	Default
31:11	RESERVED			
10	ALLOW_MC_DATA	ALLOW_MC_DATA 1: Allow 0: Drop	RW	0x1
9:8	MLDV2_OP	MLDv2 operation control 0b00: Flooding 0b01: Drop 0b10: Trap to CPU 0b11: Reserved	RW	0x0
7:6	MLDV1_OP	MLDv1 operation control 0b00: Flooding 0b01: Drop 0b10: Trap to CPU 0b11: Reserved	RW	0x0
5:4	IGMPV3_OP	IGMPv3 operation control 0b00: Flooding 0b01: Drop 0b10: Trap to CPU 0b11: Reserved	RW	0x0

Bits	Field	Description	Type	Default
3:2	IGMPV2_OP	IGMPv2 operation control 0b00: Flooding 0b01: Drop 0b10: Trap to CPU 0b11: Reserved	RW	0x0
1:0	IGMPV1_OP	IGMPv1 operation control 0b00: Flooding 0b01: Drop 0b10: Trap to CPU 0b11: Reserved	RW	0x0

## SECTION 13.3

## L3 MISC

L3 misc. features

### L34\_GLB\_CFG

REGISTER ADDRESS : 0xBB011090

DEFAULT VALUE : 0x0

L34 Global configuration

Bits	Field	Description	Type	Default
31:3	RESERVED			
2	L34_L2_LOOKUP_MISS_A CT	L34 MAC table lookup miss 0:Drop 1:Trap to CPU	RW	0x0
1	RESERVED			
0	L34_GLOBAL_CFG	L34 global config 0:Disable L34 function 1:Enable L34 function	RW	0x0

### L34\_IPMC\_TRAN\_TBL

BASE ADDRESS : 0xBB02A208

ARRAY INDEX : 0 - 15

ARRAY OFFSET : 0x4

DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

IP multicast translation table

Bits	Field	Description	Type	Default
31:11	RESERVED			

Bits	Field	Description	Type	Default
10:8	NETIF_IDX	The index for Network interface table in L34. Switch ASIC will use this index to get Gateway MAC address, for IP multicast MAC SA translate	RW	0x0
7	EN_SIP_TRANS	Enable SIP translation: 0:No SIP translation 1:SIP translation must be done, only enable for NAT or NAPT	RW	0x0
6:4	EXT_IP_IDX	Index to external IP table this field valid when EN_SIP_TRANS = 1	RW	0x0
3	IS_PPPOE_IF	Is this Interface is PPPoE interface 0:not PPPoE interface 1:PPPoE interface	RW	0x0
2:0	PPPOE_IDX	Index to PPPoE table to get PPPoE session ID this field valid when IS_PPPOE_IF = 1	RW	0x0

### L34\_IPMC\_TTL\_CFG

REGISTER ADDRESS : 0xBB02A248

DEFAULT VALUE : 0x1

L34 TTL -1 Configuration

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	IP_MCST_TTL_1	L34 IP multicast TTL -1 config 0:Disable TTL-1 function 1:Enable TTL-1 function  TTL-1 enable: TTL=0,1 ->routing port not forward, pure L2 switch will forward TTL>1 -> all forward	RW	0x1

### L34\_PORT\_TO\_WAN

BASE ADDRESS : 0xBB011094

ARRAY INDEX1 : 0 - 6

ARRAY OFFSET1 : 0x4

ARRAY INDEX2 : 0 - 7

ARRAY OFFSET2 : 1 bit

DEFAULT VALUE : 0x1

This is a Two-Dimension Register Field Array. (1 bit per field)

Bits	Field	Description	Type	Default
0	PORT_TO_WAN_PERMIT	0:Drop 1: Permit	RW	0x1

### L34\_EXTPORT\_TO\_WAN

BASE ADDRESS : 0xBB0110B0  
 ARRAY INDEX1 : 0 - 4  
 ARRAY OFFSET1 : 0x4  
 ARRAY INDEX2 : 0 - 7  
 ARRAY OFFSET2 : 1 bit  
 DEFAULT VALUE : 0x1

This is a Two-Dimension Register Field Array. (1 bit per field)

Bits	Field	Description	Type	Default
0	EXTPORT_TO_WAN_PERMIT	0:Drop 1: Permit	RW	0x1

### L34\_WAN\_TO\_PORT

BASE ADDRESS : 0xBB0110C4  
 ARRAY INDEX1 : 0 - 6  
 ARRAY OFFSET1 : 0x4  
 ARRAY INDEX2 : 0 - 7  
 ARRAY OFFSET2 : 1 bit  
 DEFAULT VALUE : 0x1

This is a Two-Dimension Register Field Array. (1 bit per field)

Bits	Field	Description	Type	Default
0	WAN_TO_PORT_PERMIT	0:Drop 1: Permit	RW	0x1

### L34\_WAN\_TO\_EXTPORT

BASE ADDRESS : 0xBB0110E0  
 ARRAY INDEX1 : 0 - 4  
 ARRAY OFFSET1 : 0x4  
 ARRAY INDEX2 : 0 - 7  
 ARRAY OFFSET2 : 1 bit

DEFAULT VALUE : 0x1

This is a Two-Dimension Register Field Array. (1 bit per field)

Bits	Field	Description	Type	Default
0	WAN_TO_EXTPORT_PERMIT	0:Drop 1: Permit	RW	0x1

## CHAPTER 14

# Table Access

The chapter describes features related to table access

### SECTION 14.1

## TABLE ACCESS

Table Access module

### TBL\_ACCESS\_CTRL

REGISTER ADDRESS : 0xBB012000

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:22	RESERVED			
21:10	ADDR	Access address for table access (1)L2 access, 4-way hash imply each hash address contain 4 entry, the access address = {1'b0, hash address[8:0], entry[1:0]}. L2 access also include BCAM, BCAM contain 64 entry, the access address = {1'b1, 5'b0, entry bits 5 0}	RW	0x0
9:7	SPA	Port number for get next address	RW	0x0
6:4	ACCESS_METHOD	Lut access method 0b000: with specify MAC/IP(read/write) 0b001: with specify lut address(read/write) 0b010: with specify next lut address(read) 0b011: with specify next lut address (only L2 UC entry, read) 0b100: with specify next lut address (only L2 MC entry, read) 0b101: with specify next lut address (only L3 MC entry, read) 0b110: with specify next lut address (only L2+L3 MC entry, read) 0b111: with specify next lut address (only L2 UC + SPA match entry, read)	RW	0x0
3	CMD_TYPE	Table Read/Write type 0b0:read 0b1:write	RW	0x0

Bits	Field	Description	Type	Default
2:0	TBL_TYPE	table access select see below table 0: LUT 1: CVLAN 2: ACL 3: ACL ACT 4: Classification(128 entries) 5: Classification Action(512 entries)	RW	0x0

## TBL\_ACCESS\_STS

REGISTER ADDRESS : 0xBB012004

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:14	RESERVED			
13	BUSY_FLAG	Busy Flag 0:Access operation is Done 1:Access operation is performing	RO	0x0
12	HIT_STATUS	read or write with specify MAC status 0b0:unhit status, didn't have such specify MAC entry in LUT 0b1:hit, have specify MAC entry already	RO	0x0
11	TYPE	bcam or l2 address 0b0:L2 address 0b1:BCAM address	RO	0x0
10:0	ADDR	Address	RO	0x0

## TBL\_ACCESS\_WR\_DATA

REGISTER ADDRESS : 0xBB012008

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
159:128	DATA4	Data content bits 159 128 of the entry for the specified table.	RW	0x0
127:96	DATA3	Data content bits 127 96 of the entry for the specified table.	RW	0x0
95:64	DATA2	Data content bits 95 64 of the entry for the specified table.	RW	0x0
63:32	DATA1	Data content bits 63 32 of the entry for the specified table.	RW	0x0
31:0	DATA0	Data content bits 31 0 of the entry for the specified table.	RW	0x0

## TBL\_ACCESS\_RD\_DATA



REGISTER ADDRESS : 0xBB01201C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
159:128	DATA4	Data content bits 159 128 of the entry for the specified table.	RO	0x0
127:96	DATA3	Data content bits 127 96 of the entry for the specified table.	RO	0x0
95:64	DATA2	Data content bits 95 64 of the entry for the specified table.	RO	0x0
63:32	DATA1	Data content bits 63 32 of the entry for the specified table.	RO	0x0
31:0	DATA0	Data content bits 31 0 of the entry for the specified table.	RO	0x0

## ACL\_ACTION\_TABLE

TABLE TYPE : 0x3

TABLE INDEX : 0 - 127

ACL action Table

Bits	Field	Description
51	HIT	ACL hit indicator (For Classification Check)
50:49	CFACT	0x0:none 0x1:Stream ID assign 0x2:LLID 0x3:DSL and EXT forward portmask
48:42	CFIDX	Stream ID for PON(7-bits)/LLID(3-bits)/DSL_VIDX(5-bits)
41	ACLINT	ACL interrupt
40:38	PRIACT	Priority action 0x0: ACL Priority 0x1: DSCP Remarking 0x2: 1P Remarking 0x3: Policing 0x4: Logging
37:32	PRIDX	ACL priority(0x0-3bits)/DSCP(0x1-6bits)/1P Priority(0x2-3bits) ./ Shared meter for Policing(5-bits) /Logging Counter MIB index(5-bits)
31:30	FWDACT	ACL forward decision 0x0: Copy frame with ACLPMSK 0x1: Redirect frame with ACLPMSK 0x2: Ingress mirror to ACLPMSK 0x3: Trap to CPU
29:23	FWD_PMSK	forwarding related port mask
22	POLICACT	0x0:Policing 0x1:Logging
21:17	METER_IDX	Share meter or Logging Counter MIB index

Bits	Field	Description
16:14	SACT	SVLAN action 0x0:Ingress SVLAN action(down stream only) 0x1:Egress SVLAN action(replace egress SVID only, both upstream and downstream) 0x2:Using CVID(SVID is C-tag, but S-member is from SVIDX_SACT, unstream only) 0x3:Policing 0x4:Logging 0x5:1p remark 0x6:dscp remark
13:8	SVIDX	SVIDX(6-bits) of SVLAN member configuration/ Shared meter for Policing(5-bits) /Logging Counter MIB index(5-bits)//1P priority(3-bits)/dscp(6-bits)
7:5	CACT	CVLAN action type 0x0:Ingress CVLAN action 0x1:Egress CVLAN action(replace egress CVID only and CVID is inner 4K) 0x2:Using SVID(down stream only) 0x3:Policing 0x4:Logging 0x5:1p remark
4:0	CVIDX	CVIDX(5-bits) of CVLAN member configuration index/Shared meter for Policing(5-bits) /Logging Counter MIB index(5-bits)/1P priority(3-bits)

## ACL\_DATA

TABLE TYPE : 0x2

TABLE INDEX : 0 - 63

ACL rule data bits Table

Bits	Field	Description
144	VALID	Valid bit
143:128	FIELD7	field 7
127:112	FIELD6	field 6
111:96	FIELD5	field 5
95:80	FIELD4	field 4
79:64	FIELD3	field 3
63:48	FIELD2	field 2
47:32	FIELD1	field 1
31:16	FIELD0	field 0
15:9	PMSK	Active port mask
8:2	TAGS	care tags
1:0	TYPE	ACL template number

## ACL\_DATA2

TABLE TYPE : 0x2

TABLE INDEX : 0 - 63

ACL rule data bits Table

Bits	Field	Description
144	VALID	Valid bit
143:128	FIELD3_0	field 3 of Pattern 0
127:112	FIELD2_0	field 2 of Pattern 0
111:96	FIELD1_0	field 1 of Pattern 0
95:80	FIELD0_0	field 0 of Pattern 0
79:73	PMSK_0	Active port mask of Pattern 0
72:66	TAGS_0	care tags of Pattern 0
65:64	TYPE_0	ACL template number of Pattern 0
63:48	FIELD2_1	field 2 of Pattern 1
47:32	FIELD1_1	field 1 of Pattern 1
31:16	FIELD0_1	field 0 of Pattern 1
15:9	PMSK_1	Active port mask of Pattern 1
8:2	TAGS_1	care tags of Pattern 1
1:0	TYPE_1	ACL template number of Pattern 1

## ACL\_MASK

TABLE TYPE : 0x2

TABLE INDEX : 0 - 63

ACL rule mask bits Table

Bits	Field	Description
143:128	FIELD7	field 7
127:112	FIELD6	field 6
111:96	FIELD5	field 5
95:80	FIELD4	field 4
79:64	FIELD3	field 3
63:48	FIELD2	field 2
47:32	FIELD1	field 1
31:16	FIELD0	field 0
15:9	PMSK	Active port mask
8:2	TAGS	care tags
1:0	TYPE	ACL template number

## ACL\_MASK2

TABLE TYPE : 0x2  
TABLE INDEX : 0 - 63

ACL rule mask bits Table

Bits	Field	Description
143:128	FIELD3_0	field 3 of Pattern 0
127:112	FIELD2_0	field 2 of Pattern 0
111:96	FIELD1_0	field 1 of Pattern 0
95:80	FIELD0_0	field 0 of Pattern 0
79:73	PMSK_0	Active port mask of Pattern 0
72:66	TAGS_0	care tags of Pattern 0
65:64	TYPE_0	ACL template number of Pattern 0
63:48	FIELD2_1	field 2 of Pattern 1
47:32	FIELD1_1	field 1 of Pattern 1
31:16	FIELD0_1	field 0 of Pattern 1
15:9	PMSK_1	Active port mask of Pattern 1
8:2	TAGS_1	care tags of Pattern 1
1:0	TYPE_1	ACL template number of Pattern 1

## CF\_ACTION\_DS

TABLE TYPE : 0x5  
TABLE INDEX : 0 - 511

Classification downstream action control table

Bits	Field	Description
56	DSCP_REMARK	0b0: none 0b1:Enable DSCP remarking
55:49	UNI_PMSK	forced forward/flooding port mask bit 0-3:MAC0-3, bit 4:MAC5(RGMII) bit5:MAC6(aka CPU)
48	UNI_ACT	Forced forward port mask 0b0: forwarding member mask to UNI_MASK only 0b1: assign UNI_MASK to forced forwarding
47:45	CF_PRI	Assigned classification priority
44	CFPRI_ACT	Classification priority assignment for packets 0b0:Internal priority follow switch core 0b1:Forced internal priority to CFPRI
43:42	CPRI_ACT	0b00: Assigned to TAG_PRI 0b01: Copy from 1st tag Priority 0b10: Copy from 2nd tag Priority 0b11: Assign from internal priority

Bits	Field	Description
41:40	CVID_ACT	0b00: Assigned to TAG_VID 0b01: Copy from 1st tag VID 0b10: Copy from 2nd tag VID 0b11: Egress CVLAN VID by LUT MAC VID learning
39:37	C_PRI	Assigned C tag P-bits
36:25	C_VID	Assigned C tag VID
24:23	CSPRI_ACT	0b00: Assigned to CSPRI 0b01: Copy from 1st tag P-bits 0b10: Copy from 2nd tag P-bits 0b11: Assign from internal priority
22:21	CSVID_ACT	0b00: Assigned to VID 0b01: Copy from 1st tag VID 0b10: Copy from 2nd tag VID Other:reserved
20:18	CS_PRI	Assigned S tag P-bits
17:6	CS_VID	Assigned S tag VID
5:3	CACT	0b000:nop(following switch-core) 0b001:tagging (reference to CVID_ACT/CPRI_ACT) 0b010:Enable VLAN translation with SP2C table with 1st tag VID(both unmath and unhit will un-Ctag) 0b011: un-tagging 0b100: transparent Other: reserved
2:0	CSACT	0b000:nop(follow switch-core) 0b001:add classification tag which TPID as VS_TPID (reference to CSVID_ACT/CSPRI_ACT) 0b010:add classification tag which TPID as 0x8100 (reference to CSVID_ACT/CSPRI_ACT) 0b011:delete Stag 0b100: transparent 0b101: Enable VLAN translation with SP2C table with 1st tag VID(both unmath and unhit will un-Stag) Other: reserved

## CF\_ACTION\_US

TABLE TYPE : 0x5

TABLE INDEX : 0 - 511

Classification upstream action control table

Bits	Field	Description
63:59	COUNTER_IDX	
58	LOG	0b0:disable logging 0b1:enable logging
57	DROP	0b0:none 0b1:drop
56	DSCP_REMARK	0b0:none 0b1:Enable DSCP remarking
55:49	ASSIGN_IDX	Assigned PON MAC stream ID or QID

Bits	Field	Description
48	SID_ACT	0b0:Assign to SID 0b1:Assign to QID
47:45	CF_PRI	Assigned classification priority
44	CFPRI_ACT	Classification priority assignment for packets 0b0:Internal priority follow switch core 0b1:Forced internal priority to CFPRI
43:42	CPRI_ACT	0b00:Assigned to CPRI 0b01:Copy from 1st tag P-bits (if 1st tag is not existed, then using C_PRI) 0b10:Copy from 2nd tag P-bits (if 2nd tag is not existed, then using C_PRI) 0b11: Assign from internal priority
41:40	CVID_ACT	0b00:Assigned to VID 0b01:Copy from 1st tag VID (if tag 1st is not existed, then using C_VID) 0b10:Copy from 2nd tag VID (if tag 2nd is not existed, then using C_VID) 0b11: Assign from internal VID
39:37	C_PRI	Assigned Ctag P-bits
36:25	C_VID	Assigned Ctag VID
24:23	CSPRI_ACT	0b00:Assigned to CSPRI 0b01:Copy from 1st tag P-bits (if 1st tag is not existed, then using CS_PRI) 0b10: Copy from 2nd tag P-bits (if 2nd tag is not existed, then using CS_PRI) 0b11: Assign from internal priority
22:21	CSVID_ACT	0b00:Assigned to VID 0b01:Copy from 1st tag VID (if 1st tag is not existed, then using CS_VID) 0b10:Copy from 2nd tag VID (if 2nd tag is not existed, then using CS_VID) Other:reserved
20:18	CS_PRI	Assigned Stag P-bits
17:6	CS_VID	Assigned Stag VID
5:3	CACT	0b000:nop 0b001: tagging(reference to CVID_ACT/CPRI_ACT) 0b010:Translation with C2S table, unmatch => SVID of svidx 0 0b011:un-tagging 0b100: transparent Other: reserved
2:0	CSACT	0b000:nop (follow switch-core) 0b001:add classification tag which TPID as VS_TPID (reference to CSVID_ACT/CSPRI_ACT) 0b010:add classification tag which TPID as 0x8100 (reference to CSVID_ACT/CSPRI_ACT) 0b011:delete Stag 0b100: transparent Other: reserved

## CF\_MASK

TABLE TYPE : 0x4  
TABLE INDEX : 0 - 127

Classification rule mask table

Bits	Field	Description
143:128	ETH_TYPE_0	For entry 0-63: IGMP[128], MLD[129], IP4MC[130], IP6MC[131], DEI[132], Reserved[133-143]. For entry 64-128: Ether type
127	U_D_0	Rule of upstream or downstream 0b0:upstream 0b1:downstream
126:119	TOS_GEMIDX_0	Upstream TOS or downstream GEMIDX or LLID
118:107	VID_0	VID of outer tag
106:104	PRI_0	priority of outer tag
103:101	INTER_PRI_0	Internal priority
100	IF_STAG_0	has S-tag
99	IF_CTAG_0	has C-tag
98:96	UNI_0	UNI/UTP port
95	U_D_1	Rule of upstream or downstream 0b0:upstream 0b1:downstream
94:87	TOS_GEMIDX_1	Upstream TOS or downstream GEMIDX or LLID
86:75	VID_1	VID of outer tag
74:72	PRI_1	priority of outer tag
71:69	INTER_PRI_1	Internal priority
68	IF_STAG_1	has S-tag
67	IF_CTAG_1	has C-tag
66:64	UNI_1	UNI/UTP port
63	U_D_2	Rule of upstream or downstream 0b0:upstream 0b1:downstream
62:55	TOS_GEMIDX_2	Upstream TOS or downstream GEMIDX or LLID
54:43	VID_2	VID of outer tag
42:40	PRI_2	priority of outer tag
39:37	INTER_PRI_2	Internal priority
36	IF_STAG_2	has S-tag
35	IF_CTAG_2	has C-tag
34:32	UNI_2	UNI/UTP port
31	U_D_3	Rule of upstream or downstream 0b0:upstream 0b1:downstream
30:23	TOS_GEMIDX_3	Upstream TOS or Downstream SID
22:11	VID_3	VID of outer tag
10:8	PRI_3	priority of outer tag
7:5	INTER_PRI_3	Internal priority
4	IF_STAG_3	has S-tag
3	IF_CTAG_3	has C-tag

Bits	Field	Description
2:0	UNI_3	UNI/UTP port

## CF\_MASK\_L34

TABLE TYPE : 0x4

TABLE INDEX : 0 - 63

Classification rule mask table for L34

Bits	Field	Description
144	VALID	valid bit
143:140	PORT_RNG_CHK_0	L4 port range check bit143: hit L4 port range bit140-142: L4 port range entry index
139:136	IP_RNG_CHK_0	IP range check bit139: hit IP range bit138-136: IP range entry index
135:128	ACL_HIT_0	ACL hit check bit135: hit ACL entry bit134-128: ACL entry index
127	U_D_0	Rule of upstream or downstream 0b0:upstream 0b1:downstream
126:124	WAN_IF_0	egress WAN interface
123	IP6_MC	IPv6 multicast packet
122	IP4_MC	IPv4 multicast packet
121	MLD	MLD control packet
120	IGMP	IGMP control packet
119	DEI	VLAN CFI or SVLAN DEI bit of outer tag
118:107	VID_0	VID of outer tag
106:104	PRI_0	priority of outer tag
103:101	INTER_PRI_0	Internal priority
100	IF_STAG_0	has S-tag
99	IF_CTAG_0	has C-tag
98:96	UNI_0	UNI/UTP port
95	U_D_1	Rule of upstream or downstream 0b0:upstream 0b1:downstream
94:87	TOS_GEMIDX_1	Upstream TOS or downstream GEMIDX or LLID
86:75	VID_1	VID of outer tag
74:72	PRI_1	priority of outer tag
71:69	INTER_PRI_1	Internal priority
68	IF_STAG_1	has S-tag
67	IF_CTAG_1	has C-tag



Bits	Field	Description
66:64	UNI_1	ACL template number
63	U_D_2	Rule of upstream or downstream 0b0:upstream 0b1:downstream
62:55	TOS_GEMIDX_2	Upstream TOS or downstream GEMIDX or LLID
54:43	VID_2	VID of outer tag
42:40	PRI_2	priority of outer tag
39:37	INTER_PRI_2	Internal priority
36	IF_STAG_2	has S-tag
35	IF_CTAG_2	has C-tag
34:32	UNI_2	UNI/UTP port
31	U_D_3	Rule of upstream or downstream 0b0:upstream 0b1:downstream
30:23	TOS_GEMIDX_3	Upstream TOS or downstream GEMIDX or LLID
22:11	VID_3	VID of outer tag
10:8	PRI_3	priority of outer tag
7:5	INTER_PRI_3	Internal priority
4	IF_STAG_3	has S-tag
3	IF_CTAG_3	has C-tag
2:0	UNI_3	UNI/UTP port

## CF\_RULE

TABLE TYPE : 0x4

TABLE INDEX : 0 - 127

Classification rule data table

Bits	Field	Description
144	VALID	valid bit
143:128	ETH_TYPE_0	For entry 0-63: IGMP[128], MLD[129], IP4MC[130], IP6MC[131], DEI[132], Reserved[133-143]. For entry 64-128: Ether type
127	U_D_0	Rule of upstream or downstream 0b0:upstream 0b1:downstream
126:119	TOS_GEMIDX_0	Upstream TOS or downstream GEMIDX or LLID
118:107	VID_0	VID of outer tag
106:104	PRI_0	priority of outer tag
103:101	INTER_PRI_0	Internal priority
100	IF_STAG_0	has S-tag
99	IF_CTAG_0	has C-tag

Bits	Field	Description
98:96	UNI_0	UNI/UTP port
95	U_D_1	Rule of upstream or downstream 0b0:upstream 0b1:downstream
94:87	TOS_GEMIDX_1	Upstream TOS or downstream GEMIDX or LLID
86:75	VID_1	VID of outer tag
74:72	PRI_1	priority of outer tag
71:69	INTER_PRI_1	Internal priority
68	IF_STAG_1	has S-tag
67	IF_CTAG_1	has C-tag
66:64	UNI_1	ACL template number
63	U_D_2	Rule of upstream or downstream 0b0:upstream 0b1:downstream
62:55	TOS_GEMIDX_2	Upstream TOS or downstream GEMIDX or LLID
54:43	VID_2	VID of outer tag
42:40	PRI_2	priority of outer tag
39:37	INTER_PRI_2	Internal priority
36	IF_STAG_2	has S-tag
35	IF_CTAG_2	has C-tag
34:32	UNI_2	UNI/UTP port
31	U_D_3	Rule of upstream or downstream 0b0:upstream 0b1:downstream
30:23	TOS_GEMIDX_3	Upstream TOS or downstream GEMIDX or LLID
22:11	VID_3	VID of outer tag
10:8	PRI_3	priority of outer tag
7:5	INTER_PRI_3	Internal priority
4	IF_STAG_3	has S-tag
3	IF_CTAG_3	has C-tag
2:0	UNI_3	UNI/UTP port

## CF\_RULE\_L34

TABLE TYPE : 0x4

TABLE INDEX : 0 - 63

Classification rule data table for L34

Bits	Field	Description
144	VALID	valid bit

Bits	Field	Description
143:140	PORT_RNG_CHK_0	L4 port range check bit143: hit L4 port range bit140-142: L4 port range entry index
139:136	IP_RNG_CHK_0	IP range check bit139: hit IP range bit138-136: IP range entry index
135:128	ACL_HIT_0	ACL hit check bit135: hit ACL entry bit134-128: ACL entry index
127	U_D_0	Rule of upstream or downstream 0b0:upstream 0b1:downstream
126:124	WAN_IF_0	egress WAN interface
123	IP6_MC	IPv6 multicast packet
122	IP4_MC	IPv4 multicast packet
121	MLD	MLD control packet
120	IGMP	IGMP control packet
119	DEI	VLAN CFI or SVLAN DEI bit of outer tag
118:107	VID_0	VID of outer tag
106:104	PRI_0	priority of outer tag
103:101	INTER_PRI_0	Internal priority
100	IF_STAG_0	has S-tag
99	IF_CTAG_0	has C-tag
98:96	UNI_0	UNI/UTP port
95	U_D_1	Rule of upstream or downstream 0b0:upstream 0b1:downstream
94:87	TOS_GEMIDX_1	Upstream TOS or downstream GEMIDX or LLID
86:75	VID_1	VID of outer tag
74:72	PRI_1	priority of outer tag
71:69	INTER_PRI_1	Internal priority
68	IF_STAG_1	has S-tag
67	IF_CTAG_1	has C-tag
66:64	UNI_1	ACL template number
63	U_D_2	Rule of upstream or downstream 0b0:upstream 0b1:downstream
62:55	TOS_GEMIDX_2	Upstream TOS or downstream GEMIDX or LLID
54:43	VID_2	VID of outer tag
42:40	PRI_2	priority of outer tag
39:37	INTER_PRI_2	Internal priority
36	IF_STAG_2	has S-tag
35	IF_CTAG_2	has C-tag
34:32	UNI_2	UNI/UTP port

Bits	Field	Description
31	U_D_3	Rule of upstream or downstream 0b0:upstream 0b1:downstream
30:23	TOS_GEMIDX_3	Upstream TOS or downstream GEMIDX or LLID
22:11	VID_3	VID of outer tag
10:8	PRI_3	priority of outer tag
7:5	INTER_PRI_3	Internal priority
4	IF_STAG_3	has S-tag
3	IF_CTAG_3	has C-tag
2:0	UNI_3	UNI/UTP port

## L2\_MC\_DSL

TABLE TYPE : 0x0

TABLE INDEX : 0 - 2111

L2 Table (Multicast)

Bits	Field	Description
88	VALID	CAM valid bit
87	NOT_SALEARN	ASIC auto SA learning indicator 0:ASIC auto learning
86	FWDPRI_EN	Enable forwarding priority
85:83	FWDPRI	forwarding priority
82:77	EXT_MBR	extension port member
76:70	MBR	port member
69:62	RESERVED	
61	IVL_SVL	IVL=1 or SVL=0
60	L3LOOKUP	IP Multicast 0b0: Non IP multicast entry 0b1: IP multicast entry
59:48	VID_FID	12-bits VID for IVL 4-bits FID for SVL
47:0	MAC	MAC address

## L2\_UC

TABLE TYPE : 0x0

TABLE INDEX : 0 - 2111

L2 Table (Unicast)

Bits	Field	Description
88	VALID	CAM valid bit
87	NOT_SALEARN	ASIC auto SA learning indicator 0:ASIC auto learning
86	FWDPRI_EN	Enable forwarding priority
85:83	FWDPRI	forwarding priority
82	ARP_USAGE	ARP uage
81:79	EXT_DSL_SPA	DSL or EXT source port address
78	DA_BLK	DA block
77	SA_BLK	SA block
76	AUTH	802.1X MAC-based authorized
75:73	AGE	Aging time
72:70	SPA	source port address
69	SAPRI_EN	SA-based priority enable
68:65	FID	FID
64:62	EFID	Enhanced FID
61	IVL_SVL	IVL=1 or SVL=0
60	L3LOOKUP	IP Multicast 0b0: Non IP multicast entry 0b1: IP multicast entry
59:48	CVID	VID
47:0	MAC	MAC address

### L3\_MC\_DSL

TABLE TYPE : 0x0

TABLE INDEX : 0 - 2111

#### L3 Table (Multicast)

Bits	Field	Description
88	VALID	CAM valid bit
87	NOT_SALEARN	ASIC auto SA learning indicator 0:ASIC auto learning
86	FWDPRI_EN	Enable forwarding priority
85:83	FWDPRI	forwarding priority
82:77	EXT_MBR	extension port member
76:70	MBR	port member
69:62	RESERVED	
61	GIP_ONLY	hash method with GIP only
60	L3LOOKUP	IP Multicast 0b0: Non IP multicast entry 0b1: IP multicast entry
59:28	SIP_VID	Source IP address or CVID

Bits	Field	Description
27:0	GIP	Group IP address

## L3\_MC\_ROUTE

TABLE TYPE : 0x0

TABLE INDEX : 0 - 2111

L3 Table (Multicast)

Bits	Field	Description
88	VALID	CAM valid bit
87	NOT_SALEARN	ASIC auto SA learning indicator 0:ASIC auto learning
86	FWDPRI_EN	Enable forwarding priority
85:83	FWDPRI	forwarding priority
82:77	EXT_MBR	extension port member
76:70	MBR	port member
69:62	RESERVED	
61	GIP_ONLY	hash method with GIP only
60	L3LOOKUP	IP Multicast 0b0: Non IP multicast entry 0b1: IP multicast entry
59:58	RESERVED	
57	WAN_SA	Enable L3 multicast routing forward
56	EXT_FR	Force L3 multicast route
55:28	L3_IDX	WAN interface
27:0	GIP	Group IP address

## VLAN

TABLE TYPE : 0x1

TABLE INDEX : 0 - 4095

VLAN Table

Bits	Field	Description
50:45	EXT_MBR	extension port member
44:29	RESERVED	
28	IVL_SVL	IVL=1 or SVL=0
27:23	METERIDX	meter index for VLAN policing
22	POLICING	VLAN-based policing

Bits	Field	Description
21:19	VBPRI	VLAN-based priority
18	VB_EN	Enable VLAN-based priority
17:14	FID_MSTI	FID or MSTI
13:7	UNTAG	untag set
6:0	MBR	VLAN member





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## CHAPTER 15

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# Miscellaneous

The chapter describes miscellaneous features

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### SECTION 15.1

## SPECIAL TRAP

Specific traps for trapping particular control packets

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### SECTION 15.2

## ETHERNET AV

Ethernet(802.1Qat & 802.1Qav) AV module

### AVB\_PORT\_EN

BASE ADDRESS : 0xBB0110F4  
PORT INDEX : 0 - 6  
PORT OFFSET : 1 bit  
DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

Per port specify EAV mode

Bits	Field	Description	Type	Default
0	EN	per-port EAV mode 0: Disable 1: Enable	RW	0x0

### AVB\_PRI\_REMAP

BASE ADDRESS : 0xBB0110F8  
ARRAY INDEX : 0 - 7  
ARRAY OFFSET : 3 bits  
DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (3 bits per field)

User priority remapping control for EAV egress port

Bits	Field	Description	Type	Default
2:0	PRI	The priority value that is to be used to override user priority for egress port is EAV port	RW	0x0

## SECTION 15.3

## PTP (PRECISION TIME PROTOCOL)

PTP (Precision Time Protocol) module

### PTP\_TIME\_SEC

REGISTER ADDRESS : 0xBB01B034

DEFAULT VALUE : 0x0

current second of PTP reference time clock.

Bits	Field	Description	Type	Default
63:48	RESERVED			
47:32	SEC_47_32	Second bits 47 32 in the reference time clock.	RO	0x0
31:0	SEC_31_0	Second bits 31 0 in the reference time clock.	RO	0x0

### PTP\_TIME\_NSEC

REGISTER ADDRESS : 0xBB01B03C

DEFAULT VALUE : 0x0

current nanosecond of PTP reference time clock.

Bits	Field	Description	Type	Default
31:3	NSEC_UNIT	Nanosecond in the reference time clock. (Unit: 8 nanoseconds)	RO	0x0
2:0	RESERVED			

### PTP\_TIME\_OFFSET\_SEC

REGISTER ADDRESS : 0xBB01B040

DEFAULT VALUE : 0x0

second offset tuning of PTP reference time clock.

Bits	Field	Description	Type	Default
63:48	RESERVED			
47:32	SEC_47_32	offset second bits 47 32 in the reference time clock.	RW	0x0

Bits	Field	Description	Type	Default
31:0	SEC_31_0	offset second bits 31:0 in the reference time clock.	RW	0x0

## PTP\_TIME\_OFFSET\_8NSEC

REGISTER ADDRESS : 0xBB01B048

DEFAULT VALUE : 0x0

nanosecond offset tuning of PTP reference time clock.

Bits	Field	Description	Type	Default
31:3	NSEC_UNIT	offset nanosecond in the reference time clock. (Unit: 8 nanoseconds)	RW	0x0
2:0	RESERVED			

## PTP\_TIME\_FREQ

REGISTER ADDRESS : 0xBB01B04C

DEFAULT VALUE : 0x80000

Configure frequency of PTP system time

Bits	Field	Description	Type	Default
31:27	RESERVED			
26:0	FREQ	Frequency of PTP system time	RW	0x0080000

## PTP\_TIME\_CTRL

REGISTER ADDRESS : 0xBB01B050

DEFAULT VALUE : 0x0

The register can be used to operate the time of reference time clock.

Bits	Field	Description	Type	Default
31:2	RESERVED			
1	PTP_TIME_LATCH	Latch current time to PTP_TIME_SEC and PTP_TIME_NSEC	RWAC	0x0
0	CMD	Enable system time tuning with system offset timer, write to clear	RWAC	0x0

**PTP\_TRANSPARENT\_CFG**

BASE ADDRESS : 0xBB0110FC  
PORT INDEX : 0 - 6  
PORT OFFSET : 1 bit  
DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

The register can be used to control transparent port.

Bits	Field	Description	Type	Default
0	TRANSPARENT_PORT	Transparent active port for PTP messages	RW	0x0

**PTP\_IGR\_MSG\_ACT**

BASE ADDRESS : 0xBB011100  
ARRAY INDEX : 0 - 9  
ARRAY OFFSET : 2 bits  
DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (2 bits per field)

Ingress action config for PTP message class

Bits	Field	Description	Type	Default
1:0	ACT	Action for ingress PTP message class x(0-7) 0b00: none 0b01: trap to CPU with PTP timestamp CPU-tag 0b10: Forward to transparent active port mask 0b11: Forward to transparent active port mask and Rx mirror to CPU with PTP timestamp CPU-tag	RW	0x0

**PTP\_EGR\_MSG\_ACT**

BASE ADDRESS : 0xBB011104  
ARRAY INDEX : 0 - 9  
ARRAY OFFSET : 2 bits  
DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (2 bits per field)

Egress action config for PTP message class

Bits	Field	Description	Type	Default
1:0	ACT	Action foregress PTP message class x(0-7) 0b00: none 0b01: Latch egress timestamp 0b10: Latch egress timestamp and Tx mirror to CPU with PTP timestamp CPU-tag 0b11: Modify correctionField	RW	0x0

## PTP\_MEANPATH\_DEALY

REGISTER ADDRESS : 0xBB01B054

DEFAULT VALUE : 0x0

Calculated PTP mean path delay time

Bits	Field	Description	Type	Default
31	RESERVED			
30:0	DELAY	mean path delay bits 46 16 for correcting	RW	0x0

## PTP\_RX\_TIME

REGISTER ADDRESS : 0xBB011108

DEFAULT VALUE : 0x0

Get the Tx timestamp of the last transmitted PTP packet on a port.

Bits	Field	Description	Type	Default
63:35	RESERVED			
34:32	SEC_2_0	second bits 31 0 of PTP latching time	RW	0x0
31:30	RESERVED			
29:3	NSEC_UNIT	8 nano-second bits of PTP latching time	RW	0x0
2:0	RESERVED			

## PTP\_P\_EN

BASE ADDRESS : 0xBB011110

PORT INDEX : 0 - 6

PORT OFFSET : 0x4

DEFAULT VALUE : 0x0

This is a One-Dimension Port Register Array.

PTP per port state

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	PTP_EN	enable or disable PTP state	RW	0x0

## SECTION 15.4

## PARSER

Configurations related to parser including field selector

### PARSER\_FIELD\_SELECTOR\_CTRL

BASE ADDRESS : 0xBB023224  
 ARRAY INDEX : 0 - 15  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

ACL 16-bits user defined field selector configuration

Bits	Field	Description	Type	Default
31:11	RESERVED			
10:3	OFFSET	Offset in bytes.	RW	0x0
2:0	FMT	Field selector format. It defines the start address for 16-bit data. 0x0:ASIC default setting 0x1: Raw packet(Start after SFDbegin with DA) 0x2: LLC packet(Start after SABegin with length 0000-05FF) 0x3: ARP packet (Start from ARP Ethernet II EtherType 0x0806) 0x4: IPv4 packet (Start from IPv4 header) 0x5: IPv6 packet (Start from IPv6 header) 0x6: IP payload(Start from IP payloadalso means start of layer 4 packet) 0x7: L4 payload (Start after TCP/UDP/ICMP header)	RW	0x0

## CHAPTER 16

# PON MAC

The chapter describes PON MAC features

### SECTION 16.1

## PON MAC SCHEDULING CONFIG

PON MAC Scheduling Configuration and Status

### PON\_CFG

REGISTER ADDRESS : 0xBB02D900

DEFAULT VALUE : 0x20000

PON MAC general control register

Bits	Field	Description	Type	Default
31:19	RESERVED			
18	PON_REV	reserve for feature used	RW	0x0
17	PIR_EXCEED_DROP	0b0:forward exceed PIR rate packet 0b1:drop exceed PIR rate packet	RW	0x1
16:0	EGR_RATE	Egress rate of Ethernet Fiber mode, unit 8Kbps	RW	0x0

### PON\_SID\_TO\_QID

BASE ADDRESS : 0xBB01C33C

ARRAY INDEX : 0 - 127

ARRAY OFFSET : 7 bits

DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (7 bits per field)

QID for Classification SID register

Bits	Field	Description	Type	Default
6:0	QID	QID assignment for PON MAC stream id scheduling packet queueing ID assignment	RW	0x0

**PON\_QID\_CIR\_RATE**

BASE ADDRESS : 0xBB02D904  
ARRAY INDEX : 0 - 127  
ARRAY OFFSET : 17 bits  
DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (17 bits per field)

CIR rate control register

Bits	Field	Description	Type	Default
16:0	RATE	Fiber MAC per-queue CIR rate, unit 64Kpbs	RW	0x0

**PON\_QID\_PIR\_RATE**

BASE ADDRESS : 0xBB02DB04  
ARRAY INDEX : 0 - 127  
ARRAY OFFSET : 17 bits  
DEFAULT VALUE : 0x1FFFF

This is a One-Dimension Register Field Array. (17 bits per field)

PIR rate control register

Bits	Field	Description	Type	Default
16:0	RATE	Fiber MAC per-queue PIR/APR rate, unit 64Kpbs	RW	0x1FFFF

**PON\_SCH\_QMAP**

BASE ADDRESS : 0xBB02DD04  
ARRAY INDEX : 0 - 31  
ARRAY OFFSET : 0x4  
DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

scheduling queue usage mapping register

Bits	Field	Description	Type	Default
31:0	MAPPING_TBL	32 queues usage mapping control	RW	0x0

**PON\_WFQ\_WEIGHT**



BASE ADDRESS : 0xBB02DD84  
 ARRAY INDEX : 0 - 127  
 ARRAY OFFSET : 10 bits  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (10 bits per field)

PON WFQ weigth related configuration

Bits	Field	Description	Type	Default
9:0	WEIGHT	Weight of PON WFQ	RW	0x0

## PON\_WFQ\_TYPE

BASE ADDRESS : 0xBB02DE30  
 ARRAY INDEX : 0 - 127  
 ARRAY OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

PON queue scheuling type configuration

Bits	Field	Description	Type	Default
0	QUEUE_TYPE	WFQ or strict queue type setting for PON 0b0:strict queue type 0b1:WFQ queue type	RW	0x0

## FC\_PON\_Q\_EGR\_DROP\_EN

BASE ADDRESS : 0xBB01C3BC  
 ARRAY INDEX : 0 - 127  
 ARRAY OFFSET : 1 bit  
 DEFAULT VALUE : 0x1

This is a One-Dimension Register Field Array. (1 bit per field)

Specify pon port per queue egress drop enable.

Bits	Field	Description	Type	Default
0	TH	Per queue egress drop enable of port. 0b0: disable 0b1: enable	RW	0x1

## PON\_TCONT\_EN

BASE ADDRESS : 0xBB02DE40  
 ARRAY INDEX : 0 - 31  
 ARRAY OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

Specify pon port per queue egress drop enable.

Bits	Field	Description	Type	Default
0	TCONT_EN	Per T-CONT enable/disable. 0b0: disable 0b1: enable	RW	0x0

## QUEUE\_SEL\_IND

REGISTER ADDRESS : 0xBB02D120  
 DEFAULT VALUE : 0x0

queue indirect access selector

Bits	Field	Description	Type	Default
31:19	RESERVED			
18:13	CIR_SEL_IND	cir queueing selection of indirect access	RW	0x0
12:7	PIR_SEL_IND	pir queueing selection of indirect access	RW	0x0
6:0	QCNT_SEL_IND	queue number of indirect access for per queue current/max page of pon port	RW	0x0

## QUEUE\_SEL\_IND\_DATA

REGISTER ADDRESS : 0xBB02D124  
 DEFAULT VALUE : 0x0

queue indirect access data

Bits	Field	Description	Type	Default
31:16	CIR_QIN	cir queueing of selected tcont	RO	0x0
15:0	PIR_QIN	pir queueing of selected tcont	RO	0x0

## GPON\_DPRU\_RPT\_PRD

REGISTER ADDRESS : 0xBB02D128  
 DEFAULT VALUE : 0x0

GPON dbru report period

Bits	Field	Description	Type	Default
31:5	RESERVED			
4:0	RPT_PRD	GPON dbru report period	RW	0x0

## PON\_PIR\_CIR\_IFG

REGISTER ADDRESS : 0xBB02D12C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:2	RESERVED			
1	DBA_IFG	dba calculation included IFG	RW	0x0
0	PIR_CIR_IFG	pir/cir bucket include IFG	RW	0x0

## PON\_PORT\_CTRL

REGISTER ADDRESS : 0xBB023264

DEFAULT VALUE : 0x0

PON port control

Bits	Field	Description	Type	Default
31:6	RESERVED			
5:0	BW_THRESHOLD		RW	0x0

## PONMAC\_DRN\_CTRL

REGISTER ADDRESS : 0xBB023268

DEFAULT VALUE : 0x0

PON MAC drain out control

Bits	Field	Description	Type	Default
31:9	RESERVED			
8	PON_DRN_SEL	PON MAC drain out select	RW	0x0
7:1	PON_DRN_IDX	PON MAC drain out index	RW	0x0
0	PON_DRN_EN	PON MAC drain out enable	RW	0x0

**PON\_OLT\_BW\_MTR\_FULL**

REGISTER ADDRESS : 0xBB02DE44

DEFAULT VALUE : 0x3FF

OLT Bandwidth Meter full

Bits	Field	Description	Type	Default
31:18	RESERVED			
17:0	OLT_BW_MTR_FULL	upbond of meter for OLT allocated bandwidth	RW	0x003FF

**PON\_WFQ\_IFG\_CTRL**

REGISTER ADDRESS : 0xBB02DE48

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	PON_WFQ_IFG	wfq leakt bucket include IFG	RW	0x0

## CHAPTER 17

# GPON MAC

The chapter describes GPON MAC features

### SECTION 17.1

## GPON MAC GENERAL CONFIG

GPON MAC General Configuration and Status

### GPON\_INT\_DLT

REGISTER ADDRESS : 0xBB700000

DEFAULT VALUE : 0x0

GPON MAC top interruption status

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	GPON_IRQ	0x0: GPON MAC top interrupt output is inactive 0x1: GPON MAC top interrupt output is active GPON_IRQ = (GTC_DS_INTR and GTC_DS_M) or (GTC_DS_CAP_INTR and GTC_DS_CAP_M) or (AES_DECRYPT_INTR and AES_DECRYPT_M) or (GEM_DS_INTR and GEM_DS_M) or (GTC_US_INTR and GTC_US_M) or (GEM_US_INTR and GEM_US_M)	RO	0x0
14:0	RESERVED			

### GPON\_RESET

REGISTER ADDRESS : 0xBB70000C

DEFAULT VALUE : 0x0

GPON MAC reset and status

Bits	Field	Description	Type	Default
31:9	RESERVED			

Bits	Field	Description	Type	Default
8	RST_DONE	0x0: the reset action is not done or the reset action is not triggered 0x1: Reset done. GPON MAC functions when RST_DONE = 1. Once GPON MAC is reset, either by hardware or software reset, this status register will be cleared automatically then be set after 30 cycles (in VCI bus clock). Value 1 of this register means that GPON MAC is ready to operate, and software can configure other registers.	RO	0x0
7:1	RESERVED			
0	SOFT_RST	Software writes 1 to this bit to reset all GPON MAC logics and clear all registers.	RW	0x0

## GPON\_VERSION

REGISTER ADDRESS : 0xBB700010

DEFAULT VALUE : 0x0

It contains design id and version id of GPON MAC TOP.

Bits	Field	Description	Type	Default
31:0	VER_ID	Design version number of GPON MAC TOP. The value will be changed with design version, check from release note.	RO	0x0

## GPON\_TEST

REGISTER ADDRESS : 0xBB700014

DEFAULT VALUE : 0x12345678

Registers for read/write testing

Bits	Field	Description	Type	Default
31:0	TEST_REG	Register for read/write testing.	RW	0x12345678

## GPON\_AES\_BYPASS

REGISTER ADDRESS : 0xBB700020

DEFAULT VALUE : 0x0

Bypass AES\_DECRYPT module

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	M_BYPASS_AES_MOD	0x0: normal operation 0x1: bypass AES_DECRYPT module, only for debug	RW	0x0

## GPON\_INTR\_MASK

REGISTER ADDRESS : 0xBB700040

DEFAULT VALUE : 0x0

GPON MAC TOP interrupt mask

Bits	Field	Description	Type	Default
31:11	RESERVED			
10	GEM_US_M	0x0: prevent GEM_US_INTR from contributing to generation of GPON MAC TOP interrupt. 0x1: GEM_US_INTR can generate interrupt.	RW	0x0
9	RESERVED			
8	GTC_US_M	0x0: prevent "GTC_US_INTR" from contributing to generation of GPON MAC TOP interrupt. 0x1: GTC_US_INTR can generate interrupt.	RW	0x0
7:5	RESERVED			
4	GEM_DS_M	0x0: prevent "GEM_DS_INTR" from contributing to generation of GPON MAC TOP interrupt. 0x1: GEM_DS_INTR can generate interrupt.	RW	0x0
3	AES_DECRYPT_M	0x0: prevent "AES_DECRYPT_INTR" from contributing to generation of GPON MAC TOP interrupt. 0x1: AES_DECRYPT_INTR can generate interrupt.	RW	0x0
2	GTC_DS_CAP_M	0x0: prevent "GTC_DS_CAP_INTR" from contributing to generation of GPON MAC TOP interrupt. 0x1: GTC_DS_CAP_INTR can generate interrupt.	RW	0x0
1	GTC_DS_M	0x0: prevent "GTC_DS_INTR" from contributing to generation of GPON MAC TOP interrupt. 0x1: GTC_DS_INTR can generate interrupt.	RW	0x0
0	RESERVED			

## GPON\_INTR\_STS

REGISTER ADDRESS : 0xBB700044

DEFAULT VALUE : 0x0

GPON MAC TOP interrupt status

Bits	Field	Description	Type	Default
31:11	RESERVED			
10	GEM_US_INTR	Interrupt status of GEM_US, this bit keeps the same value with GEM_US_INTR in FILE GemUS.	RO	0x0
9	RESERVED			
8	GTC_US_INTR	Interrupt status of GTC_US, this bit keeps the same value with GTC_US_INTR in FILE GtcUs.	RO	0x0
7:5	RESERVED			
4	GEM_DS_INTR	Interrupt status of GEM_DS, this bit keeps the same value with GEM_DS_INTR in FILE GemDs.	RO	0x0
3	AES_DECRYPT_INTR	Interrupt status of AES_DECRYPT, this bit keeps the same value with AES_DECRYPT_INTR in FILE AesDecrypt.	RO	0x0
2	GTC_DS_CAP_INTR	Interrupt status of GTC_DS_CAP, this bit keeps the same value with GTC_DS_CAP_INTR in FILE xxx.	RO	0x0
1	GTC_DS_INTR	Interrupt status of GTC_DS, this bit keeps the same value with GTC_DS_INTR in FILE GtcDs.	RO	0x0
0	RESERVED			

## SECTION 17.2

## GTC DOWNSTREAM

GTC downstream control and status

### GPON\_GTC\_DS\_INTR\_DLT

REGISTER ADDRESS : 0xBB701000

DEFAULT VALUE : 0x0

GTC downstream intrrupt indicator

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	GTC_DS_INTR	Interrupt status of GTC_DS page. GTC_DS_INTR = (LOS_DLT and LOS_M) or (LOF_DLT and LOF_M) or (DS_FEC_STA_DLT and DS_FEC_STA_M) or (LOM_DLT and LOM_M) or (SN_REQ_HIS and SN_REQ_M) or (RNG_REQ_HIS and RNG_REQ_M) or (PLM_BUF_REQ and PLM_BUF_M)	RO	0x0
14:11	RESERVED			
10	PLM_BUF_REQ	When PLOAMd buffer is not empty, this bit is set to high.	RO	0x0
9	RNG_REQ_HIS	One or more Ranging Request received since last time of reading.	RC	0x0
8	SN_REQ_HIS	One or more SN Request received since last time of reading.	RC	0x0



Bits	Field	Description	Type	Default
7:4	RESERVED			
3	LOM_DLT	It indicates the Super-Frame status has changed since last time of reading.	RC	0x0
2	DS_FEC_STA_DLT	It indicates the downstream FEC on/off status has changed since last time of reading.	RC	0x0
1	LOF_DLT	It indicates the status of LOF has changed since last time of reading.	RC	0x0
0	LOS_DLT	It indicates the status of LOS has changed since last time of reading.	RC	0x0

## GPON\_GTC\_DS\_INTR\_MASK

REGISTER ADDRESS : 0xBB701004

DEFAULT VALUE : 0x0

GTC downstream intrrupt mask

Bits	Field	Description	Type	Default
31:11	RESERVED			
10	PLM_BUF_M	0x0: PLM_BUF_REQ can not generate inrerrupt. 0x1: PLM_BUF_REQ can generate inrerrupt.	RW	0x0
9	RNG_REQ_M	0x0: RNG_REQ_HIS can not generate inrerrupt. 0x1: RNG_REQ_HIS can generate inrerrupt.	RW	0x0
8	SN_REQ_M	0x0: SN_REQ_HIS can not generate inrerrupt. 0x1: SN_REQ_HIS can generate inrerrupt.	RW	0x0
7:4	RESERVED			
3	LOM_M	0x0: LOM_DLT can not generate inrerrupt. 0x1: LOM_DLT can generate inrerrupt.	RW	0x0
2	DS_FEC_STA_M	0x0: DS_FEC_STA_DLT can not generate inrerrupt. 0x1: DS_FEC_STA_DLT can generate inrerrupt.	RW	0x0
1	LOF_M	0x0: LOF_DLT can not generate inrerrupt. 0x1: LOF_DLT can generate inrerrupt.	RW	0x0
0	LOS_M	0x0: LOS_DLT can not generate inrerrupt. 0x1: LOS_DLT can generate inrerrupt.	RW	0x0

## GPON\_GTC\_DS\_INTR\_STS

REGISTER ADDRESS : 0xBB701008

DEFAULT VALUE : 0x2

GTC downstream intrrupt status

Bits	Field	Description	Type	Default
31:4	RESERVED			
3	LOM	Super-Frame Loss of Synchronization.	RO	0x0
2	DS_FEC_STS	Downstream FEC on/off status, detected from Ident field.	RO	0x0
1	LOF	Status of Loss of Downstream Frame.	RO	0x1
0	LOS	Loss of Signal. LOS = ((OPTIC_LOS_POLAR $\text{nxor}$ OPTIC_LOS_SIG) and OPTIC_LOS_ENA) or ((CDR_LOS_POLAR $\text{nxor}$ CDR_LOS_SIG) and CDR_LOS_ENA);	RO	0x0

## GPON\_GTC\_DS\_ONU\_ID\_STATUS

REGISTER ADDRESS : 0xBB701010

DEFAULT VALUE : 0xFF01

ONU Identifier and status

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:8	ONU_ID	ONU Identifier. Used to filter received PLOAMd message and BWMap allocations. Should be set to 0xFF before ranging, and changed to the real ONUID assigned by OLT.	RW	0xFF
7:4	RESERVED			
3:0	ONU_STATE	ONU State Coding. 0x0: unknown state 0x1: O1 state 0x2: O2 state 0x3: O3 state 0x4: O4 state 0x5: O5 state 0x6: O6 state 0x7: O7 state	RW	0x1

## GPON\_GTC\_DS\_CFG

REGISTER ADDRESS : 0xBB701014

DEFAULT VALUE : 0x602

GTC downstream configuration

Bits	Field	Description	Type	Default
31:11	RESERVED			
10	BWM_FILT_ONUID	0x0: Accept all BWMap items, for debug. 0x1: Only accept BWMap items matching provisioned T-CONTs.	RW	0x1

Bits	Field	Description	Type	Default
9	CHK_BWM_CRC	0x0: Accept BWM items even with CRC error, for debug. 0x1: Only accept BWM items which has not CRC error.	RW	0x1
8	PLEND_STRICT_MODE	0x0: processing in standard mode. 0x1: process received PLEND in strict mode, only 2 usable matching PLEND structures are accepted.	RW	0x0
7:6	EXTRA_SN_TX	Times of Extra SN transmission, defined in Upstream Overhead PLOAMd message. This function is deprecated in latest G.984.3.	RW	0x0
5	RESERVED			
4	FEC_CORRECT_DIS	0x0: Enable downstream FEC correction. 0x1: Disable downstream FEC correction even when DS FEC encoding is enabled. The encoded parity bytes are ignored and the data will be passed to following processing modules.	RW	0x0
3:1	FEC_DET_THRSH	Downstream FEC status detection threshold, number of GPON frames. By default, it should be set to 1. Only keep this configurable just to improve compatibility.	RW	0x1
0	DESCRAM_DIS	0x0: Enable de-scrambling. 0x1: Disable de-scrambling. Only for debugging.	RW	0x0

## GPON\_GTC\_DS\_PLOAM\_CFG

REGISTER ADDRESS : 0xBB70101C

DEFAULT VALUE : 0x70B

PLOAMd message configuration

Bits	Field	Description	Type	Default
31:11	RESERVED			
10	PLM_DROP_CRCE	0x0: accept and buffer received PLOAMd messages with CRC error, for software to process/debug. 0x1: dropping received PLOAMd messages with CRC error. (counters will be increased)	RW	0x1
9	PLM_BC_ACC_EN	0x0: Discard broadcast PLOAMd message. 0x1: Accept broadcast PLOAMd message. Should be always set.	RW	0x1
8	PLM_DS_ONUID_FLT_EN	0x0: Disable ONU_ID filter for downstream PLOAM. 0x1: Enable ONU_ID filter for downstream PLOAM.	RW	0x1
7:0	PLM_DS_NOMSG_ID	Message ID of downstream NO_MSG PLOAM message. Should always keep the default value. Here make it configurable just for debugging.	RW	0x0B

## GPON\_GTC\_DS\_LOS\_CFG\_STS

REGISTER ADDRESS : 0xBB701040

DEFAULT VALUE : 0x0

LOS configuration and status

Bits	Field	Description	Type	Default
31:11	RESERVED			
10	CDR_LOS_SIG	Status of LOS signal input from CDR.	RO	0x0
9	RESERVED			
8	OPTIC_LOS_SIG	Status of LOS signal input from OPTIC.	RO	0x0
7:5	RESERVED			
4	LOS_FILTER_EN	0x0: Disable LOS filtering and holdover. 0x1: Enable LOS holdover function. If its enabled, LOS will only be raised after being stable for more than 1ms.	RW	0x0
3	CDR_LOS_POLAR	CDR LOS input polarity.	RW	0x0
2	CDR_LOS_EN	0x0: Disable CDR LOS input. 0x1: Enable CDR LOS input.	RW	0x0
1	OPTIC_LOS_POLAR	Optical LOS input polarity.	RW	0x0
0	OPTIC_LOS_EN	0x0: Disable optical LOS input. 0x1: Enable optical LOS input.	RW	0x0

## GPON\_GTC\_DS\_SUPERFRAME\_CNT

REGISTER ADDRESS : 0xBB701048

DEFAULT VALUE : 0x0

Superframe Counter

Bits	Field	Description	Type	Default
31:30	RESERVED			
29:0	SF_CNTR	Superframe Counter.	RO	0x0

## GPON\_GTC\_DS\_PLOAM\_IND

REGISTER ADDRESS : 0xBB701080

DEFAULT VALUE : 0x20

Downstream PLOAM message indication

Bits	Field	Description	Type	Default
31:6	RESERVED			

Bits	Field	Description	Type	Default
5	PLM_BUF_EMPTY	Indicate the PLOAMd buffer is empty.	RO	0x1
4	PLM_BUF_FULL	Indicate the PLOAMd buffer is full.	RO	0x0
3:1	RESERVED			
0	PLM_DEQ	Write 0x1 to refresh PLOAM_RDATA. PLOAMd reading is triggered by interrupt generated by PLM_BUF_REQ, then follows this procedure: 1. Read PLM_BUF_EMPTY, if PLM_BUF_EMPTY = 0, goto step 2; else exit; 2. Read PLOAM_RDATA for 7 times 3. Write 0 then 1 to PLM_DEQ, to clear the recently read message buffer block 4. Goto step 1, to check once again	RW	0x0

## GPON\_GTC\_DS\_PLOAM\_MSG

BASE ADDRESS : 0xBB7010A0  
 ARRAY INDEX : 0 - 7  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

Downstream PLOAM message indication

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	PLOAM_RDATA	Received PLOAM data.	RO	0x0

## GPON\_GTC\_DS\_ALLOC\_IND

REGISTER ADDRESS : 0xBB7010C0  
 DEFAULT VALUE : 0x0

AllocID operation indication

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	ALLOCID_OP_REQ	CPU write 0x0 then 0x1 to start an operation.	RW	0x0
14	ALLOCID_OP_COMPL	Operation complete flag. 0x1: Operation complete.	RO	0x0
13	ALLOCID_OP_HIT	0x0: ALLOCID_OP_RDATA is not valid since no item configured for this index. 0x1: ALLOCID_OP_RDATA is valid.	RO	0x0
12:10	RESERVED			

Bits	Field	Description	Type	Default
9:8	ALLOCID_OP_MODE	Operation code: 0b00: no operation 0b01: write operation 0b10: read operation 0b11: clean operation	RW	0x0
7:5	RESERVED			
4:0	ALLOCID_OP_IDX	Index of T-CONT of AllocID configuration. AllocID filtering is done by CAM structure which is configured by software. ALLOCID_OP_xxx registers are provisioned for AllocID CAM configuration and enquiry. Operation should follow the procedure: 1. Write ALLOCID_OP_IDX and ALLOCID_OP_MODE. 2. Write ALLOCID_OP_WDATA if the operation is writing. 3. Write '0' then '1' to ALLOCID_OP_REQ 4. Wait until ALLOCID_OP_COMPL = '1' 5. If the operation is reading, read ALLOCID_OP_HIT. If it's high, go to 6; else there is no match for this index. 6. Read ALLOCID_OP_RDATA.	RW	0x0

## GPON\_GTC\_DS\_ALLOC\_WR

REGISTER ADDRESS : 0xBB7010C4

DEFAULT VALUE : 0x0

AllocID write operation

Bits	Field	Description	Type	Default
31:12	RESERVED			
11:0	ALLOCID_OP_WDATA	Write Data of AllocID configuration.	RW	0x0

## GPON\_GTC\_DS\_ALLOC\_RD

REGISTER ADDRESS : 0xBB7010CC

DEFAULT VALUE : 0x0

AllocID read operation

Bits	Field	Description	Type	Default
31:12	RESERVED			
11:0	ALLOCID_OP_RDATA	Read Data of AllocID configuration.	RO	0x0

## GPON\_GTC\_DS\_PORT\_IND

REGISTER ADDRESS : 0xBB701100

DEFAULT VALUE : 0x0

GEM Port ID operation indication

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	PORTID_OP_REQ	CPU write 0x0 then 0x1 to start an operation.	RW	0x0
14	PORTID_OP_COMPL	Operation complete flag. 0x1: Operation complete.	RO	0x0
13	PORTID_OP_HIT	0x0: PORTID_OP_RDATA is not valid since no item configured for this index. 0x1: PORTID_OP_RDATA is valid.	RO	0x0
12:10	RESERVED			
9:8	PORTID_OP_MODE	Operation code: 0b00: no operation 0b01: write operation 0b10: read operation 0b11: clean operation	RW	0x0
7	RESERVED			
6:0	PORTID_OP_IDX	GEM Port index. PortID filtering is done by CAM structure which is configured by software. PORTID_OP_XXX registers are provisioned for PortID CAM configuration and enquiry. Operation should follow the procedure: 1. Write PORTID_OP_IDX and PORTCID_OP_MODE 2. Write PORTID_OP_WDATA if the operation is writing. 3. Write '0' then '1' to PORTID_OP_REQ 4. Wait until PORTID_OP_COMPL = '1' 5. If the operation is reading, read PORTID_OP_HIT. If it's high, go to 6; else there is no match for this index. 6. Read PORTID_OP_RDATA.	RW	0x0

## GPON\_GTC\_DS\_PORT\_WR

REGISTER ADDRESS : 0xBB701104

DEFAULT VALUE : 0x0

PortID write operation

Bits	Field	Description	Type	Default
31:12	RESERVED			
11:0	PORTID_OP_WDATA	Write Data of PortID configuration.	RW	0x0

## GPON\_GTC\_DS\_PORT\_RD

REGISTER ADDRESS : 0xBB70110C

DEFAULT VALUE : 0x0

PortID read operation

Bits	Field	Description	Type	Default
31:12	RESERVED			
11:0	PORTID_OP_RDATA	Read Data of PortID configuration.	RO	0x0

## GPON\_GTC\_DS\_PORT\_CNTR\_IND

REGISTER ADDRESS : 0xBB701140

DEFAULT VALUE : 0x0

Downstream GEM port counter indicator

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	GEM_CNTR_R_ACK	Read Acknowledge: 0x0: CNTR_DS_GEM_STAT is not valid since operation is still in progress. 0x1: CNTR_DS_GEM_STAT is valid.	RO	0x0
14:9	RESERVED			
8	GEM_CNTR_RSEL	0x0: To read GEM packet counter. 0x1: To read GEM bytes counter.	RW	0x0
7	RESERVED			
6:0	GEM_CNTR_IDX	Index for the downstream GEM port. GPON_GTC_DS_PORT_CNTR_STAT reading procedure: 1. Write GEM_CNTR_IDX and GEM_CNTR_RSEL (0: GEM packet; 1: GEM Bytes) at same time 2. Wait until GEM_CNTR_R_ACK = '1' 3. Read GEM_CNTR	RW	0x0

## GPON\_GTC\_DS\_PORT\_CNTR\_STAT

REGISTER ADDRESS : 0xBB701144

DEFAULT VALUE : 0x0

Downstream GEM port statistics counter.

Bits	Field	Description	Type	Default
31:0	GEM_CNTR	Downstream GEM port statistics counter.	RO	0x0



Bits	Field	Description	Type	Default
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## GPON\_GTC\_DS\_MISC\_CNTR\_BIP\_ERR\_BLK

REGISTER ADDRESS : 0xBB701184

DEFAULT VALUE : 0x0

Downstream statistics.

Bits	Field	Description	Type	Default
31:0	CNTR_DS_BIP_ERR_BLOCK	Number of D/S BIP blocks with error, based on block. That is, each erroneous BIP is counted as 1, not matter how many bits in the BIP are incorrect. 32 bits.	RC	0x0

## GPON\_GTC\_DS\_MISC\_CNTR\_BIP\_ERR\_BIT

REGISTER ADDRESS : 0xBB701188

DEFAULT VALUE : 0x0

Downstream statistics.

Bits	Field	Description	Type	Default
31:0	CNTR_DS_BIP_ERR_BITS	Number of erroneous bits in D/S BIP. 32 bits.	RC	0x0

## GPON\_GTC\_DS\_MISC\_CNTR\_FEC\_CORRECT\_BIT

REGISTER ADDRESS : 0xBB70118C

DEFAULT VALUE : 0x0

Downstream statistics.

Bits	Field	Description	Type	Default
31:0	CNTR_FEC_CORRECTED_BITS	Number of corrected bits by D/S FEC decoding. 32 bits.	RC	0x0

## GPON\_GTC\_DS\_MISC\_CNTR\_FEC\_CORRECT\_BYTE

REGISTER ADDRESS : 0xBB701190

DEFAULT VALUE : 0x0

Downstream statistics.

Bits	Field	Description	Type	Default
31:0	CNTR_FEC_CORRECTED_BYTES	Number of bytes corrected by D/S FEC decoding.. 32 bits.	RC	0x0

## GPON\_GTC\_DS\_MISC\_CNTR\_FEC\_CORRECT\_CW

REGISTER ADDRESS : 0xBB701194

DEFAULT VALUE : 0x0

Downstream statistics.

Bits	Field	Description	Type	Default
31:0	CNTR_FEC_CORRECTED_CW	Number of code words corrected by D/S FEC decoding. 32 bits.	RC	0x0

## GPON\_GTC\_DS\_MISC\_CNTR\_FEC\_UNCOR\_CW

REGISTER ADDRESS : 0xBB701198

DEFAULT VALUE : 0x0

Downstream statistics.

Bits	Field	Description	Type	Default
31:0	CNTR_FEC_UNCORRECTABLE_CW	Number of uncorrectable FEC blocks. 32 bits.	RC	0x0

## GPON\_GTC\_DS\_MISC\_CNTR\_LOM

REGISTER ADDRESS : 0xBB70119C

DEFAULT VALUE : 0x0

Downstream statistics.

Bits	Field	Description	Type	Default
31:16	CNTR_PLEND_FAIL	Times of Plend parsing failure. 16 bits.	RC	0x0
15:0	CNTR_SUPERFRAME_LOS	Times of Superframe Loss of Synchronization. 16 bits.	RC	0x0

## GPON\_GTC\_DS\_MISC\_CNTR\_PLOAM\_ACPT

REGISTER ADDRESS : 0xBB7011A0

DEFAULT VALUE : 0x0

Downstream statistics.

Bits	Field	Description	Type	Default
31:0	CNTR_PLOAMD_ACCEPTED	Number of PLOAMd messages received, after filtering on ONUID, MSGID and CRC checking. 32 bits.	RC	0x0

## GPON\_GTC\_DS\_MISC\_CNTR\_PLOAM\_FAIL

REGISTER ADDRESS : 0xBB7011A4

DEFAULT VALUE : 0x0

Downstream statistics.

Bits	Field	Description	Type	Default
31:16	CNTR_PLOAMD_OVERFLOW	Number of received PLOAMd messages dropped due to buffer overflow. 16 bits.	RC	0x0
15:0	CNTR_PLOAMD_CRC_ERR	Number of PLOAMd messages with CRC error. 16 bits.	RC	0x0

## GPON\_GTC\_DS\_MISC\_CNTR\_BWM\_FAIL

REGISTER ADDRESS : 0xBB7011A8

DEFAULT VALUE : 0x0

Downstream statistics.

Bits	Field	Description	Type	Default
31:16	CNTR_BWMAP_OVERFLOW	Number of BWMap items dropped due to BWMap buffering limitation (32 items per GPON frame). 16 bits.	RC	0x0
15:0	CNTR_BWMAP_CRC_ERR	Number of BWMap items dropped due to CRC error. 16 bits.	RC	0x0

## GPON\_GTC\_DS\_MISC\_CNTR\_BWM\_INV

REGISTER ADDRESS : 0xBB7011AC

DEFAULT VALUE : 0x0

Downstream statistics.

Bits	Field	Description	Type	Default
31:16	CNTR_BWMAP_INV1	Number of BWMap items dropped due to Sstop > 19439. 16 bits.	RC	0x0
15:0	CNTR_BWMAP_INV0	Number of BWMap items dropped due to Sstop < Sstart. 16 bits.	RC	0x0

## GPON\_GTC\_DS\_MISC\_CNTR\_ACTIVE

REGISTER ADDRESS : 0xBB7011B0

DEFAULT VALUE : 0x0

Downstream statistics.

Bits	Field	Description	Type	Default
31:16	CNTR_RANGING_REQ	Number of received Ranging Request when ONU is in Ranging State. 16 bits.	RC	0x0
15:0	CNTR_SN_REQ	Number of received SN Request when ONU is in SN State. 16 bits.	RC	0x0

## GPON\_GTC\_DS\_MISC\_CNTR\_BWM\_ACPT

REGISTER ADDRESS : 0xBB7011B4

DEFAULT VALUE : 0x0

Downstream statistics.

Bits	Field	Description	Type	Default
31:0	CNTR_BWMAP_ACCPTED	Number of accepted BWMap items. 32 bits.	RC	0x0

## GPON\_GTC\_DS\_MISC\_CNTR\_GEM\_LOS

REGISTER ADDRESS : 0xBB7011B8

DEFAULT VALUE : 0x0

Downstream statistics.

Bits	Field	Description	Type	Default
31:0	CNTR_GEM_LOS	Times of D/S GEM loss of delimitation due to HEC errors. 32 bits.	RC	0x0

**GPON\_GTC\_DS\_MISC\_CNTR\_HEC\_CORRECT**

REGISTER ADDRESS : 0xBB7011BC

DEFAULT VALUE : 0x0

Downstream statistics.

Bits	Field	Description	Type	Default
31:0	CNTR_HEC_CORRECTED	Number of GEM headers corrected by HEC decoding. 32 bits.	RC	0x0

**GPON\_GTC\_DS\_MISC\_CNTR\_GEM\_IDLE**

REGISTER ADDRESS : 0xBB7011C0

DEFAULT VALUE : 0x0

Downstream statistics.

Bits	Field	Description	Type	Default
31:0	CNTR_GEM_IDLE	Number of Idle GEM packets received from OLT. 32 bits.	RC	0x0

**GPON\_GTC\_DS\_MISC\_CNTR\_GEM\_FAIL**

REGISTER ADDRESS : 0xBB7011C4

DEFAULT VALUE : 0x0

Downstream statistics.

Bits	Field	Description	Type	Default
31:16	CNTR_PORTID_MMATCH	Counting the received GEM fragments which match multiple provisioned GEM port ID. This only happen when duplicated GEM port IDs are provisioned. 16 bits.	RC	0x0
15:0	CNTR_GEM_LEN_MISM	Counter of GEM Packet length mismatch. 16 bits.	RC	0x0

**GPON\_GTC\_DS\_MISC\_CNTR\_GEM\_NON\_IDLE**

REGISTER ADDRESS : 0xBB7011C8

DEFAULT VALUE : 0x0

Downstream statistics.

Bits	Field	Description	Type	Default
31:0	CNTR_RX_GEM_NON_IDLE	Total number of non-dile GEM fragments received in downstream.	RC	0x0

## GPON\_GTC\_DS\_MISC\_CNTR\_PLEN\_CORRECT

REGISTER ADDRESS : 0xBB7011CC

DEFAULT VALUE : 0x0

Downstream statistics.

Bits	Field	Description	Type	Default
31:0	CNTR_PLEND_CORRECTIO NS	Corrected PLENd structures.	RC	0x0

## GPON\_GTC\_DS\_OMCI\_PTI

REGISTER ADDRESS : 0xBB701204

DEFAULT VALUE : 0x55

OMCI payload type indicator

Bits	Field	Description	Type	Default
31:7	RESERVED			
6:4	OMCI_PTI_MASK	PTI mask for OMCI	RW	0x5
3	RESERVED			
2:0	OMCI_END_PTI	PTI pattern of OMCI end fragment For OMCI GEM, the end fragment is identified by: (received_PTI AND OMCI_PTI_MASK) == OMCI_END_PTI	RW	0x5

## GPON\_GTC\_DS\_ETH\_PTI

REGISTER ADDRESS : 0xBB701208

DEFAULT VALUE : 0x11

User data payload type indicator

Bits	Field	Description	Type	Default
31:7	RESERVED			
6:4	ETH_PTI_MASK	PTI mask for user data.	RW	0x1
3	RESERVED			

Bits	Field	Description	Type	Default
2:0	ETH_END_PTI	PTI pattern of user data end fragment For non-OMCI GEM, the end fragment is identified by: (received_PTI AND ETH_PTI_MASK) == ETH_END_PTI	RW	0x1

## GPON\_GTC\_DS\_TRAFFIC\_CFG

BASE ADDRESS : 0xBB701400  
 ARRAY INDEX : 0 - 127  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

Traffic type configuraiton for downstream GEM ports.

Bits	Field	Description	Type	Default
31:5	RESERVED			
4:0	TRAFFIC_TYPE_CFG	Traffic Type configuration for downstream GEM ports. Bit 4: AES encryption/decryption is enabled on this GEM port Bit 3: Reserved Bit 2: This GEM port is for OMCI Bit 1: This GEM port is for Ethernet service Bit 0: Only valid when bit 1 is set to 1, this GEM port is for multicast Ethernet service, GPON MAC will apply multicast filtering on received packets.	RW	0x0

### SECTION 17.3

## BWMAP CAPTURE

BWMAP Capture for Debug

## GPON\_BWMAP\_CTRL

REGISTER ADDRESS : 0xBB70200C  
 DEFAULT VALUE : 0x0

BWMAP control register

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	CAP_EN	Write 0x0 then 0x1 to start BWMAP capture.	RW	0x0
14	CAP_CLR	Write 0x0 then 0x1 to clear BWMAP capture buffer.	RW	0x0
13:8	RESERVED			

Bits	Field	Description	Type	Default
7:0	CAP_FRAME_NUM	Capture BWMAP in N GPON frames.	RW	0x0

## GPON\_BWMAP\_STS

REGISTER ADDRESS : 0xBB702010

DEFAULT VALUE : 0x0

BWMAP status register

Bits	Field	Description	Type	Default
31:9	RESERVED			
8	CAP_OVERFL	Indicate BWMAP capture buffer overflow.	RO	0x0
7:0	RESERVED			

## GPON\_BWMAP\_DATA

BASE ADDRESS : 0xBB702400

ARRAY INDEX : 0 - 255

ARRAY OFFSET : 0x4

DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

BWMAP data register

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	CAP_DATA	BWMAP data captured	RO	0x0

### SECTION 17.4

## AES DECRYPT

Specific AES Decrypt control

## GPON\_AES\_INTR\_DLT

REGISTER ADDRESS : 0xBB703000

DEFAULT VALUE : 0x0

AES interrupt indicator



Bits	Field	Description	Type	Default
31:16	RESERVED			
15	AES_DECRYPT_INTR	Interrupt status of the AES module. AES_DECRYPT_PAGE (INFO_FIFO_OVERFL_DLT INFO_FIFO_OVERF_M) (DATA_FIFO_OVERF_DLT DATA_FIFO_OVERF_M) ;	RO = and or and	0x0
14:2	RESERVED			
1	INFO_FIFO_OVERFL_DLT	INFO_FIFO_OVERFL has changed since last time of reading.	RC	0x0
0	DATA_FIFO_OVERFL_DLT	DATA_FIFO_OVERFL has changed since last time of reading.	RC	0x0

## GPON\_AES\_INTR\_MASK

REGISTER ADDRESS : 0xBB703004

DEFAULT VALUE : 0x0

AES intrrupt indicator

Bits	Field	Description	Type	Default
31:2	RESERVED			
1	INFO_FIFO_OVERFL_M	0x0: Disable INFO_FIFO_OVERFL_DLT to generate inerrupt. 0x1: Enable INFO_FIFO_OVERFL_DLT to generate inerrupt.	RW	0x0
0	DATA_FIFO_OVERFL_M	0x0: Disable DATA_FIFO_OVERFL_DLT to generate inerrupt. 0x1: Enable DATA_FIFO_OVERFL_DLT to generate inerrupt.	RW	0x0

## GPON\_AES\_INTR\_STS

REGISTER ADDRESS : 0xBB703008

DEFAULT VALUE : 0x0

AES intrrupt status

Bits	Field	Description	Type	Default
31:2	RESERVED			
1	INFO_FIFO_OVERFL	Status of Information Context FIFO	RO	0x0
0	DATA_FIFO_OVERFL	Status of Data FIFO	RO	0x0

## GPON\_AES\_KEY\_SWITCH\_REQ

REGISTER ADDRESS : 0xBB703010

DEFAULT VALUE : 0x0

AES key switch request

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	KEY_CFG_REQ	CPU write 0x0 then 0x1 to this bit to request AES key switch.	RW	0x0
14	CFG_ACTIVE_KEY	0x0: The shadow key will be written. 0x1: Active key will be change - please note this would hit the traffic and should never be used during normal operations. Software should always write to the shadow key in normal operation.	RW	0x0
13:0	RESERVED			

## GPON\_AES\_KEY\_SWITCH\_TIME

REGISTER ADDRESS : 0xBB703014

DEFAULT VALUE : 0x0

AES key switch timing

Bits	Field	Description	Type	Default
31:30	RESERVED			
29:0	SWITCH_SUPERFRAME	The super-frame counter from which the key being configured should be used.	RW	0x0

## GPON\_AES\_KEY\_WORD\_IND

REGISTER ADDRESS : 0xBB703020

DEFAULT VALUE : 0x0

AES key word indicator

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	KEY_WR_REQ	Write request from CPU.	RW	0x0
14	KEY_WR_COMPL	When the bit is 0x1, it means AES key previous writing operation is complete, CPU can began next operation.	RO	0x0
13:8	RESERVED			

Bits	Field	Description	Type	Default
7	KEY_USE_IND	0x1: Currently the key bank CPU is operating is the same bank used for decryption. For debug only. Only for debug. Currently this register is not useful.	RO	0x0
6:3	RESERVED			
2:0	KEY_WORD_IDX	0x0-0x7, index of AES key words. 0x0: correponds to AES-128 key[127:112] 0x7: correponds to AES-128 key[15:0] Procedure of configure AES key: 1. Write CFG_ACTIVE_KEY: write '0' to configure the shadow key and '1' to change the currently active key. Please note changing active key would hit the traffic and should never be used during normal operations. 2. Write '0' then '1' to KEY_CFG_REQ to finish writing key 3. Write 128-bit key, word-by-word: 1) Write KEY_WORD_IDX and the corresponding word (16-bit) to KEY_DATA 2) Write '0' then '1' to KEY_WR_REQ 3) Wait until KEY_WR_COMPL = '1' 4) Repeat 1) to 3) for next word until 128-bit key is written.	RW	0x0

## GPON\_AES\_WORD\_DATA

REGISTER ADDRESS : 0xBB703024

DEFAULT VALUE : 0x0

AES key word data

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	KEY_DATA	AES key write/read data.	RW	0x0

### SECTION 17.5

## GEM PORT DOWNSTREAM

GEM Port downstream control and status

## GPON\_GEM\_DS\_RX\_CNTR\_IND

REGISTER ADDRESS : 0xBB704040

DEFAULT VALUE : 0x0

Downstream GEM port rx counter indicator

Bits	Field	Description	Type	Default
31:16	RESERVED			

Bits	Field	Description	Type	Default
15	ETH_PKT_RX_R_ACK	Acknowledge of reading operation to CNTR_ETH_RX.	RO	0x0
14:7	RESERVED			
6:0	ETH_PKT_RX_IDX	GEM port index for CNTR_ETH_RX. ETH_PKT_RX is 32-bit per GEM port counter. The read procedure for it is 1. Write local GEM port index to ETH_PKT_RX_IDX 2. Wait until ETH_PKT_RX_R_ACK = '1' 3. Read ETH_PKT_RX	RW	0x0

## GPON\_GEM\_DS\_RX\_CNTR\_STAT

REGISTER ADDRESS : 0xBB704044

DEFAULT VALUE : 0x0

Downstream GEM port rx statistics counter

Bits	Field	Description	Type	Default
31:0	ETH_PKT_RX	Number of received Ethernet packets	RO	0x0

## GPON\_GEM\_DS\_FWD\_CNTR\_IND

REGISTER ADDRESS : 0xBB70404C

DEFAULT VALUE : 0x0

Downstream GEM port forward counter indicator

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	ETH_PKT_FWD_R_ACK	Acknowledge of reading operation to CNTR_ETH_FWD.	RO	0x0
14:7	RESERVED			
6:0	ETH_PKT_FWD_IDX	GEM port index for CNTR_ETH_FWD. ETH_PKT_FWD is 32-bit per GEM port counter. The read procedure for it is 1. Write local GEM port index to ETH_PKT_FWD_IDX 2. Wait until ETH_PKT_FWD_R_ACK = '1' 3. Read ETH_PKT_FWD	RW	0x0

## GPON\_GEM\_DS\_FWD\_CNTR\_STAT

REGISTER ADDRESS : 0xBB704050

DEFAULT VALUE : 0x0

Downstream GEM port fwd statistics counter

Bits	Field	Description	Type	Default
31:0	ETH_PKT_FWD	Number of forwarded Ethernet packets.	RO	0x0

## GPON\_GEM\_DS\_MISC\_IND

REGISTER ADDRESS : 0xBB704064

DEFAULT VALUE : 0x0

Downstream GEM port miscellaneous counter indicator

Bits	Field	Description	Type	Default
31:4	RESERVED			
3:0	MISC_CNTR_IDX	Index of GPON_GEM_DS_MISC_CNTR_STAT.	RW	0x0

## GPON\_GEM\_DS\_MISC\_CNTR\_STAT

REGISTER ADDRESS : 0xBB704068

DEFAULT VALUE : 0x0

Downstream GEM port miscellaneous statistics counter

Bits	Field	Description	Type	Default
31:0	MISC_CNTR	Miscellaneous counter in GEM_DS block.	RO	0x0

## GPON\_GEM\_DS\_MC\_CFG

REGISTER ADDRESS : 0xBB704080

DEFAULT VALUE : 0x8

Downstream GEM block multicast filtering configuration

Bits	Field	Description	Type	Default
31:11	RESERVED			
10	IPV6_MC_FORCE_PASS	0x1: Always pass through IPv6 multicast frames.	RW	0x0
9	IPV6_MC_FORCE_DROP	0x1: Always drop through IPv6 multicast frames, when IPV4_MC_FORCE_PASS = 0.	RW	0x0
8:7	RESERVED			

Bits	Field	Description	Type	Default
6	BROADCAST_PASS	0x1: Forward broadcast packets, i.e., bypass multicast filtering for broadcast packets.	RW	0x0
5	RESERVED			
4	NON_MULTICAST_PASS	0x0: Drop received non-broadcast frames which are neither IPv4 or IPv6 multicast frames 0x1: Pass received non-broadcast frames which are neither IPv4 or IPv6 multicast frames	RW	0x0
3	FCS_CHK_EN	0x0: Disable FCS check. 0x1: Enable FCS check.	RW	0x1
2	IPV4_MC_FORCE_PASS	0x1: Always pass through IPv4 multicast frames.	RW	0x0
1	IPV4_MC_FORCE_DROP	0x1: Always drop through IPv4 multicast frames, when IPV4_MC_FORCE_PASS = 0.	RW	0x0
0	MC_EXCL_MODE	0x1: Multicast filtering works in Excluding mode. By default its 0x0: inclusive mode.	RW	0x0

## GPON\_GEM\_DS\_MC\_IND

REGISTER ADDRESS : 0xBB704084

DEFAULT VALUE : 0x0

Downstream GEM block multicast filtering indicator

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	MC_ITEM_OP_REQ	Write 0x0 then 0x1 to this bit to trigger an operation.	RW	0x0
14	MC_ITEM_OP_COMPL	0x1: Operation completed, and MC_ITEM_OP_RDATA is updated for reading operation.	RO	0x0
13	MC_ITEM_OP_HIT	0x1: MC_ITEM_OP_RDATA is valid.	RO	0x0
12:10	RESERVED			
9:8	MC_ITEM_OP_MODE	Operation Mode: 0b00: no operation 0b01: write operation 0b10: read operation 0b11: clearn operation	RW	0x0
7:0	MC_ITEM_OP_IDX	Multicast filter item configuration index, 0 255. Multicast Filtering is implemented through CAM. The items of CAM are configured by software by steps: 1. Write MC_ITEM_OP_IDX and MC_ITEM_OP_MODE. 2. Write MC_ITEM_OP_WDATA if the operation is writing. 3. Write '0' then '1' to MC_ITEM_OP_REQ 4. Wait until MC_ITEM_OP_COMPL = '1' 5. If the operation is reading, read MC_ITEM_OP_HIT. If it's high, go to 6; else there is no match for this index. 6. Read MC_ITEM_OP_RDATA.	RW	0x0

## GPON\_GEM\_DS\_MC\_WR

REGISTER ADDRESS : 0xBB704088

DEFAULT VALUE : 0x0

Downstream GEM block multicast write data

Bits	Field	Description	Type	Default
31:0	MC_ITEM_OP_WDATA	Write Data.	RW	0x0

## GPON\_GEM\_DS\_MC\_RD

REGISTER ADDRESS : 0xBB704090

DEFAULT VALUE : 0x0

Downstream GEM block multicast read data

Bits	Field	Description	Type	Default
31:0	MC_ITEM_OP_RDATA	Read Data.	RO	0x0

## GPON\_GEM\_DS\_FRM\_TIMEOUT

REGISTER ADDRESS : 0xBB704098

DEFAULT VALUE : 0x110

Downstream GEM block multicast read data

Bits	Field	Description	Type	Default
31:9	RESERVED			
8	OMCI_TR_MODE	0x0: OMCI Forward without bank treatment. 0x1: OMCI Forward with bank treatment.	RW	0x1
7:5	RESERVED			
4:0	ASSM_TIMEOUT_FRM	Number of GPON Frames for assembly timeout threshold.	RW	0x10

## GPON\_GEM\_DS\_MC\_ADDR\_PTN\_IPV4

REGISTER ADDRESS : 0xBB70409C

DEFAULT VALUE : 0x1005E

Multicast MAC address pattern for IPv4

Bits	Field	Description	Type	Default
31:24	RESERVED			
23:0	IPV4_MC_MAC_PREFIX	IPv4 multicast MAC DA prefix (24-bit).	RW	0x01005E

## GPON\_GEM\_DS\_MC\_ADDR\_PTN\_IPV6

REGISTER ADDRESS : 0xBB7040A0

DEFAULT VALUE : 0x3333

Multicast MAC address pattern for IPv6

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	IPV6_MC_MAC_PREFIX	IPv4 multicast MAC DA prefix (16-bit).	RW	0x3333

### SECTION 17.6

## GTC UPSTREAM

GTC upstream control and status

## GPON\_GTC\_US\_INTR\_DLT

REGISTER ADDRESS : 0xBB705000

DEFAULT VALUE : 0x0

GTC upstream interrupt indicator

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	GTC_US_INTR	Interrupt status of GTC_US page. GTC_US_INTR = (US_FEC_STA_DLT and US_FEC_STA_M) or (PLM_URG_EMPTY_DLT and PLM_URG_EMPTY_M) or (PLM_NRM_EMPTY_DLT and PLM_NRM_EMPTY_M);	RO	0x0
14:10	RESERVED			
9	OPTIC_SD_MISM_DLT	0x1: upstream optic SD mis-matches with the GPON MAC output Burst Enable signal. The ONT is suspicious of a rogue ONT	RC	0x0
8	OPTIC_SD_TOOLONG_DLT	0x1: upstream optic SD is asserted for too long time. The ONT is suspicious of a rogue ONT.	RC	0x0
7	PLM_NRM_EMPTY_DLT	0x1: PLM_NRM_EMPTY changed to 0x0 since last time reading this address.	RC	0x0
6	RESERVED			
5	PLM_URG_EMPTY_DLT	0x1: PLM_URG_EMPTY changed to 0x0 since last time reading this address.	RC	0x0



Bits	Field	Description	Type	Default
4:3	RESERVED			
2	US_FEC_STS_DLT	0x1: US_FEC_STS changed since last time reading this address.	RC	0x0
1	RESERVED			
0	DG_MSG_TX_DLT	0x1: counter of transmitted Dying Gasp MSG reaching the DG_MSG_TX_CNT_THRESHOLD. This bit cannot be cleared!	RO	0x0

## GPON\_GTC\_US\_INTR\_MASK

REGISTER ADDRESS : 0xBB705004

DEFAULT VALUE : 0x0

GTC upstream interrupt mask

Bits	Field	Description	Type	Default
31:10	RESERVED			
9	OPTIC_SD_MISM_M	0x0: Not generating interrupt when OPTIC_SD_MISM_DLT is set. 0x1: Enable OPTIC_SD_MISM_DLT to generating interrupt.	RW	0x0
8	OPTIC_SD_TOOLONG_M	0x0: Not generating interrupt when OPTIC_SD_TOOLONG_DLT is set. 0x1: Enable OPTIC_SD_TOOLONG_DLT to generating interrupt.	RW	0x0
7	PLM_NRM_EMPTY_M	0x0: Not generating interrupt when PLM_NRM_EMPTY_DLT is set. 0x1: Enable PLM_NRM_EMPTY_DLT to generating interrupt.	RW	0x0
6	RESERVED			
5	PLM_URG_EMPTY_M	0x0: Not generating interrupt when PLM_URG_EMPTY_DLT is set. 0x1: Enable PLM_URG_EMPTY_DLT to generating interrupt.	RW	0x0
4:3	RESERVED			
2	US_FEC_STS_M	0x0: Not generating interrupt when US_FEC_STA_DLT is set.. 0x1: Enable US_FEC_STS_DLT to generating interrupt.	RW	0x0
1	RESERVED			
0	DG_MSG_TX_M	0x0: Not generating interrupt when DG_MSG_TX_IRQ is set.. 0x1: Enable DG_MSG_TX_IRQ to generating interrupt.	RW	0x0

## GPON\_GTC\_US\_INTR\_STS

REGISTER ADDRESS : 0xBB705008

DEFAULT VALUE : 0x0

GTC upstream intrrupt status

Bits	Field	Description	Type	Default
31:3	RESERVED			
2	US_FEC_STS	Present U/S FEC Status, updated by latest received BWMap allocation.	RO	0x0
1:0	RESERVED			

## GPON\_GTC\_US\_ONU\_ID

REGISTER ADDRESS : 0xBB705010

DEFAULT VALUE : 0xFF00

ONU Identifier

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:8	ONU_ID	ONU Identifier, use to compose PLOAMu messages.	RW	0xFF
7:0	RESERVED			

## GPON\_GTC\_US\_CFG

REGISTER ADDRESS : 0xBB705014

DEFAULT VALUE : 0x18

GTC upstream configuration. The register is protected.

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	FS_LON	0x1: Force turning on optical transmission when FS_LOFF is zero.	RW	0x0
14	FS_LOFF	0x1: Force turning off optical transmission.	RW	0x0
13:11	RESERVED			
10	IND_NRM_PLM	0x0: IND[7] is set only when urgent PLOAMu waiting. 0x1: IND[7] is set when any PLOAMu waiting	RW	0x0
9	PLM_DIS	0x1: Disable sending PLOAMu to OLT. If PLOAMu is requested by BWMap, US_NOMSG will be send.	RW	0x0
8	DBRU_DIS	0x1: Disable sending DBRu to OLT. If PLOAMu is requested by BWMap, all 0 will be send.	RW	0x0

Bits	Field	Description	Type	Default
7:5	RESERVED			
4	ENA_AUTO_DG	0x0: Disable sending Dying Gasp message automatically. 0x1: Enable sending Dying Gasp message automatically	RW	0x1
3	US_BEN_POLAR	The polarity of burst control. 0x0: Low to enable laser transmission 0x1: High to enable laser transmission	RW	0x1
2:1	RESERVED			
0	SCRM_DIS	0x1: Disable scrambling in upstream.	RW	0x0

## GPON\_GTC\_US\_WRITE\_PROTECT

REGISTER ADDRESS : 0xBB705018

DEFAULT VALUE : 0x0

Write protection

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	RSV_REG_WRITE_PROTECTION	Write protection register for reserved registers. What's protected includes registers of GTC_US_CFG, GTC_US_MIN_DELAY, and GTC_US_PROC_MODE. Only when the write protection register is equal to 0xCC19 these protected registers can be changed.	RW	0x0

## GPON\_GTC\_US\_TX\_PATTERN\_CTL

REGISTER ADDRESS : 0xBB705020

DEFAULT VALUE : 0x0

Tx pattern control. The register is protected.

Bits	Field	Description	Type	Default
31:9	RESERVED			
8	TX_PATTERN_MODE_NO_FG	Refer to table xxx	RW	0x0
7:6	RESERVED			
5:4	TX_PATTERN_MODE_BG	Refer to table xxx	RW	0x0
3:2	RESERVED			
1:0	TX_PATTERN_MODE_FG	Refer to table xxx	RW	0x0

**GPON\_GTC\_US\_TX\_PATTERN\_BG**

REGISTER ADDRESS : 0xBB705024

DEFAULT VALUE : 0x0

Tx pattern BG. The register is protected.

Bits	Field	Description	Type	Default
31:0	TX_PATTERN_BG	Refer to table xxx	RW	0x0

**GPON\_GTC\_US\_TX\_PATTERN\_FG**

REGISTER ADDRESS : 0xBB705028

DEFAULT VALUE : 0x0

Tx pattern FG. The register is protected.

Bits	Field	Description	Type	Default
31:0	TX_PATTERN_FG	Refer to table xxx	RW	0x0

**GPON\_GTC\_US\_MIN\_DELAY**

REGISTER ADDRESS : 0xBB705040

DEFAULT VALUE : 0x9132

Minimum delay control. The register is protected.

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:7	MIN_DELAY1	Internal timing control register, should not be changed by software. Should never be changed.	RW	0x122
6:0	MIN_DELAY2	Internal timing control register, should not be changed by software. Should never be changed.	RW	0x32

**GPON\_GTC\_US\_EQD**

REGISTER ADDRESS : 0xBB705044

DEFAULT VALUE : 0x9100

EqD configuration

Bits	Field	Description	Type	Default
31:27	RESERVED			
26:24	EQD1_MULTIFRAME	EqD configuration parameter of multi-frame.	RW	0x0
23:18	RESERVED			
17:0	EQD1_INFRAME	EqD configuration parameter of intra-frame. Provided Software get EQD from OLT through Ranging_Time message, then EQD1 = PLOAM_EQD + MIN_DELAY1 * 16 * 8; EQD1_MULTIFRAME = EQD1 / (19440 * 8); EQD1_INFRAME = EQD1 / (EQD1_MULTIFRAME * 19440 * 8);	RW	0x09100

## GPON\_GTC\_US\_LASER

REGISTER ADDRESS : 0xBB70504C

DEFAULT VALUE : 0x2018

Optical control

Bits	Field	Description	Type	Default
31:14	RESERVED			
13:8	LON_TIME	Optical control offset. 0x0-0x37 is valid	RW	0x20
7:6	RESERVED			
5:0	LOFF_TIME	Optical control offset. 0x0-0x37 is valid	RW	0x18

## GPON\_GTC\_US\_BOH\_CFG

REGISTER ADDRESS : 0xBB705054

DEFAULT VALUE : 0x880

Upstream Burst Overhead configuration

Bits	Field	Description	Type	Default
31:12	RESERVED			
11:8	BOH_REPEAT	Nth byte of BOH_DATA will be repeated to get total overhead to reach length BOH_LENGTH. Here N is BOH_REPEAT. Valid value: 0x1 0xB.	RW	0x8
7:0	BOH_LENGTH	Length of Upstream Burst Overhead (Preamble and Delimiter, including Guard Bits).	RW	0x80

## GPON\_GTC\_US\_BOH\_DATA

BASE ADDRESS : 0xBB705080  
 ARRAY INDEX : 0 - 11  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

Upstream Burst Overhead data

Bits	Field	Description	Type	Default
31:8	RESERVED			
7:0	BOH_DATA	Burst Overhead Data. BOH_DATA: total 12 bytes and the content are as below. Guard bits: A bytes Type 1 preamble: B bytes Type 2 preamble: C bytes Type 3 preamble: D bytes Delimiter: 3 bytes  BOH_LEN: total burst overhead length BOH_REP: indicate the byte of the type 3 preamble which will be repeated. BOH_REP should indicate to the location of (A+B+C). If the BOH_LEN <= 12, the GPON MAC will send the first BOH_LEN bytes in BOH_DATA. If the BOH_LEN > 12, the GPON MAC will send first (BOH_REP) bytes, and repeat the byte indicated by BOH_REP until the transmit bytes reach to (BOH_LEN - 3), and then send last 3 bytes of BOH_DATA (Delimiter).	RW	0x0

## GPON\_GTC\_US\_PLOAM\_IND

REGISTER ADDRESS : 0xBB7050C0  
 DEFAULT VALUE : 0xA0

PLOAMu indication

Bits	Field	Description	Type	Default
31:11	RESERVED			
10:8	PLM_TYPE	PLOAMu type: 0b000: Normal PLOAMu 0b001: Urgent PLOAMu 0b101: Dying Gasp PLOAMu 0b110: SN PLOAMu 0b111: US_NOMSG PLOAMu	RW	0x0
7	PLM_NRM_EMPTY	0x1: Normal PLOAMu buffer is empty.	RO	0x1
6	PLM_NRM_FULL	0x1: Normal PLOAMu buffer is full.	RO	0x0
5	PLM_URG_EMPTY	0x1: Urgent PLOAMu buffer is empty.	RO	0x1
4	PLM_URG_FULL	0x1: Urgent PLOAMu buffer is full.	RO	0x0
3:1	RESERVED			

Bits	Field	Description	Type	Default
0	PLM_ENQ	PLOAMu write Refresh. CPU write 0x0 then 0x1 to this bit to push the written message to buffer. Software writes PLOAMu messages to message buffer following the procedure: 1. Write PLM_TYPE 2. Wait PLM_URG_FULL = '0' when software try to write urgent PLOAMu; Wait PLM_NRM_FULL = '0' when software try to write normal PLOAMu. 3. Write message data to PLM_DATA 4. Write '0' then '1' to PLM_ENQ 5. If software has more messages to write, go back to Step 1.	RW	0x0

## GPON\_GTC\_US\_PLOAM\_DATA

BASE ADDRESS : 0xBB7050E0  
 ARRAY INDEX : 0 - 7  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

PLOAMu data

Bits	Field	Description	Type	Default
31:16	RESERVED			
15:0	PLM_DATA	PLOAMu Data. [7:0] will be sent first.	RW	0x0

## GPON\_GTC\_US\_PLOAM\_CFG

REGISTER ADDRESS : 0xBB705100  
 DEFAULT VALUE : 0x3

PLOAMu configuration

Bits	Field	Description	Type	Default
31:5	RESERVED			
4	PLM_FLUSH_BUF	Writing 0 then 1 to this bit to flush the PLOAM Tx buffer. Better to flush buffer before entering O5. SNmsg, NOmsg and DGmsg will not be impacted.	RW	0x0
3:2	RESERVED			
1	PLM_US_CRC_GEN_EN	0x1: GPON_MAC will generate CRC byte and override the original last byte.	RW	0x1
0	PLM_US_ONUID_OVRD_EN	0x1: GPON_MAC will override the ONU_ID field in PLOAMu.	RW	0x1

**GPON\_GTC\_US\_MISC\_CNTR\_IDX**

REGISTER ADDRESS : 0xBB705140

DEFAULT VALUE : 0x0

GTC upstream miscellaneous counter index

Bits	Field	Description	Type	Default
31:3	RESERVED			
2:0	MISC_IDX	Index of GPON_GTC_US_MISC_CNTR_STAT.	RW	0x0

**GPON\_GTC\_US\_MISC\_CNTR\_STAT**

REGISTER ADDRESS : 0xBB705148

DEFAULT VALUE : 0x0

GTC upstream miscellaneous statistics counter

Bits	Field	Description	Type	Default
31:0	MISC_CNTR	Miscellaneous counters in GTC_US block.	RO	0x0

**GPON\_GTC\_US\_RDI**

REGISTER ADDRESS : 0xBB705180

DEFAULT VALUE : 0x0

ONU RDI detected

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	ONU_RDI	0x1: ONU RDI is detected. Written by software, reported to OLT in PLOu field.	RW	0x0

**GPON\_GTC\_US\_DG**

REGISTER ADDRESS : 0xBB705184

DEFAULT VALUE : 0x3

ONU dying gasp



Bits	Field	Description	Type	Default
31:9	RESERVED			
8	DG_STATUS	0x1: currently in Dying Gasp status	RO	0x0
7:4	DG_MSG_TX_CNT	Counter of transmitted Dying Gasp messages	RO	0x0
3:0	DG_MSG_TX_CNT_THRESH OLD	Threshold of counter of transmitted Dying Gasp message, once the count reaching this threshold, an interrupt may be generated.	RW	0x3

## GPON\_GTC\_US\_OPTIC\_SD\_TH

REGISTER ADDRESS : 0xBB705188

DEFAULT VALUE : 0xA4BFA

Optical SD threshold

Bits	Field	Description	Type	Default
31	RESERVED			
30:16	OPTIC_SD_MISM_THREH	The threshold of time for upstream optic SD signal mismatching with the output Burst Enable	RW	0x000A
15	RESERVED			
14:0	OPTIC_SD_TOOLONG_THR ESH	The threshold of time for upstream optic SD signal assertion time. In unit of upstream byte.	RW	0x4BFA

## GPON\_GTC\_US\_PROC\_MODE

REGISTER ADDRESS : 0xBB705200

DEFAULT VALUE : 0x1

Processing mode. The register is protected.

Bits	Field	Description	Type	Default
31:2	RESERVED			
1	OPTIC_AUTO_SUPPRESS_D IS	0x1: Disable the function of suppressing laser when ONT is outside of state 3, 4 and 5. Should not be changed, only for debug.	RW	0x0
0	AUTO_PROC_SSTART	0x1: Process Small SSTART (<BOH LEN) automatically. Should not be changed, only for debug.	RW	0x1

### SECTION 17.7

## GEM UPSTREAM

GEM upstream control and status

## GPON\_GEM\_US\_INTR\_DLT

REGISTER ADDRESS : 0xBB706000

DEFAULT VALUE : 0x0

GEM upstream intrrupt indicator

Bits	Field	Description	Type	Default
31	GEM_US_INTR	Interrupt status of GEM_US page.	RO	0x0
30:10	RESERVED			
9	SD_VALID_LONG_DLT	0x1: SD_VALID_LONG_DLT changed to 0x0 since last time reading this address.	RC	0x0
8	SD_DIFF_HUGE_DLT	0x1: SD_DIFF_HUGE_DLT changed to 0x0 since last time reading this address.	RC	0x0
7	REQUEST_DELAY_DLT	0x1: REQUEST_DELAY_DLT changed to 0x0 since last time reading this address.	RC	0x0
6	BC_LESS6_DLT	0x1: BC_LESS6_DLT changed to 0x0 since last time reading this address.	RC	0x0
5	ERR_PLI_DLT	0x1: ERR_PLI_DLT changed to 0x0 since last time reading this address.	RC	0x0
4	BURST_TM_LARGER_GTC_DLT	0x1: BURST_TM_LARGER_GTC_DLT changed since last time reading this address.	RC	0x0
3	BANK_TOO_MUCH_AT_END_DLT	0x1: BANK_TOO_MUCH_AT_END_DLT changed since last time of reading this address.	RC	0x0
2	BANK_REMAIN_AFRD_DLT	0x1: BANK_REMAIN_AFRD_DLT changed since last time reading this address.	RC	0x0
1	BANK_OVERFL_DLT	0x1: BANK_OVERFL_IND changed since last time reading this address.	RC	0x0
0	BANK_UNDERFL_DLT	0x1: BANK_UNDERFL_IND changed since last time reading this address.	RC	0x0

## GPON\_GEM\_US\_INTR\_MASK

REGISTER ADDRESS : 0xBB706004

DEFAULT VALUE : 0x0

GEM upstream intrrupt mask

Bits	Field	Description	Type	Default
31:10	RESERVED			
9	SD_VALID_LONG_M	0x0: Disable SD_VALID_LONG_DLT from generating interrupt. 0x1: Enable SD_VALID_LONG_DLT to generating interrupt.	RW	0x0
8	SD_DIFF_HUGE_M	0x0: Disable SD_DIFF_HUGE_DLT from generating interrupt. 0x1: Enable SD_DIFF_HUGE_DLT to generating interrupt.	RW	0x0

Bits	Field	Description	Type	Default
7	REQUEST_DELAY_M	0x0: Disable REQUEST_DELAY_DLT from generating interrupt. 0x1: Enable REQUEST_DELAY_DLT to generating interrupt.	RW	0x0
6	BC_LESS6_M	0x0: Disable BC_LESS6_DLT from generating interrupt. 0x1: Enable BC_LESS6_DLT to generating interrupt.	RW	0x0
5	ERR_PLI_M	0x0: Disable ERR_PLI_DLT from generating interrupt. 0x1: Enable ERR_PLI_DLT to generating interrupt.	RW	0x0
4	BURST_TM_LARGER_GTC_M	0x0: Disable BURST_TM_LARGER_GTC_DLT from generating interrupt. 0x1: Enable BURST_TM_LARGER_GTC_DLT to generating interrupt.	RW	0x0
3	BANK_TOO_MUCH_AT_END_M	0x0: Disable BANK_TOO_MUCH_AT_END_DLT from generating interrupt. 0x1: Enable BANK_TOO_MUCH_AT_END_DLT to generating interrupt.	RW	0x0
2	BANK_REMAIN_AFRD_M	0x0: Disable BANK_REMAIN_AFRD_DLT from generating interrupt. 0x1: Enable BANK_REMAIN_AFRD_DLT to generating interrupt.	RW	0x0
1	BANK_OVERFL_M	0x0: Disable BANK_OVERFL_DLT from generating interrupt. 0x1: Enable BANK_OVERFL_DLT to generating interrupt.	RW	0x0
0	BANK_UNDERFL_M	0x0: Disable BANK_UNDERFL_DLT from generating interrupt. 0x1: Enable BANK_UNDERFL_DLT to generating interrupt.	RW	0x0

## GPON\_GEM\_US\_INTR\_STS

REGISTER ADDRESS : 0xBB706008

DEFAULT VALUE : 0x0

GEM upstream intrrupt status

Bits	Field	Description	Type	Default
31:10	RESERVED			
9	SD_VALID_LONG_IND	0x1: Indicate the Signal Detect valid more than 125 us.	RO	0x0
8	SD_DIFF_HUGE_IND	0x1: Indicate the Signal Detect and the TX Burst enable has the huge difference for the Transmit Optical Module. It depend on the parameter SD_DIFF_CYCYES.	RO	0x0
7	REQUEST_DELAY_IND	0x1: Indicate the GTC_US need request the next 125us packet s but the Switch also is busy on the last 125us request-acknowledge.	RO	0x0

Bits	Field	Description	Type	Default
6	BC_LESS6_IND	0x1: Indicate the Byte Counter don't take less than 6 and as Empty TCONT by Switch.	RO	0x0
5	ERR_PLI_IND	0x1: Indicate the PLI mismatching with the input cycle from the Switch.	RO	0x0
4	BURST_TM_LARGER_GTC_IND	0x1: Indicate the TM (Switch) has the larger burst bytes than the GTC indication. In this case, GEM module will insert IDLE until bank (125us) end.	RO	0x0
3	BANK_TOO_INDUCH_AT_END_IND	0x1: Indicate the 1k bytes Bank has too much data at the time of leave 800 cycles (bytes). It will force the signal buffer full indication to un-valid in order to let the Switch can send the next bank data. It means the Switch gives too many traffic from	RO	0x0
2	BANK_REMAIN_AFRD_IND	0x1: Indicate the Bank has the remained data after 125us bank read. It means the Switch give too many traffic from request. (Too many response times or too many bytes in one response, etc.).	RO	0x0
1	BANK_OVERFL_IND	0x1: Indicate Bank overflow. It means the Switch doesn't have the true back press machine.	RO	0x0
0	BANK_UNDERFL_IND	0x1: Indicate Bank underflow. It is as timeout of request to response of interface. Insert IDLE in this case.	RO	0x0

## GPON\_GEM\_US\_PTI\_CFG

REGISTER ADDRESS : 0xBB706020

DEFAULT VALUE : 0x5410

GEM upstream PTI configuration

Bits	Field	Description	Type	Default
31	FS_GEM_IDLE	0x1: Forceto send the IDLE only and don't care the data from the Switch. It is just for test.	RW	0x0
30:15	RESERVED			
14:12	PTI_VECTOR3	Translate the input token (OMCI,ENDFRAG) to PTI: (1,1): PTI_VECTOR3. It means OMCI type with End fragment.	RW	0x5
11	RESERVED			
10:8	PTI_VECTOR2	Translate the input token (OMCI,ENDFRAG) to PTI: (1,0): PTI_VECTOR2 It means OMCI type without End fragment.	RW	0x4
7	RESERVED			
6:4	PTI_VECTOR1	Translate the input token (OMCI,ENDFRAG) to PTI: (0,1): PTI_VECTOR1 It means ethernet type with End fragment.	RW	0x1
3	RESERVED			

Bits	Field	Description	Type	Default
2:0	PTI_VECTOR0	Translate the input token (OMCI,ENDFRAG) to PTI: (0,0): PTI_VECTOR0 It means ethernet type without End fragment.	RW	0x0

## GPON\_GEM\_US\_ETH\_GEM\_RX\_CNTR\_IDX

REGISTER ADDRESS : 0xBB706048

DEFAULT VALUE : 0x0

GEM upstream received ether or gem counter index

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	ETH_GEM_RX_R_ACK	Acknowledge of reading operation to ETH_GEM_RX_CNTR.	RO	0x0
14:8	RESERVED			
7:0	ETH_GEM_RX_IDX	GEM port index for CNTR_ETH_RX. Or GEM RX. Highest bit for ETH (1) or GEM(0). Others, for GEM Port index.	RW	0x0

## GPON\_GEM\_US\_ETH\_GEM\_RX\_CNTR\_STAT

REGISTER ADDRESS : 0xBB70604C

DEFAULT VALUE : 0x0

GEM upstream received ether or gem statistics counter

Bits	Field	Description	Type	Default
31:0	ETH_GEM_RX_CNTR	Number of received Ethernet packets or GEM fragment.	RO	0x0

## GPON\_GEM\_US\_PTN\_CTRL

REGISTER ADDRESS : 0xBB706054

DEFAULT VALUE : 0x55

GEM upstream pattern control register

Bits	Field	Description	Type	Default
31:17	RESERVED			

Bits	Field	Description	Type	Default
16	DEBUG_BUS_SEL	Mux of GEM US debug bus	RW	0x0
15:10	RESERVED			
9:8	GEM_PTN_MODE	0: normal GEM data from switch 1: force idle 2:fore increasing bytes 3: use the fixed patter specified in GEM_pattern_byte	RW	0x0
7:0	GEM_PTN_BYTE	Used for upstream GEM data in case GEM_pattern_mode == 3	RW	0x55

## GPON\_GEM\_US\_PORT\_MAP

BASE ADDRESS : 0xBB706400  
 ARRAY INDEX : 0 - 127  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

Upstream GEM port configuration

Bits	Field	Description	Type	Default
31:12	RESERVED			
11:0	PORT_CFG_DATA	Translate the local Port index to global GEM PortID. The array index map to the local port Index.	RW	0x0

## GPON\_GEM\_US\_BYTE\_STAT

BASE ADDRESS : 0xBB706800  
 ARRAY INDEX : 0 - 127  
 ARRAY OFFSET : 0x8  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

GEM upstream byte statistics counter

Bits	Field	Description	Type	Default
63:32	CNTR_LOW32	The low 32 bits of data bytes counter by the local Port Index. The array index map to the local Port Index.	RC	0x0
31:0	CNTR_HIGH32	The high 32 bits of data bytes counter by the local Port Index. The array index map to the local Port Index.	RC	0x0

## TCONT\_IDLE\_BYTE\_STAT

BASE ADDRESS : 0xBB706C00  
 ARRAY INDEX : 0 - 31  
 ARRAY OFFSET : 0x8  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

GEM upstream idle statistics counter

Bits	Field	Description	Type	Default
63:32	CNTR_LOW32	The low 32 bits of IDLE bytes counter by the local TCONT Index. The array index map to the local TCONT Index.	RC	0x0
31:0	CNTR_HIGH32	The high 32 bits of IDLE bytes counter by the local TCONT Index. The array index map to the local TCONT Index.	RC	0x0





## CHAPTER 18

# EPON MAC

The chapter describes EPON MAC features

### SECTION 18.1

## EPON CONFIGURATION

EPON General Configuration

### EPON\_FEC\_CONFIG

REGISTER ADDRESS : 0xBB036000

DEFAULT VALUE : 0x0

FEC configuration register

Bits	Field	Description	Type	Default
31:16	RESERVED			
15	BYPASS_FEC	1'b1: bypass FEC operation and reduce pkt latency	RW	0x0
14	DVSE_TPAR	Delay option enable signal	RW	0x0
13:11	DVS_TPAR	Delay option control word, valid when DVSE==1	RW	0x0
10	DVSE_DAT	Delay option enable signal	RW	0x0
9:7	DVS_DAT	Delay option control word, valid when DVSE==1	RW	0x0
6	DVSE_RPAR	Delay option enable signal	RW	0x0
5:3	DVS_RPAR	Delay option control word, valid when DVSE==1	RW	0x0
2	FEC_RECOVER	FEC recover, use to reset FEC state	RW	0x0
1	FEC_US_EN	enable down stream FEC	RW	0x0
0	FEC_DS_EN	enable up stream FEC	RW	0x0

### EPON\_ASIC\_TIMING\_ADJUST1

REGISTER ADDRESS : 0xBB036004

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:24	RESERVED			

Bits	Field	Description	Type	Default
23:16	RPT_TMG	control timing to send report pkt 8'd0: report pkt end at grant end 8'd1: ahead 1T (1T = 8ns) 8'd2: ahead 2T 8'd3: ahead 3T	RW	0x0
15:8	REG_TMG	control timing to send regsiter pkt 8'd0: report pkt begin after random delay 8'd1: ahead 1T 8'd2: ahead 2T 8'd3: ahead 3T ...	RW	0x0
7:0	QU_TMG	control timing to get Queue information 8'd0: at begening of the grant 8'd1: ahead 1T 8'd2: ahead 2T 8'd3: ahead 3T ...	RW	0x0

## EPON\_ASIC\_TIMING\_ADJUST2

REGISTER ADDRESS : 0xBB036008

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:25	RESERVED			
24:20	LSR_OFF_SHIFT	laser off shift, for debug purpose	RW	0x0
19:15	LSR_ON_SHIFT	laser on shift, for debug purpose	RW	0x0
14:0	ADJ_BC	adjust data byte count of each grant 15'd0 : default (data byte conut = grant length ) 15'd1 : default (data byte conut = grant length - 1) 15'd2 : default (data byte conut = grant length - 2) 15'd3 : default (data byte conut = grant length - 3) ...	RW	0x0

## EPON\_RGSTR1

REGISTER ADDRESS : 0xBB03600C

DEFAULT VALUE : 0x0

register request configuration register

Bits	Field	Description	Type	Default
31:20	RESERVED			
19	HW_REGISTRATION	0b0:registration is handle by S/W 0b1:registration is handle by ASIC	RW	0x0
18:16	REG_LLID_IDX		RW	0x0
15:0	REGISTER_MAC1	register MAC address bit 47 32	RW	0x0

Bits	Field	Description	Type	Default
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## EPON\_RGSTR2

REGISTER ADDRESS : 0xBB036010

DEFAULT VALUE : 0x0

register request configuration register

Bits	Field	Description	Type	Default
31:0	REGISTER_MAC0	register MAC address bit 31 0	RW	0x0

## EPON\_RGSTR3

REGISTER ADDRESS : 0xBB036014

DEFAULT VALUE : 0x0

register request configuration register

Bits	Field	Description	Type	Default
31:9	RESERVED			
8:1	REG_PENDDING_GRANT	register pendding grant number, max vlaue is 32	RW	0x0
0	REGISTER_REQUEST	indicator ASIC must trigger register request	RW	0x0

## EPON\_DEBUG1

REGISTER ADDRESS : 0xBB036018

DEFAULT VALUE : 0x0

debug register

Bits	Field	Description	Type	Default
31:13	RESERVED			
12	MODE0_INVALID_HDL	Mode 0 but LLID not match local LLID table handle 0: drop 1: trap to CPU	RW	0x0
11	MODE1_INVALID_HDL	Mode 1 but LLID not match local LLID table handle 0: drop 1: trap to CPU	RW	0x0

Bits	Field	Description	Type	Default
10	INV_OE_CONTROL	inverse porarity for OE control signal 0b0: not do inverse 0b1:inverse OE control signal	RW	0x0
9:0	DBG_SEL	selection for debug signals	RW	0x0

## EPON\_DEBUG2

REGISTER ADDRESS : 0xBB03601C

DEFAULT VALUE : 0x0

debug register

Bits	Field	Description	Type	Default
31:29	RESERVED			
28:24	PRB_GN	select which grant to probe out on debug signals 5'd0: grant0 on debug signals 5'd1: grant1 on debug signals 5'd3: grant2 on debug signals	RW	0x0
23:0	PRB_EPMC	debug signals for register to read	RO	0x0

## EPON\_TIMER\_CONFIG1

REGISTER ADDRESS : 0xBB036020

DEFAULT VALUE : 0x64

Bits	Field	Description	Type	Default
31:7	RESERVED			
6:0	MPCP_TIMEOUT_VALUE	Record the mpcp age value. This field is for REPORT_TIMER. Write 0 to disable mpcp timer Unit:10ms	RW	0x64

## EPON\_INTR

REGISTER ADDRESS : 0xBB036024

DEFAULT VALUE : 0x7

EPON interrupt register

Bits	Field	Description	Type	Default
31:6	RESERVED			
5	REG_LLID_TX_IMR	IMR register LLID tx	RW	0x0

Bits	Field	Description	Type	Default
4	TIME_DRIFT_IMR	IMR time drift	RW	0x0
3	MPCP_TIMEOUT_IMR	IMR mpcp timeout	RW	0x0
2	REG_LLID_TX_IMS	interrupt staus for register LLID tx write 1 clear	RW	0x1
1	TIME_DRIFT_IMS	interrupt staus for time drift write 1 clear	RW	0x1
0	MPCP_TIMEOUT_IMS	interrupt staus for mpcp timeout write 1 clear	RW	0x1

## SYNC\_TIME

REGISTER ADDRESS : 0xBB036028

DEFAULT VALUE : 0x0

sync time register

Bits	Field	Description	Type	Default
31:16	NORMAL_SYNC_TIME	normal sync time	RW	0x0
15:0	DISC_SYNC_TIME	discovery sync time	RO	0x0

## LASER\_ON\_OFF\_TIME

REGISTER ADDRESS : 0xBB03602C

DEFAULT VALUE : 0x0

laser on off time register

Bits	Field	Description	Type	Default
31:12	RESERVED			
11:6	LASER_ON_TIME	laser on time	RW	0x0
5:0	LASER_OFF_TIME	laser off time	RW	0x0

## MIN\_GRANT\_START

REGISTER ADDRESS : 0xBB036030

DEFAULT VALUE : 0x0

min grant start time

Bits	Field	Description	Type	Default
31:0	GRANT_STRAT_MIN	grant start accept min value	RW	0x0

## MAX\_GRANT\_START

REGISTER ADDRESS : 0xBB036034

DEFAULT VALUE : 0x0

max grant start time

Bits	Field	Description	Type	Default
31:0	GRANT_STRAT_MAX	grant start accept MAX value	RW	0x0

## EPON\_TIME\_CTRL

REGISTER ADDRESS : 0xBB036038

DEFAULT VALUE : 0x0

RTT and time control register

Bits	Field	Description	Type	Default
31:18	RESERVED			
17:16	QUARD_THRESHOLD	This field holds the maximal amount of drift allowed for a timestamp received at the ONU. 0b04 time quanta. 0b18 time quanta. (Default) 0b216tim quanta. 0b332time quanta.	RW	0x0
15:0	RTT_ADJ	RTT adjust. Unit (TQ) The value is signed interger. This reguster use to adjust the RTT value for RTT emulation. The timestamp from OLT will be adjust by this register then update to local time.	RW	0x0

## EP\_MISC

REGISTER ADDRESS : 0xBB03603C

DEFAULT VALUE : 0x0

misc configuration register

Bits	Field	Description	Type	Default
31:6	RESERVED			
5	SRT_GN		RW	0x0
4	STOP_LOCAL_TIME	Stop local time update, local time will stop 0b0:normal operation 0b1:local timer will stop update	RW	0x0
3	FEC_ENABLE	Enable FEC function 0b0:disable 0b1:enable	RW	0x0
2	ALWAYS_SVY	1'b1: scan grant list for appropriate next grant all the time 1'b0: scan grant list for appropriate next grant only when current grant expired	RW	0x0
1	POWER_SAVING_EN	Enable power saving function 0b0:disable 0b1:enable	RW	0x0
0	POWER_SAVING_MODE	power saving status	RO	0x0

## LLID\_TABLE

BASE ADDRESS : 0xBB036040  
 ARRAY INDEX : 0 - 7  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x57FFF

This is a One-Dimension Common Register Array.

LLID table Register. The RS layer will accept the LLID list in this table.

Bits	Field	Description	Type	Default
31:23	RESERVED			
22	REPORT_TIMEOUT	Indicator report timer is timeout, this bit will set to 1. When report packet send out this bit will set to 0.	RO	0x0
21:16	REPORT_TIMER	Record the report age value. This field is for REPORT_TIMER. Unit 10ms Set the value to 0 is disable this timer.	RW	0x05
15	VALID	Valid bit. 0b0: this LLID is invalid. 0b1: this LLID is valid.	RW	0x0
14:0	LLID	This field record the LLID	RW	0x7FFF

## EPON\_MPCP\_CTR

REGISTER ADDRESS : 0xBB036060  
 DEFAULT VALUE : 0x0

mpcp control register

Bits	Field	Description	Type	Default
31:3	RESERVED			
2	OTHER_HANDLE	mpcp packet for this EPON MAC but opcode is not Gate or Register 0b0Drop 0b1Pass	RW	0x0
1	GATE_HANDLE	0b0ASIC Handle 0b1ASIC Handle and trap to CPU	RW	0x0
0	INVALID_LEN_HANDLE	mpcp packet for this EPON MAC but length is not 64 byte 0b0Drop 0b1Pass	RW	0x0

## EPON\_GRANT\_LIST0

BASE ADDRESS : 0xBB036064

ARRAY INDEX : 0 - 31

ARRAY OFFSET : 0x4

DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

EPON grant list register0

Bits	Field	Description	Type	Default
31:0	GRANT_START	grant start	RO	0x0

## EPON\_GRANT\_LIST1

BASE ADDRESS : 0xBB0360E4

ARRAY INDEX : 0 - 31

ARRAY OFFSET : 0x4

DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

EPON grant list register1

Bits	Field	Description	Type	Default
31:0	GRANT_END	grant end time for this grant	RO	0x0



## EPON\_GRANT\_LIST2

BASE ADDRESS : 0xBB036164  
 ARRAY INDEX : 0 - 31  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

EPON grant list register2

Bits	Field	Description	Type	Default
31:5	RESERVED			
4	FORCE_REPORT	0b0:this grant not need force report 0b1:this grant is discovery grant	RO	0x0
3	DISC	0b0:this grant is normal grant 0b1:this grant is discovery grant	RO	0x0
2:0	LLID_IDX	LLID index	RO	0x0

## EPON\_TX\_CTRL

REGISTER ADDRESS : 0xBB0361E4  
 DEFAULT VALUE : 0x0

EPON tx transmission control register

Bits	Field	Description	Type	Default
31:3	RESERVED			
2:0	LLID_IDX	LLID index	RO	0x0



## CHAPTER 19

# NAT

The chapter describes features related to NAT components

### SECTION 19.1

## TABLE ACCESS

Table Access module

### NAT\_TBL\_ACCESS\_CTRL

REGISTER ADDRESS : 0xBB800100

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:26	RESERVED			
25	RD_EXE	Trigger hardware to execute read indirect table access. Also means status. 0b0: completed 0b1: executing (Note: this bit is common used by software and hardware. When hardware completes the table access, it will clear this bit. File it with 1 to perform command. )	RW	0x0
24	WR_EXE	Trigger hardware to execute write indirect table access. Also means status. 0b0: completed 0b1: executing (Note: this bit is common used by software and hardware. When hardware completes the table access, it will clear this bit. File it with 1 to perform command. )	RW	0x0
23:20	RESERVED			
19:16	TBL_IDX	Access table type. 4'd0(4'b0000): l3_rout table 4'd1(4'b0001): pppoe table 4'd2(4'b0010): nxt_hop table 4'd3(4'b0011): net_if table 4'd4(4'b0100): ext_ip table 4'd5: IPv6 Routing table (4 entry, 143 bits/entry) 4'd6: Binding Table (32 entry, 26 bits/entry) 4'd7: WAN Type Table (8 entry, 6 bits/entry) 4'd8(4'b1000): arp table 4'd9(4'b1001): npatr table 4'd10(4'b1010): napt table 4'd11: Neighbor table (128 entry, 78 bits/entry) Others: RESERVED	RW	0x0

Bits	Field	Description	Type	Default
15:0	ENTRY_IDX	Select access address of the table. Table type: l3_rout: ADDR [15:3]=RESERVED ADDR [2:0]=Index pppoe: ADDR [15:3]=RESERVED ADDR [2:0]=Index net_if: ADDR [15:3]=RESERVED ADDR [2:0]=Index ext_ip: ADDR [15:3]=RESERVED ADDR [2:0]=Index nxt_hop: ADDR [15:4]=RESERVED ADDR [3:0]=Index arp: ADDR [15:9]=RESERVED ADDR [8:0]=Index naptr: ADDR [15:10]=RESERVED ADDR [9:0]=Index napt: ADDR [15:11]=RESERVED ADDR [10:0]=Index IPv6 Routing table [1:0]=Index (4 entry) Neighbor table [6:0]=Index (128 entry) Binding Table [4:0]=Index (32 entry) WAN Type Table [2:0]=Index (8 entry)	RW	0x0

## NAT\_TBL\_ACCESS\_CLR

REGISTER ADDRESS : 0xBB800104

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:14	RESERVED			
13	RST_V6RT	Trigger hardware to quickly reset table . Also means status. 0b0: completed , 0b1: executing (Note:Set it with 1 to perform command. When hardware completes the table reset, it will clear this bit. )	RW	0x0
12	RST_NB	Trigger hardware to quickly reset table . Also means status. 0b0: completed , 0b1: executing (Note:Set it with 1 to perform command. When hardware completes the table reset, it will clear this bit. )	RW	0x0
11	RST_BD	Trigger hardware to quickly reset table . Also means status. 0b0: completed , 0b1: executing (Note:Set it with 1 to perform command. When hardware completes the table reset, it will clear this bit. )	RW	0x0
10	RST_WT	Trigger hardware to quickly reset table . Also means status. 0b0: completed , 0b1: executing (Note:Set it with 1 to perform command. When hardware completes the table reset, it will clear this bit. )	RW	0x0

Bits	Field	Description	Type	Default
9	RST_L3	Trigger hardware to quickly reset table . Also means status. 0b0: completed 0b1: executing (Note:Set it with 1 to perform command. When hardware completes the table reset, it will clear this bit. )	RW	0x0
8	RST_PP	Trigger hardware to quickly reset table . Also means status. 0b0: completed 0b1: executing (Note:Set it with 1 to perform command. When hardware completes the table reset, it will clear this bit. )	RW	0x0
7	RST_NH	Trigger hardware to quickly reset table . Also means status. 0b0: completed 0b1: executing (Note:Set it with 1 to perform command. When hardware completes the table reset, it will clear this bit. )	RW	0x0
6	RST_IF	Trigger hardware to quickly reset table . Also means status. 0b0: completed 0b1: executing (Note:Set it with 1 to perform command. When hardware completes the table reset, it will clear this bit. )	RW	0x0
5	RST_IP	Trigger hardware to quickly reset table . Also means status. 0b0: completed 0b1: executing (Note:Set it with 1 to perform command. When hardware completes the table reset, it will clear this bit. )	RW	0x0
4	RST_ARP	Trigger hardware to quickly reset table . Also means status. 0b0: completed 0b1: executing (Note:Set it with 1 to perform command. When hardware completes the table reset, it will clear this bit. )	RW	0x0
3	RST_NAPTR	Trigger hardware to quickly reset table . Also means status. 0b0: completed 0b1: executing (Note:Set it with 1 to perform command. When hardware completes the table reset, it will clear this bit. )	RW	0x0
2	RST_NAPT	Trigger hardware to quickly reset table . Also means status. 0b0: completed 0b1: executing (Note:Set it with 1 to perform command. When hardware completes the table reset, it will clear this bit. )	RW	0x0
1:0	RESERVED			

## NAT\_TBL\_ACCESS\_RDDATA

REGISTER ADDRESS : 0xBB800108

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
159:128	RDDATA4	Data content [159:128] of the entry for the table.	RO	0x0
127:96	RDDATA3	Data content [127:96] of the entry for the table.	RO	0x0
95:64	RDDATA2	Data content [95:64] of the entry for the specified table.	RO	0x0
63:32	RDDATA1	Data content [63:32] of the entry for the specified table.	RO	0x0
31:0	RDDATA0	Data content [31:0] of the entry for the specified table.	RO	0x0

## NAT\_TBL\_ACCESS\_WRDATA

REGISTER ADDRESS : 0xBB80011C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
159:128	WRDATA4	Data content [159:128] of the entry for the table.	RW	0x0
127:96	WRDATA3	Data content [127:96] of the entry for the table.	RW	0x0
95:64	WRDATA2	Data content [95:64] of the entry for the specified table.	RW	0x0
63:32	WRDATA1	Data content [63:32] of the entry for the specified table.	RW	0x0
31:0	WRDATA0	Data content [31:0] of the entry for the specified table.	RW	0x0

## ARP\_TABLE

TABLE TYPE : 0x8

TABLE INDEX : 0 - 511

ARP Table

Bits	Field	Description
11:1	NXTHOPIDX	Next Hop index(This value is a L2 table Index)
0	VALID	Valid

## BINDING\_TABLE

TABLE TYPE : 0x6  
TABLE INDEX : 0 - 31

Binding table

Bits	Field	Description
27:26	BIND_PTL	Binding Protocol (IPv6, IPv4) 0x00: this bind rule is NOT for IPv4, IPv6 0x01: this bind rule is NOT for IPv6 0x02: this bind rule is NOT for IPv4 0x00: this bind rule is for IPv4, IPv6 and others
25:23	WAN_TYPE_INDEX	WAN interface for binding. It stands for the address of the Bing WAN-Type Table.
22:11	VID_LAN	Ingress VID for binding. AS C100 in figure VID=0: Port based binding Others: Port-and-VLAN based binding
10:6	EXT_PMSK	Active binding extension port mask (for Ingress LAN ports) PORT & EXTPORT always has 1 bit Active
5:0	PORT_MASK	Active binding port mask. (for Ingress LAN ports)

## EXTERNAL\_IP\_TABLE

TABLE TYPE : 0x4  
TABLE INDEX : 0 - 7

External/Internal IP Table

Bits	Field	Description
74:72	PRIORITY	Priority selection. This is designed for NAT and LP packets use, NAPT entry should use the priority information in L4 table.
71	PRIVAL	1: Priority field is valid, 0: invalid Software programming note: NAPT type : this field should be set to 0. NAT, LP types : 0 or 1
70:67	NH_IDX	Nexthop table index. It is valid only for outbound packets (NAT flow). The IPIDX field in the pointed nexthop entry is ignored.
66:65	TYPE	The IP table is used to identify whether the IP address is 1:1 NAT translation, Local public IP address or NAPT translation. Bit 0: If the addr is 1: 1 NAT mapping Bit 1: If the addr is Local Public IP addr 00: NAPT 01: NAT 10: Local Public(LP) 11: Reserved For LP configuration, INTIP should be the same as EXTIP to ensure proper operations. In NAPT (type= 00), the INTIP should be 0.0.0.0 to prevent unexpected results.
64	VALID	1= valid entry, 0= invalid entry
63:32	EXTIP	External IP

Bits	Field	Description
31:0	INTIP	Internal IP Type = 00 : This field should keep 0.0.0.0 . This field is useless for inbound and outbound traffic. Type = 01 : local IP address Type = 10 : Local public address

## IPV6\_ROUTING\_TABLE

TABLE TYPE : 0x5

TABLE INDEX : 0 - 3

IPv6 Routing table

Bits	Field	Description
143	RT2WANINF	Route to WAN inf. This entry is for Binding case usage. It applies both to local & global route. 1: This entry routes to WAN inf. (Binding would take action only under this case). 0:This entry routes to LAN inf
142	VALID	Valid bit for this entry
141:140	PROCESS	
139:136	NEXTHOP	Nexthop Table index or DNET_IF (Destination Interface ID). Nexthop Table index : This field is valid only if Process fiels is set to the value of Global Route. DNET_IF : Destination Interface ID which point to an entry of the network interface table when the Process field is set to the Local Route. The legal range is from 0 to 7.
135:128	IP6_PREFIX_LEN	
127:0	IP6_DIP	

## L3\_ROUTING\_DROP\_TRAP

TABLE TYPE : 0x0

TABLE INDEX : 0 - 7

L3 Routing Table for drop or trap

Bits	Field	Description
58	RT2WANINF	This entry is for Binding case usage. It applies both to local & global route. 1: This entry routes to WAN inf. (Binding would take action only under this case). 0:This entry routes to LAN inf
57:41	RESERVED	
40	INT	1: Internal Interface, 0: External Interface



Bits	Field	Description
39:38	PROCESS	This field defines the process when this entry is matched. 00: CPU 01: DROP 10: ARP ( for Local Route ) 11: Nexthop (for Global Route ) ARP: Destination is directly connected. Get DMAC via ARP table entry. NextHop: The nexthop information is obtained via NextHop table entry, for NAPT and routing. Drop: Drop the packet even the packet is trapped to CPU. CPU: The packet is trapped to CPU for monitoring
37	VALID	Valid
36:32	MASK	IP mask for IP CAM lookup 0: {1b1, 31b0} 1: {2d3, 30b0} 30: {31h7ffffff, 1b0} 31: {32hffffff}
31:0	IP	IP of destination host/network

### L3\_ROUTING\_GLOBAL\_ROUTE

TABLE TYPE : 0x0

TABLE INDEX : 0 - 7

L3 Routing Table for Global Route

Bits	Field	Description
58	RT2WANINF	This entry is for Binding case usage. It applies both to local & global route. 1: This entry routes to WAN inf. (Binding would take action only under this case). 0: This entry routes to LAN inf
57:55	IPDOMAIN	IP domain number. Limits search range for internal IP in IP table and used to search the NAPT flow class table. 0: Entry 0-1 4 : Entry 0-3 1: Entry 2-3 5: Entry 4-7 2: Entry 4-5 6: Entry 0-7 3: Entry 6-7 An IP Domain is an independent WAN IP address z
54:53	NHALGO	Next Hop Selection Algorithm: (load-balancing). 0: Per-packet 1: Per-session 2: Per-source IP Select the load-balancing selection algorithm to decide source IP, next hop and PPPoE session. Note : The loading balance is useless for NAT/ NAPT packets. It only works for pure L3 route. Because the related L4 table will indicate the output interface according individual tcp/udp connection flow. Such setting is controlled by software. Software is easy to implement specific policy route which meet vendors requirement.

Bits	Field	Description
52:48	NHNXT	Next entry index to be used in NextHop table if per packet load balance is used on this routing entry. If NH_ALGO=0, point to current next hop entry and auto-increment after adapted Bit{3:0} are valid. Bit{4} is reserved bit.
47:44	NH_ADDR_START	Next Hop Starting Address Start position of next hop table. Exact position=Value
43:41	NH_NUM	Number of Entries allocated for this routing entry Number of Entries used, start from NHSTA 0: 1 entries: only available for per-packet based. 1: 2 entries 2: 4 entries 3: 8 entries 4: 16 entries
40	INT	1: Internal Interface, 0: External Interface
39:38	PROCESS	This field defines the process when this entry is matched. 00: CPU 01: DROP 10: ARP ( for Local Route ) 11: Nexthop (for Global Route ) ARP: Destination is directly connected. Get DMAC via ARP table entry. NextHop: The nexthop information is obtained via NextHop table entry, for NAPT and routing. Drop: Drop the packet even the packet is trapped to CPU. CPU: The packet is trapped to CPU for monitoring
37	VALID	Valid
36:32	MASK	IP mask for IP CAM lookup 0: {1b1, 31b0} 1: {2d3, 30b0} 30: {31h7ffffff, 1b0} 31: {32hffffff}
31:0	IP	IP of destination host/network

### L3\_ROUTING\_LOCAL\_ROUTE

TABLE TYPE : 0x0

TABLE INDEX : 0 - 7

L3 Routing Table for Local Route

Bits	Field	Description
58	RT2WANINF	This entry is for Binding case usage. It applies both to local & global route. 1: This entry routes to WAN inf. (Binding would take action only under this case). 0: This entry routes to LAN inf
57:51	ARPEND	ARP Ending address 2 bit alignment, i.e. each block is 4-entry long

Bits	Field	Description
50:44	ARPSTA	ARP Starting Address (2 bit alignment)
43:41	DENTIF	Destination Network Interface index
40	INT	Is internal routing 1: Internal Interface, 0: External Interface
39:38	PROCESS	This field defines the process when this entry is matched. 00: CPU 01: DROP 10: ARP ( for Local Route ) 11: Nexthop (for Global Route ) ARP: Destination is directly connected. Get DMAC via ARP table entry. NextHop: The nexthop information is obtained via NextHop table entry, for NAPT and routing. Drop: Drop the packet even the packet is trapped to CPU. CPU: The packet is trapped to CPU for monitoring
37	VALID	Valid
36:32	MASK	IP mask for IP CAM lookup 0: {1b1, 31b0} 1: {2d3, 30b0} 30: {31h7ffffff, 1b0} 31: {32hffffff}
31:0	IP	IP of destination host/network

## NAPT\_TABLE

TABLE TYPE : 0xA

TABLE INDEX : 0 - 2047

TCP/UDP NAPT Table for Egress

Bits	Field	Description
10	VALID	Valid bit
9:0	HASHIN_IDX	An address pointed to one entry of the NAPTR inbound table to get related information about this outbound flow.

## NAPTR\_TABLE

TABLE TYPE : 0x9

TABLE INDEX : 0 - 1023

TCP/UDP NAPTR Table for Ingress

Bits	Field	Description
81:79	PRIORITY	Output priority selection

Bits	Field	Description
78	PRI_VALID	0: Invalid, 1= valid
77:76	VALID	It indicates that entry type. 0: Invalid entry 1: Valid entry but the field of REM_HASH is invalid, this is, dont care both remote IP and Port number (for full cone flows). 2: REM_HASH = hash( remote IP, remote port number) (for Port Restricted cone flows) 3: REM_HASH = hash( remote IP ) (for Restricted cone flows)
75	TCP	1: TCP entry, 0: UDP entry
74:67	EXTPRT_LSB	The translated port{7:0} = EXTPRT_LSB{7:0}
66:64	EXTIP_IDX	It pointes to an entry of external IP table, which provide a mapped IP address.
63:48	REM_HASH	Valid=0, 1 : this field is invalid Valid= 2 : REM_HASH= hash(remote IP, remote port) REM_HASH = SIP{15:0} xor SIP{31:16} xor SPORT{15:0} Valid= 3 : REM_HASH= hash( remote IP) REM_HASH = SIP{15:0} xor SIP{31:16} If this field is valid, the remote hash ID should be calculated and compared with this field.
47:32	INTPORT	Local internal Port number
31:0	INTIP	Local internal IP address

## NEIGHBOR\_TABLE

TABLE TYPE : 0xB

TABLE INDEX : 0 - 127

Neighbor table

Bits	Field	Description
77	VALID	Valid bit for this entry
76:66	L2_TABLE_IDX	
65:64	RT_MATCH_IDX	
63:0	IP6IF_ID	

## NETIF

TABLE TYPE : 0x3

TABLE INDEX : 0 - 7

Network Interface Table

Bits	Field	Description
78:65	MTU	MTU limit, if packet length > MTU, packet will be trapped to CPU Data link packet datagram length, that is MTU = Total L2Length (exclude Preamble & SFD) DA SA CRC LEN VLAN-HEADER if exist
64	ENRTR	This field can be used to block the L3 routing for this VLAN packets.
63:61	MACMASK	To provide a VLAN with multiple continuous MAC Address (for multiple SA of PPPoE Session ID) 111: No mask, : LSB 110 bit Mask (2 MAC) 100: LSB 2 bit Mask (4MAC), 000: LSB 3 bit Mask (8MAC)
60:13	GMAC	This field represents gateway MAC address in this VLAN. If the received packets DA=GMAC, then the packet will be forward to routing engine for L3, L4 operations.
12:1	VLANID	VLAN ID
0	VALID	This field is used to validate this entry(VLAN)

## NEXT\_HOP\_TABLE

TABLE TYPE : 0x2  
 TABLE INDEX : 0 - 15

### NextHop Table

Bits	Field	Description
17:7	NXTHOPIDX	Next Hop Entry : This field represents the nexthop MAC information pointing to L2 entry index
6:4	PPPIDX	PPPoE Table Index : If the type is PPPoE, this field represents the pointer to PPPoE table to get the PPPoE session ID.
3:1	IFIDX	Destination Vlan ID index: Routing resulting interface Vlan index to VLAN table. The valid range is from 0 to 3.
0	TYPE	Type: Ethernet, PPPoE 0: Ethernet 1: PPPoE This field defines the type of next hop when this entry is selected. Ethernet: The next hop is Ethernet type. PPPoE: The next hop is PPPoE type.

## PPPOE\_TABLE

TABLE TYPE : 0x1  
 TABLE INDEX : 0 - 7

### PPPoE Table

Bits	Field	Description
15:0	SESID	Session ID of the PPPoE interface

## WAN\_TYPE\_TABLE

TABLE TYPE : 0x7

TABLE INDEX : 0 - 7

WAN Type Table

Bits	Field	Description
5:2	NxHopTBIIdx	NextHop table index, which address to an entry of the NextHop table.
1:0	WAN_Type	It indicates the type of the Bound WAN interface. 0: L2 Bridged interface 1: L3 Routed interface 2: L34 NAT Routed interface 3: L34 Customized

### SECTION 19.2

## ALE AND TM FOR L3L4

ALE and TM for L3L4 module

## NIFP

REGISTER ADDRESS : 0xBB800000

DEFAULT VALUE : 0x0

Net Interface Index for Port

Bits	Field	Description	Type	Default
31:18	RESERVED			
17:15	INTP5	Index for Port 5, pointing to Interface table.	RW	0x0
14:12	INTP4	Index for Port 4, pointing to Interface table.	RW	0x0
11:9	INTP3	Index for Port 3, pointing to Interface table.	RW	0x0
8:6	INTP2	Index for Port 2, pointing to Interface table.	RW	0x0
5:3	INTP1	Index for Port 1, pointing to Interface table.	RW	0x0
2:0	INTP0	Index for Port 0, pointing to Interface table.	RW	0x0

## NIFEP

REGISTER ADDRESS : 0xBB800004

DEFAULT VALUE : 0x0

## Net Interface Index for Extension Port

Bits	Field	Description	Type	Default
31:15	RESERVED			
14:12	INTEXTTP4	Index for Extension Port 4, pointing to Interface table.	RW	0x0
11:9	INTEXTTP3	Index for Extension Port 3, pointing to Interface table.	RW	0x0
8:6	INTEXTTP2	Index for Port 2, pointing to Interface table.	RW	0x0
5:3	INTEXTTP1	Index for Extension Port 1, pointing to Interface table.	RW	0x0
2:0	INTEXTTP0	Index for Extension Port 0, pointing to Interface table.	RW	0x0

**NIFVCH**

REGISTER ADDRESS : 0xBB800008

DEFAULT VALUE : 0x0

## Net Interface Index for 16VCs high

Bits	Field	Description	Type	Default
31:24	RESERVED			
23:21	VC15	Index for VC15 , pointing to Interface table.	RW	0x0
20:18	VC14	Index for VC14 , pointing to Interface table.	RW	0x0
17:15	VC13	Index for VC13 , pointing to Interface table.	RW	0x0
14:12	VC12	Index for VC12 , pointing to Interface table.	RW	0x0
11:9	VC11	Index for VC11 , pointing to Interface table.	RW	0x0
8:6	VC10	Index for VC10 , pointing to Interface table.	RW	0x0
5:3	VC9	Index for VC9 , pointing to Interface table.	RW	0x0
2:0	VC8	Index for VC8 , pointing to Interface table.	RW	0x0

**NIFVCL**

REGISTER ADDRESS : 0xBB80000C

DEFAULT VALUE : 0x0

## Net Interface Index for 16VCs low

Bits	Field	Description	Type	Default
31:24	RESERVED			
23:21	VC7	Index for VC7 , pointing to Interface table.	RW	0x0

Bits	Field	Description	Type	Default
20:18	VC6	Index for VC6 , pointing to Interface table.	RW	0x0
17:15	VC5	Index for VC5 , pointing to Interface table.	RW	0x0
14:12	VC4	Index for VC4 , pointing to Interface table.	RW	0x0
11:9	VC3	Index for VC3 , pointing to Interface table.	RW	0x0
8:6	VC2	Index for VC2 , pointing to Interface table.	RW	0x0
5:3	VC1	Index for VC1 , pointing to Interface table.	RW	0x0
2:0	VC0	Index for VC0 , pointing to Interface table.	RW	0x0

## SWTCR0

REGISTER ADDRESS : 0xBB800010

DEFAULT VALUE : 0x0

Switch Table Control Register 0

Bits	Field	Description	Type	Default
31:26	RESERVED			
25:24	IPMST_CTRL	2bit, enable multicast control, 0:disable, 1:enable, 2:trap IP multicast packet to CPU, 3:reserve	RW	0x0
23	FRAGMENT2CPU	When ACL is enabled, enable all fragmented IP packet to be trapped to CPU (because L4 is needed) When ACL are not enabled, if this bit is set, L2 forwarding as before, L3 above operation will trap the packet to CPU. 0 = Disable; IP fragment packet will be forwarding as normal via L3 routing or NAT translation. 1 = Enable; IP fragment packet will be trap to CPU.	RW	0x0
22	L4_TRF_HWWRK_SEL	0= Select the Traffic table 0 as working table 1= Select the Traffic table 1 as working table The ASIC will update the new flow traffic information to the selected working table. There are 2 Traffic tables in ASIC to improve the efficiency during software needs to scan 2k bits in L4 traffic table. When software needs the table information, it should switch the working table and read the data from the ex-working table. It provides the following advantage. Both software and HW wont have read/write contentions.	RW	0x0
21	L4_TRF_CHG	1: TRF_HWWRK_SEL Changing, 0: done SW must probe this to make sure TRF_HWWRK_SEL complete It will set by TRF_WHWRK_SEL changing and reset as HW Really been changed	RO	0x0



Bits	Field	Description	Type	Default
20:19	L4_TRF_EXEC_CLR	01= Execute Clear command to Traffic table0. When the command is finished, this bit should be self-clear. 10= Execute Clear command to Traffic table1. When the command is finished, this bit should be self-clear. 00= Done 11: clear both	RW	0x0
18	ARP_TRF_HWWRK_SEL	0= Select the Traffic table 0 as working table 1= Select the Traffic table 1 as working table The ASIC will update the new flow traffic information to the selected working table. There are 2 Traffic tables in ASIC to improve the efficiency during software needs to scan 2k bits in L4 traffic table. When software needs the table information, it should switch the working table and read the data from the ex-working table. It provides the following advantage. Both software and HW wont have read/write contentions.	RW	0x0
17	ARP_TRF_CHG	1: TRF_HWWRK_SEL Changing, 0: done SW must probe this to make sure TRF_HWWRK_SEL complete It will set by TRF_WHWK_SEL changing and reset as HW Really been changed	RO	0x0
16:15	ARP_TRF_EXEC_CLR	01= Execute Clear command to Traffic table0. When the command is finished, this bit should be self-clear. 10= Execute Clear command to Traffic table1. When the command is finished, this bit should be self-clear. 00= Done 11: clear both	RW	0x0
14	L4CHKSERRALLOW	L4 Checksum Error Allow. 0: Not Allowed 1: Allowed If a L4 Checksum Error packet is allowed, L4 checksum re-calculation for this packet is not guaranteed.	RW	0x0
13	L3CHKSERRALLOW	L3 Checksum Error Allow. 0: Not Allowed 1: Allowed If a L3 Checksum Error packet is allowed, L3 checksum re-calculation for this packet is not guaranteed.	RW	0x0
12	TTL_1ENABLE	Enable TTL-1 operation for L3 routing 0: Disable 1: Enable	RW	0x0
11:10	NATMODE	Switch operation layer function Mode Bit 0= 0: disable L3. 1: enable L3 Bit 1= 0: disable L4. 1: enable L4	RW	0x0

Bits	Field	Description	Type	Default
9:8	LIMDBC	LAN interface Mutilayer-Decision-Base Control . This chip supports Mutilayer-Decision-Base for LAN interface lookup. The register define which method to be followed. 00 = by VLAN Based. (8 valid entries in the Network interface table.) 01 = by Port Based (8 valid entries in the Network interface table) 10 = by MAC based (7 valid entries in the Network interface table). 11 = reserved .	RW	0x0
7:6	WANROUTEMODE	00: Forward, 01: Forward to CPU 10: DROP, 11: Reserved Note: This is valid only when L4 is enabled. If only L3 is enabled, it sees no difference between the external interface and internal interface and the setting is always Forward.	RW	0x0
5	RESERVED			
4	ENNATT2LOG	Enable sending suspicious attack packets to CPU for logging purpose (pkts from Remote Public host to internal host)	RW	0x0
3:0	MONSEL	debug/monitor signal select. . NOW, RESERVED!	RW	0x0

## PP\_AGE

REGISTER ADDRESS : 0xBB800014

DEFAULT VALUE : 0x0

PPPoE Table age bit

Bits	Field	Description	Type	Default
31:8	RESERVED			
7:0	PPPOE_TRF_BMP	PPPoE Traffic Bit Map for Entry [7:0], Read Only and clear the actual table traffic fields.Indicate Traffic on this flow. ASIC will set 1 to indicate traffic was forwarded. Software scan register periodically (read clear)	RO	0x0

## NB\_TRF

REGISTER ADDRESS : 0xBB800018

DEFAULT VALUE : 0x0

nb traffic

Bits	Field	Description	Type	Default
127:96	NBT3	[127 96 ] of the entry for the specified table. neighbor table traffic bit	RC	0x0

Bits	Field	Description	Type	Default
95:64	NBT2	[ 95 64 ] of the entry for the specified table. neighbor table traffic bit	RC	0x0
63:32	NBT1	[ 63 32 ] of the entry for the specified table. neighbor table traffic bit	RC	0x0
31:0	NBT0	[ 31 0 ] of the entry for the specified table. neighbor table traffic bit	RC	0x0

## V6\_BD\_CTL

REGISTER ADDRESS : 0xBB800028

DEFAULT VALUE : 0x0

IPv6 routing and binding control bit

Bits	Field	Description	Type	Default
31	RESERVED			
30	PB_EN	PortBinding enable 0: disable, normal route 1: enable port binding, SW must configure binding table and related linking table entry.	RW	0x0
29:0	RESERVED			

## BD\_TRF

REGISTER ADDRESS : 0xBB80002C

DEFAULT VALUE : 0x0

Binding table traffic

Bits	Field	Description	Type	Default
31:0	BD_TRF_BMP	Each bit mapping to each IP6 binding table entry. This register is self-clear-after-read. It indicates traffic on this interface( host ). ASIC will set 1 to indicate traffic was forwarded. Software scan this table periodically.	RC	0x0

## BD\_CFG

REGISTER ADDRESS : 0xBB800030

DEFAULT VALUE : 0x0

Binding configure for every scenarios

Bits	Field	Description	Type	Default
31:30	WAN_BINDING_UNMATCHED_L2L3	Action for binding unmatched for lookup L2 bridge WAN interface to binding L3 routing WAN interface 0b00:Drop 0b01:Trap 0b10:Forced L2 bridge to binding WAN(for LAN/WAN bridging L2/L3)	RW	0x0
29:28	WAN_BINDING_UNMATCHED_L2L34	Action for binding unmatched for lookup L2 bridge WAN interface to binding L34 routing WAN interface 0b00:Drop 0b01:Trap 0b10:Forced L2 bridge to binding WAN(for LAN/WAN bridging L2/L34)	RW	0x0
27:26	WAN_BINDING_UNMATCHED_L3L2	Action for binding unmatched for lookup L3 bridge WAN interface to binding L34 routing WAN interface 0b00:Drop 0b01:Trap 0b10:Permit and L2 Bridge	RW	0x0
25	WAN_BINDING_UNMATCHED_L3L34	Action for binding unmatched for lookup L3 bridge WAN interface to binding L34 routing WAN interface 0b0:Trap 0b1:Force lookup L4 table	RW	0x0
24:23	WAN_BINDING_UNMATCHED_L34L2	Action for binding unmatched for lookup L34 bridge WAN interface to binding L2 bridge WAN interface 0b00:Drop 0b01:Trap 0b10:Permit and L2 Bridge	RW	0x0
22	WAN_BINDING_UNMATCHED_L34L3	Action for binding unmatched for lookup L34 routing WAN interface to binding L3 routing WAN interface 0b1:Trap 0b0: Force binding L3 & skip L4 table lookup	RW	0x0
21	WAN_BINDING_UNMATCHED_L3L3	Action for lookup L3 routing WAN interface to binding L3 routing WAN interface 0b0:Trap 0b1:Force binding L3	RW	0x0
20:19	WAN_BINDING_CUSTOMIZED_L2	Action for lookup L2 routing WAN interface to binding customized WAN interface 0b00:Permit and L2 bridge 0b01:Drop 0b10:Trap	RW	0x0
18:17	WAN_BINDING_CUSTOMIZED_L3	Action for lookup L3 routing WAN interface to binding customized WAN interface 0b00:Force binding L3 0b01:Drop 0b10:Trap 0b11:Force lookup L4 table	RW	0x0

Bits	Field	Description	Type	Default
16:15	WAN_BINDING_CUSTOMIZED_L34	Action for lookup L34 routing WAN interface to binding customized WAN interface 0b00:Normal L34 lookup 0b01:Drop 0b10:Trap 0b11:Force binding L3 & skip L4 table lookup	RW	0x0
14:0	RESERVED			

## SECTION 19.3

## NAT HSB HAS

NAT HSBA module

### HSBA\_CTRL

REGISTER ADDRESS : 0xBB800200

DEFAULT VALUE : 0x4

HSB, HSA Ctrl Register

Bits	Field	Description	Type	Default
31:5	RESERVED			
4:2	TST_LOG_MD	Test and Log:(3) 0: Test Mode, HSB/HSA both Log 1: Normal Mode, No Log (default) 2: Normal Mode, Log All 3: Normal Mode, Log First Drop 4: Normal Mode Log First Pass 5: Normal Mode Log First To CPU 6 7: Reserve Note: Always return <1> for clear HSB/HAS	RW	0x1
1	HSB_ATV	HSB Active. Test Mode Only. It will be generate a pulse as SW write 1. And it will be self cleared as has_ok from ALE	RW	0x0
0	ALE34_BZ	Busy flag, SW polling this after stopping ALE lookup	RO	0x0

### HSB\_DESC

BASE ADDRESS : 0xBB800204

ARRAY INDEX : 0 - 9

ARRAY OFFSET : 0x4

DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

HSB descriptor

Bits	Field	Description	Type	Default
31:0	HSB_DATA	HSB descriptor	RW	0x0

## HSA\_DESC

BASE ADDRESS : 0xBB80022C  
 ARRAY INDEX : 0 - 3  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

HSA descriptor

Bits	Field	Description	Type	Default
31:0	HSA_DATA	HSA descriptor	RO	0x0

## L34\_HSA

TABLE TYPE : 0x0  
 TABLE INDEX : 0 - 0

L34 HSA Data Format

Bits	Field	Description
127	BIND_VIDTRANS	ALE34 Inform L2SW to overwrite DVID. It is independent of L2Trans or L3L4Trans. (BIND RELATED)
126	INTERNAL_VLAN_IF	If the packet is from internal interface (L4-TX mac uses this information to decide translate sip/sport or dip/dport. if L3L4Trans = 1.)

Bits	Field	Description
125:120	REASON	Trap to CPU reason (BIND RELATED issue not yet defined its value!) 1: Protocol parsing failure : CFI=1 in VLAN header 2: Protocol parsing failure : IPv4 packet with optional header 3: Protocol parsing failure : IPv6 packet 4: IP multicasting packets to CPU, for example, disable IPMulticast. 5: Disable L3 but DA= gateway MAC address, or Disable L4 but packets are LAN-to-WAN or WAN-to-LAN 6: PPPoE ID lookup miss for Layer 3/4 forwarding 7: Packets are from LP, NI or NPI to NPE/NE, or Packets are from RP to NPI/NI, or Packets are from WAN to WAN (programmable) 8: NAT/NAPT (Layer 4) Fragmented IPv4 packets 9: Routed (Layer 3) Fragmented IPv4 packets 16: The process of Layer3 routing table is to CPU. 17: TTL reason. 18: ARP table lookup miss. 19: The MTU of the destination interface is smaller than datagram size. 33: Match TCP packets with any of syn, fin and rst. Flag. 34: L4 table (either NAPT or NAPTR tables) lookup miss; for example, non-tcp/udp packets. 35: L4 Traffic table lookup miss for inbound NAPTR packets.
119	L3I4TRANS	To indicate if L3 (IP) translation and L4 (PORT) translation is needed (bounded because the L3 translation will influence the L4 checksum insertion)
118	L2TRANS	To indicate if L2 (MAC Address) translation is needed
117:116	ACTION	Lookup action (BIND RELATED also use this ACTION fields as L2 bridging) (0)= to cpu indication (1)= Pass 0x = Drop 10 = Pass 11= To cpu
115	L4HP_V	Layer4 flow priority valid bit 1= L4HP is valid 0= L4HP is invalid
114:112	L4HP	Layer4 NAT/NAPT flow priority selection
111	FRAG	If this packet is fragment packet?
110:108	DIFID	Destination Interface ID ( MAC uses this to get gateway MAC if L2Trans = 1)
107:96	DVID	The destination VLAN, for VLAN Tagging. It is valid if L2Trans=1. Or bindVIDTrans (BIND RELATED)
95:94	PPPOE_IF	To indicate if PPPoE session stage header is needed to be tagged 00: intact, 01: tagging, 10: remove, 11: modify
93:91	PPPID_IDX	The PPPoE Session ID Index (to a 8-entry register table) for tagging in the translated packet header if needed
90:80	NEXTHOP_MAC_IDX	ARP MAC (next hop MAC address) address index which point to the address of the L2 table.
79:64	L4_CHECKSUM_OFFSET	The substrate distance to fix the L4 Checksum MAC TX requires to consider the TTL-1 simultaneously.
63:48	L3_CHECKSUM_OFFSET	The substrate distance to fix the L3 Checksum MAC-TX requires to consider the TTL-1 simultaneously.

Bits	Field	Description
47:32	PORT	Translated port this field is valid only for TCP and UDP frames. It should be ignored by other type packets, PPTP and ICMP packets for example.
31:0	IP	Translated IP

## L34\_HSB

TABLE TYPE : 0x0

TABLE INDEX : 0 - 0

### L34 HSB Data Format

Bits	Field	Description
311	IS_FROM_WAN_PORT	L2SW indicate the ingress port is WAN or not. (BIND RELATED)
310	L2BRIDGE	S/W Directs ALE to do L2 lookup only for those packets from extension and CPU ports; its valid if the incoming packets are from extension/CPU ports
309	IPFRAGOFS	IPv4 fragmentation offset status 0: IPv4 fragmentation offset = 0 1: not 0
308	IPMF	IPv4 flag : more fragment Ipv6 packet : MF field in the Fragmentation extension header
307	L4CSOK	L4 checksum OK, which includes TCP, UDP, ICMPv4/v6 and IGMP packets. CPUDirTX : this field must be keep 1.
306	L3CSOK	L3 checksum OK Both CPUDirTX and IPv6 packets : this field must be keep 1. If this packet is IPv6 format, this field should keep to 1.
305	CPU_DIRECT_TX	CPU-Direct-TX to UTP ports and DSL VCs  Note : CPU-Dir-TX : ALE wont do any lookup and S/W could command ASIC to do L3/4 checksum offload, and the insertion /removement of PPPoE and VLAN headers
304	UDP_NOCS	UDP and checksum=0x0000
303	PARS_FAIL	Protocol parsing failure, this packet may need software to deal with
302	PPPOE_IF	To indicate if the incoming packet is a PPPoE packet
301	SVLAN_TAG_IF	To indicate if the incoming packet is SVLAN tagged
300:299	TTLST	IPv4 TTL or IPv6 Hop Limit status. 00: TTL=0, 01: TTL=1, 10: TTL>1
298:296	TYPE	The type categories after Input packet parsing flow 000: Ethernet, 01: Reserved, 010: IPv4, 011: ICMP, 100: IGMP, 101: TCP, 110: UDP, 111: IPv6(for S/W reference) (1 6: is for IPv4 packets)
295:288	TCP_FLAG_PROTOCOL_PARSING_FAILURE_REASON	TCP Flag (TCP) or ICMP Code (ICMP) or Reason to CPU (Protocol parsing failure), bit[0] : VLAN-CFI=1, [1]= IPv4 with optional fields, [2]= IPv6 with Hop-by-Hop extension header CPUDirTX : { DoPPPoETAG, PPPoEID[2:0]}



Bits	Field	Description
287	CVLAN_TAG_IF	To indicate if the incoming packet is CVLAN tagged
286:282	SPA	source port number 0 5: rx port0-5, 6: cpu 8 12 : extension ports 1 5 16 31: ATM VC0 15
281:270	CVLANID	VLANID for normal packets
269:256	LEN	PACKET BYTE COUNT WHICH INCLUDING CRC FIELD. IT DOES NOT COUNT CPU TAG HEADER IN.
255:240	DPORT_L4CHKSUM	Destination Port / L4 Checksum (CPUDirectTx)
239:224	PPPOE_ID	PPPoE ID
223:96	DIP	Destination IP address, DIP[31:0] for IPv4 and IPv6 packets DIP[127:32] for IPv6 packets only
95:64	SIP	IPv4 Source IP address
63:48	SPORT_ICMPID_CHKSUM	Source Port (TCP/UDP) / L3 Checksum (CPUDIRECTTX)
47:0	DMAC	Destination MAC

## SECTION 19.4

## L4 TRAFFIC TABLE0

L4 Traffic Table0 module

### L4\_TRF0

BASE ADDRESS : 0xBB800300

ARRAY INDEX : 0 - 2047

ARRAY OFFSET : 1 bit

DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

Bits	Field	Description	Type	Default
0	TRF	Indicate Traffic on this flow. ASIC will set 1 to indicate traffic was forwarded. Software scan this table periodically and write 0 to clear. These field are mapped to all entries in the NAPT table. There are 2k bits in this table and every bit maps to an entry of NAPT table. For example : Entry 1: Traffic[31:0] maps to the packet flows which are recorded in the entry#31 0 of NAPT table. Entry 2: Traffic[31:0] maps to the entry#61 32 of NAPT table. and so on	RO	0x0

## L4\_TRF1

BASE ADDRESS : 0xBB800400  
 ARRAY INDEX : 0 - 2047  
 ARRAY OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

Bits	Field	Description	Type	Default
0	TRF	<p>Indicate Traffic on this flow. ASIC will set 1 to indicate traffic was forwarded. Software scan this table periodically and write 0 to clear.</p> <p>These field are mapped to all entries in the NAPT table. There are 2k bits in this table and every bit maps to an entry of NAPT table.</p> <p>For example :</p> <p>Entry 1: Traffic[31:0] maps to the packet flows which are recorded in the entry#31 0 of NAPT table.</p> <p>Entry 2: Traffic[31:0] maps to the entry#61 32 of NAPT table.</p> <p>and so on</p>	RO	0x0

## ARP\_TRF0

BASE ADDRESS : 0xBB800500  
 ARRAY INDEX : 0 - 511  
 ARRAY OFFSET : 1 bit  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

Bits	Field	Description	Type	Default
0	TRF	<p>Indicate Traffic on this flow. ASIC will set 1 to indicate traffic was forwarded. Software scan this table periodically and write 0 to clear.</p> <p>These field are mapped to all entries in the ARP table. There are 512 bits in this table and every bit maps to an entry of ARP table.</p> <p>For example :</p> <p>Entry 1: Traffic[31:0] maps to the packet flows which are recorded in the entry#31 0 of ARP table.</p> <p>Entry 2: Traffic[31:0] maps to the entry#61 32 of NAPT table. and so on</p>	RO	0x0

**ARP\_TRF1**

BASE ADDRESS : 0xBB800600  
ARRAY INDEX : 0 - 511  
ARRAY OFFSET : 1 bit  
DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (1 bit per field)

Bits	Field	Description	Type	Default
0	TRF	Indicate Traffic on this flow. ASIC will set 1 to indicate traffic was forwarded. Software scan this table periodically and write 0 to clear. These field are mapped to all entries in the ARP table. There are 512 bits in this table and every bit maps to an entry of ARP table. For example : Entry 1: Traffic[31:0] maps to the packet flows which are recorded in the entry#31 0 of ARP table. Entry 2: Traffic[31:0] maps to the entry#61 32 of NAPT table. and so on	RO	0x0



## CHAPTER 20

# TEMP Register

TEMP register

SECTION 20.1

### TEMP REGISTER

Temp register

#### RGF\_VER\_GLB\_CTRL

REGISTER ADDRESS : 0xBB0001CC

DEFAULT VALUE : 0x12051100

register file version (for FPGA)

Bits	Field	Description	Type	Default
31:0	REGFILE_VER	register file version (for FPGA)	RW	0x12051100

#### RGF\_VER\_ALE\_GLB

REGISTER ADDRESS : 0xBB01112C

DEFAULT VALUE : 0x12051100

register file version (for FPGA)

Bits	Field	Description	Type	Default
31:0	REGFILE_VER	register file version (for FPGA)	RW	0x12051100

#### RGF\_VER\_ALE\_ACL

REGISTER ADDRESS : 0xBB0154D0

DEFAULT VALUE : 0x12051100

register file version (for FPGA)

Bits	Field	Description	Type	Default
31:0	REGFILE_VER	register file version (for FPGA)	RW	0x12051100

## RGF\_VER\_ALE\_CVLAN

REGISTER ADDRESS : 0xBB0131A0

DEFAULT VALUE : 0x12051100

register file version (for FPGA)

Bits	Field	Description	Type	Default
31:0	REGFILE_VER	register file version (for FPGA)	RW	0x12051100

## RGF\_VER\_ALE\_DPM

REGISTER ADDRESS : 0xBB01C3CC

DEFAULT VALUE : 0x12051100

register file version (for FPGA)

Bits	Field	Description	Type	Default
31:0	REGFILE_VER	register file version (for FPGA)	RW	0x12051100

## RGF\_VER\_ALE\_L2

REGISTER ADDRESS : 0xBB0170BC

DEFAULT VALUE : 0x12051100

register file version (for FPGA)

Bits	Field	Description	Type	Default
31:0	REGFILE_VER	register file version (for FPGA)	RW	0x12051100

## RGF\_VER\_ALE\_MLTVLAN

REGISTER ADDRESS : 0xBB018060

DEFAULT VALUE : 0x12051100

register file version (for FPGA)

Bits	Field	Description	Type	Default
31:0	REGFILE_VER	register file version (for FPGA)	RW	0x12051100

## RGF\_VER\_ALE\_SVLAN

REGISTER ADDRESS : 0xBB014410

DEFAULT VALUE : 0x12051100

register file version (for FPGA)

Bits	Field	Description	Type	Default
31:0	REGFILE_VER	register file version (for FPGA)	RW	0x12051100

## RGF\_VER\_ALE\_EEE\_LLDP

REGISTER ADDRESS : 0xBB019000

DEFAULT VALUE : 0x12051100

register file version (for FPGA)

Bits	Field	Description	Type	Default
31:0	REGFILE_VER	register file version (for FPGA)	RW	0x12051100

## RGF\_VER\_ALE\_RLDP

REGISTER ADDRESS : 0xBB01A038

DEFAULT VALUE : 0x12051100

register file version (for FPGA)

Bits	Field	Description	Type	Default
31:0	REGFILE_VER	register file version (for FPGA)	RW	0x12051100

## RGF\_VER\_ALE\_EAV\_AFBK

REGISTER ADDRESS : 0xBB01B058

DEFAULT VALUE : 0x12051100

register file version (for FPGA)

Bits	Field	Description	Type	Default
31:0	REGFILE_VER	register file version (for FPGA)	RW	0x12051100

## RGF\_VER\_INTR

REGISTER ADDRESS : 0xBB01D01C

DEFAULT VALUE : 0x12051100

register file version (for FPGA)

Bits	Field	Description	Type	Default
31:0	REGFILE_VER	register file version (for FPGA)	RW	0x12051100

## RGF\_VER\_LED

REGISTER ADDRESS : 0xBB01E0C0

DEFAULT VALUE : 0x12051100

register file version (for FPGA)

Bits	Field	Description	Type	Default
31:0	REGFILE_VER	register file version (for FPGA)	RW	0x12051100

## RGF\_VER\_PER\_PORT\_MAC

BASE ADDRESS : 0xBB020078

PORT INDEX : 0 - 6

PORT OFFSET : 0x400

DEFAULT VALUE : 0x12051100

This is a One-Dimension Port Register Array.

register file version (for FPGA)

Bits	Field	Description	Type	Default
31:0	REGFILE_VER	register file version (for FPGA)	RW	0x12051100



**RGF\_VER\_SDSREG**

REGISTER ADDRESS : 0xBB02214C

DEFAULT VALUE : 0x12051100

register file version (for FPGA)

Bits	Field	Description	Type	Default
31:0	REGFILE_VER	register file version (for FPGA)	RW	0x12051100

**RGF\_VER\_SWCORE**

REGISTER ADDRESS : 0xBB02326C

DEFAULT VALUE : 0x12051100

register file version (for FPGA)

Bits	Field	Description	Type	Default
31:0	REGFILE_VER	register file version (for FPGA)	RW	0x12051100

**RGF\_VER\_EPON\_CTRL**

REGISTER ADDRESS : 0xBB0361E8

DEFAULT VALUE : 0x12051100

register file version (for FPGA)

Bits	Field	Description	Type	Default
31:0	REGFILE_VER	register file version (for FPGA)	RW	0x12051100

**RGF\_VER\_ALE\_RMA\_ATTACK**

REGISTER ADDRESS : 0xBB026014

DEFAULT VALUE : 0x12051100

register file version (for FPGA)

Bits	Field	Description	Type	Default
31:0	REGFILE_VER	register file version (for FPGA)	RW	0x12051100

**RGF\_VER\_BIST\_CTRL**

REGISTER ADDRESS : 0xBB031048

DEFAULT VALUE : 0x12051100

register file version (for FPGA)

Bits	Field	Description	Type	Default
31:0	REGFILE_VER	register file version (for FPGA)	RW	0x12051100

**RGF\_VER\_EGR\_OUTQ**

REGISTER ADDRESS : 0xBB02D130

DEFAULT VALUE : 0x12051100

register file version (for FPGA)

Bits	Field	Description	Type	Default
31:0	REGFILE_VER	register file version (for FPGA)	RW	0x12051100

**RGF\_VER\_EGR\_SCH**

REGISTER ADDRESS : 0xBB02DE4C

DEFAULT VALUE : 0x12051100

register file version (for FPGA)

Bits	Field	Description	Type	Default
31:0	REGFILE_VER	register file version (for FPGA)	RW	0x12051100

**RGF\_VER\_ALE\_HSA**

REGISTER ADDRESS : 0xBB02A24C

DEFAULT VALUE : 0x12051100

register file version (for FPGA)

Bits	Field	Description	Type	Default
31:0	REGFILE_VER	register file version (for FPGA)	RW	0x12051100

## RGF\_VER\_ALE\_METER

REGISTER ADDRESS : 0xBB025110

DEFAULT VALUE : 0x12051100

register file version (for FPGA)

Bits	Field	Description	Type	Default
31:0	REGFILE_VER	register file version (for FPGA)	RW	0x12051100

## RGF\_VER\_MIB\_CTRL

REGISTER ADDRESS : 0xBB03401C

DEFAULT VALUE : 0x12051100

register file version (for FPGA)

Bits	Field	Description	Type	Default
31:0	REGFILE_VER	register file version (for FPGA)	RW	0x12051100

## RGF\_VER\_ALE\_PISO

REGISTER ADDRESS : 0xBB02703C

DEFAULT VALUE : 0x12051100

register file version (for FPGA)

Bits	Field	Description	Type	Default
31:0	REGFILE_VER	register file version (for FPGA)	RW	0x12051100

## RSVD\_GLB\_CTRL

BASE ADDRESS : 0xBB0001D0

ARRAY INDEX : 0 - 15

ARRAY OFFSET : 0x4

DEFAULT VALUE : 0x55555555

This is a One-Dimension Common Register Array.

reserve memory address

Bits	Field	Description	Type	Default
31:0	RSVD_MEM	reserve memory address	RW	0x55555555

## RSVD\_ALE\_GLB

BASE ADDRESS : 0xBB011130  
 ARRAY INDEX : 0 - 15  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x55555555

This is a One-Dimension Common Register Array.

reserve memory address

Bits	Field	Description	Type	Default
31:0	RSVD_MEM	reserve memory address	RW	0x55555555

## RSVD\_ALE\_ACL

BASE ADDRESS : 0xBB0154D4  
 ARRAY INDEX : 0 - 15  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x55555555

This is a One-Dimension Common Register Array.

reserve memory address

Bits	Field	Description	Type	Default
31:0	RSVD_MEM	reserve memory address	RW	0x55555555

## RSVD\_ALE\_CVLAN

BASE ADDRESS : 0xBB0131A4  
 ARRAY INDEX : 0 - 15  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x55555555

This is a One-Dimension Common Register Array.

reserve memory address

Bits	Field	Description	Type	Default
31:0	RSVD_MEM	reserve memory address	RW	0x55555555

Bits	Field	Description	Type	Default
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## RSVD\_ALE\_DPM

BASE ADDRESS : 0xBB01C3D0  
 ARRAY INDEX : 0 - 15  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x55555555

This is a One-Dimension Common Register Array.

reserve memory address

Bits	Field	Description	Type	Default
31:0	RSVD_MEM	reserve memory address	RW	0x55555555

## RSVD\_ALE\_L2

BASE ADDRESS : 0xBB0170C0  
 ARRAY INDEX : 0 - 15  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x55555555

This is a One-Dimension Common Register Array.

reserve memory address

Bits	Field	Description	Type	Default
31:0	RSVD_MEM	reserve memory address	RW	0x55555555

## RSVD\_ALE\_MLTVLAN

BASE ADDRESS : 0xBB018064  
 ARRAY INDEX : 0 - 15  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x55555555

This is a One-Dimension Common Register Array.

reserve memory address

Bits	Field	Description	Type	Default
31:0	RSVD_MEM	reserve memory address	RW	0x55555555

**RSVD\_ALE\_SVLAN**

BASE ADDRESS : 0xBB014414  
ARRAY INDEX : 0 - 15  
ARRAY OFFSET : 0x4  
DEFAULT VALUE : 0x55555555

This is a One-Dimension Common Register Array.

reserve memory address

Bits	Field	Description	Type	Default
31:0	RSVD_MEM	reserve memory address	RW	0x55555555

**RSVD\_ALE\_EEE\_LLDP**

BASE ADDRESS : 0xBB019004  
ARRAY INDEX : 0 - 15  
ARRAY OFFSET : 0x4  
DEFAULT VALUE : 0x55555555

This is a One-Dimension Common Register Array.

reserve memory address

Bits	Field	Description	Type	Default
31:0	RSVD_MEM	reserve memory address	RW	0x55555555

**RSVD\_ALE\_RLDP**

BASE ADDRESS : 0xBB01A03C  
ARRAY INDEX : 0 - 15  
ARRAY OFFSET : 0x4  
DEFAULT VALUE : 0x55555555

This is a One-Dimension Common Register Array.

reserve memory address

Bits	Field	Description	Type	Default
31:0	RSVD_MEM	reserve memory address	RW	0x55555555

**RSVD\_ALE\_EAV\_AFBK**

BASE ADDRESS : 0xBB01B05C  
ARRAY INDEX : 0 - 15  
ARRAY OFFSET : 0x4  
DEFAULT VALUE : 0x55555555

This is a One-Dimension Common Register Array.

reserve memory address

Bits	Field	Description	Type	Default
31:0	RSVD_MEM	reserve memory address	RW	0x55555555

## RSVD\_INTR

BASE ADDRESS : 0xBB01D020  
ARRAY INDEX : 0 - 15  
ARRAY OFFSET : 0x4  
DEFAULT VALUE : 0x55555555

This is a One-Dimension Common Register Array.

reserve memory address

Bits	Field	Description	Type	Default
31:0	RSVD_MEM	reserve memory address	RW	0x55555555

## RSVD\_LED

BASE ADDRESS : 0xBB01E0C4  
ARRAY INDEX : 0 - 15  
ARRAY OFFSET : 0x4  
DEFAULT VALUE : 0x55555555

This is a One-Dimension Common Register Array.

reserve memory address

Bits	Field	Description	Type	Default
31:0	RSVD_MEM	reserve memory address	RW	0x55555555

## RSVD\_PER\_PORT\_MAC

BASE ADDRESS : 0xBB02007C  
PORT INDEX : 0 - 6

PORT OFFSET : 0x400  
 ARRAY INDEX : 0 - 15  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x55555555

This is a Two-Dimension Port Register Array.

reserve memory address

Bits	Field	Description	Type	Default
31:0	RSVD_MEM	reserve memory address	RW	0x55555555

## RSVD\_SDSREG

BASE ADDRESS : 0xBB022150  
 ARRAY INDEX : 0 - 15  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x55555555

This is a One-Dimension Common Register Array.

reserve memory address

Bits	Field	Description	Type	Default
31:0	RSVD_MEM	reserve memory address	RW	0x55555555

## RSVD\_SWCORE

BASE ADDRESS : 0xBB023270  
 ARRAY INDEX : 0 - 15  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x55555555

This is a One-Dimension Common Register Array.

reserve memory address

Bits	Field	Description	Type	Default
31:0	RSVD_MEM	reserve memory address	RW	0x55555555

## RSVD\_EPON\_CTRL

BASE ADDRESS : 0xBB0361EC  
 ARRAY INDEX : 0 - 15



ARRAY OFFSET : 0x4  
DEFAULT VALUE : 0x55555555

This is a One-Dimension Common Register Array.

reserve memory address

Bits	Field	Description	Type	Default
31:0	RSVD_MEM	reserve memory address	RW	0x55555555

## RSVD\_ALE\_RMA\_ATTACK

BASE ADDRESS : 0xBB026018  
ARRAY INDEX : 0 - 15  
ARRAY OFFSET : 0x4  
DEFAULT VALUE : 0x55555555

This is a One-Dimension Common Register Array.

reserve memory address

Bits	Field	Description	Type	Default
31:0	RSVD_MEM	reserve memory address	RW	0x55555555

## RSVD\_BIST\_CTRL

BASE ADDRESS : 0xBB03104C  
ARRAY INDEX : 0 - 15  
ARRAY OFFSET : 0x4  
DEFAULT VALUE : 0x55555555

This is a One-Dimension Common Register Array.

reserve memory address

Bits	Field	Description	Type	Default
31:0	RSVD_MEM	reserve memory address	RW	0x55555555

## RSVD\_EGR\_OUTQ

BASE ADDRESS : 0xBB02D134  
ARRAY INDEX : 0 - 15  
ARRAY OFFSET : 0x4  
DEFAULT VALUE : 0x55555555

This is a One-Dimension Common Register Array.

reserve memory address

Bits	Field	Description	Type	Default
31:0	RSVD_MEM	reserve memory address	RW	0x55555555

## RSVD\_EGR\_SCH

BASE ADDRESS : 0xBB02DE50

ARRAY INDEX : 0 - 15

ARRAY OFFSET : 0x4

DEFAULT VALUE : 0x55555555

This is a One-Dimension Common Register Array.

reserve memory address

Bits	Field	Description	Type	Default
31:0	RSVD_MEM	reserve memory address	RW	0x55555555

## RSVD\_ALE\_HSA

BASE ADDRESS : 0xBB02A250

ARRAY INDEX : 0 - 15

ARRAY OFFSET : 0x4

DEFAULT VALUE : 0x55555555

This is a One-Dimension Common Register Array.

reserve memory address

Bits	Field	Description	Type	Default
31:0	RSVD_MEM	reserve memory address	RW	0x55555555

## RSVD\_ALE\_METER

BASE ADDRESS : 0xBB025114

ARRAY INDEX : 0 - 15

ARRAY OFFSET : 0x4

DEFAULT VALUE : 0x55555555

This is a One-Dimension Common Register Array.

reserve memory address

Bits	Field	Description	Type	Default
31:0	RSVD_MEM	reserve memory address	RW	0x55555555

## RSVD\_MIB\_CTRL

BASE ADDRESS : 0xBB034020  
 ARRAY INDEX : 0 - 15  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x55555555

This is a One-Dimension Common Register Array.

reserve memory address

Bits	Field	Description	Type	Default
31:0	RSVD_MEM	reserve memory address	RW	0x55555555

## RSVD\_ALE\_PISO

BASE ADDRESS : 0xBB027040  
 ARRAY INDEX : 0 - 15  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x55555555

This is a One-Dimension Common Register Array.

reserve memory address

Bits	Field	Description	Type	Default
31:0	RSVD_MEM	reserve memory address	RW	0x55555555

## HSA\_TX\_DBG

BASE ADDRESS : 0xBB02A290  
 ARRAY INDEX : 0 - 15  
 ARRAY OFFSET : 0x4  
 DEFAULT VALUE : 0x0

This is a One-Dimension Common Register Array.

debug for has\_bus

Bits	Field	Description	Type	Default
31:0	DBG_HSA_BUS	dbg for tx bus has	RO	0x0

## BYTE\_TOKEN\_METER

REGISTER ADDRESS : 0xBB02DE90

DEFAULT VALUE : 0x42

Bits	Field	Description	Type	Default
31:8	RESERVED			
7:0	BYTES_PERTKN_BWMTR	bytes per token for ONU bandwidth meter	RW	0x42

## HSARAM\_5\_CFG

REGISTER ADDRESS : 0xBB02A2D0

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:5	RESERVED			
4	HSARAM_5_DVSE		RW	0x0
3:0	HSARAM_5_DVS		RW	0x0

## DBG\_EP\_CFG

REGISTER ADDRESS : 0xBB02A2D4

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:3	RESERVED			
2:0	DBG_EP	selection port to store packet information	RW	0x0

## TRUNK\_DROP\_CFG

REGISTER ADDRESS : 0xBB02A2D8

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	TRUNK_DROP		RW	0x0

Bits	Field	Description	Type	Default
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## PAUSE\_ALL\_LW\_CFG

REGISTER ADDRESS : 0xBB02A2DC

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	PAUSE_ALL_LW		RW	0x0

## HYS\_PUSAL\_CFG

REGISTER ADDRESS : 0xBB02A2E0

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	HYS_PUSAL		RW	0x0

## EPON\_DECRYPT\_CFG

REGISTER ADDRESS : 0xBB03622C

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:2	RESERVED			
1:0	EPON_DECRYPT	epon decryption mode	RW	0x0

## EPON\_DECRYPT\_KEY0

BASE ADDRESS : 0xBB036230

ARRAY INDEX : 0 - 7

ARRAY OFFSET : 24 bits

DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (24 bits per field)

Bits	Field	Description	Type	Default
23:0	EPON_DECRYPT_KEY0	epon decryption key0	RW	0x0

Bits	Field	Description	Type	Default
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## EPON\_DECRYPT\_KEY1

BASE ADDRESS : 0xBB036250  
 ARRAY INDEX : 0 - 7  
 ARRAY OFFSET : 24 bits  
 DEFAULT VALUE : 0x0

This is a One-Dimension Register Field Array. (24 bits per field)

Bits	Field	Description	Type	Default
23:0	EPON_DECRYPT_KEY1	epon decryption key1	RW	0x0

## EPON\_MISC\_CFG

REGISTER ADDRESS : 0xBB036270  
 DEFAULT VALUE : 0x2

Bits	Field	Description	Type	Default
31:2	RESERVED			
1	GMII_RXER_EN		RW	0x1
0	PRB_LST_GN		RW	0x0

## CHANGE\_DUPLEX\_CTRL

REGISTER ADDRESS : 0xBB0232B0  
 DEFAULT VALUE : 0x22

Bits	Field	Description	Type	Default
31:8	RESERVED			
7	CFG_CHG_DUP_EN	change duplex function enable 0 : disable 1 : enable	RW	0x0
6:2	CFG_CHG_DUP_THR	change duplex function threshold	RW	0x08
1	CFG_CHG_DUP_CONGEST	if include force collision which caused by congestion 0 : filter force collision which caused by congestion 1 : include force collision which caused by congestion	RW	0x1

Bits	Field	Description	Type	Default
0	CFG_CHG_DUP_REF	when to change duplex 1 : ck_txcom & rxdv = 0 0 : ck_txcom = 0	RW	0x0

## RLDP\_BUZZER

REGISTER ADDRESS : 0xBB01E104

DEFAULT VALUE : 0x0

Bits	Field	Description	Type	Default
31:1	RESERVED			
0	LED_LOOP_DET_BUZZER_EN		RW	0x0

## PON\_LED\_CFG

REGISTER ADDRESS : 0xBB01E108

DEFAULT VALUE : 0x3

Bits	Field	Description	Type	Default
31:2	RESERVED			
1	SWLED_PONN_ALARM		RW	0x1
0	SWLED_PON_WARN		RW	0x1

## FB\_GPHY\_ADDR\_CTRL

REGISTER ADDRESS : 0xBB01B09C

DEFAULT VALUE : 0x100A44

Configure auto-fallback GPHY Address

Bits	Field	Description	Type	Default
31:21	RESERVED			
20:16	GPHY_REG_ADDR		RW	0x10
15:0	GPHY_REG_PAGE		RW	0x0A44

## HSA\_DEBUG\_DATA

TABLE TYPE : 0x0

TABLE INDEX : 0 - 0

## HSA tx bus debug information

Bits	Field	Description
511:474	TXHSA0_RESERVED_02	
473:471	TXHSA1_EP	
470:467	TXHSA1_DSL_VC	
466:451	TXHSA1_34PPPOE	
450:403	TXHSA1_34SMAC	
402:397	TXHSA1_RSV0	
396	TXHSA1_TTLPMASK	
395:391	TXHSA1_TTLEXMSK	
390:343	TXHSA1_NEWMAC	
342:327	TXHSA1_NEWPRT	
326:295	TXHSA1_NEWIP	
294:279	TXHSA1_L4CKSUM	
278:263	TXHSA1_L3CKSUM	
262:261	TXHSA1_PPPOEACT	
260	TXHSA1_SRC_MOD	
259	TXHSA1_L34TRANS	
258	TXHSA1_L2TRANS	
257	TXHSA1_ORG	
256	TXHSA1_L3R	
255:232	TXHSA0_RESERVED_01	
231	TXHSA0_SV_DEI	
230	TXHSA0_STYP	
229:216	TXHSA0_PKTLEN_ORI	
215:209	TXHSA0_QID	
208:196	TXHSA0_STDSC	
195:193	TXHSA0_CPUPRI	
192:190	TXHSA0_SPRI	
189	TXHSA0_CORI	
188	TXHSA0_CMDY	
187	TXHSA0_CRMS	
186	TXHSA0_CINS	
185:174	TXHSA0_CVID	
173:172	TXHSA0_RSV1	
171	TXHSA0_CFI	
170:139	TXHSA0_PTPNSEC	
138:91	TXHSA0_PTPSEC	
90:89	TXHSA0_PTPACT	
88	TXHSA0_REGENCRC	
87	TXHSA0_PPPOE	
86	TXHSA0_RFC1042	
85	TXHSA0_IPV6	
84	TXHSA0_IPV4	



Bits	Field	Description
83	TXHSA0_PTP	
82:77	TXHSA0_REMDSCP_PRI	
76:74	TXHSA0_REM1Q_PRI	
73	TXHSA0_REMDSCP_EN	
72	TXHSA0_REM1Q_EN	
71:60	TXHSA0_SVID	
59	TXHSA0_INSTAG	
58	TXHSA0_INCTAG	
57:44	TXHSA0_PKTLEN	
43:41	TXHSA0_SPA	
40:37	TXHSA0_DPC	
36:31	TXHSA0_EXTMSK	
30:15	TXHSA0_VCMSK	
14:8	TXHSA0_PONSID	
7:0	TXHSA0_TRPRSN	



# Index: Alphabetical List

Alphabetical List of Registers and Tables. This section is a quick reference to all the tables and register in this datasheet.

## A

All registers and tables starting with a A.

Register	Address	Default	Reference
ABLTY_FORCE_MODE	0xBB000124	0x0	Page <a href="#">34</a>
ACCEPT_MAX_LEN_CTRL	0xBB01100C	0x0	Page <a href="#">52</a>
ACL_ACTION	0xBB01510C	0x7F	Page <a href="#">276</a>
ACL_ACTION_TABLE	<Indirect> Type:3 Size:128	—	Page <a href="#">311</a>
ACL_CFG	0xBB01530C	0x0	Page <a href="#">276</a>
ACL_DATA	<Indirect> Type:2 Size:64	—	Page <a href="#">312</a>
ACL_DATA2	<Indirect> Type:2 Size:64	—	Page <a href="#">312</a>
ACL_EN	0xBB015104	0x0	Page <a href="#">275</a>
ACL_MASK	<Indirect> Type:2 Size:64	—	Page <a href="#">313</a>
ACL_MASK2	<Indirect> Type:2 Size:64	—	Page <a href="#">314</a>
ACL_PERMIT	0xBB015108	0x0	Page <a href="#">275</a>
ACL_TEMPLATE_CTRL	0xBB015000	0x0	Page <a href="#">273</a>
AD5_ALARM	0xBB000178	0x0	Page <a href="#">41</a>
AD5_CTRL	0xBB000160	0x136	Page <a href="#">39</a>
AD5_DATA	0xBB00017C	0x0	Page <a href="#">42</a>
AFE_VER	0xBB00014C	0x0	Page <a href="#">37</a>
ALL_PORT_LKDN_TIME	0xBB000154	0x0	Page <a href="#">38</a>
APR_EN_PORT_CFG	0xBB02D8B0	0x0	Page <a href="#">268</a>
APR_METER_PORT_CFG	0xBB02D8D0	0x0	Page <a href="#">269</a>
ARP_TABLE	<Indirect> Type:8 Size:512	—	Page <a href="#">396</a>
ARP_TRF0	0xBB800500	0x0	Page <a href="#">416</a>
ARP_TRF1	0xBB800600	0x0	Page <a href="#">416</a>
AVB_PORT_EN	0xBB0110F4	0x0	Page <a href="#">327</a>
AVB_PRI_REMAP	0xBB0110F8	0x0	Page <a href="#">327</a>

## B

All registers and tables starting with a B.

Register	Address	Default	Reference
BD_CFG	0xBB800030	0x0	Page 409
BD_TRF	0xBB80002C	0x0	Page 409
BINDING_TABLE	<Indirect> Type:6 Size:32	—	Page 396
BIST_CFG	0xBB000070	0x0	Page 18
BIST_CFG0	0xBB03103C	0x0	Page 17
BIST_CFG1	0xBB031038	0x0	Page 17
BIST_CFG12	0xBB03101C	0x0	Page 16
BIST_CFG13	0xBB031018	0x0	Page 15
BIST_CFG14	0xBB031014	0x0	Page 15
BIST_CFG15	0xBB031010	0x0	Page 15
BIST_CFG16	0xBB03100C	0x0	Page 15
BIST_CFG17	0xBB031008	0x0	Page 14
BIST_CFG18	0xBB031004	0x0	Page 14
BIST_CFG19	0xBB031000	0x0	Page 14
BIST_CFG2	0xBB031034	0x0	Page 17
BIST_CFG3	0xBB031030	0x0	Page 17
BIST_CFG4	0xBB03102C	0x0	Page 16
BIST_CFG7	0xBB031028	0x0	Page 16
BIST_CFG8	0xBB031024	0x0	Page 16
BIST_CFG9	0xBB031020	0x0	Page 16
BOND_INFO	0xBB010008	0x0	Page 28
BOND_STRAP_STS0	0xBB000194	0x0	Page 43
BOND_STRAP_STS1	0xBB000198	0x0	Page 44
BOND_STRAP_STS2	0xBB00019C	0x0	Page 44
BYPS_ABLTY_LOCK	0xBB000138	0x0	Page 36
BYTE_TOKEN_METER	0xBB02DE90	0x42	Page 434

## C

All registers and tables starting with a C.

Register	Address	Default	Reference
CFG_BACKPRESSURE	0xBB023058	0x2	Page 54
CFG_PCSXF	0xBB000040	0x0	Page 8
CFG_PHY_CTRL	0xBB000044	0x0	Page 8
CFG_PHY_POLL_ADR_0	0xBB00004C	0xA4340000	Page 9
CFG_PHY_POLL_ADR_1	0xBB000050	0x0	Page 9
CFG_PHY_POLL_CMD	0xBB000048	0xB110	Page 9
CFG_PHY_POLL_INV_0	0xBB000054	0x0	Page 10
CFG_PHY_POLL_INV_1	0xBB000058	0x0	Page 10

Register	Address	Default	Reference
CFG_PHY_POLL_WD_0	0xBB00005C	0x0	Page 10
CFG_PHY_POLL_WD_1	0xBB000060	0x0	Page 11
CFG_UNHIOL	0xBB02305C	0xA8	Page 54
CF_ACTION_DS	<Indirect> Type:5 Size:512	—	Page 314
CF_ACTION_US	<Indirect> Type:5 Size:512	—	Page 315
CF_CFG	0xBB0150E0	0x0	Page 274
CF_MASK	<Indirect> Type:4 Size:128	—	Page 316
CF_MASK_L34	<Indirect> Type:4 Size:64	—	Page 318
CF_OP_DS	0xBB015020	0x0	Page 273
CF_OP_US	0xBB015060	0x0	Page 274
CF_RULE	<Indirect> Type:4 Size:128	—	Page 319
CF_RULE_L34	<Indirect> Type:4 Size:64	—	Page 320
CF_VALID	0xBB0150A0	0x0	Page 274
CHANGE_DUPLEX_CTRL	0xBB0232B0	0x22	Page 436
CHIP_DEBUG_OUT	0xBB000064	0x0	Page 11
CHIP_INFO	0xBB010004	0x16266	Page 27
CHIP_INF_SEL	0xBB000184	0x0	Page 42
CHIP_RST	0xBB000068	0x0	Page 11
CLR_MAX_USED_PAGE_CNT	0xBB02313C	0x0	Page 248
CPU_PORT_RATE_CFG	0xBB02D8CC	0x0	Page 268

## D

All registers and tables starting with a D.

Register	Address	Default	Reference
DATA_LED_CFG	0xBB01E004	0x0	Page 22
DBG_BLK_SEL	0xBB0001C8	0x0	Page 295
DBG_EP_CFG	0xBB02A2D4	0x0	Page 434
DBG_HSA_EP	0xBB02A204	0x0	Page 271
DEBUG_SEL	0xBB000128	0x0	Page 34
DFR_TEST_RESUME	0xBB031044	0x0	Page 18
DIAG_MODE	0xBB031040	0x0	Page 18
DIGITAL_INTERFACE_SELECT	0xBB023000	0x0	Page 1
DOS_CFG	0xBB026004	0x0	Page 219
DOS_EN	0xBB026000	0x0	Page 218
DOS_FINFLOOD_TH	0xBB02600C	0x0	Page 221
DOS_ICMPFLOOD_TH	0xBB026010	0x0	Page 221
DOS_SYN Flood_TH	0xBB026008	0x0	Page 221
DOT1X_CFG_0	0xBB01C0BC	0x0	Page 217

Register	Address	Default	Reference
DOT1X_CFG_1	0xBB017090	0x0	Page 217
DOT1X_P_CTRL	0xBB017094	0x0	Page 218
DOT3_BROADCAST_BIT_PLUS_ONU_LLID	0xBB032B2C	0x0	Page 237
DOT3_BROADCAST_NOT_ONUID	0xBB032B30	0x0	Page 237
DOT3_CRC8_ERRORS	0xBB032B34	0x0	Page 238
DOT3_EPON_FEC_CODING_VIO	0xBB032B24	0x0	Page 236
DOT3_EPON_FEC_CORRECTED_BLOCKS	0xBB032B1C	0x0	Page 236
DOT3_EPON_FEC_UNCORRECTED_BLOCKS	0xBB032B20	0x0	Page 236
DOT3_LLID_RX_BROADCAST_DROP_FRAMES	0xBB032B38	0x0	Page 238
DOT3_MPCP_EX_GATE	0xBB032B5C	0x0	Page 238
DOT3_MPCP_RX_DISC	0xBB032B18	0x0	Page 236
DOT3_MPCP_TX_REG_REQ	0xBB032BBC	0x0	Page 239
DOT3_MPCP_TX_REPORT	0xBB032B3C	0x0	Page 238
DOT3_NOT_BROADCAST_BIT_NOT_ONU_LLID	0xBB032B28	0x0	Page 237
DOT3_ONUID_NOT_BROADCAST	0xBB032B7C	0x0	Page 239
DOT3_Q_TX_FRAMES	0xBB032918	0x0	Page 235
Page ??			
Page ??			
Page ??			
Page ??			
Page ??			
Page ??			
Page ??			
Page ??			
Page ??			
Page ??			
Page ??			
DYNGASP_CTRL	0xBB000190	0x7F0	Page 43

## E

All registers and tables starting with a E.

Register	Address	Default	Reference
EEELDP_CTRL_0	0xBB01C0A8	0x0	Page 168
EEELDP_CTRL_1	0xBB01C0AC	0x0	Page 168
EEEP_CFG	0xBB0230A8	0x0	Page 120
EEEP_RX_RATE_100M_CTRL	0xBB0230D0	0x1410	Page 124
EEEP_RX_RATE_500M_CTRL	0xBB0230CC	0x1410	Page 124
EEEP_RX_RATE_GIGA_CTRL	0xBB0230C8	0x1410	Page 123
EEEP_RX_SLEEP_STEP_CTRL	0xBB0230D4	0x1	Page 124
EEEP_RX_TIMER_100M_CTRL	0xBB0230EC	0x800FF0A	Page 127
EEEP_RX_TIMER_500M_CTRL	0xBB0230E4	0x800FF0A	Page 126
EEEP_RX_TIMER_GIGA_CTRL	0xBB0230DC	0x800FF0A	Page 125
EEEP_RX_WAKE_TIMER_100M_CTRL	0xBB0230E8	0x14	Page 126

Register	Address	Default	Reference
EEEP_RX_WAKE_TIMER_500M_CTRL	0xBB0230E0	0x2828	Page <a href="#">126</a>
EEEP_RX_WAKE_TIMER_GIGA_CTRL	0xBB0230D8	0x1414	Page <a href="#">125</a>
EEEP_TIMER_UNIT_CTRL	0xBB0230AC	0x15	Page <a href="#">120</a>
EEEP_TX_100M_CTRL	0xBB0230C4	0x1411	Page <a href="#">123</a>
EEEP_TX_500M_CTRL	0xBB0230C0	0x1410	Page <a href="#">122</a>
EEEP_TX_GIGA_CTRL	0xBB0230BC	0x1411	Page <a href="#">122</a>
EEEP_TX_TIMER_100M_CTRL	0xBB0230B8	0x404	Page <a href="#">121</a>
EEEP_TX_TIMER_500M_CTRL	0xBB0230B4	0x404	Page <a href="#">121</a>
EEEP_TX_TIMER_GIGA_CTRL	0xBB0230B0	0x404	Page <a href="#">121</a>
EEE_100M_CTRL0	0xBB02308C	0x240A	Page <a href="#">117</a>
EEE_100M_CTRL1	0xBB023090	0xC80A	Page <a href="#">117</a>
EEE_BURSTSIZE	0xBB023094	0x1000	Page <a href="#">118</a>
EEE_DECISION_WINDOW	0xBB0230A0	0x2D1010	Page <a href="#">118</a>
EEE_EEEP_PORT_CFG	0xBB020014	0x0	Page <a href="#">112</a>
EEE_GIGA_CTRL0	0xBB023084	0x14140A	Page <a href="#">116</a>
EEE_GIGA_CTRL1	0xBB023088	0xC80A	Page <a href="#">117</a>
EEE_IFG_CFG	0xBB023098	0x1	Page <a href="#">118</a>
EEE_MISC	0xBB023080	0x50	Page <a href="#">115</a>
EEE_RXIDLE	0xBB02309C	0x101	Page <a href="#">118</a>
EEE_RX_FC_REG	0xBB02307C	0x120	Page <a href="#">115</a>
EEE_TX_SEL_CTRL	0xBB0001C0	0x0	Page <a href="#">112</a>
EEE_TX_THR_FE	0xBB023078	0xD	Page <a href="#">115</a>
EEE_TX_THR_GIGA	0xBB023074	0xD	Page <a href="#">114</a>
EFUSE_CFG	0xBB000018	0x0	Page <a href="#">3</a>
EFUSE_IND_CMD	0xBB000020	0x0	Page <a href="#">4</a>
EFUSE_IND_RD	0xBB000024	0x0	Page <a href="#">4</a>
EFUSE_IND_WD	0xBB00001C	0x0	Page <a href="#">4</a>
EGR_BWCTRL_P_CTRL	0xBB02D804	0x3FFFE	Page <a href="#">265</a>
EN_FORCE_P_DMP	0xBB011008	0x0	Page <a href="#">26</a>
EPON_ASIC_TIMING_ADJUST1	0xBB036004	0x0	Page <a href="#">383</a>
EPON_ASIC_TIMING_ADJUST2	0xBB036008	0x0	Page <a href="#">384</a>
EPON_DEBUG1	0xBB036018	0x0	Page <a href="#">385</a>
EPON_DEBUG2	0xBB03601C	0x0	Page <a href="#">386</a>
EPON_DECRYPT_CFG	0xBB03622C	0x0	Page <a href="#">435</a>
EPON_DECRYPT_KEY0	0xBB036230	0x0	Page <a href="#">435</a>
EPON_DECRYPT_KEY1	0xBB036250	0x0	Page <a href="#">436</a>
EPON_FEC_CONFIG	0xBB036000	0x0	Page <a href="#">383</a>
EPON_GRANT_LIST0	0xBB036064	0x0	Page <a href="#">390</a>
EPON_GRANT_LIST1	0xBB0360E4	0x0	Page <a href="#">390</a>
EPON_GRANT_LIST2	0xBB036164	0x0	Page <a href="#">390</a>
EPON_INTR	0xBB036024	0x7	Page <a href="#">386</a>
EPON_MISC_CFG	0xBB036270	0x2	Page <a href="#">436</a>
EPON_MPCP_CTR	0xBB036060	0x0	Page <a href="#">389</a>
EPON_RGSTR1	0xBB03600C	0x0	Page <a href="#">384</a>
EPON_RGSTR2	0xBB036010	0x0	Page <a href="#">385</a>
EPON_RGSTR3	0xBB036014	0x0	Page <a href="#">385</a>

Register	Address	Default	Reference
EPON_STAT_RST	0xBB034018	0x0	Page <a href="#">235</a>
EPON_TIMER_CONFIG1	0xBB036020	0x64	Page <a href="#">386</a>
EPON_TIME_CTRL	0xBB036038	0x0	Page <a href="#">388</a>
EPON_TX_CTRL	0xBB0361E4	0x0	Page <a href="#">391</a>
EP_MISC	0xBB03603C	0x0	Page <a href="#">388</a>
EXTERNAL_IP_TABLE	<Indirect> Type:4 Size:8	—	Page <a href="#">397</a>
EXT_RGMXF	0xBB000004	0x0	Page <a href="#">1</a>
EXT_STS	0xBB000148	0x0	Page <a href="#">37</a>
EXT_TXC_DLY	0xBB000008	0x0	Page <a href="#">2</a>

## F

All registers and tables starting with a F.

Register	Address	Default	Reference
FB_CTRL	0xBB01B000	0x0	Page <a href="#">128</a>
FB_GPHY_ADDR_CTRL	0xBB01B09C	0x100A44	Page <a href="#">437</a>
FB_PORT_CFG	0xBB01B004	0x0	Page <a href="#">129</a>
FB_PORT_ERR_CNT	0xBB01B018	0x0	Page <a href="#">130</a>
FB_PORT_MONITOR_CNT	0xBB01B020	0x0	Page <a href="#">130</a>
FC_CTRL	0xBB023100	0xB	Page <a href="#">241</a>
FC_DBG_CTRL	0xBB02D028	0x0	Page <a href="#">248</a>
FC_DROP_ALL_TH	0xBB023104	0x1B58	Page <a href="#">241</a>
FC_GLB_FCOFF_HI_TH	0xBB02310C	0xCDA0C94	Page <a href="#">242</a>
FC_GLB_FCOFF_LO_TH	0xBB023110	0xC080BC2	Page <a href="#">242</a>
FC_GLB_HI_TH	0xBB023114	0xCDA0C94	Page <a href="#">243</a>
FC_GLB_LO_TH	0xBB023118	0xC080BC2	Page <a href="#">243</a>
FC_JUMBO_GLB_HI_TH	0xBB02312C	0x173E02BC	Page <a href="#">245</a>
FC_JUMBO_GLB_LO_TH	0xBB023130	0x0	Page <a href="#">245</a>
FC_JUMBO_P_HI_TH	0xBB023134	0x41A0348	Page <a href="#">245</a>
FC_JUMBO_P_LO_TH	0xBB023138	0x39C0150	Page <a href="#">246</a>
FC_PAUSE_ALL_TH	0xBB023108	0x1A86	Page <a href="#">242</a>
FC_PE_USED_PAGE_CNT	0xBB02D030	0x0	Page <a href="#">249</a>
FC_PON_GLB_HI_TH	0xBB02316C	0x7780746	Page <a href="#">252</a>
FC_PON_GLB_LO_TH	0xBB023170	0x3520320	Page <a href="#">252</a>
FC_PON_P_HI_TH	0xBB023174	0x12C00FA	Page <a href="#">252</a>
FC_PON_P_LO_TH	0xBB023178	0x140014	Page <a href="#">253</a>
FC_PON_Q_EGR_DROP_EN	0xBB01C3BC	0x1	Page <a href="#">335</a>
FC_PON_Q_EGR_DROP_IDX	0xBB02317C	0x0	Page <a href="#">253</a>
FC_PON_Q_EGR_DROP_TH	0xBB0231B0	0xF0	Page <a href="#">253</a>
FC_PON_Q_EGR_GAP_TH	0xBB0231C0	0x18	Page <a href="#">254</a>
FC_PON_Q_USED_PAGE_CNT	0xBB0231C8	0x0	Page <a href="#">254</a>
FC_PON_Q_USED_PAGE_CTRL	0xBB0231C4	0x0	Page <a href="#">254</a>
FC_PUB_FCOFF_USED_PAGE_CNT	0xBB023148	0x0	Page <a href="#">250</a>



Register	Address	Default	Reference
FC_PUB_JUMBO_USED_PAGE_CNT	0xBB02314C	0x0	Page <a href="#">251</a>
FC_PUB_USED_PAGE_CNT	0xBB023144	0x0	Page <a href="#">250</a>
FC_P_DBG_PKT_PAGE_CNT	0xBB020038	0x0	Page <a href="#">251</a>
FC_P_EGR_DROP_TH	0xBB02D010	0x1B58	Page <a href="#">246</a>
FC_P_EGR_GAP_TH	0xBB02D024	0x15E	Page <a href="#">247</a>
FC_P_FCOFF_HI_TH	0xBB023124	0x54004EC	Page <a href="#">244</a>
FC_P_FCOFF_LO_TH	0xBB023128	0xE00054	Page <a href="#">244</a>
FC_P_HI_TH	0xBB02311C	0x54004EC	Page <a href="#">243</a>
FC_P_LO_TH	0xBB023120	0xE00054	Page <a href="#">244</a>
FC_P_Q_EGR_DROP_EN	0xBB01C0D8	0x1	Page <a href="#">247</a>
FC_P_USED_PAGE_CNT	0xBB023150	0x0	Page <a href="#">251</a>
FC_Q_EGR_DROP_TH	0xBB02D000	0x2BC	Page <a href="#">246</a>
FC_Q_EGR_GAP_TH	0xBB02D020	0xA8	Page <a href="#">247</a>
FC_Q_USED_PAGE_CNT	0xBB02D04C	0x0	Page <a href="#">249</a>
FC_TL_USED_PAGE_CNT	0xBB023140	0x0	Page <a href="#">250</a>
FC_TOTAL_PAGE_CNT	0xBB02D02C	0x0	Page <a href="#">248</a>
FIB_EXT_REG0	0xBB022E00	0x1140	Page <a href="#">105</a>
FIB_EXT_REG1	0xBB022E04	0x6109	Page <a href="#">106</a>
FIB_EXT_REG13	0xBB022E30	0x0	Page <a href="#">108</a>
FIB_EXT_REG14	0xBB022E34	0x0	Page <a href="#">108</a>
FIB_EXT_REG16	0xBB022E3C	0x416	Page <a href="#">108</a>
FIB_EXT_REG17	0xBB022E40	0x0	Page <a href="#">108</a>
FIB_EXT_REG18	0xBB022E44	0x124	Page <a href="#">109</a>
FIB_EXT_REG19	0xBB022E48	0x31B	Page <a href="#">109</a>
FIB_EXT_REG2	0xBB022E08	0x0	Page <a href="#">106</a>
FIB_EXT_REG20	0xBB022E4C	0x1F33	Page <a href="#">109</a>
FIB_EXT_REG21	0xBB022E50	0x0	Page <a href="#">109</a>
FIB_EXT_REG22	0xBB022E54	0x0	Page <a href="#">110</a>
FIB_EXT_REG23	0xBB022E58	0x1408	Page <a href="#">110</a>
FIB_EXT_REG24	0xBB022E5C	0x0	Page <a href="#">110</a>
FIB_EXT_REG25	0xBB022E60	0x0	Page <a href="#">110</a>
FIB_EXT_REG26	0xBB022E64	0x0	Page <a href="#">111</a>
FIB_EXT_REG27	0xBB022E68	0x0	Page <a href="#">111</a>
FIB_EXT_REG28	0xBB022E6C	0x0	Page <a href="#">111</a>
FIB_EXT_REG29	0xBB022E70	0x0	Page <a href="#">111</a>
FIB_EXT_REG30	0xBB022E74	0x0	Page <a href="#">112</a>
FIB_EXT_REG4	0xBB022E0C	0x1A0	Page <a href="#">106</a>
FIB_EXT_REG5	0xBB022E10	0x0	Page <a href="#">107</a>
FIB_EXT_REG6	0xBB022E14	0x0	Page <a href="#">107</a>
FIB_EXT_REG7	0xBB022E18	0x4	Page <a href="#">107</a>
FIB_EXT_REG8	0xBB022E1C	0x0	Page <a href="#">107</a>
FIB_REG0	0xBB022C00	0x1140	Page <a href="#">100</a>
FIB_REG1	0xBB022C04	0x6109	Page <a href="#">100</a>
FIB_REG13	0xBB022C30	0x0	Page <a href="#">102</a>
FIB_REG14	0xBB022C34	0x0	Page <a href="#">102</a>
FIB_REG16	0xBB022C3C	0x83	Page <a href="#">103</a>

Register	Address	Default	Reference
FIB_REG17	0xBB022C40	0x0	Page 103
FIB_REG18	0xBB022C44	0x0	Page 103
FIB_REG19	0xBB022C48	0x0	Page 103
FIB_REG2	0xBB022C08	0x0	Page 101
FIB_REG20	0xBB022C4C	0x0	Page 104
FIB_REG21	0xBB022C50	0x0	Page 104
FIB_REG22	0xBB022C54	0x1	Page 104
FIB_REG23	0xBB022C58	0x4001	Page 104
FIB_REG28	0xBB022C5C	0x33FA	Page 104
FIB_REG29	0xBB022C60	0xE46A	Page 105
FIB_REG30	0xBB022C64	0x71E	Page 105
FIB_REG4	0xBB022C0C	0x1A0	Page 101
FIB_REG5	0xBB022C10	0x0	Page 101
FIB_REG6	0xBB022C14	0x0	Page 101
FIB_REG7	0xBB022C18	0x4	Page 102
FIB_REG8	0xBB022C1C	0x0	Page 102
FIFO_ERR_STS	0xBB00013C	0x0	Page 36
FORCE_P_ABLTY	0xBB000088	0x0	Page 29
FORCE_P_DMP	0xBB011000	0x0	Page 25
FPGA_VER_MAC	0xBB023040	0x0	Page 51

## G

All registers and tables starting with a G.

Register	Address	Default	Reference
GATING_CLK_1	0xBB0000AC	0x0	Page 30
GLB_MAC_MISC	0xBB023034	0x0	Page 26
GPHY_AFE_DBG_CFG	0xBB00015C	0x0	Page 39
GPHY_IND_CMD	0xBB000010	0x0	Page 3
GPHY_IND_RD	0xBB000014	0x0	Page 3
GPHY_IND_WD	0xBB00000C	0x0	Page 2
GPIO_CTRL_0	0xBB0000D0	0x0	Page 31
GPIO_CTRL_1	0xBB0000DC	0x0	Page 31
GPIO_CTRL_2	0xBB0000E8	0x0	Page 32
GPIO_CTRL_3	0xBB0000F4	0x0	Page 32
GPIO_CTRL_4	0xBB000100	0x0	Page 32
GPON_AES_BYPASS	0xBB700020	0x0	Page 340
GPON_AES_INTR_DLT	0xBB703000	0x0	Page 358
GPON_AES_INTR_MASK	0xBB703004	0x0	Page 359
GPON_AES_INTR_STS	0xBB703008	0x0	Page 359
GPON_AES_KEY_SWITCH_REQ	0xBB703010	0x0	Page 359
GPON_AES_KEY_SWITCH_TIME	0xBB703014	0x0	Page 360
GPON_AES_KEY_WORD_IND	0xBB703020	0x0	Page 360
GPON_AES_WORD_DATA	0xBB703024	0x0	Page 361

Register	Address	Default	Reference
GPON_BWMAP_CTRL	0xBB70200C	0x0	Page <a href="#">357</a>
GPON_BWMAP_DATA	0xBB702400	0x0	Page <a href="#">358</a>
GPON_BWMAP_STS	0xBB702010	0x0	Page <a href="#">358</a>
GPON_DPRU_RPT_PRD	0xBB02D128	0x0	Page <a href="#">336</a>
GPON_GEM_DS_FRM_TIMEOUT	0xBB704098	0x110	Page <a href="#">365</a>
GPON_GEM_DS_FWD_CNTR_IND	0xBB70404C	0x0	Page <a href="#">362</a>
GPON_GEM_DS_FWD_CNTR_STAT	0xBB704050	0x0	Page <a href="#">362</a>
GPON_GEM_DS_MC_ADDR_PTN_IPV4	0xBB70409C	0x1005E	Page <a href="#">365</a>
GPON_GEM_DS_MC_ADDR_PTN_IPV6	0xBB7040A0	0x3333	Page <a href="#">366</a>
GPON_GEM_DS_MC_CFG	0xBB704080	0x8	Page <a href="#">363</a>
GPON_GEM_DS_MC_IND	0xBB704084	0x0	Page <a href="#">364</a>
GPON_GEM_DS_MC_RD	0xBB704090	0x0	Page <a href="#">365</a>
GPON_GEM_DS_MC_WR	0xBB704088	0x0	Page <a href="#">365</a>
GPON_GEM_DS_MISC_CNTR_STAT	0xBB704068	0x0	Page <a href="#">363</a>
GPON_GEM_DS_MISC_IND	0xBB704064	0x0	Page <a href="#">363</a>
GPON_GEM_DS_RX_CNTR_IND	0xBB704040	0x0	Page <a href="#">361</a>
GPON_GEM_DS_RX_CNTR_STAT	0xBB704044	0x0	Page <a href="#">362</a>
GPON_GEM_US_BYTE_STAT	0xBB706800	0x0	Page <a href="#">380</a>
GPON_GEM_US_ETH_GEM_RX_CNTR_IDX	0xBB706048	0x0	Page <a href="#">379</a>
GPON_GEM_US_ETH_GEM_RX_CNTR_STAT	0xBB70604C	0x0	Page <a href="#">379</a>
GPON_GEM_US_INTR_DLT	0xBB706000	0x0	Page <a href="#">375</a>
GPON_GEM_US_INTR_MASK	0xBB706004	0x0	Page <a href="#">376</a>
GPON_GEM_US_INTR_STS	0xBB706008	0x0	Page <a href="#">377</a>
GPON_GEM_US_PORT_MAP	0xBB706400	0x0	Page <a href="#">380</a>
GPON_GEM_US_PTI_CFG	0xBB706020	0x5410	Page <a href="#">378</a>
GPON_GEM_US_PTN_CTRL	0xBB706054	0x55	Page <a href="#">379</a>
GPON_GTC_DS_ALLOC_IND	0xBB7010C0	0x0	Page <a href="#">347</a>
GPON_GTC_DS_ALLOC_RD	0xBB7010CC	0x0	Page <a href="#">348</a>
GPON_GTC_DS_ALLOC_WR	0xBB7010C4	0x0	Page <a href="#">348</a>
GPON_GTC_DS_CFG	0xBB701014	0x602	Page <a href="#">344</a>
GPON_GTC_DS_ETH_PTI	0xBB701208	0x11	Page <a href="#">356</a>
GPON_GTC_DS_INTR_DLT	0xBB701000	0x0	Page <a href="#">342</a>
GPON_GTC_DS_INTR_MASK	0xBB701004	0x0	Page <a href="#">343</a>
GPON_GTC_DS_INTR_STS	0xBB701008	0x2	Page <a href="#">343</a>
GPON_GTC_DS_LOS_CFG_STS	0xBB701040	0x0	Page <a href="#">345</a>
GPON_GTC_DS_MISC_CNTR_ACTIVE	0xBB7011B0	0x0	Page <a href="#">354</a>
GPON_GTC_DS_MISC_CNTR_BIP_ERR_BIT	0xBB701188	0x0	Page <a href="#">351</a>
GPON_GTC_DS_MISC_CNTR_BIP_ERR_BLK	0xBB701184	0x0	Page <a href="#">351</a>
GPON_GTC_DS_MISC_CNTR_BWM_ACPT	0xBB7011B4	0x0	Page <a href="#">354</a>
GPON_GTC_DS_MISC_CNTR_BWM_FAIL	0xBB7011A8	0x0	Page <a href="#">353</a>
GPON_GTC_DS_MISC_CNTR_BWM_INV	0xBB7011AC	0x0	Page <a href="#">353</a>
GPON_GTC_DS_MISC_CNTR_FEC_CORRECT_BIT	0xBB70118C	0x0	Page <a href="#">351</a>
GPON_GTC_DS_MISC_CNTR_FEC_CORRECT_BYTE	0xBB701190	0x0	Page <a href="#">351</a>

Register	Address	Default	Reference
GPON_GTC_DS_MISC_CNTR_FEC_CORRECT_CW	0xBB701194	0x0	Page <a href="#">352</a>
GPON_GTC_DS_MISC_CNTR_FEC_UNCOR_CW	0xBB701198	0x0	Page <a href="#">352</a>
GPON_GTC_DS_MISC_CNTR_GEM_FAIL	0xBB7011C4	0x0	Page <a href="#">355</a>
GPON_GTC_DS_MISC_CNTR_GEM_IDLE	0xBB7011C0	0x0	Page <a href="#">355</a>
GPON_GTC_DS_MISC_CNTR_GEM_LOS	0xBB7011B8	0x0	Page <a href="#">354</a>
GPON_GTC_DS_MISC_CNTR_GEM_NON_IDLE	0xBB7011C8	0x0	Page <a href="#">355</a>
GPON_GTC_DS_MISC_CNTR_HEC_CORRECT	0xBB7011BC	0x0	Page <a href="#">355</a>
GPON_GTC_DS_MISC_CNTR_LOM	0xBB70119C	0x0	Page <a href="#">352</a>
GPON_GTC_DS_MISC_CNTR_PLEN_CORRECT	0xBB7011CC	0x0	Page <a href="#">356</a>
GPON_GTC_DS_MISC_CNTR_PLOAM_ACPT	0xBB7011A0	0x0	Page <a href="#">352</a>
GPON_GTC_DS_MISC_CNTR_PLOAM_FAIL	0xBB7011A4	0x0	Page <a href="#">353</a>
GPON_GTC_DS_OMCI_PTI	0xBB701204	0x55	Page <a href="#">356</a>
GPON_GTC_DS_ONU_ID_STATUS	0xBB701010	0xFF01	Page <a href="#">344</a>
GPON_GTC_DS_PLOAM_CFG	0xBB70101C	0x70B	Page <a href="#">345</a>
GPON_GTC_DS_PLOAM_IND	0xBB701080	0x20	Page <a href="#">346</a>
GPON_GTC_DS_PLOAM_MSG	0xBB7010A0	0x0	Page <a href="#">347</a>
GPON_GTC_DS_PORT_CNTR_IND	0xBB701140	0x0	Page <a href="#">350</a>
GPON_GTC_DS_PORT_CNTR_STAT	0xBB701144	0x0	Page <a href="#">350</a>
GPON_GTC_DS_PORT_IND	0xBB701100	0x0	Page <a href="#">348</a>
GPON_GTC_DS_PORT_RD	0xBB70110C	0x0	Page <a href="#">349</a>
GPON_GTC_DS_PORT_WR	0xBB701104	0x0	Page <a href="#">349</a>
GPON_GTC_DS_SUPERFRAME_CNT	0xBB701048	0x0	Page <a href="#">346</a>
GPON_GTC_DS_TRAFFIC_CFG	0xBB701400	0x0	Page <a href="#">357</a>
GPON_GTC_US_BOH_CFG	0xBB705054	0x880	Page <a href="#">371</a>
GPON_GTC_US_BOH_DATA	0xBB705080	0x0	Page <a href="#">371</a>
GPON_GTC_US_CFG	0xBB705014	0x18	Page <a href="#">368</a>
GPON_GTC_US_DG	0xBB705184	0x3	Page <a href="#">374</a>
GPON_GTC_US_EQD	0xBB705044	0x9100	Page <a href="#">370</a>
GPON_GTC_US_INTR_DLT	0xBB705000	0x0	Page <a href="#">366</a>
GPON_GTC_US_INTR_MASK	0xBB705004	0x0	Page <a href="#">367</a>
GPON_GTC_US_INTR_STS	0xBB705008	0x0	Page <a href="#">367</a>
GPON_GTC_US_LASER	0xBB70504C	0x2018	Page <a href="#">371</a>
GPON_GTC_US_MIN_DELAY	0xBB705040	0x9132	Page <a href="#">370</a>
GPON_GTC_US_MISC_CNTR_IDX	0xBB705140	0x0	Page <a href="#">374</a>
GPON_GTC_US_MISC_CNTR_STAT	0xBB705148	0x0	Page <a href="#">374</a>
GPON_GTC_US_ONU_ID	0xBB705010	0xFF00	Page <a href="#">368</a>
GPON_GTC_US_OPTIC_SD_TH	0xBB705188	0xA4BFA	Page <a href="#">375</a>
GPON_GTC_US_PLOAM_CFG	0xBB705100	0x3	Page <a href="#">373</a>
GPON_GTC_US_PLOAM_DATA	0xBB7050E0	0x0	Page <a href="#">373</a>
GPON_GTC_US_PLOAM_IND	0xBB7050C0	0xA0	Page <a href="#">372</a>
GPON_GTC_US_PROC_MODE	0xBB705200	0x1	Page <a href="#">375</a>
GPON_GTC_US_RDI	0xBB705180	0x0	Page <a href="#">374</a>
GPON_GTC_US_TX_PATTERN_BG	0xBB705024	0x0	Page <a href="#">369</a>
GPON_GTC_US_TX_PATTERN_CTL	0xBB705020	0x0	Page <a href="#">369</a>
GPON_GTC_US_TX_PATTERN_FG	0xBB705028	0x0	Page <a href="#">370</a>

Register	Address	Default	Reference
GPON_GTC_US_WRITE_PROTECT	0xBB705018	0x0	Page <a href="#">369</a>
GPON_INTR_MASK	0xBB700040	0x0	Page <a href="#">341</a>
GPON_INTR_STS	0xBB700044	0x0	Page <a href="#">341</a>
GPON_INT_DLT	0xBB700000	0x0	Page <a href="#">339</a>
GPON_RESET	0xBB70000C	0x0	Page <a href="#">339</a>
GPON_TEST	0xBB700014	0x12345678	Page <a href="#">340</a>
GPON_VERSION	0xBB700010	0x0	Page <a href="#">340</a>

## H

All registers and tables starting with a H.

Register	Address	Default	Reference
HIGH_QUEUE_MSK	0xBB02D114	0x0	Page <a href="#">255</a>
HSARAM_5_CFG	0xBB02A2D0	0x0	Page <a href="#">434</a>
HSA_DATA	0xBB0280C0	0x0	Page <a href="#">292</a>
HSA_DATA_NAT	<Indirect> Type:0 Size:1	—	Page <a href="#">292</a>
HSA_DATA_TABLE	<Indirect> Type:0 Size:1	—	Page <a href="#">294</a>
HSA_DEBUG_DATA	<Indirect> Type:0 Size:1	—	Page <a href="#">437</a>
HSA_DESC	0xBB80022C	0x0	Page <a href="#">412</a>
HSA_TX_DBG	0xBB02A290	0x0	Page <a href="#">433</a>
HSBA_CTRL	0xBB800200	0x4	Page <a href="#">411</a>
HSB_CTRL	0xBB028000	0x0	Page <a href="#">289</a>
HSB_DATA	0xBB028040	0x0	Page <a href="#">289</a>
HSB_DATA_TABLE	<Indirect> Type:0 Size:1	—	Page <a href="#">290</a>
HSB_DESC	0xBB800204	0x0	Page <a href="#">411</a>
HTRAM_DVS_CFG	0xBB023038	0x0	Page <a href="#">38</a>
HWPKT_GEN_STA	0xBB02303C	0x0	Page <a href="#">38</a>
HYS_PUSAL_CFG	0xBB02A2E0	0x0	Page <a href="#">435</a>

## I

All registers and tables starting with a I.

Register	Address	Default	Reference
I2C_CLOCK_DIV	0xBB023004	0xF9	Page <a href="#">2</a>
I2C_IND_CMD	0xBB000030	0x0	Page <a href="#">5</a>
I2C_IND_RD	0xBB000038	0x0	Page <a href="#">5</a>
I2C_IND_WD	0xBB000028	0x0	Page <a href="#">5</a>
IGMP_GLB_CTRL	0xBB011070	0x0	Page <a href="#">303</a>

Register	Address	Default	Reference
IGMP_MC_GROUP	0xBB01C13C	0x0	Page <a href="#">303</a>
IGMP_P_CTRL	0xBB011074	0x400	Page <a href="#">304</a>
IGR_BWCTRL_GLB_CTRL	0xBB01C0B8	0x0	Page <a href="#">213</a>
IGR_BWCTRL_P_CTRL	0xBB020034	0x7FFFC	Page <a href="#">212</a>
INBW_BOUND	0xBB02306C	0xED	Page <a href="#">55</a>
INTR_CTRL	0xBB01D000	0x0	Page <a href="#">12</a>
INTR_IMR	0xBB01D004	0x0	Page <a href="#">12</a>
INTR_IMS	0xBB01D008	0x0	Page <a href="#">13</a>
INTR_STAT	0xBB01D00C	0x0	Page <a href="#">14</a>
IOL_RXDROP_CFG	0xBB023054	0x14	Page <a href="#">53</a>
IOPAD_CFG	0xBB023010	0x0	Page <a href="#">6</a>
IO_LED_EN	0xBB023014	0x0	Page <a href="#">7</a>
IO_MODE_EN	0xBB023018	0x60000	Page <a href="#">7</a>
IPV6_ROUTING_TABLE	<Indirect> Type:5 Size:4	—	Page <a href="#">398</a>

## L

All registers and tables starting with a L.

Register	Address	Default	Reference
L2_EFID	0xBB017030	0x0	Page <a href="#">138</a>
L2_IPMC_ISO_LEAKY	0xBB01C030	0x0	Page <a href="#">140</a>
L2_IPMC_VLAN_LEAKY	0xBB01C02C	0x0	Page <a href="#">139</a>
L2_LRN_CNT	0xBB017018	0x0	Page <a href="#">134</a>
L2_LRN_OVER_STS	0xBB01D010	0x0	Page <a href="#">134</a>
L2_MC_DSL	<Indirect> Type:0 Size:2112	—	Page <a href="#">322</a>
L2_SRC_EXT_PERMIT	0xBB01C0B4	0x0	Page <a href="#">169</a>
L2_SRC_PORT_PERMIT	0xBB01C0B0	0x0	Page <a href="#">168</a>
L2_SYS_LRN_CNT	0xBB01702C	0x0	Page <a href="#">135</a>
L2_SYS_LRN_OVER_STS	0xBB01D014	0x0	Page <a href="#">135</a>
L2_TBL_FLUSH_CTRL	0xBB017038	0x0	Page <a href="#">138</a>
L2_TBL_FLUSH_EN	0xBB01703C	0x0	Page <a href="#">139</a>
L2_UC	<Indirect> Type:0 Size:2112	—	Page <a href="#">322</a>
L34_EXTPORT_TO_WAN	0xBB0110B0	0x1	Page <a href="#">307</a>
L34_GLB_CFG	0xBB011090	0x0	Page <a href="#">305</a>
L34_HSA	<Indirect> Type:0 Size:1	—	Page <a href="#">412</a>
L34_HSB	<Indirect> Type:0 Size:1	—	Page <a href="#">414</a>
L34_IPMC_TRAN_TBL	0xBB02A208	0x0	Page <a href="#">305</a>
L34_IPMC_TTL_CFG	0xBB02A248	0x1	Page <a href="#">306</a>

Register	Address	Default	Reference
L34_PORT_TO_WAN	0xBB011094	0x1	Page 306
L34_WAN_TO_EXTPORT	0xBB0110E0	0x1	Page 307
L34_WAN_TO_PORT	0xBB0110C4	0x1	Page 307
L3_MC_DSL	<Indirect> Type:0 Size:2112	—	Page 323
L3_MC_ROUTE	<Indirect> Type:0 Size:2112	—	Page 324
L3_ROUTING_DROP_TRAP	<Indirect> Type:0 Size:8	—	Page 398
L3_ROUTING_GLOBAL_ROUTE	<Indirect> Type:0 Size:8	—	Page 399
L3_ROUTING_LOCAL_ROUTE	<Indirect> Type:0 Size:8	—	Page 400
L4_TRF0	0xBB800300	0x0	Page 415
L4_TRF1	0xBB800400	0x0	Page 415
LASER_ON_OFF_TIME	0xBB03602C	0x0	Page 387
LED_ACTIVE_LOW_CFG	0xBB01E084	0x1	Page 22
LED_BLINK_RATE_CFG	0xBB01E094	0x249	Page 23
LED_EN	0xBB01E0A0	0x0	Page 25
LED_FORCE_VALUE_CFG	0xBB01E08C	0x1	Page 23
LED_LED	0xBB01E000	0x0	Page 21
LINE_RATE_100M	0xBB02D828	0x3333	Page 266
LINE_RATE_10M	0xBB02D82C	0x51E	Page 266
LINE_RATE_1G	0xBB02D820	0x1FFFF	Page 265
LINE_RATE_500M	0xBB02D824	0x0	Page 265
LLID_TABLE	0xBB036040	0x57FFF	Page 389
LOW_QUEUE_TH	0xBB02D110	0x1	Page 255
LOW_RATE_BLINK_CFG	0xBB01E098	0x0	Page 24
LUT_AGEOUT_CTRL	0xBB017004	0x1	Page 133
LUT_BC_FLOOD	0xBB01C020	0x1	Page 137
LUT_CFG	0xBB017000	0x600BB8	Page 132
LUT_LEARN_OVER_CTRL	0xBB01C00C	0x0	Page 132
LUT_LRN_LIMITNO	0xBB017008	0xFFFF	Page 133
LUT_SYS_LRN_LIMITNO	0xBB017028	0xFFFF	Page 134
LUT_SYS_LRN_OVER_CTRL	0xBB017034	0x0	Page 138
LUT_UNKN_MC_FLOOD	0xBB01C024	0x1	Page 137
LUT_UNKN_SA_CTRL	0xBB01C004	0x0	Page 131
LUT_UNKN_UC_DA_CTRL	0xBB01C008	0x0	Page 132
LUT_UNKN_UC_FLOOD	0xBB01C028	0x1	Page 137
LUT_UNMATCHED_SA_CTRL	0xBB01C000	0x0	Page 131

## M

All registers and tables starting with a M.



Register	Address	Default	Reference
MAC_ACT_CFG	0xBB000134	0xFE00	Page <a href="#">35</a>
MAC_CPU_TAG_AWARE_CTRL	0xBB023048	0x0	Page <a href="#">51</a>
MAC_CPU_TAG_CTRL	0xBB023044	0x100	Page <a href="#">51</a>
MAC_DLYLNK	0xBB0001AC	0x26	Page <a href="#">48</a>
MAX_FIFO_SIZE	0xBB023070	0x0	Page <a href="#">55</a>
MAX_GRANT_START	0xBB036034	0x0	Page <a href="#">388</a>
MAX_LENGTH_CFG0	0xBB02304C	0x3FF0	Page <a href="#">53</a>
MAX_LENGTH_CFG1	0xBB011028	0x3FF0	Page <a href="#">52</a>
MAX_LENGTH_LIMINT_IPG	0xBB023050	0x3F87	Page <a href="#">53</a>
MDX_PHY_REG1	0xBB0000A4	0x1F	Page <a href="#">29</a>
METER_GLB_CTRL	0xBB025004	0x258	Page <a href="#">213</a>
METER_LB_EXCEED_STS	0xBB025104	0x0	Page <a href="#">214</a>
METER_PKT_RATE	0xBB02510C	0x0	Page <a href="#">215</a>
METER_TB_CTRL	0xBB025000	0x11A1D	Page <a href="#">213</a>
MIN_GRANT_START	0xBB036030	0x0	Page <a href="#">387</a>
MIR_CTRL	0xBB0230FC	0x0	Page <a href="#">223</a>
MISCELLANEOUS_BONDING	0xBB0001A0	0xC000	Page <a href="#">44</a>
MISCELLANEOUS_CONFIGURE0	0xBB000084	0x0	Page <a href="#">28</a>
MISCELLANEOUS_STRAPPING0	0xBB0001A8	0x0	Page <a href="#">47</a>
MISCELLANEOUS_STRAPPING1	0xBB0001A4	0x0	Page <a href="#">46</a>
MOCIR_BPT	0xBB02D8F4	0x42	Page <a href="#">270</a>
MOCIR_FRC_MD	0xBB02D8F8	0x0	Page <a href="#">270</a>
MOCIR_FRC_VAL	0xBB02D8FC	0x0	Page <a href="#">270</a>
MOCIR_TH_H	0xBB02D8EC	0x20E	Page <a href="#">269</a>
MOCIR_TH_L	0xBB02D8F0	0x1F0	Page <a href="#">270</a>
MODEL_CFG	0xBB000114	0x0	Page <a href="#">33</a>
MODEL_NAME_INFO	0xBB010000	0x86906800	Page <a href="#">27</a>
MODE_EXT	0xBB000158	0x0	Page <a href="#">38</a>
MSTI_CTRL	0xBB017040	0x3	Page <a href="#">152</a>

## N

All registers and tables starting with a N.

Register	Address	Default	Reference
NAPTR_TABLE	<Indirect> Type:9 Size:1024	—	Page <a href="#">401</a>
NAPT_TABLE	<Indirect> Type:10 Size:2048	—	Page <a href="#">401</a>
NAT_TBL_ACCESS_CLR	0xBB800104	0x0	Page <a href="#">394</a>
NAT_TBL_ACCESS_CTRL	0xBB800100	0x0	Page <a href="#">393</a>
NAT_TBL_ACCESS_RDDATA	0xBB800108	0x0	Page <a href="#">396</a>
NAT_TBL_ACCESS_WRDATA	0xBB80011C	0x0	Page <a href="#">396</a>
NB_TRF	0xBB800018	0x0	Page <a href="#">408</a>



Register	Address	Default	Reference
NEIGHBOR_TABLE	<Indirect> Type:11 Size:128	—	Page <a href="#">402</a>
NETIF	<Indirect> Type:3 Size:8	—	Page <a href="#">402</a>
NEXT_HOP_TABLE	<Indirect> Type:2 Size:16	—	Page <a href="#">403</a>
NIC_COM	0xBB710038	0x0	Page <a href="#">175</a>
NIC_CONFIG	0xBB71005C	0x20000000	Page <a href="#">182</a>
NIC_CPUTAG	0xBB710058	0x0	Page <a href="#">181</a>
NIC_CPUTAG1	0xBB710060	0x0	Page <a href="#">183</a>
NIC_DIAGNOSE1	0xBB720104	0x0	Page <a href="#">202</a>
NIC_ETNRXCPU1	0xBB720130	0x0	Page <a href="#">203</a>
NIC_ETN_IO_CMD	0xBB720134	0x0	Page <a href="#">203</a>
NIC_ETN_IO_CMD1	0xBB720138	0x0	Page <a href="#">205</a>
NIC_ID_CRTL0	0xBB710000	0x0	Page <a href="#">171</a>
NIC_ID_CRTL1	0xBB710004	0x0	Page <a href="#">171</a>
NIC_IMR0_CFG	0xBB710040	0x0	Page <a href="#">177</a>
NIC_IMR1_CFG	0xBB710044	0x0	Page <a href="#">178</a>
NIC_INTR	0xBB71003C	0x0	Page <a href="#">175</a>
NIC_INT_ROUTE	0xBB71004C	0x0	Page <a href="#">179</a>
NIC_ISR1_CFG	0xBB710048	0x0	Page <a href="#">178</a>
NIC_LED_CR	0xBB710080	0x0	Page <a href="#">186</a>
NIC_MC_CRTL0	0xBB710008	0x0	Page <a href="#">171</a>
NIC_MC_CRTL1	0xBB71000C	0x0	Page <a href="#">172</a>
NIC_MIB0	0xBB710010	0x0	Page <a href="#">172</a>
NIC_MIB1	0xBB710014	0x0	Page <a href="#">173</a>
NIC_MIB2	0xBB710018	0x0	Page <a href="#">173</a>
NIC_MIB3	0xBB71001C	0x0	Page <a href="#">173</a>
NIC_MIB4	0xBB710020	0x0	Page <a href="#">174</a>
NIC_MIB5	0xBB710024	0x0	Page <a href="#">174</a>
NIC_MIB6	0xBB710028	0x0	Page <a href="#">174</a>
NIC_MIIA	0xBB71006C	0x0	Page <a href="#">185</a>
NIC_MS	0xBB710068	0x0	Page <a href="#">183</a>
NIC_PROBE_SELECT	0xBB720100	0x0	Page <a href="#">201</a>
NIC_RC	0xBB710054	0x0	Page <a href="#">181</a>
NIC_RRING_ROUTING1	0xBB720070	0x0	Page <a href="#">190</a>
NIC_RRING_ROUTING2	0xBB720074	0x0	Page <a href="#">190</a>
NIC_RRING_ROUTING3	0xBB720078	0x0	Page <a href="#">191</a>
NIC_RRING_ROUTING4	0xBB72007C	0x0	Page <a href="#">191</a>
NIC_RRING_ROUTING5	0xBB720080	0x0	Page <a href="#">192</a>
NIC_RRING_ROUTING6	0xBB720084	0x0	Page <a href="#">193</a>
NIC_RXCDORINGRS1	0xBB7200F4	0x0	Page <a href="#">201</a>
NIC_RXCDORINGRS2	0xBB720094	0x0	Page <a href="#">194</a>
NIC_RXCDORINGRS3	0xBB7200A4	0x0	Page <a href="#">195</a>
NIC_RXCDORINGRS4	0xBB7200B4	0x0	Page <a href="#">196</a>

Register	Address	Default	Reference
NIC_RXCDORINGRS5	0xBB7200C4	0x0	Page 198
NIC_RXCDORINGRS6	0xBB7200D4	0x0	Page 199
NIC_RXFDP1	0xBB7200F0	0x0	Page 200
NIC_RXFDP2	0xBB720090	0x0	Page 193
NIC_RXFDP3	0xBB7200A0	0x0	Page 195
NIC_RXFDP4	0xBB7200B0	0x0	Page 196
NIC_RXFDP5	0xBB7200C0	0x0	Page 198
NIC_RXFDP6	0xBB7200D0	0x0	Page 199
NIC_RX_CPU_DESN2	0xBB720098	0x0	Page 194
NIC_RX_CPU_DESN3	0xBB7200A8	0x0	Page 196
NIC_RX_CPU_DESN4	0xBB7200B8	0x0	Page 197
NIC_RX_CPU_DESN5	0xBB7200C8	0x0	Page 198
NIC_RX_CPU_DESN6	0xBB7200D8	0x0	Page 200
NIC_RX_DES_THRES2	0xBB72009C	0x0	Page 194
NIC_RX_DES_THRES3	0xBB7200AC	0x0	Page 196
NIC_RX_DES_THRES4	0xBB7200BC	0x0	Page 197
NIC_RX_DES_THRES5	0xBB7200CC	0x0	Page 199
NIC_RX_DES_THRES6	0xBB7200DC	0x0	Page 200
NIC_RX_PSE1_TXC_OUT_SEL1	0xBB72012C	0x0	Page 202
NIC_SMSA	0xBB7200FC	0x0	Page 201
NIC_STS	0xBB710034	0x0	Page 174
NIC_SWINT	0xBB710070	0x0	Page 186
NIC_TC	0xBB710050	0x0	Page 180
NIC_TXCDO1	0xBB720004	0x0	Page 187
NIC_TXCDO2	0xBB720014	0x0	Page 188
NIC_TXCDO3	0xBB720024	0x0	Page 188
NIC_TXCDO4	0xBB720034	0x0	Page 189
NIC_TXCDO5	0xBB720044	0x0	Page 189
NIC_TXFDP2	0xBB720010	0x0	Page 187
NIC_TXFDP3	0xBB720020	0x0	Page 188
NIC_TXFDP4	0xBB720030	0x0	Page 188
NIC_TXFDP5	0xBB720040	0x0	Page 189
NIC_TXFPD1	0xBB720000	0x0	Page 187
NIC_VLAN	0xBB710074	0x0	Page 186
NIC_WOL	0xBB72013C	0x0	Page 206
NIFEP	0xBB800004	0x0	Page 404
NIFP	0xBB800000	0x0	Page 404
NIFVCH	0xBB800008	0x0	Page 405
NIFVCL	0xBB80000C	0x0	Page 405

## O

All registers and tables starting with a O.

Register	Address	Default	Reference
OAM_CTRL_0	0xBB01C138	0x0	Page <a href="#">282</a>
OAM_CTRL_1	0xBB0170B8	0x0	Page <a href="#">282</a>
OAM_P_CTRL_0	0xBB0170B0	0x0	Page <a href="#">281</a>
OAM_P_CTRL_1	0xBB0170B4	0x0	Page <a href="#">281</a>
OMCI_CRC_ERROR_PKT_CNT	0xBB032914	0x0	Page <a href="#">234</a>
OMCI_DROP_PKT_CNT	0xBB032900	0x0	Page <a href="#">233</a>
OMCI_RX_BYTE_CNT	0xBB032910	0x0	Page <a href="#">234</a>
OMCI_RX_PKT_CNT	0xBB032908	0x0	Page <a href="#">234</a>
OMCI_TX_BYTE_CNT	0xBB03290C	0x0	Page <a href="#">234</a>
OMCI_TX_PKT_CNT	0xBB032904	0x0	Page <a href="#">233</a>
OUTPUT_DROP_CFG	0xBB011068	0x6	Page <a href="#">266</a>
OUTPUT_DROP_EN	0xBB01106C	0x0	Page <a href="#">267</a>

## P

All registers and tables starting with a P.

Register	Address	Default	Reference
PARSER_FIELD_SELECTOR_CTRL	0xBB023224	0x0	Page <a href="#">332</a>
PAUSE_ALL_LW_CFG	0xBB02A2DC	0x0	Page <a href="#">435</a>
PISO_CTRL	0xBB027038	0x0	Page <a href="#">154</a>
PISO_EXT_MODE0_CTRL	0xBB027020	0x1FFF	Page <a href="#">153</a>
PISO_EXT_MODE1_CTRL	0xBB02702C	0x1FFF	Page <a href="#">154</a>
PISO_P_MODE0_CTRL	0xBB027000	0x1FFF	Page <a href="#">153</a>
PISO_P_MODE1_CTRL	0xBB027010	0x1FFF	Page <a href="#">153</a>
PLL_RGM_CTRL1	0xBB0001B0	0x8000000	Page <a href="#">48</a>
PLL_RGM_CTRL2	0xBB0001B4	0x7EA5B421	Page <a href="#">49</a>
PLL_RGM_CTRL3	0xBB0001B8	0xF0FFE0	Page <a href="#">49</a>
PONMAC_DRN_CTRL	0xBB023268	0x0	Page <a href="#">337</a>
PON_CFG	0xBB02D900	0x20000	Page <a href="#">333</a>
PON_INTEGRATION	0xBB000074	0x0	Page <a href="#">21</a>
PON_LED_CFG	0xBB01E108	0x3	Page <a href="#">437</a>
PON_MODE_CFG	0xBB000150	0x1	Page <a href="#">37</a>
PON_OLT_BW_MTR_FULL	0xBB02DE44	0x3FF	Page <a href="#">337</a>
PON_PIR_CIR_IFG	0xBB02D12C	0x0	Page <a href="#">337</a>
PON_PORT_CTRL	0xBB023264	0x0	Page <a href="#">337</a>
PON_QID_CIR_RATE	0xBB02D904	0x0	Page <a href="#">333</a>
PON_QID_PIR_RATE	0xBB02DB04	0x1FFFF	Page <a href="#">334</a>
PON_SCH_QMAP	0xBB02DD04	0x0	Page <a href="#">334</a>
PON_SID_TO_QID	0xBB01C33C	0x0	Page <a href="#">333</a>
PON_TB_CTRL	0xBB025108	0x13042	Page <a href="#">214</a>
PON_TCONT_EN	0xBB02DE40	0x0	Page <a href="#">335</a>
PON_WFQ_IFG_CTRL	0xBB02DE48	0x0	Page <a href="#">338</a>
PON_WFQ_TYPE	0xBB02DE30	0x0	Page <a href="#">335</a>
PON_WFQ_WEIGHT	0xBB02DD84	0x0	Page <a href="#">334</a>

Register	Address	Default	Reference
PORT_TRUNK_CTRL	0xBB01C050	0x100	Page <a href="#">151</a>
PORT_TRUNK_GROUP_EN	0xBB01C040	0x0	Page <a href="#">151</a>
PORT_TRUNK_HASH_MAPPING	0xBB01C054	0x0	Page <a href="#">152</a>
PORT_VM_EN	0xBB020044	0x0	Page <a href="#">295</a>
PORT_VM_RX	0xBB020048	0x0	Page <a href="#">296</a>
PORT_VM_TX	0xBB02004C	0x0	Page <a href="#">296</a>
PPPOE_TABLE	<Indirect> Type:1 Size:8	—	Page <a href="#">403</a>
PP_AGE	0xBB800014	0x0	Page <a href="#">408</a>
PRI_SEL_TBL_CTRL	0xBB01C130	0x0	Page <a href="#">261</a>
PRI_SEL_TBL_CTRL2	0xBB01C134	0x0	Page <a href="#">262</a>
PS_LINKID_GATCLK_CTRL	0xBB0230A4	0x0	Page <a href="#">119</a>
PTP_EGR_MSG_ACT	0xBB011104	0x0	Page <a href="#">330</a>
PTP_IGR_MSG_ACT	0xBB011100	0x0	Page <a href="#">330</a>
PTP_MEANPATH_DEALY	0xBB01B054	0x0	Page <a href="#">331</a>
PTP_P_EN	0xBB011110	0x0	Page <a href="#">331</a>
PTP_RX_TIME	0xBB011108	0x0	Page <a href="#">331</a>
PTP_TIME_CTRL	0xBB01B050	0x0	Page <a href="#">329</a>
PTP_TIME_FREQ	0xBB01B04C	0x80000	Page <a href="#">329</a>
PTP_TIME_NSEC	0xBB01B03C	0x0	Page <a href="#">328</a>
PTP_TIME_OFFSET_8NSEC	0xBB01B048	0x0	Page <a href="#">329</a>
PTP_TIME_OFFSET_SEC	0xBB01B040	0x0	Page <a href="#">328</a>
PTP_TIME_SEC	0xBB01B034	0x0	Page <a href="#">328</a>
PTP_TRANSPARENT_CFG	0xBB0110FC	0x0	Page <a href="#">329</a>
PWM_CTRL1	0xBB000164	0x1AA8	Page <a href="#">39</a>
PWM_CTRL2	0xBB000168	0x564A83A	Page <a href="#">40</a>
P_ABLTY	0xBB0000B4	0x0	Page <a href="#">30</a>
P_CFG_FRC_RATE	0xBB02000C	0x0	Page <a href="#">57</a>
P_CGSTTIMER	0xBB020004	0x0	Page <a href="#">56</a>
P_CUR_RATE	0xBB020010	0x0	Page <a href="#">57</a>
P_EEECFG	0xBB020018	0x0	Page <a href="#">113</a>
P_EEEPRXMTR	0xBB02002C	0x0	Page <a href="#">128</a>
P_EEEPTXMTR	0xBB020028	0x0	Page <a href="#">127</a>
P_EEEP_CFG	0xBB020024	0x0	Page <a href="#">119</a>
P_EEERXMTR	0xBB020020	0x0	Page <a href="#">114</a>
P_EEETXMTR	0xBB02001C	0x0	Page <a href="#">114</a>
P_MISC	0xBB020008	0x20	Page <a href="#">56</a>
P_QUEUE_EMPTY	0xBB02D11C	0x0	Page <a href="#">269</a>
P_TX_ERR_CNT	0xBB020000	0x0	Page <a href="#">56</a>

## Q

All registers and tables starting with a Q.

Register	Address	Default	Reference
QOS_1Q_PRI_REMAP	0xBB01C10C	0x0	Page <a href="#">260</a>
QOS_DSCP_REMAP	0xBB01C110	0x0	Page <a href="#">260</a>
QOS_INTPRI_TO_QID	0xBB01C0F4	0x0	Page <a href="#">259</a>
QOS_PB_PRI	0xBB01C12C	0x0	Page <a href="#">261</a>
QOS_PORT_QMAP_CTRL	0xBB01C104	0x0	Page <a href="#">259</a>
QOS_PRI_REMAP_IN_CPU	0xBB01C108	0x0	Page <a href="#">260</a>
QUEUE_SEL_IND	0xBB02D120	0x0	Page <a href="#">336</a>
QUEUE_SEL_IND_DATA	0xBB02D124	0x0	Page <a href="#">336</a>

## R

All registers and tables starting with a R.

Register	Address	Default	Reference
RAM_DVS_CFG0	0xBB02301C	0x0	Page <a href="#">18</a>
RAM_DVS_CFG1	0xBB023020	0x0	Page <a href="#">19</a>
RAM_DVS_CFG2	0xBB023024	0x0	Page <a href="#">19</a>
RAM_DVS_CFG3	0xBB023028	0x0	Page <a href="#">20</a>
RAM_DVS_CFG4	0xBB02302C	0x0	Page <a href="#">20</a>
RAM_DVS_CFG5	0xBB023030	0x0	Page <a href="#">20</a>
REGCTRL_GLB	0xBB02300C	0x1FFFFFFF	Page <a href="#">6</a>
REVISION_CFG	0xBB000110	0x0	Page <a href="#">33</a>
RGF_VER_ALE_ACL	0xBB0154D0	0x12051100	Page <a href="#">419</a>
RGF_VER_ALE_CVLAN	0xBB0131A0	0x12051100	Page <a href="#">420</a>
RGF_VER_ALE_DPM	0xBB01C3CC	0x12051100	Page <a href="#">420</a>
RGF_VER_ALE_EAV_AFBK	0xBB01B058	0x12051100	Page <a href="#">421</a>
RGF_VER_ALE_EEE_LLDP	0xBB019000	0x12051100	Page <a href="#">421</a>
RGF_VER_ALE_GLB	0xBB01112C	0x12051100	Page <a href="#">419</a>
RGF_VER_ALE_HSA	0xBB02A24C	0x12051100	Page <a href="#">424</a>
RGF_VER_ALE_L2	0xBB0170BC	0x12051100	Page <a href="#">420</a>
RGF_VER_ALE_METER	0xBB025110	0x12051100	Page <a href="#">424</a>
RGF_VER_ALE_MLTVLAN	0xBB018060	0x12051100	Page <a href="#">420</a>
RGF_VER_ALE_PISO	0xBB02703C	0x12051100	Page <a href="#">425</a>
RGF_VER_ALE_RLDP	0xBB01A038	0x12051100	Page <a href="#">421</a>
RGF_VER_ALE_RMA_ATTACK	0xBB026014	0x12051100	Page <a href="#">423</a>
RGF_VER_ALE_SVLAN	0xBB014410	0x12051100	Page <a href="#">421</a>
RGF_VER_BIST_CTRL	0xBB031048	0x12051100	Page <a href="#">423</a>
RGF_VER_EGR_OUTQ	0xBB02D130	0x12051100	Page <a href="#">424</a>
RGF_VER_EGR_SCH	0xBB02DE4C	0x12051100	Page <a href="#">424</a>
RGF_VER_EPON_CTRL	0xBB0361E8	0x12051100	Page <a href="#">423</a>
RGF_VER_GLB_CTRL	0xBB0001CC	0x12051100	Page <a href="#">419</a>
RGF_VER_INTR	0xBB01D01C	0x12051100	Page <a href="#">422</a>
RGF_VER_LED	0xBB01E0C0	0x12051100	Page <a href="#">422</a>
RGF_VER_MIB_CTRL	0xBB03401C	0x12051100	Page <a href="#">425</a>
RGF_VER_PER_PORT_MAC	0xBB020078	0x12051100	Page <a href="#">422</a>

Register	Address	Default	Reference
RGF_VER_SDSREG	0xBB02214C	0x12051100	Page <a href="#">422</a>
RGF_VER_SWCORE	0xBB02326C	0x12051100	Page <a href="#">423</a>
RGM_EEE	0xBB000120	0x0	Page <a href="#">34</a>
RLDP_BUZZER	0xBB01E104	0x0	Page <a href="#">437</a>
RLDP_CHK_STS_CTRL	0xBB01A004	0x0	Page <a href="#">283</a>
RLDP_CTRL_0	0xBB0231EC	0x0	Page <a href="#">283</a>
RLDP_CTRL_1	0xBB01A000	0x2	Page <a href="#">283</a>
RLDP_LP_STS_CTRL	0xBB01A008	0x0	Page <a href="#">284</a>
RLDP_MAGIC_NUM	0xBB01A014	0x0	Page <a href="#">284</a>
RLDP_PORT_CPU_LP_STS	0xBB01A02C	0x0	Page <a href="#">286</a>
RLDP_PORT_LP_ENTER_STS	0xBB01A020	0x0	Page <a href="#">285</a>
RLDP_PORT_LP_LEAVE_STS	0xBB01A024	0x0	Page <a href="#">285</a>
RLDP_PORT_LP_PNUM	0xBB01A030	0x0	Page <a href="#">286</a>
RLDP_PORT_LP_STS	0xBB01A028	0x0	Page <a href="#">286</a>
RLDP_PORT_TX_EN	0xBB01A01C	0x0	Page <a href="#">285</a>
RLDP_RNDM_NUM	0xBB01A00C	0x0	Page <a href="#">284</a>
RLPP_CTRL	0xBB01A034	0x0	Page <a href="#">287</a>
RMA_CFG	0xBB01C0A4	0x0	Page <a href="#">167</a>
RMA_CTRL00	0xBB01C058	0x0	Page <a href="#">155</a>
RMA_CTRL01	0xBB01C05C	0x20	Page <a href="#">155</a>
RMA_CTRL02	0xBB01C060	0x20	Page <a href="#">156</a>
RMA_CTRL03	0xBB01C064	0x0	Page <a href="#">157</a>
RMA_CTRL04	0xBB01C068	0x0	Page <a href="#">157</a>
RMA_CTRL08	0xBB01C06C	0x0	Page <a href="#">158</a>
RMA_CTRL0D	0xBB01C070	0x0	Page <a href="#">159</a>
RMA_CTRL0E	0xBB01C074	0x0	Page <a href="#">159</a>
RMA_CTRL10	0xBB01C078	0x0	Page <a href="#">160</a>
RMA_CTRL11	0xBB01C07C	0x0	Page <a href="#">161</a>
RMA_CTRL12	0xBB01C080	0x0	Page <a href="#">161</a>
RMA_CTRL13	0xBB01C084	0x0	Page <a href="#">162</a>
RMA_CTRL18	0xBB01C088	0x0	Page <a href="#">163</a>
RMA_CTRL1A	0xBB01C08C	0x0	Page <a href="#">163</a>
RMA_CTRL20	0xBB01C090	0x0	Page <a href="#">164</a>
RMA_CTRL21	0xBB01C094	0x0	Page <a href="#">165</a>
RMA_CTRL22	0xBB01C098	0x0	Page <a href="#">165</a>
RMA_CTRL_CDP	0xBB01C09C	0x0	Page <a href="#">166</a>
RMA_CTRL_SSTP	0xBB01C0A0	0x0	Page <a href="#">167</a>
RMK_1Q_CTRL	0xBB0231CC	0x0	Page <a href="#">262</a>
RMK_DOT1Q_RMK_EN_CTRL	0xBB020040	0x0	Page <a href="#">262</a>
RMK_DSCP_CF_PRI_CTRL	0xBB0150E4	0x0	Page <a href="#">275</a>
RMK_DSCP_CTRL	0xBB01102C	0x0	Page <a href="#">263</a>
RMK_DSCP_INT_PRI_CTRL	0xBB011060	0x0	Page <a href="#">263</a>
RMK_DSCP_RMK_EN_CTRL	0xBB0231D0	0x0	Page <a href="#">263</a>
RMK_P_DSCP_SEL	0xBB02A200	0x0	Page <a href="#">264</a>
RNG_CHK_IP_RNG	0xBB015330	0x0	Page <a href="#">277</a>
RNG_CHK_IP_RNG_CF	0xBB015430	0xFFFFFFFF	Page <a href="#">279</a>

Register	Address	Default	Reference
RNG_CHK_L4PORT_RNG	0xBB015390	0x0	Page 278
RNG_CHK_L4PORT_RNG_CF	0xBB015490	0xFFFF	Page 279
RNG_CHK_PKTLEN_RNG	0xBB015410	0x0	Page 278
RNG_CHK_VID_RNG	0xBB015310	0x0	Page 277
ROUTER_UPS_CFG	0xBB0000B0	0x0	Page 30
RST_SYNC_FIFO	0xBB00012C	0x0	Page 35
RSVD_ALE_ACL	0xBB0154D4	0x55555555	Page 426
RSVD_ALE_CVLAN	0xBB0131A4	0x55555555	Page 426
RSVD_ALE_DPM	0xBB01C3D0	0x55555555	Page 427
RSVD_ALE_EAV_AFBK	0xBB01B05C	0x55555555	Page 428
RSVD_ALE_EEE_LLDP	0xBB019004	0x55555555	Page 428
RSVD_ALE_GLB	0xBB011130	0x55555555	Page 426
RSVD_ALE_HSA	0xBB02A250	0x55555555	Page 432
RSVD_ALE_L2	0xBB0170C0	0x55555555	Page 427
RSVD_ALE_METER	0xBB025114	0x55555555	Page 432
RSVD_ALE_MLTVLAN	0xBB018064	0x55555555	Page 427
RSVD_ALE_PISO	0xBB027040	0x55555555	Page 433
RSVD_ALE_RLDP	0xBB01A03C	0x55555555	Page 428
RSVD_ALE_RMA_ATTACK	0xBB026018	0x55555555	Page 431
RSVD_ALE_SVLAN	0xBB014414	0x55555555	Page 428
RSVD_BIST_CTRL	0xBB03104C	0x55555555	Page 431
RSVD_EGR_OUTQ	0xBB02D134	0x55555555	Page 431
RSVD_EGR_SCH	0xBB02DE50	0x55555555	Page 432
RSVD_EPON_CTRL	0xBB0361EC	0x55555555	Page 430
RSVD_GLB_CTRL	0xBB0001D0	0x55555555	Page 425
RSVD_INTR	0xBB01D020	0x55555555	Page 429
RSVD_LED	0xBB01E0C4	0x55555555	Page 429
RSVD_MIB_CTRL	0xBB034020	0x55555555	Page 433
RSVD_PER_PORT_MAC	0xBB02007C	0x55555555	Page 429
RSVD_SDSREG	0xBB022150	0x55555555	Page 430
RSVD_SWCORE	0xBB023270	0x55555555	Page 430
RTL_OUI_CFG	0xBB00010C	0x0	Page 33

## S

All registers and tables starting with a S.

Register	Address	Default	Reference
SC_P_CTRL_0	0xBB02003C	0x0	Page 256
SC_P_CTRL_1	0xBB01D018	0x0	Page 256
SDS_AN_RX_CFG	0xBB000140	0x0	Page 36
SDS_CFG	0xBB000130	0x8	Page 35
SDS_EXT_REG0	0xBB022A00	0x0	Page 94
SDS_EXT_REG1	0xBB022A04	0xC000	Page 94
SDS_EXT_REG10	0xBB022A28	0x6D2C	Page 96



Register	Address	Default	Reference
SDS_EXT_REG11	0xBB022A2C	0x2BE8	Page 96
SDS_EXT_REG12	0xBB022A30	0xEA14	Page 97
SDS_EXT_REG13	0xBB022A34	0x304F	Page 97
SDS_EXT_REG14	0xBB022A38	0xA84C	Page 97
SDS_EXT_REG15	0xBB022A3C	0xAA12	Page 97
SDS_EXT_REG16	0xBB022A40	0x3292	Page 98
SDS_EXT_REG2	0xBB022A08	0x0	Page 94
SDS_EXT_REG24	0xBB022A44	0x0	Page 98
SDS_EXT_REG25	0xBB022A48	0x0	Page 98
SDS_EXT_REG26	0xBB022A4C	0x0	Page 98
SDS_EXT_REG27	0xBB022A50	0x0	Page 99
SDS_EXT_REG28	0xBB022A54	0x0	Page 99
SDS_EXT_REG29	0xBB022A58	0x0	Page 99
SDS_EXT_REG3	0xBB022A0C	0xA170	Page 95
SDS_EXT_REG30	0xBB022A5C	0x0	Page 99
SDS_EXT_REG4	0xBB022A10	0x0	Page 95
SDS_EXT_REG5	0xBB022A14	0xF000	Page 95
SDS_EXT_REG6	0xBB022A18	0x6E1B	Page 95
SDS_EXT_REG7	0xBB022A1C	0x858B	Page 96
SDS_EXT_REG8	0xBB022A20	0x850	Page 96
SDS_EXT_REG9	0xBB022A24	0x24A3	Page 96
SDS_FIB_STATUS	0xBB000144	0x0	Page 36
SDS_REG0	0xBB022800	0x403	Page 84
SDS_REG1	0xBB022804	0xF00	Page 85
SDS_REG10	0xBB022828	0x8CA4	Page 89
SDS_REG11	0xBB02282C	0x0	Page 89
SDS_REG12	0xBB022830	0x8E4	Page 89
SDS_REG13	0xBB022834	0x4664	Page 90
SDS_REG14	0xBB022838	0x2053	Page 90
SDS_REG15	0xBB02283C	0x0	Page 91
SDS_REG16	0xBB022840	0x0	Page 91
SDS_REG17	0xBB022844	0x0	Page 91
SDS_REG18	0xBB022848	0x0	Page 91
SDS_REG19	0xBB02284C	0x4001	Page 91
SDS_REG2	0xBB022808	0x7000	Page 85
SDS_REG20	0xBB022850	0x1	Page 92
SDS_REG21	0xBB022854	0x4001	Page 92
SDS_REG22	0xBB022858	0x9800	Page 92
SDS_REG23	0xBB02285C	0x9800	Page 92
SDS_REG24	0xBB022860	0x1C	Page 93
SDS_REG25	0xBB022864	0x1C	Page 93
SDS_REG26	0xBB022868	0x3810	Page 93
SDS_REG27	0xBB02286C	0x0	Page 93
SDS_REG28	0xBB022870	0xC040	Page 93
SDS_REG29	0xBB022874	0x0	Page 94
SDS_REG3	0xBB02280C	0x7106	Page 85



Register	Address	Default	Reference
SDS_REG4	0xBB022810	0x749	Page <a href="#">86</a>
SDS_REG5	0xBB022814	0x8E80	Page <a href="#">87</a>
SDS_REG6	0xBB022818	0x8F0F	Page <a href="#">87</a>
SDS_REG7	0xBB02281C	0x5359	Page <a href="#">88</a>
SDS_REG8	0xBB022820	0x524B	Page <a href="#">88</a>
SDS_REG9	0xBB022824	0x0	Page <a href="#">89</a>
SERI_LED_ACTIVE_LOW_CFG	0xBB01E088	0x0	Page <a href="#">23</a>
SERI_LED_CLK_PER	0xBB01E0A4	0x1	Page <a href="#">25</a>
SERI_LED_REFRESH_TIME	0xBB01E0A8	0x2	Page <a href="#">25</a>
SKIP_MII_RXER	0xBB000000	0x0	Page <a href="#">1</a>
SLIC_INSEL_CTRL	0xBB000188	0x0	Page <a href="#">42</a>
SOFTWARE_RST	0xBB00006C	0x0	Page <a href="#">11</a>
SPG_GLB_CTRL	0xBB0231F0	0xFFFF0000	Page <a href="#">297</a>
SPG_PAYLOAD	0xBB0231F4	0x0	Page <a href="#">300</a>
SPG_PORT_STS	0xBB020054	0x0	Page <a href="#">297</a>
SPG_PORT_TX_GRP_CTRL	0xBB020050	0x0	Page <a href="#">297</a>
SPG_PORT_USER_PKT	0xBB020074	0x0	Page <a href="#">301</a>
SPG_P_DA	0xBB02006C	0x0	Page <a href="#">300</a>
SPG_P_LEN_CTRL	0xBB02005C	0x0	Page <a href="#">299</a>
SPG_P_SA	0xBB020064	0x0	Page <a href="#">300</a>
SPG_P_TX_CNT	0xBB020060	0x0	Page <a href="#">299</a>
SPG_P_TX_GRP_CTRL	0xBB020058	0x0	Page <a href="#">298</a>
STAT_ACL_CNT	0xBB032880	0x0	Page <a href="#">231</a>
STAT_ACL_CNT_MODE	0xBB034004	0x0	Page <a href="#">231</a>
STAT_ACL_CNT_RST	0xBB03400C	0x0	Page <a href="#">232</a>
STAT_ACL_CNT_TYPE	0xBB034008	0x0	Page <a href="#">232</a>
STAT_ACL_REASON	0xBB01C0CC	0x0	Page <a href="#">224</a>
STAT_BRIDGE_DOT1DTPLEARNEDENTRYDIS CARDS	0xBB032840	0x0	Page <a href="#">230</a>
STAT_CF_REASON	0xBB01C0D4	0x0	Page <a href="#">224</a>
STAT_CTRL	0xBB034000	0xC	Page <a href="#">231</a>
STAT_DOT3_LLIDRXFRAMESDROP	0xBB032B9C	0x0	Page <a href="#">239</a>
STAT_PORT_OAM_MIB	0xBB032800	0x0	Page <a href="#">230</a>
STAT_PORT_RST	0xBB034010	0x0	Page <a href="#">233</a>
STAT_PORT_RX_MIB	0xBB032400	0x0	Page <a href="#">227</a>
STAT_PORT_TX_MIB	0xBB032000	0x0	Page <a href="#">225</a>
STAT_PRIVATE_REASON	0xBB01C0C0	0x0	Page <a href="#">224</a>
STAT_RST	0xBB034014	0x0	Page <a href="#">233</a>
STORM_CTRL_ALT_TYPE_SEL	0xBB01708C	0x0	Page <a href="#">211</a>
STORM_CTRL_BC_CTRL	0xBB017068	0x0	Page <a href="#">210</a>
STORM_CTRL_BC_METER_IDX	0xBB017084	0x0	Page <a href="#">211</a>
STORM_CTRL_MC_CTRL	0xBB017064	0x0	Page <a href="#">210</a>
STORM_CTRL_MC_METER_IDX	0xBB01707C	0x0	Page <a href="#">211</a>
STORM_CTRL_UC_CTRL	0xBB017060	0x0	Page <a href="#">209</a>
STORM_CTRL_UC_METER_IDX	0xBB017074	0x0	Page <a href="#">210</a>
STORM_CTRL_UM_CTRL	0xBB01705C	0x0	Page <a href="#">209</a>

Register	Address	Default	Reference
STORM_CTRL_UM_METER_IDX	0xBB01706C	0x0	Page <a href="#">210</a>
SVLAN_C2S	0xBB014000	0x0	Page <a href="#">146</a>
SVLAN_CFG	0xBB0230F8	0x88A8	Page <a href="#">149</a>
SVLAN_CTRL	0xBB01420C	0x0	Page <a href="#">148</a>
SVLAN_EP_DMAC_CTRL	0xBB014200	0x0	Page <a href="#">147</a>
SVLAN_LOOK_UP_TYPE	0xBB0230F4	0x0	Page <a href="#">145</a>
SVLAN_MBRCFG	0xBB014210	0x0	Page <a href="#">149</a>
SVLAN_MC2S	0xBB018000	0x0	Page <a href="#">146</a>
SVLAN_P_SVIDX	0xBB014204	0x0	Page <a href="#">147</a>
SVLAN_SP2C	0xBB02A000	0x0	Page <a href="#">147</a>
SVLAN_UPLINK_PMSK	0xBB0230F0	0x0	Page <a href="#">145</a>
SWITCH_CTRL	0xBB023068	0x3	Page <a href="#">55</a>
SWITCH_MAC	0xBB023060	0x0	Page <a href="#">54</a>
SWTCR0	0xBB800010	0x0	Page <a href="#">406</a>
SW_PWRSV_CTRL	0xBB0001C4	0xF102	Page <a href="#">128</a>
SYNC_TIME	0xBB036028	0x0	Page <a href="#">387</a>
SYS_PKT_BUF_CTRL	0xBB00018C	0x1	Page <a href="#">43</a>

## T

All registers and tables starting with a T.

Register	Address	Default	Reference
TBL_ACCESS_CTRL	0xBB012000	0x0	Page <a href="#">309</a>
TBL_ACCESS_RD_DATA	0xBB01201C	0x0	Page <a href="#">310</a>
TBL_ACCESS_STS	0xBB012004	0x0	Page <a href="#">310</a>
TBL_ACCESS_WR_DATA	0xBB012008	0x0	Page <a href="#">310</a>
TCONT_IDLE_BYTE_STAT	0xBB706C00	0x0	Page <a href="#">381</a>
TH_TX_PREFET	0xBB02D10C	0x2	Page <a href="#">255</a>
TM_ALARM	0xBB000180	0x0	Page <a href="#">42</a>
TM_CTRL	0xBB000170	0x0	Page <a href="#">41</a>
TM_DLY	0xBB00016C	0xFA57E4	Page <a href="#">40</a>
TM_STS	0xBB000174	0x0	Page <a href="#">41</a>
TRUNK_DROP_CFG	0xBB02A2D8	0x0	Page <a href="#">434</a>

## U

All registers and tables starting with a U.

Register	Address	Default	Reference
UNKN_IP4_MC	0xBB01C014	0x0	Page <a href="#">136</a>
UNKN_IP6_MC	0xBB01C018	0x0	Page <a href="#">136</a>
UNKN_L2_MC	0xBB01C010	0x0	Page <a href="#">135</a>
UNKN_MC_PRI	0xBB01C01C	0x0	Page <a href="#">136</a>

Register	Address	Default	Reference
UPS_CTRL2	0xBB0000A8	0x0	Page <a href="#">30</a>
UTP_FIBER_AUTODET	0xBB0001BC	0x0	Page <a href="#">58</a>

## V

All registers and tables starting with a V.

Register	Address	Default	Reference
V6_BD_CTL	0xBB800028	0x0	Page <a href="#">409</a>
VLAN	<Indirect> Type:1 Size:4096	—	Page <a href="#">324</a>
VLAN_CTRL	0xBB013108	0x0	Page <a href="#">142</a>
VLAN_EGRESS_KEEP	0xBB01C038	0x0	Page <a href="#">144</a>
VLAN_EGRESS_TAG	0xBB020030	0x3	Page <a href="#">141</a>
VLAN_EXT_VIDX	0xBB01311C	0x0	Page <a href="#">145</a>
VLAN_INGRESS	0xBB013004	0x0	Page <a href="#">141</a>
VLAN_MBR_CFG	0xBB013008	0x0	Page <a href="#">142</a>
VLAN_PB_FID	0xBB01310C	0x0	Page <a href="#">143</a>
VLAN_PB_FIDEN	0xBB013110	0x0	Page <a href="#">143</a>
VLAN_PB_PRI	0xBB01C034	0x0	Page <a href="#">143</a>
VLAN_PB_VIDX	0xBB013114	0x0	Page <a href="#">144</a>
VLAN_PORT_ACCEPT_FRAME_TYPE	0xBB013000	0x0	Page <a href="#">140</a>
VLAN_PORT_PPVB_VLAN	0xBB013130	0x0	Page <a href="#">150</a>
VLAN_PPVB_VLAN_VAL	0xBB013120	0x0	Page <a href="#">150</a>

## W

All registers and tables starting with a W.

Register	Address	Default	Reference
WAKELPI_SLOT	0xBB00011C	0x0	Page <a href="#">34</a>
WAKELPI_SLOT_PRD	0xBB000118	0x1F	Page <a href="#">33</a>
WAN_TYPE_TABLE	<Indirect> Type:7 Size:8	—	Page <a href="#">404</a>
WFQ_CTRL	0xBB02D800	0x3FFF	Page <a href="#">264</a>
WFQ_PORT_CFG0	0xBB02D830	0x0	Page <a href="#">267</a>
WFQ_PORT_CFG1_7	0xBB02D840	0x0	Page <a href="#">267</a>
WFQ_TYPE_PORT_CFG	0xBB02D894	0x0	Page <a href="#">268</a>
WRAP_GPHY_MISC	0xBB000080	0x0	Page <a href="#">26</a>
WSDS_ANA_00	0xBB022000	0x5026	Page <a href="#">58</a>
WSDS_ANA_01	0xBB022004	0x3	Page <a href="#">59</a>
WSDS_ANA_02	0xBB022008	0x2D18	Page <a href="#">59</a>
WSDS_ANA_03	0xBB02200C	0x6001	Page <a href="#">59</a>

Register	Address	Default	Reference
WSDS_ANA_04	0xBB022010	0x7C	Page 60
WSDS_ANA_05	0xBB022014	0x4003	Page 60
WSDS_ANA_06	0xBB022018	0xFF	Page 60
WSDS_ANA_07	0xBB02201C	0x2490	Page 61
WSDS_ANA_08	0xBB022020	0x1B7	Page 61
WSDS_ANA_09	0xBB022024	0x5	Page 61
WSDS_ANA_0A	0xBB022028	0x730C	Page 62
WSDS_ANA_0B	0xBB02202C	0x10C9	Page 62
WSDS_ANA_0C	0xBB022030	0xE511	Page 63
WSDS_ANA_0D	0xBB022034	0x828	Page 63
WSDS_ANA_0E	0xBB022038	0x1566	Page 63
WSDS_ANA_0F	0xBB02203C	0x9	Page 64
WSDS_ANA_10	0xBB022040	0x1185	Page 64
WSDS_ANA_11	0xBB022044	0x4F80	Page 64
WSDS_ANA_12	0xBB022048	0x0	Page 65
WSDS_ANA_13	0xBB02204C	0x0	Page 65
WSDS_ANA_14	0xBB022050	0x265D	Page 65
WSDS_ANA_15	0xBB022054	0x3072	Page 66
WSDS_ANA_16	0xBB022058	0x2000	Page 66
WSDS_ANA_17	0xBB02205C	0x66	Page 66
WSDS_ANA_18	0xBB022060	0xA8C2	Page 66
WSDS_ANA_19	0xBB022064	0x0	Page 67
WSDS_ANA_1A	0xBB022068	0xDDE0	Page 67
WSDS_ANA_1B	0xBB02206C	0x0	Page 68
WSDS_ANA_1C	0xBB022070	0x8	Page 68
WSDS_ANA_1D	0xBB022074	0x0	Page 68
WSDS_ANA_1E	0xBB022078	0x5450	Page 68
WSDS_ANA_1F	0xBB02207C	0xC970	Page 69
WSDS_ANA_20	0xBB022080	0x267	Page 69
WSDS_ANA_21	0xBB022084	0x27B	Page 69
WSDS_ANA_22	0xBB022088	0x5D80	Page 69
WSDS_ANA_23	0xBB02208C	0x608	Page 70
WSDS_ANA_24	0xBB022090	0x3C0	Page 70
WSDS_ANA_25	0xBB022094	0x1240	Page 71
WSDS_DIG_00	0xBB022098	0xF30	Page 71
WSDS_DIG_01	0xBB02209C	0x0	Page 72
WSDS_DIG_02	0xBB0220A0	0x0	Page 72
WSDS_DIG_03	0xBB0220A4	0x40	Page 72
WSDS_DIG_04	0xBB0220A8	0x0	Page 73
WSDS_DIG_05	0xBB0220AC	0x0	Page 73
WSDS_DIG_06	0xBB0220B0	0xFF	Page 73
WSDS_DIG_07	0xBB0220B4	0x0	Page 73
WSDS_DIG_08	0xBB0220B8	0x0	Page 74
WSDS_DIG_09	0xBB0220BC	0x0	Page 74
WSDS_DIG_0A	0xBB0220C0	0x886	Page 74
WSDS_DIG_0B	0xBB0220C4	0x353	Page 75

Register	Address	Default	Reference
WSDS_DIG_0C	0xBB0220C8	0x5F	Page <a href="#">75</a>
WSDS_DIG_0D	0xBB0220CC	0x3A	Page <a href="#">75</a>
WSDS_DIG_0E	0xBB0220D0	0x0	Page <a href="#">75</a>
WSDS_DIG_0F	0xBB0220D4	0x0	Page <a href="#">76</a>
WSDS_DIG_10	0xBB0220D8	0x0	Page <a href="#">76</a>
WSDS_DIG_11	0xBB0220DC	0x0	Page <a href="#">76</a>
WSDS_DIG_12	0xBB0220E0	0x1E4	Page <a href="#">76</a>
WSDS_DIG_13	0xBB0220E4	0x2000	Page <a href="#">77</a>
WSDS_DIG_14	0xBB0220E8	0x186	Page <a href="#">77</a>
WSDS_DIG_15	0xBB0220EC	0x2	Page <a href="#">77</a>
WSDS_DIG_16	0xBB0220F0	0x0	Page <a href="#">78</a>
WSDS_DIG_17	0xBB0220F4	0x0	Page <a href="#">78</a>
WSDS_DIG_18	0xBB0220F8	0x0	Page <a href="#">78</a>
WSDS_DIG_19	0xBB0220FC	0x0	Page <a href="#">79</a>
WSDS_DIG_1A	0xBB022100	0x0	Page <a href="#">79</a>
WSDS_DIG_1B	0xBB022104	0x0	Page <a href="#">79</a>
WSDS_DIG_1C	0xBB022108	0x0	Page <a href="#">79</a>
WSDS_DIG_1D	0xBB02210C	0x4000	Page <a href="#">80</a>
WSDS_DIG_1E	0xBB022110	0x82	Page <a href="#">80</a>
WSDS_DIG_1F	0xBB022114	0x37256E5	Page <a href="#">80</a>
WSDS_DIG_20	0xBB022118	0x182A	Page <a href="#">81</a>
WSDS_DIG_21	0xBB02211C	0x0	Page <a href="#">81</a>
WSDS_DIG_22	0xBB022120	0x0	Page <a href="#">81</a>
WSDS_DIG_23	0xBB022124	0x0	Page <a href="#">82</a>
WSDS_DIG_24	0xBB022128	0x0	Page <a href="#">82</a>
WSDS_DIG_25	0xBB02212C	0x0	Page <a href="#">82</a>
WSDS_DIG_26	0xBB022130	0x0	Page <a href="#">82</a>
WSDS_DIG_27	0xBB022134	0x0	Page <a href="#">82</a>
WSDS_DIG_28	0xBB022138	0x0	Page <a href="#">83</a>
WSDS_DIG_29	0xBB02213C	0x0	Page <a href="#">83</a>
WSDS_DIG_2A	0xBB022140	0x0	Page <a href="#">83</a>
WSDS_DIG_2B	0xBB022144	0xFFFF	Page <a href="#">83</a>
WSDS_DIG_2C	0xBB022148	0xFFFF	Page <a href="#">83</a>



## Appendix A: Hardware Block View

Hardware block of the chip design. This section is a quick reference to all the tables and register in this datasheet.

### GLB\_CTRL (0x0)

All registers located at GLB\_CTRL memory block.

Register	Offset	P.Array	C.Array	Bits
SKIP_MII_RXER	0x0	NO (0)	NO (0)	32
EXT_RGMXF	0x4	NO (0)	NO (0)	32
EXT_TXC_DLY	0x8	NO (0)	NO (0)	32
GPHY_IND_WD	0xC	NO (0)	NO (0)	32
GPHY_IND_CMD	0x10	NO (0)	NO (0)	32
GPHY_IND_RD	0x14	NO (0)	NO (0)	32
EFUSE_CFG	0x18	NO (0)	NO (0)	32
EFUSE_IND_WD	0x1C	NO (0)	NO (0)	32
EFUSE_IND_CMD	0x20	NO (0)	NO (0)	32
EFUSE_IND_RD	0x24	NO (0)	NO (0)	32
I2C_IND_WD	0x28	NO (0)	YES (2)	32
I2C_IND_CMD	0x30	NO (0)	YES (2)	32
I2C_IND_RD	0x38	NO (0)	YES (2)	32
CFG_PCSXF	0x40	NO (0)	NO (0)	32
CFG_PHY_CTRL	0x44	NO (0)	NO (0)	32
CFG_PHY_POLL_CMD	0x48	NO (0)	NO (0)	32
CFG_PHY_POLL_ADR_0	0x4C	NO (0)	NO (0)	32
CFG_PHY_POLL_ADR_1	0x50	NO (0)	NO (0)	32
CFG_PHY_POLL_INV_0	0x54	NO (0)	NO (0)	32
CFG_PHY_POLL_INV_1	0x58	NO (0)	NO (0)	32
CFG_PHY_POLL_WD_0	0x5C	NO (0)	NO (0)	32
CFG_PHY_POLL_WD_1	0x60	NO (0)	NO (0)	32
CHIP_DEBUG_OUT	0x64	NO (0)	NO (0)	32
CHIP_RST	0x68	NO (0)	NO (0)	32
SOFTWARE_RST	0x6C	NO (0)	NO (0)	32
BIST_CFG	0x70	NO (0)	NO (0)	32
PON_INTEGRATION	0x74	NO (0)	NO (0)	32
WRAP_GPHY_MISC	0x80	NO (0)	NO (0)	32
MISCELLANEOUS_CONFIGURE0	0x84	NO (0)	NO (0)	32
FORCE_P_ABLTY	0x88	YES (7)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
MDX_PHY_REG1	0xA4	NO (0)	NO (0)	32
UPS_CTRL2	0xA8	NO (0)	NO (0)	32
GATING_CLK_1	0xAC	NO (0)	NO (0)	32
ROUTER_UPS_CFG	0xB0	NO (0)	NO (0)	32
P_ABLTY	0xB4	YES (7)	NO (0)	32
GPIO_CTRL_0	0xD0	NO (0)	YES (72)	1
GPIO_CTRL_1	0xDC	NO (0)	YES (72)	1
GPIO_CTRL_2	0xE8	NO (0)	YES (72)	1
GPIO_CTRL_3	0xF4	NO (0)	YES (72)	1
GPIO_CTRL_4	0x100	NO (0)	YES (72)	1
RTL_OUI_CFG	0x10C	NO (0)	NO (0)	32
REVISION_CFG	0x110	NO (0)	NO (0)	32
MODEL_CFG	0x114	NO (0)	NO (0)	32
WAKELPI_SLOT_PRD	0x118	NO (0)	NO (0)	32
WAKELPI_SLOT	0x11C	YES (5)	NO (0)	5
RGM_EEE	0x120	NO (0)	NO (0)	32
ABLTY_FORCE_MODE	0x124	NO (0)	NO (0)	32
DEBUG_SEL	0x128	NO (0)	NO (0)	32
RST_SYNC_FIFO	0x12C	NO (0)	NO (0)	32
SDS_CFG	0x130	NO (0)	NO (0)	32
MAC_ACT_CFG	0x134	NO (0)	NO (0)	32
BYPSS_ABLTY_LOCK	0x138	NO (0)	NO (0)	32
FIFO_ERR_STS	0x13C	NO (0)	NO (0)	32
SDS_AN_RX_CFG	0x140	NO (0)	NO (0)	32
SDS_FIB_STATUS	0x144	NO (0)	NO (0)	32
EXT_STS	0x148	NO (0)	NO (0)	32
AFE_VER	0x14C	NO (0)	NO (0)	32
PON_MODE_CFG	0x150	NO (0)	NO (0)	32
ALL_PORT_LKDN_TIME	0x154	NO (0)	NO (0)	32
MODE_EXT	0x158	NO (0)	NO (0)	32
GPHY_AFE_DBG_CFG	0x15C	NO (0)	NO (0)	32
AD5_CTRL	0x160	NO (0)	NO (0)	32
PWM_CTRL1	0x164	NO (0)	NO (0)	32
PWM_CTRL2	0x168	NO (0)	NO (0)	32
TM_DLY	0x16C	NO (0)	NO (0)	32
TM_CTRL	0x170	NO (0)	NO (0)	32
TM_STS	0x174	NO (0)	NO (0)	32
AD5_ALARM	0x178	NO (0)	NO (0)	32
AD5_DATA	0x17C	NO (0)	NO (0)	32
TM_ALARM	0x180	NO (0)	NO (0)	32
CHIP_INF_SEL	0x184	NO (0)	NO (0)	32
SLIC_INSEL_CTRL	0x188	NO (0)	NO (0)	32
SYS_PKT_BUF_CTRL	0x18C	NO (0)	NO (0)	32
DYNGASP_CTRL	0x190	NO (0)	NO (0)	32
BOND_STRAP_STS0	0x194	NO (0)	NO (0)	32
BOND_STRAP_STS1	0x198	NO (0)	NO (0)	32



Register	Offset	P.Array	C.Array	Bits
BOND_STRAP_STS2	0x19C	NO (0)	NO (0)	32
MISCELLANEOUS_BONDING	0x1A0	NO (0)	NO (0)	32
MISCELLANEOUS_STRAPPING1	0x1A4	NO (0)	NO (0)	32
MISCELLANEOUS_STRAPPING0	0x1A8	NO (0)	NO (0)	32
MAC_DLYLNK	0x1AC	NO (0)	NO (0)	32
PLL_RGM_CTRL1	0x1B0	NO (0)	NO (0)	32
PLL_RGM_CTRL2	0x1B4	NO (0)	NO (0)	32
PLL_RGM_CTRL3	0x1B8	NO (0)	NO (0)	32
UTP_FIBER_AUTODET	0x1BC	NO (0)	NO (0)	32
EEE_TX_SEL_CTRL	0x1C0	NO (0)	NO (0)	32
SW_PWRSV_CTRL	0x1C4	NO (0)	NO (0)	32
DBG_BLK_SEL	0x1C8	NO (0)	NO (0)	32
RGF_VER_GLB_CTRL	0x1CC	NO (0)	NO (0)	32
RSVD_GLB_CTRL	0x1D0	NO (0)	YES (16)	32

### RESERVED (0x400)

All registers located at RESERVED memory block.

Register	Offset	P.Array	C.Array	Bits
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### CHIP\_INFO (0x10000)

All registers located at CHIP\_INFO memory block.

Register	Offset	P.Array	C.Array	Bits
MODEL_NAME_INFO	0x10000	NO (0)	NO (0)	32
CHIP_INFO	0x10004	NO (0)	NO (0)	32
BOND_INFO	0x10008	NO (0)	NO (0)	32

### ALE\_GLB (0x11000)

All registers located at ALE\_GLB memory block.

Register	Offset	P.Array	C.Array	Bits
FORCE_P_DMP	0x11000	NO (0)	YES (7)	7
EN_FORCE_P_DMP	0x11008	NO (0)	NO (0)	32
ACCEPT_MAX_LEN_CTRL	0x1100C	YES (7)	NO (0)	32
MAX_LENGTH_CFG1	0x11028	NO (0)	NO (0)	32
RMK_DSCP_CTRL	0x1102C	NO (0)	YES (64)	6
RMK_DSCP_INT_PRI_CTRL	0x11060	NO (0)	YES (8)	6
OUTPUT_DROP_CFG	0x11068	NO (0)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
OUTPUT_DROP_EN	0x1106C	YES (7)	NO (0)	1
IGMP_GLB_CTRL	0x11070	NO (0)	NO (0)	32
IGMP_P_CTRL	0x11074	YES (7)	NO (0)	32
L34_GLB_CFG	0x11090	NO (0)	NO (0)	32
L34_PORT_TO_WAN	0x11094	YES (7)	YES (8)	1
L34_EXTPORT_TO_WAN	0x110B0	YES (5)	YES (8)	1
L34_WAN_TO_PORT	0x110C4	YES (7)	YES (8)	1
L34_WAN_TO_EXTPORT	0x110E0	YES (5)	YES (8)	1
AVB_PORT_EN	0x110F4	YES (7)	NO (0)	1
AVB_PRI_REMAP	0x110F8	NO (0)	YES (8)	3
PTP_TRANSPARENT_CFG	0x110FC	YES (7)	NO (0)	1
PTP_IGR_MSG_ACT	0x11100	NO (0)	YES (10)	2
PTP_EGR_MSG_ACT	0x11104	NO (0)	YES (10)	2
PTP_RX_TIME	0x11108	NO (0)	NO (0)	64
PTP_P_EN	0x11110	YES (7)	NO (0)	32
RGF_VER_ALE_GLB	0x1112C	NO (0)	NO (0)	32
RSVD_ALE_GLB	0x11130	NO (0)	YES (16)	32

### ALE\_TABLE (0x12000)

All registers located at ALE\_TABLE memory block.

Register	Offset	P.Array	C.Array	Bits
TBL_ACCESS_CTRL	0x12000	NO (0)	NO (0)	32
TBL_ACCESS_STS	0x12004	NO (0)	NO (0)	32
TBL_ACCESS_WR_DATA	0x12008	NO (0)	NO (0)	160
TBL_ACCESS_RD_DATA	0x1201C	NO (0)	NO (0)	160

### ALE\_CVLAN (0x13000)

All registers located at ALE\_CVLAN memory block.

Register	Offset	P.Array	C.Array	Bits
VLAN_PORT_ACCEPT_FRAME_TYPE	0x13000	YES (7)	NO (0)	2
VLAN_INGRESS	0x13004	YES (7)	NO (0)	1
VLAN_MBR_CFG	0x13008	NO (0)	YES (32)	64
VLAN_CTRL	0x13108	NO (0)	NO (0)	32
VLAN_PB_FID	0x1310C	YES (7)	NO (0)	4
VLAN_PB_FIDEN	0x13110	YES (7)	NO (0)	1
VLAN_PB_VIDX	0x13114	YES (7)	NO (0)	5
VLAN_EXT_VIDX	0x1311C	NO (0)	YES (5)	5
VLAN_PPB_VLAN_VAL	0x13120	NO (0)	YES (4)	32
VLAN_PORT_PPB_VLAN	0x13130	YES (7)	YES (4)	32
RGF_VER_ALE_CVLAN	0x131A0	NO (0)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
RSVD_ALE_CVLAN	0x131A4	NO (0)	YES (16)	32

### ALE\_SVLAN (0x14000)

All registers located at ALE\_SVLAN memory block.

Register	Offset	P.Array	C.Array	Bits
SVLAN_C2S	0x14000	NO (0)	YES (128)	32
SVLAN_EP_DMACH_CTRL	0x14200	YES (7)	NO (0)	1
SVLAN_P_SVIDX	0x14204	YES (7)	NO (0)	6
SVLAN_CTRL	0x1420C	NO (0)	NO (0)	32
SVLAN_MBRCFG	0x14210	NO (0)	YES (64)	64
RGF_VER_ALE_SVLAN	0x14410	NO (0)	NO (0)	32
RSVD_ALE_SVLAN	0x14414	NO (0)	YES (16)	32

### ALE\_ACL (0x15000)

All registers located at ALE\_ACL memory block.

Register	Offset	P.Array	C.Array	Bits
ACL_TEMPLATE_CTRL	0x15000	YES (4)	YES (8)	7
CF_OP_DS	0x15020	NO (0)	YES (512)	1
CF_OP_US	0x15060	NO (0)	YES (512)	1
CF_VALID	0x150A0	NO (0)	YES (512)	1
CF_CFG	0x150E0	NO (0)	NO (0)	32
RMK_DSCP_CF_PRI_CTRL	0x150E4	NO (0)	YES (8)	32
ACL_EN	0x15104	YES (7)	NO (0)	1
ACL_PERMIT	0x15108	YES (7)	NO (0)	1
ACL_ACTION	0x1510C	NO (0)	YES (128)	32
ACL_CFG	0x1530C	NO (0)	NO (0)	32
RNG_CHK_VID_RNG	0x15310	NO (0)	YES (8)	32
RNG_CHK_IP_RNG	0x15330	NO (0)	YES (8)	96
RNG_CHK_L4PORT_RNG	0x15390	NO (0)	YES (16)	64
RNG_CHK_PKTLEN_RNG	0x15410	NO (0)	YES (8)	32
RNG_CHK_IP_RNG_CF	0x15430	NO (0)	YES (8)	96
RNG_CHK_L4PORT_RNG_CF	0x15490	NO (0)	YES (8)	64
RGF_VER_ALE_ACL	0x154D0	NO (0)	NO (0)	32
RSVD_ALE_ACL	0x154D4	NO (0)	YES (16)	32

### RESERVED (0x16000)

All registers located at RESERVED memory block.

Register	Offset	P.Array	C.Array	Bits
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## ALE\_L2 (0x17000)

All registers located at ALE\_L2 memory block.

Register	Offset	P.Array	C.Array	Bits
LUT_CFG	0x17000	NO (0)	NO (0)	32
LUT_AGEOUT_CTRL	0x17004	YES (7)	NO (0)	1
LUT_LRN_LIMITNO	0x17008	YES (7)	NO (0)	12
L2_LRN_CNT	0x17018	YES (7)	NO (0)	12
LUT_SYS_LRN_LIMITNO	0x17028	NO (0)	NO (0)	32
L2_SYS_LRN_CNT	0x1702C	NO (0)	NO (0)	32
L2_EFID	0x17030	YES (7)	NO (0)	3
LUT_SYS_LRN_OVER_CTRL	0x17034	NO (0)	NO (0)	32
L2_TBL_FLUSH_CTRL	0x17038	NO (0)	NO (0)	32
L2_TBL_FLUSH_EN	0x1703C	YES (7)	NO (0)	1
MSTI_CTRL	0x17040	YES (7)	YES (16)	2
STORM_CTRL_UM_CTRL	0x1705C	YES (7)	NO (0)	1
STORM_CTRL_UC_CTRL	0x17060	YES (7)	NO (0)	1
STORM_CTRL_MC_CTRL	0x17064	YES (7)	NO (0)	1
STORM_CTRL_BC_CTRL	0x17068	YES (7)	NO (0)	1
STORM_CTRL_UM_METER_IDX	0x1706C	YES (7)	NO (0)	5
STORM_CTRL_UC_METER_IDX	0x17074	YES (7)	NO (0)	5
STORM_CTRL_MC_METER_IDX	0x1707C	YES (7)	NO (0)	5
STORM_CTRL_BC_METER_IDX	0x17084	YES (7)	NO (0)	5
STORM_CTRL_ALT_TYPE_SEL	0x1708C	NO (0)	NO (0)	32
DOT1X_CFG_1	0x17090	NO (0)	NO (0)	32
DOT1X_P_CTRL	0x17094	YES (7)	NO (0)	32
OAM_P_CTRL_0	0x170B0	YES (7)	NO (0)	2
OAM_P_CTRL_1	0x170B4	YES (7)	NO (0)	2
OAM_CTRL_1	0x170B8	NO (0)	NO (0)	32
RGF_VER_ALE_L2	0x170BC	NO (0)	NO (0)	32
RSVD_ALE_L2	0x170C0	NO (0)	YES (16)	32

## ALE\_MLTVLAN (0x18000)

All registers located at ALE\_MLTVLAN memory block.

Register	Offset	P.Array	C.Array	Bits
SVLAN_MC2S	0x18000	NO (0)	YES (8)	96
RGF_VER_ALE_MLTVLAN	0x18060	NO (0)	NO (0)	32
RSVD_ALE_MLTVLAN	0x18064	NO (0)	YES (16)	32

### ALE\_EEE\_LLDP (0x19000)

All registers located at ALE\_EEE\_LLDP memory block.

Register	Offset	P.Array	C.Array	Bits
RGF_VER_ALE_EEE_LLDP	0x19000	NO (0)	NO (0)	32
RSVD_ALE_EEE_LLDP	0x19004	NO (0)	YES (16)	32

### ALE\_RLDP (0x1A000)

All registers located at ALE\_RLDP memory block.

Register	Offset	P.Array	C.Array	Bits
RLDP_CTRL_1	0x1A000	NO (0)	NO (0)	32
RLDP_CHK_STS_CTRL	0x1A004	NO (0)	NO (0)	32
RLDP_LP_STS_CTRL	0x1A008	NO (0)	NO (0)	32
RLDP_RNDM_NUM	0x1A00C	NO (0)	NO (0)	64
RLDP_MAGIC_NUM	0x1A014	NO (0)	NO (0)	64
RLDP_PORT_TX_EN	0x1A01C	YES (6)	NO (0)	1
RLDP_PORT_LP_ENTER_STS	0x1A020	YES (6)	NO (0)	1
RLDP_PORT_LP_LEAVE_STS	0x1A024	YES (6)	NO (0)	1
RLDP_PORT_LP_STS	0x1A028	YES (6)	NO (0)	1
RLDP_PORT_CPU_LP_STS	0x1A02C	YES (6)	NO (0)	1
RLDP_PORT_LP_PNUM	0x1A030	YES (6)	NO (0)	3
RLPP_CTRL	0x1A034	NO (0)	NO (0)	32
RGF_VER_ALE_RLDP	0x1A038	NO (0)	NO (0)	32
RSVD_ALE_RLDP	0x1A03C	NO (0)	YES (16)	32

### ALE\_EAV\_AFBK (0x1B000)

All registers located at ALE\_EAV\_AFBK memory block.

Register	Offset	P.Array	C.Array	Bits
FB_CTRL	0x1B000	NO (0)	NO (0)	32
FB_PORT_CFG	0x1B004	YES (5)	NO (0)	32
FB_PORT_ERR_CNT	0x1B018	YES (5)	NO (0)	8
FB_PORT_MONITOR_CNT	0x1B020	YES (5)	NO (0)	28
PTP_TIME_SEC	0x1B034	NO (0)	NO (0)	64
PTP_TIME_NSEC	0x1B03C	NO (0)	NO (0)	32
PTP_TIME_OFFSET_SEC	0x1B040	NO (0)	NO (0)	64
PTP_TIME_OFFSET_8NSEC	0x1B048	NO (0)	NO (0)	32
PTP_TIME_FREQ	0x1B04C	NO (0)	NO (0)	32
PTP_TIME_CTRL	0x1B050	NO (0)	NO (0)	32
PTP_MEANPATH_DEALY	0x1B054	NO (0)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
RGF_VER_ALE_EAV_AFBK	0x1B058	NO (0)	NO (0)	32
RSVD_ALE_EAV_AFBK	0x1B05C	NO (0)	YES (16)	32
FB_GPHY_ADDR_CTRL	0x1B09C	NO (0)	NO (0)	32

### ALE\_DPM (0x1C000)

All registers located at ALE\_DPM memory block.

Register	Offset	P.Array	C.Array	Bits
LUT_UNMATCHED_SA_CTRL	0x1C000	YES (7)	NO (0)	2
LUT_UNKN_SA_CTRL	0x1C004	YES (7)	NO (0)	2
LUT_UNKN_UC_DA_CTRL	0x1C008	YES (7)	NO (0)	2
LUT_LEARN_OVER_CTRL	0x1C00C	YES (7)	NO (0)	2
UNKN_L2_MC	0x1C010	YES (7)	NO (0)	2
UNKN_IP4_MC	0x1C014	YES (7)	NO (0)	2
UNKN_IP6_MC	0x1C018	YES (7)	NO (0)	2
UNKN_MC_PRI	0x1C01C	NO (0)	NO (0)	32
LUT_BC_FLOOD	0x1C020	YES (7)	NO (0)	1
LUT_UNKN_MC_FLOOD	0x1C024	YES (7)	NO (0)	1
LUT_UNKN_UC_FLOOD	0x1C028	YES (7)	NO (0)	1
L2_IPMC_VLAN_LEAKY	0x1C02C	YES (7)	NO (0)	1
L2_IPMC_ISO_LEAKY	0x1C030	YES (7)	NO (0)	1
VLAN_PB_PRI	0x1C034	YES (7)	NO (0)	3
VLAN_EGRESS_KEEP	0x1C038	YES (7)	NO (0)	7
PORT_TRUNK_GROUP_EN	0x1C040	YES (4)	NO (0)	32
PORT_TRUNK_CTRL	0x1C050	NO (0)	NO (0)	32
PORT_TRUNK_HASH_MAPPING	0x1C054	NO (0)	YES (16)	2
RMA_CTRL00	0x1C058	NO (0)	NO (0)	32
RMA_CTRL01	0x1C05C	NO (0)	NO (0)	32
RMA_CTRL02	0x1C060	NO (0)	NO (0)	32
RMA_CTRL03	0x1C064	NO (0)	NO (0)	32
RMA_CTRL04	0x1C068	NO (0)	NO (0)	32
RMA_CTRL08	0x1C06C	NO (0)	NO (0)	32
RMA_CTRL0D	0x1C070	NO (0)	NO (0)	32
RMA_CTRL0E	0x1C074	NO (0)	NO (0)	32
RMA_CTRL10	0x1C078	NO (0)	NO (0)	32
RMA_CTRL11	0x1C07C	NO (0)	NO (0)	32
RMA_CTRL12	0x1C080	NO (0)	NO (0)	32
RMA_CTRL13	0x1C084	NO (0)	NO (0)	32
RMA_CTRL18	0x1C088	NO (0)	NO (0)	32
RMA_CTRL1A	0x1C08C	NO (0)	NO (0)	32
RMA_CTRL20	0x1C090	NO (0)	NO (0)	32
RMA_CTRL21	0x1C094	NO (0)	NO (0)	32
RMA_CTRL22	0x1C098	NO (0)	NO (0)	32
RMA_CTRL_CDP	0x1C09C	NO (0)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
RMA_CTRL_SSTP	0x1C0A0	NO (0)	NO (0)	32
RMA_CFG	0x1C0A4	NO (0)	NO (0)	32
EEELDP_CTRL_0	0x1C0A8	NO (0)	NO (0)	32
EEELDP_CTRL_1	0x1C0AC	NO (0)	NO (0)	32
L2_SRC_PORT_PERMIT	0x1C0B0	YES (7)	NO (0)	1
L2_SRC_EXT_PERMIT	0x1C0B4	NO (0)	YES (5)	1
IGR_BWCTRL_GLB_CTRL	0x1C0B8	NO (0)	NO (0)	32
DOT1X_CFG_0	0x1C0BC	NO (0)	NO (0)	32
STAT_PRIVATE_REASON	0x1C0C0	YES (7)	NO (0)	10
STAT_ACL_REASON	0x1C0CC	NO (0)	YES (6)	8
STAT_CF_REASON	0x1C0D4	NO (0)	YES (2)	10
FC_P_Q_EGR_DROP_EN	0x1C0D8	YES (7)	YES (8)	1
QOS_INTPRI_TO_QID	0x1C0F4	YES (4)	YES (8)	3
QOS_PORT_QMAP_CTRL	0x1C104	YES (7)	NO (0)	2
QOS_PRI_REMAP_IN_CPU	0x1C108	NO (0)	YES (8)	3
QOS_1Q_PRI_REMAP	0x1C10C	NO (0)	YES (8)	3
QOS_DSCP_REMAP	0x1C110	NO (0)	YES (64)	3
QOS_PB_PRI	0x1C12C	YES (7)	NO (0)	3
PRI_SEL_TBL_CTRL	0x1C130	NO (0)	NO (0)	32
PRI_SEL_TBL_CTRL2	0x1C134	NO (0)	NO (0)	32
OAM_CTRL_0	0x1C138	NO (0)	NO (0)	32
IGMP_MC_GROUP	0x1C13C	NO (0)	YES (64)	64
PON_SID_TO_QID	0x1C33C	NO (0)	YES (128)	7
FC_PON_Q_EGR_DROP_EN	0x1C3BC	NO (0)	YES (128)	1
RGF_VER_ALE_DPM	0x1C3CC	NO (0)	NO (0)	32
RSVD_ALE_DPM	0x1C3D0	NO (0)	YES (16)	32

## INTR (0x1D000)

All registers located at INTR memory block.

Register	Offset	P.Array	C.Array	Bits
INTR_CTRL	0x1D000	NO (0)	NO (0)	32
INTR_IMR	0x1D004	NO (0)	NO (0)	32
INTR_IMS	0x1D008	NO (0)	NO (0)	32
INTR_STAT	0x1D00C	NO (0)	NO (0)	32
L2_LRN_OVER_STS	0x1D010	YES (7)	NO (0)	1
L2_SYS_LRN_OVER_STS	0x1D014	NO (0)	NO (0)	32
SC_P_CTRL_1	0x1D018	NO (0)	NO (0)	32
RGF_VER_INTR	0x1D01C	NO (0)	NO (0)	32
RSVD_INTR	0x1D020	NO (0)	YES (16)	32

## LED (0x1E000)

All registers located at LED memory block.

Register	Offset	P.Array	C.Array	Bits
LED_LED	0x1E000	NO (0)	NO (0)	32
DATA_LED_CFG	0x1E004	NO (0)	YES (32)	32
LED_ACTIVE_LOW_CFG	0x1E084	NO (0)	YES (17)	1
SERI_LED_ACTIVE_LOW_CFG	0x1E088	NO (0)	NO (0)	32
LED_FORCE_VALUE_CFG	0x1E08C	NO (0)	YES (32)	2
LED_BLINK_RATE_CFG	0x1E094	NO (0)	NO (0)	32
LOW_RATE_BLINK_CFG	0x1E098	NO (0)	NO (0)	32
LED_EN	0x1E0A0	NO (0)	NO (0)	32
SERI_LED_CLK_PER	0x1E0A4	NO (0)	NO (0)	32
SERI_LED_REFRESH_TIME	0x1E0A8	NO (0)	NO (0)	32
RGF_VER_LED	0x1E0C0	NO (0)	NO (0)	32
RSVD_LED	0x1E0C4	NO (0)	YES (16)	32
RLDP_BUZZER	0x1E104	NO (0)	NO (0)	32
PON_LED_CFG	0x1E108	NO (0)	NO (0)	32

## RESERVED (0x1F000)

All registers located at RESERVED memory block.

Register	Offset	P.Array	C.Array	Bits
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## PER\_PORT\_MAC (0x20000)

All registers located at PER\_PORT\_MAC memory block.

Register	Offset	P.Array	C.Array	Bits
P_TX_ERR_CNT	0x20000	YES (7)	NO (0)	32
P_CGSTTIMER	0x20004	YES (7)	NO (0)	32
P_MISC	0x20008	YES (7)	NO (0)	32
P_CFG_FRC_RATE	0x2000C	YES (7)	NO (0)	32
P_CUR_RATE	0x20010	YES (7)	NO (0)	32
EEE_EEEP_PORT_CFG	0x20014	YES (5)	NO (0)	32
P_EEECFG	0x20018	YES (5)	NO (0)	32
P_EEETXMTR	0x2001C	YES (5)	NO (0)	32
P_EEERXMTR	0x20020	YES (5)	NO (0)	32
P_EEEP_CFG	0x20024	YES (5)	NO (0)	32
P_EEEPTXMTR	0x20028	YES (5)	NO (0)	32
P_EEEPRXMTR	0x2002C	YES (5)	NO (0)	32
VLAN_EGRESS_TAG	0x20030	YES (7)	NO (0)	32



Register	Offset	P.Array	C.Array	Bits
IGR_BWCTRL_P_CTRL	0x20034	YES (7)	NO (0)	32
FC_P_DBG_PKT_PAGE_CNT	0x20038	YES (7)	NO (0)	32
SC_P_CTRL_0	0x2003C	YES (7)	NO (0)	32
RMK_DOT1Q_RMK_EN_CTRL	0x20040	YES (7)	NO (0)	32
PORT_VM_EN	0x20044	YES (7)	NO (0)	32
PORT_VM_RX	0x20048	YES (7)	NO (0)	32
PORT_VM_TX	0x2004C	YES (7)	NO (0)	32
SPG_PORT_TX_GRP_CTRL	0x20050	YES (7)	NO (0)	32
SPG_PORT_STS	0x20054	YES (7)	NO (0)	32
SPG_P_TX_GRP_CTRL	0x20058	YES (7)	NO (0)	32
SPG_P_LEN_CTRL	0x2005C	YES (7)	NO (0)	32
SPG_P_TX_CNT	0x20060	YES (7)	NO (0)	32
SPG_P_SA	0x20064	YES (7)	NO (0)	64
SPG_P_DA	0x2006C	YES (7)	NO (0)	64
SPG_PORT_USER_PKT	0x20074	YES (7)	NO (0)	32
RGF_VER_PER_PORT_MAC	0x20078	YES (7)	NO (0)	32
RSVD_PER_PORT_MAC	0x2007C	YES (7)	YES (16)	32

### RESERVED (0x20400)

All registers located at RESERVED memory block.

Register	Offset	P.Array	C.Array	Bits
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### SDSREG (0x22000)

All registers located at SDSREG memory block.

Register	Offset	P.Array	C.Array	Bits
WSDS_ANA_00	0x22000	NO (0)	NO (0)	32
WSDS_ANA_01	0x22004	NO (0)	NO (0)	32
WSDS_ANA_02	0x22008	NO (0)	NO (0)	32
WSDS_ANA_03	0x2200C	NO (0)	NO (0)	32
WSDS_ANA_04	0x22010	NO (0)	NO (0)	32
WSDS_ANA_05	0x22014	NO (0)	NO (0)	32
WSDS_ANA_06	0x22018	NO (0)	NO (0)	32
WSDS_ANA_07	0x2201C	NO (0)	NO (0)	32
WSDS_ANA_08	0x22020	NO (0)	NO (0)	32
WSDS_ANA_09	0x22024	NO (0)	NO (0)	32
WSDS_ANA_0A	0x22028	NO (0)	NO (0)	32
WSDS_ANA_0B	0x2202C	NO (0)	NO (0)	32
WSDS_ANA_0C	0x22030	NO (0)	NO (0)	32
WSDS_ANA_0D	0x22034	NO (0)	NO (0)	32
WSDS_ANA_0E	0x22038	NO (0)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
WSDS_ANA_0F	0x2203C	NO (0)	NO (0)	32
WSDS_ANA_10	0x22040	NO (0)	NO (0)	32
WSDS_ANA_11	0x22044	NO (0)	NO (0)	32
WSDS_ANA_12	0x22048	NO (0)	NO (0)	32
WSDS_ANA_13	0x2204C	NO (0)	NO (0)	32
WSDS_ANA_14	0x22050	NO (0)	NO (0)	32
WSDS_ANA_15	0x22054	NO (0)	NO (0)	32
WSDS_ANA_16	0x22058	NO (0)	NO (0)	32
WSDS_ANA_17	0x2205C	NO (0)	NO (0)	32
WSDS_ANA_18	0x22060	NO (0)	NO (0)	32
WSDS_ANA_19	0x22064	NO (0)	NO (0)	32
WSDS_ANA_1A	0x22068	NO (0)	NO (0)	32
WSDS_ANA_1B	0x2206C	NO (0)	NO (0)	32
WSDS_ANA_1C	0x22070	NO (0)	NO (0)	32
WSDS_ANA_1D	0x22074	NO (0)	NO (0)	32
WSDS_ANA_1E	0x22078	NO (0)	NO (0)	32
WSDS_ANA_1F	0x2207C	NO (0)	NO (0)	32
WSDS_ANA_20	0x22080	NO (0)	NO (0)	32
WSDS_ANA_21	0x22084	NO (0)	NO (0)	32
WSDS_ANA_22	0x22088	NO (0)	NO (0)	32
WSDS_ANA_23	0x2208C	NO (0)	NO (0)	32
WSDS_ANA_24	0x22090	NO (0)	NO (0)	32
WSDS_ANA_25	0x22094	NO (0)	NO (0)	32
WSDS_DIG_00	0x22098	NO (0)	NO (0)	32
WSDS_DIG_01	0x2209C	NO (0)	NO (0)	32
WSDS_DIG_02	0x220A0	NO (0)	NO (0)	32
WSDS_DIG_03	0x220A4	NO (0)	NO (0)	32
WSDS_DIG_04	0x220A8	NO (0)	NO (0)	32
WSDS_DIG_05	0x220AC	NO (0)	NO (0)	32
WSDS_DIG_06	0x220B0	NO (0)	NO (0)	32
WSDS_DIG_07	0x220B4	NO (0)	NO (0)	32
WSDS_DIG_08	0x220B8	NO (0)	NO (0)	32
WSDS_DIG_09	0x220BC	NO (0)	NO (0)	32
WSDS_DIG_0A	0x220C0	NO (0)	NO (0)	32
WSDS_DIG_0B	0x220C4	NO (0)	NO (0)	32
WSDS_DIG_0C	0x220C8	NO (0)	NO (0)	32
WSDS_DIG_0D	0x220CC	NO (0)	NO (0)	32
WSDS_DIG_0E	0x220D0	NO (0)	NO (0)	32
WSDS_DIG_0F	0x220D4	NO (0)	NO (0)	32
WSDS_DIG_10	0x220D8	NO (0)	NO (0)	32
WSDS_DIG_11	0x220DC	NO (0)	NO (0)	32
WSDS_DIG_12	0x220E0	NO (0)	NO (0)	32
WSDS_DIG_13	0x220E4	NO (0)	NO (0)	32
WSDS_DIG_14	0x220E8	NO (0)	NO (0)	32
WSDS_DIG_15	0x220EC	NO (0)	NO (0)	32
WSDS_DIG_16	0x220F0	NO (0)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
WSDS_DIG_17	0x220F4	NO (0)	NO (0)	32
WSDS_DIG_18	0x220F8	NO (0)	NO (0)	32
WSDS_DIG_19	0x220FC	NO (0)	NO (0)	32
WSDS_DIG_1A	0x22100	NO (0)	NO (0)	32
WSDS_DIG_1B	0x22104	NO (0)	NO (0)	32
WSDS_DIG_1C	0x22108	NO (0)	NO (0)	32
WSDS_DIG_1D	0x2210C	NO (0)	NO (0)	32
WSDS_DIG_1E	0x22110	NO (0)	NO (0)	32
WSDS_DIG_1F	0x22114	NO (0)	NO (0)	32
WSDS_DIG_20	0x22118	NO (0)	NO (0)	32
WSDS_DIG_21	0x2211C	NO (0)	NO (0)	32
WSDS_DIG_22	0x22120	NO (0)	NO (0)	32
WSDS_DIG_23	0x22124	NO (0)	NO (0)	32
WSDS_DIG_24	0x22128	NO (0)	NO (0)	32
WSDS_DIG_25	0x2212C	NO (0)	NO (0)	32
WSDS_DIG_26	0x22130	NO (0)	NO (0)	32
WSDS_DIG_27	0x22134	NO (0)	NO (0)	32
WSDS_DIG_28	0x22138	NO (0)	NO (0)	32
WSDS_DIG_29	0x2213C	NO (0)	NO (0)	32
WSDS_DIG_2A	0x22140	NO (0)	NO (0)	32
WSDS_DIG_2B	0x22144	NO (0)	NO (0)	32
WSDS_DIG_2C	0x22148	NO (0)	NO (0)	32
RGF_VER_SDSREG	0x2214C	NO (0)	NO (0)	32
RSVD_SDSREG	0x22150	NO (0)	YES (16)	32

### SDS\_IP (0x22800)

All registers located at SDS\_IP memory block.

Register	Offset	P.Array	C.Array	Bits
SDS_REG0	0x22800	NO (0)	NO (0)	32
SDS_REG1	0x22804	NO (0)	NO (0)	32
SDS_REG2	0x22808	NO (0)	NO (0)	32
SDS_REG3	0x2280C	NO (0)	NO (0)	32
SDS_REG4	0x22810	NO (0)	NO (0)	32
SDS_REG5	0x22814	NO (0)	NO (0)	32
SDS_REG6	0x22818	NO (0)	NO (0)	32
SDS_REG7	0x2281C	NO (0)	NO (0)	32
SDS_REG8	0x22820	NO (0)	NO (0)	32
SDS_REG9	0x22824	NO (0)	NO (0)	32
SDS_REG10	0x22828	NO (0)	NO (0)	32
SDS_REG11	0x2282C	NO (0)	NO (0)	32
SDS_REG12	0x22830	NO (0)	NO (0)	32
SDS_REG13	0x22834	NO (0)	NO (0)	32
SDS_REG14	0x22838	NO (0)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
SDS_REG15	0x2283C	NO (0)	NO (0)	32
SDS_REG16	0x22840	NO (0)	NO (0)	32
SDS_REG17	0x22844	NO (0)	NO (0)	32
SDS_REG18	0x22848	NO (0)	NO (0)	32
SDS_REG19	0x2284C	NO (0)	NO (0)	32
SDS_REG20	0x22850	NO (0)	NO (0)	32
SDS_REG21	0x22854	NO (0)	NO (0)	32
SDS_REG22	0x22858	NO (0)	NO (0)	32
SDS_REG23	0x2285C	NO (0)	NO (0)	32
SDS_REG24	0x22860	NO (0)	NO (0)	32
SDS_REG25	0x22864	NO (0)	NO (0)	32
SDS_REG26	0x22868	NO (0)	NO (0)	32
SDS_REG27	0x2286C	NO (0)	NO (0)	32
SDS_REG28	0x22870	NO (0)	NO (0)	32
SDS_REG29	0x22874	NO (0)	NO (0)	32
DUMMY	0x22878	NO (0)	YES (98)	32
SDS_EXT_REG0	0x22A00	NO (0)	NO (0)	32
SDS_EXT_REG1	0x22A04	NO (0)	NO (0)	32
SDS_EXT_REG2	0x22A08	NO (0)	NO (0)	32
SDS_EXT_REG3	0x22A0C	NO (0)	NO (0)	32
SDS_EXT_REG4	0x22A10	NO (0)	NO (0)	32
SDS_EXT_REG5	0x22A14	NO (0)	NO (0)	32
SDS_EXT_REG6	0x22A18	NO (0)	NO (0)	32
SDS_EXT_REG7	0x22A1C	NO (0)	NO (0)	32
SDS_EXT_REG8	0x22A20	NO (0)	NO (0)	32
SDS_EXT_REG9	0x22A24	NO (0)	NO (0)	32
SDS_EXT_REG10	0x22A28	NO (0)	NO (0)	32
SDS_EXT_REG11	0x22A2C	NO (0)	NO (0)	32
SDS_EXT_REG12	0x22A30	NO (0)	NO (0)	32
SDS_EXT_REG13	0x22A34	NO (0)	NO (0)	32
SDS_EXT_REG14	0x22A38	NO (0)	NO (0)	32
SDS_EXT_REG15	0x22A3C	NO (0)	NO (0)	32
SDS_EXT_REG16	0x22A40	NO (0)	NO (0)	32
SDS_EXT_REG24	0x22A44	NO (0)	NO (0)	32
SDS_EXT_REG25	0x22A48	NO (0)	NO (0)	32
SDS_EXT_REG26	0x22A4C	NO (0)	NO (0)	32
SDS_EXT_REG27	0x22A50	NO (0)	NO (0)	32
SDS_EXT_REG28	0x22A54	NO (0)	NO (0)	32
SDS_EXT_REG29	0x22A58	NO (0)	NO (0)	32
SDS_EXT_REG30	0x22A5C	NO (0)	NO (0)	32
DUMMY	0x22A60	NO (0)	YES (104)	32
FIB_REG0	0x22C00	NO (0)	NO (0)	32
FIB_REG1	0x22C04	NO (0)	NO (0)	32
FIB_REG2	0x22C08	NO (0)	NO (0)	32
FIB_REG4	0x22C0C	NO (0)	NO (0)	32
FIB_REG5	0x22C10	NO (0)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
FIB_REG6	0x22C14	NO (0)	NO (0)	32
FIB_REG7	0x22C18	NO (0)	NO (0)	32
FIB_REG8	0x22C1C	NO (0)	NO (0)	32
DUMMY	0x22C20	NO (0)	YES (4)	32
FIB_REG13	0x22C30	NO (0)	NO (0)	32
FIB_REG14	0x22C34	NO (0)	NO (0)	32
DUMMY	0x22C38	NO (0)	NO (0)	32
FIB_REG16	0x22C3C	NO (0)	NO (0)	32
FIB_REG17	0x22C40	NO (0)	NO (0)	32
FIB_REG18	0x22C44	NO (0)	NO (0)	32
FIB_REG19	0x22C48	NO (0)	NO (0)	32
FIB_REG20	0x22C4C	NO (0)	NO (0)	32
FIB_REG21	0x22C50	NO (0)	NO (0)	32
FIB_REG22	0x22C54	NO (0)	NO (0)	32
FIB_REG23	0x22C58	NO (0)	NO (0)	32
FIB_REG28	0x22C5C	NO (0)	NO (0)	32
FIB_REG29	0x22C60	NO (0)	NO (0)	32
FIB_REG30	0x22C64	NO (0)	NO (0)	32
DUMMY	0x22C68	NO (0)	YES (102)	32
FIB_EXT_REG0	0x22E00	NO (0)	NO (0)	32
FIB_EXT_REG1	0x22E04	NO (0)	NO (0)	32
FIB_EXT_REG2	0x22E08	NO (0)	NO (0)	32
FIB_EXT_REG4	0x22E0C	NO (0)	NO (0)	32
FIB_EXT_REG5	0x22E10	NO (0)	NO (0)	32
FIB_EXT_REG6	0x22E14	NO (0)	NO (0)	32
FIB_EXT_REG7	0x22E18	NO (0)	NO (0)	32
FIB_EXT_REG8	0x22E1C	NO (0)	NO (0)	32
DUMMY	0x22E20	NO (0)	YES (4)	32
FIB_EXT_REG13	0x22E30	NO (0)	NO (0)	32
FIB_EXT_REG14	0x22E34	NO (0)	NO (0)	32
DUMMY	0x22E38	NO (0)	NO (0)	32
FIB_EXT_REG16	0x22E3C	NO (0)	NO (0)	32
FIB_EXT_REG17	0x22E40	NO (0)	NO (0)	32
FIB_EXT_REG18	0x22E44	NO (0)	NO (0)	32
FIB_EXT_REG19	0x22E48	NO (0)	NO (0)	32
FIB_EXT_REG20	0x22E4C	NO (0)	NO (0)	32
FIB_EXT_REG21	0x22E50	NO (0)	NO (0)	32
FIB_EXT_REG22	0x22E54	NO (0)	NO (0)	32
FIB_EXT_REG23	0x22E58	NO (0)	NO (0)	32
FIB_EXT_REG24	0x22E5C	NO (0)	NO (0)	32
FIB_EXT_REG25	0x22E60	NO (0)	NO (0)	32
FIB_EXT_REG26	0x22E64	NO (0)	NO (0)	32
FIB_EXT_REG27	0x22E68	NO (0)	NO (0)	32
FIB_EXT_REG28	0x22E6C	NO (0)	NO (0)	32
FIB_EXT_REG29	0x22E70	NO (0)	NO (0)	32
FIB_EXT_REG30	0x22E74	NO (0)	NO (0)	32

## SWCORE (0x23000)

All registers located at SWCORE memory block.

Register	Offset	P.Array	C.Array	Bits
DIGITAL_INTERFACE_SELECT	0x23000	NO (0)	NO (0)	32
I2C_CLOCK_DIV	0x23004	NO (0)	YES (2)	32
REGCTRL_GLB	0x2300C	NO (0)	NO (0)	32
IOPAD_CFG	0x23010	NO (0)	NO (0)	32
IO_LED_EN	0x23014	NO (0)	NO (0)	32
IO_MODE_EN	0x23018	NO (0)	NO (0)	32
RAM_DVS_CFG0	0x2301C	NO (0)	NO (0)	32
RAM_DVS_CFG1	0x23020	NO (0)	NO (0)	32
RAM_DVS_CFG2	0x23024	NO (0)	NO (0)	32
RAM_DVS_CFG3	0x23028	NO (0)	NO (0)	32
RAM_DVS_CFG4	0x2302C	NO (0)	NO (0)	32
RAM_DVS_CFG5	0x23030	NO (0)	NO (0)	32
GLB_MAC_MISC	0x23034	NO (0)	NO (0)	32
HTRAM_DVS_CFG	0x23038	NO (0)	NO (0)	32
HWPKT_GEN_STA	0x2303C	NO (0)	NO (0)	32
FPGA_VER_MAC	0x23040	NO (0)	NO (0)	32
MAC_CPU_TAG_CTRL	0x23044	NO (0)	NO (0)	32
MAC_CPU_TAG_AWARE_CTRL	0x23048	YES (7)	NO (0)	1
MAX_LENGTH_CFG0	0x2304C	NO (0)	NO (0)	32
MAX_LENGTH_LIMINT_IPG	0x23050	NO (0)	NO (0)	32
IOL_RXDROP_CFG	0x23054	NO (0)	NO (0)	32
CFG_BACKPRESSURE	0x23058	NO (0)	NO (0)	32
CFG_UNHIOL	0x2305C	NO (0)	NO (0)	32
SWITCH_MAC	0x23060	NO (0)	NO (0)	64
SWITCH_CTRL	0x23068	NO (0)	NO (0)	32
INBW_BOUND	0x2306C	NO (0)	NO (0)	32
MAX_FIFO_SIZE	0x23070	NO (0)	NO (0)	32
EEE_TX_THR_GIGA	0x23074	NO (0)	NO (0)	32
EEE_TX_THR_FE	0x23078	NO (0)	NO (0)	32
EEE_RX_FC_REG	0x2307C	NO (0)	NO (0)	32
EEE_MISC	0x23080	NO (0)	NO (0)	32
EEE_GIGA_CTRL0	0x23084	NO (0)	NO (0)	32
EEE_GIGA_CTRL1	0x23088	NO (0)	NO (0)	32
EEE_100M_CTRL0	0x2308C	NO (0)	NO (0)	32
EEE_100M_CTRL1	0x23090	NO (0)	NO (0)	32
EEE_BURSTSIZE	0x23094	NO (0)	NO (0)	32
EEE_IFG_CFG	0x23098	NO (0)	NO (0)	32
EEE_RXIDLE	0x2309C	NO (0)	NO (0)	32
EEE_DECISION_WINDOW	0x230A0	NO (0)	NO (0)	32
PS_LINKID_GATCLK_CTRL	0x230A4	NO (0)	NO (0)	32
EEEP_CFG	0x230A8	NO (0)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
EEEP_TIMER_UNIT_CTRL	0x230AC	NO (0)	NO (0)	32
EEEP_TX_TIMER_GIGA_CTRL	0x230B0	NO (0)	NO (0)	32
EEEP_TX_TIMER_500M_CTRL	0x230B4	NO (0)	NO (0)	32
EEEP_TX_TIMER_100M_CTRL	0x230B8	NO (0)	NO (0)	32
EEEP_TX_GIGA_CTRL	0x230BC	NO (0)	NO (0)	32
EEEP_TX_500M_CTRL	0x230C0	NO (0)	NO (0)	32
EEEP_TX_100M_CTRL	0x230C4	NO (0)	NO (0)	32
EEEP_RX_RATE_GIGA_CTRL	0x230C8	NO (0)	NO (0)	32
EEEP_RX_RATE_500M_CTRL	0x230CC	NO (0)	NO (0)	32
EEEP_RX_RATE_100M_CTRL	0x230D0	NO (0)	NO (0)	32
EEEP_RX_SLEEP_STEP_CTRL	0x230D4	NO (0)	NO (0)	32
EEEP_RX_WAKE_TIMER_GIGA_CTRL	0x230D8	NO (0)	NO (0)	32
EEEP_RX_TIMER_GIGA_CTRL	0x230DC	NO (0)	NO (0)	32
EEEP_RX_WAKE_TIMER_500M_CTRL	0x230E0	NO (0)	NO (0)	32
EEEP_RX_TIMER_500M_CTRL	0x230E4	NO (0)	NO (0)	32
EEEP_RX_WAKE_TIMER_100M_CTRL	0x230E8	NO (0)	NO (0)	32
EEEP_RX_TIMER_100M_CTRL	0x230EC	NO (0)	NO (0)	32
SVLAN_UPLINK_PMSK	0x230F0	YES (7)	NO (0)	1
SVLAN_LOOK_UP_TYPE	0x230F4	NO (0)	NO (0)	32
SVLAN_CFG	0x230F8	NO (0)	NO (0)	32
MIR_CTRL	0x230FC	NO (0)	NO (0)	32
FC_CTRL	0x23100	NO (0)	NO (0)	32
FC_DROP_ALL_TH	0x23104	NO (0)	NO (0)	32
FC_PAUSE_ALL_TH	0x23108	NO (0)	NO (0)	32
FC_GLB_FCOFF_HI_TH	0x2310C	NO (0)	NO (0)	32
FC_GLB_FCOFF_LO_TH	0x23110	NO (0)	NO (0)	32
FC_GLB_HI_TH	0x23114	NO (0)	NO (0)	32
FC_GLB_LO_TH	0x23118	NO (0)	NO (0)	32
FC_P_HI_TH	0x2311C	NO (0)	NO (0)	32
FC_P_LO_TH	0x23120	NO (0)	NO (0)	32
FC_P_FCOFF_HI_TH	0x23124	NO (0)	NO (0)	32
FC_P_FCOFF_LO_TH	0x23128	NO (0)	NO (0)	32
FC_JUMBO_GLB_HI_TH	0x2312C	NO (0)	NO (0)	32
FC_JUMBO_GLB_LO_TH	0x23130	NO (0)	NO (0)	32
FC_JUMBO_P_HI_TH	0x23134	NO (0)	NO (0)	32
FC_JUMBO_P_LO_TH	0x23138	NO (0)	NO (0)	32
CLR_MAX_USED_PAGE_CNT	0x2313C	NO (0)	NO (0)	32
FC_TL_USED_PAGE_CNT	0x23140	NO (0)	NO (0)	32
FC_PUB_USED_PAGE_CNT	0x23144	NO (0)	NO (0)	32
FC_PUB_FCOFF_USED_PAGE_CNT	0x23148	NO (0)	NO (0)	32
FC_PUB_JUMBO_USED_PAGE_CNT	0x2314C	NO (0)	NO (0)	32
FC_P_USED_PAGE_CNT	0x23150	YES (7)	NO (0)	32
FC_PON_GLB_HI_TH	0x2316C	NO (0)	NO (0)	32
FC_PON_GLB_LO_TH	0x23170	NO (0)	NO (0)	32
FC_PON_P_HI_TH	0x23174	NO (0)	NO (0)	32
FC_PON_P_LO_TH	0x23178	NO (0)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
FC_PON_Q_EGR_DROP_IDX	0x2317C	NO (0)	YES (128)	3
FC_PON_Q_EGR_DROP_TH	0x231B0	NO (0)	YES (8)	13
FC_PON_Q_EGR_GAP_TH	0x231C0	NO (0)	NO (0)	32
FC_PON_Q_USED_PAGE_CTRL	0x231C4	NO (0)	NO (0)	32
FC_PON_Q_USED_PAGE_CNT	0x231C8	NO (0)	NO (0)	32
RMK_1Q_CTRL	0x231CC	NO (0)	YES (8)	3
RMK_DSCP_RMK_EN_CTRL	0x231D0	YES (7)	NO (0)	32
RLDP_CTRL_0	0x231EC	NO (0)	NO (0)	32
SPG_GLB_CTRL	0x231F0	NO (0)	NO (0)	32
SPG_PAYLOAD	0x231F4	NO (0)	YES (48)	8
PARSER_FIELD_SELTOR_CTRL	0x23224	NO (0)	YES (16)	32
PON_PORT_CTRL	0x23264	NO (0)	NO (0)	32
PONMAC_DRN_CTRL	0x23268	NO (0)	NO (0)	32
RGF_VER_SWCORE	0x2326C	NO (0)	NO (0)	32
RSVD_SWCORE	0x23270	NO (0)	YES (16)	32
CHANGE_DUPLEX_CTRL	0x232B0	NO (0)	NO (0)	32

### RESERVED (0x24000)

All registers located at RESERVED memory block.

Register	Offset	P.Array	C.Array	Bits
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### ALE\_METER (0x25000)

All registers located at ALE\_METER memory block.

Register	Offset	P.Array	C.Array	Bits
METER_TB_CTRL	0x25000	NO (0)	NO (0)	32
METER_GLB_CTRL	0x25004	NO (0)	YES (32)	64
METER_LB_EXCEED_STS	0x25104	NO (0)	YES (32)	1
PON_TB_CTRL	0x25108	NO (0)	NO (0)	32
METER_PKT_RATE	0x2510C	NO (0)	NO (0)	32
RGF_VER_ALE_METER	0x25110	NO (0)	NO (0)	32
RSVD_ALE_METER	0x25114	NO (0)	YES (16)	32

### ALE\_RMA\_ATTACK (0x26000)

All registers located at ALE\_RMA\_ATTACK memory block.

Register	Offset	P.Array	C.Array	Bits
DOS_EN	0x26000	YES (7)	NO (0)	1



Register	Offset	P.Array	C.Array	Bits
DOS_CFG	0x26004	NO (0)	NO (0)	32
DOS_SYN Flood_TH	0x26008	NO (0)	NO (0)	32
DOS_Fin Flood_TH	0x2600C	NO (0)	NO (0)	32
DOS_ICMP Flood_TH	0x26010	NO (0)	NO (0)	32
RGF_VER_ALE_RMA_ATTACK	0x26014	NO (0)	NO (0)	32
RSVD_ALE_RMA_ATTACK	0x26018	NO (0)	YES (16)	32

### ALE\_PISO (0x27000)

All registers located at ALE\_PISO memory block.

Register	Offset	P.Array	C.Array	Bits
PISO_P_MODE0_CTRL	0x27000	YES (7)	NO (0)	13
PISO_P_MODE1_CTRL	0x27010	YES (7)	NO (0)	13
PISO_EXT_MODE0_CTRL	0x27020	NO (0)	YES (5)	13
PISO_EXT_MODE1_CTRL	0x2702C	NO (0)	YES (5)	13
PISO_CTRL	0x27038	NO (0)	NO (0)	32
RGF_VER_ALE_PISO	0x2703C	NO (0)	NO (0)	32
RSVD_ALE_PISO	0x27040	NO (0)	YES (16)	32

### ALE\_HSB (0x28000)

All registers located at ALE\_HSB memory block.

Register	Offset	P.Array	C.Array	Bits
HSB_CTRL	0x28000	NO (0)	NO (0)	32
HSB_DATA	0x28040	NO (0)	YES (20)	32
HSA_DATA	0x280C0	NO (0)	YES (13)	32

### ALE\_HSM (0x29000)

All registers located at ALE\_HSM memory block.

Register	Offset	P.Array	C.Array	Bits
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### ALE\_HSA (0x2A000)

All registers located at ALE\_HSA memory block.

Register	Offset	P.Array	C.Array	Bits
SVLAN_SP2C	0x2A000	NO (0)	YES (128)	32

Register	Offset	P.Array	C.Array	Bits
RMK_P_DSCP_SEL	0x2A200	NO (0)	YES (7)	1
DBG_HSA_EP	0x2A204	NO (0)	NO (0)	32
L34_IPMC_TRAN_TBL	0x2A208	NO (0)	YES (16)	32
L34_IPMC_TTL_CFG	0x2A248	NO (0)	NO (0)	32
RGF_VER_ALE_HSA	0x2A24C	NO (0)	NO (0)	32
RSVD_ALE_HSA	0x2A250	NO (0)	YES (16)	32
HSA_TX_DBG	0x2A290	NO (0)	YES (16)	32
HSARAM_5_CFG	0x2A2D0	NO (0)	NO (0)	32
DBG_EP_CFG	0x2A2D4	NO (0)	NO (0)	32
TRUNK_DROP_CFG	0x2A2D8	NO (0)	NO (0)	32
PAUSE_ALL_LW_CFG	0x2A2DC	NO (0)	NO (0)	32
HYS_PUSAL_CFG	0x2A2E0	NO (0)	NO (0)	32

### ALE\_DEBUG (0x2B000)

All registers located at ALE\_DEBUG memory block.

Register	Offset	P.Array	C.Array	Bits
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### ALE\_PKTGEN (0x2C000)

All registers located at ALE\_PKTGEN memory block.

Register	Offset	P.Array	C.Array	Bits
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### EGR\_OUTQ (0x2D000)

All registers located at EGR\_OUTQ memory block.

Register	Offset	P.Array	C.Array	Bits
FC_Q_EGR_DROP_TH	0x2D000	NO (0)	YES (8)	13
FC_P_EGR_DROP_TH	0x2D010	YES (7)	NO (0)	13
FC_Q_EGR_GAP_TH	0x2D020	NO (0)	NO (0)	32
FC_P_EGR_GAP_TH	0x2D024	NO (0)	NO (0)	32
FC_DBG_CTRL	0x2D028	NO (0)	NO (0)	32
FC_TOTAL_PAGE_CNT	0x2D02C	NO (0)	NO (0)	32
FC_PE_USED_PAGE_CNT	0x2D030	YES (7)	NO (0)	32
FC_Q_USED_PAGE_CNT	0x2D04C	YES (6)	YES (8)	32
TH_TX_PREFET	0x2D10C	NO (0)	NO (0)	32
LOW_QUEUE_TH	0x2D110	NO (0)	NO (0)	32
HIGH_QUEUE_MSK	0x2D114	YES (7)	NO (0)	8
P_QUEUE_EMPTY	0x2D11C	NO (0)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
QUEUE_SEL_IND	0x2D120	NO (0)	NO (0)	32
QUEUE_SEL_IND_DATA	0x2D124	NO (0)	NO (0)	32
GPON_DPRU_RPT_PRD	0x2D128	NO (0)	NO (0)	32
PON_PIR_CIR_IFG	0x2D12C	NO (0)	NO (0)	32
RGF_VER_EGR_OUTQ	0x2D130	NO (0)	NO (0)	32
RSVD_EGR_OUTQ	0x2D134	NO (0)	YES (16)	32

### EGR\_SCH (0x2D800)

All registers located at EGR\_SCH memory block.

Register	Offset	P.Array	C.Array	Bits
WFQ_CTRL	0x2D800	NO (0)	NO (0)	32
EGR_BWCTRL_P_CTRL	0x2D804	YES (7)	NO (0)	32
LINE_RATE_1G	0x2D820	NO (0)	NO (0)	32
LINE_RATE_500M	0x2D824	NO (0)	NO (0)	32
LINE_RATE_100M	0x2D828	NO (0)	NO (0)	32
LINE_RATE_10M	0x2D82C	NO (0)	NO (0)	32
WFQ_PORT_CFG0	0x2D830	YES (7)	NO (0)	16
WFQ_PORT_CFG1_7	0x2D840	YES (7)	YES (7)	10
WFQ_TYPE_PORT_CFG	0x2D894	YES (7)	YES (8)	1
APR_EN_PORT_CFG	0x2D8B0	YES (7)	YES (8)	1
CPU_PORT_RATE_CFG	0x2D8CC	NO (0)	NO (0)	32
APR_METER_PORT_CFG	0x2D8D0	YES (7)	YES (8)	3
MOCIR_TH_H	0x2D8EC	NO (0)	NO (0)	32
MOCIR_TH_L	0x2D8F0	NO (0)	NO (0)	32
MOCIR_BPT	0x2D8F4	NO (0)	NO (0)	32
MOCIR_FRC_MD	0x2D8F8	NO (0)	NO (0)	32
MOCIR_FRC_VAL	0x2D8FC	NO (0)	NO (0)	32
PON_CFG	0x2D900	NO (0)	NO (0)	32
PON_QID_CIR_RATE	0x2D904	NO (0)	YES (128)	17
PON_QID_PIR_RATE	0x2DB04	NO (0)	YES (128)	17
PON_SCH_QMAP	0x2DD04	NO (0)	YES (32)	32
PON_WFQ_WEIGHT	0x2DD84	NO (0)	YES (128)	10
PON_WFQ_TYPE	0x2DE30	NO (0)	YES (128)	1
PON_TCONT_EN	0x2DE40	NO (0)	YES (32)	1
PON_OLT_BW_MTR_FULL	0x2DE44	NO (0)	NO (0)	32
PON_WFQ_IFG_CTRL	0x2DE48	NO (0)	NO (0)	32
RGF_VER_EGR_SCH	0x2DE4C	NO (0)	NO (0)	32
RSVD_EGR_SCH	0x2DE50	NO (0)	YES (16)	32
BYTE_TOKEN_METER	0x2DE90	NO (0)	NO (0)	32

## PKT\_ENCAP (0x2E000)

All registers located at PKT\_ENCAP memory block.

Register	Offset	P.Array	C.Array	Bits
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## PKT\_PARSER (0x2F000)

All registers located at PKT\_PARSER memory block.

Register	Offset	P.Array	C.Array	Bits
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## CFM\_GEN (0x30000)

All registers located at CFM\_GEN memory block.

Register	Offset	P.Array	C.Array	Bits
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## BIST\_CTRL (0x31000)

All registers located at BIST\_CTRL memory block.

Register	Offset	P.Array	C.Array	Bits
BIST_CFG19	0x31000	NO (0)	NO (0)	32
BIST_CFG18	0x31004	NO (0)	NO (0)	32
BIST_CFG17	0x31008	NO (0)	NO (0)	32
BIST_CFG16	0x3100C	NO (0)	NO (0)	32
BIST_CFG15	0x31010	NO (0)	NO (0)	32
BIST_CFG14	0x31014	NO (0)	NO (0)	32
BIST_CFG13	0x31018	NO (0)	NO (0)	32
BIST_CFG12	0x3101C	NO (0)	NO (0)	32
BIST_CFG9	0x31020	NO (0)	NO (0)	32
BIST_CFG8	0x31024	NO (0)	NO (0)	32
BIST_CFG7	0x31028	NO (0)	NO (0)	32
BIST_CFG4	0x3102C	NO (0)	NO (0)	32
BIST_CFG3	0x31030	NO (0)	NO (0)	32
BIST_CFG2	0x31034	NO (0)	NO (0)	32
BIST_CFG1	0x31038	NO (0)	NO (0)	32
BIST_CFG0	0x3103C	NO (0)	NO (0)	32
DIAG_MODE	0x31040	NO (0)	NO (0)	32
DFR_TEST_RESUME	0x31044	NO (0)	NO (0)	32
RGF_VER_BIST_CTRL	0x31048	NO (0)	NO (0)	32
RSVD_BIST_CTRL	0x3104C	NO (0)	YES (16)	32

## MIB\_DATA (0x32000)

All registers located at MIB\_DATA memory block.

Register	Offset	P.Array	C.Array	Bits
STAT_PORT_TX_MIB	0x32000	YES (7)	NO (0)	1024
STAT_PORT_RX_MIB	0x32400	YES (7)	NO (0)	1024
STAT_PORT_OAM_MIB	0x32800	YES (7)	NO (0)	64
STAT_BRIDGE_DOT1DTPLEARNEDENTRYDISCARDS	0x32840	NO (0)	NO (0)	32
STAT_ACL_CNT	0x32880	NO (0)	YES (32)	32
OMCI_DROP_PKT_CNT	0x32900	NO (0)	NO (0)	32
OMCI_TX_PKT_CNT	0x32904	NO (0)	NO (0)	32
OMCI_RX_PKT_CNT	0x32908	NO (0)	NO (0)	32
OMCI_TX_BYTE_CNT	0x3290C	NO (0)	NO (0)	32
OMCI_RX_BYTE_CNT	0x32910	NO (0)	NO (0)	32
OMCI_CRC_ERROR_PKT_CNT	0x32914	NO (0)	NO (0)	32
DOT3_Q_TX_FRAMES	0x32918	NO (0)	YES (128)	32
DOT3_MPCP_RX_DISC	0x32B18	NO (0)	NO (0)	32
DOT3_EPON_FEC_CORRECTED_BLOCKS	0x32B1C	NO (0)	NO (0)	32
DOT3_EPON_FEC_UNCORRECTED_BLOCKS	0x32B20	NO (0)	NO (0)	32
DOT3_EPON_FEC_CODING_VIO	0x32B24	NO (0)	NO (0)	32
DOT3_NOT_BROADCAST_BIT_NOT_ONU_LLID	0x32B28	NO (0)	NO (0)	32
DOT3_BROADCAST_BIT_PLUS_ONU_LLID	0x32B2C	NO (0)	NO (0)	32
DOT3_BROADCAST_NOT_ONUID	0x32B30	NO (0)	NO (0)	32
DOT3_CRC8_ERRORS	0x32B34	NO (0)	NO (0)	32
DOT3_LLID_RX_BROADCAST_DROP_FRAMES	0x32B38	NO (0)	NO (0)	32
DOT3_MPCP_TX_REPORT	0x32B3C	NO (0)	YES (8)	32
DOT3_MPCP_EX_GATE	0x32B5C	NO (0)	YES (8)	32
DOT3_ONUID_NOT_BROADCAST	0x32B7C	NO (0)	YES (8)	32
STAT_DOT3_LLIDRXFRAMESDROP	0x32B9C	NO (0)	YES (8)	32
DOT3_MPCP_TX_REG_REQ	0x32BBC	NO (0)	NO (0)	32

## MIB\_CTRL (0x34000)

All registers located at MIB\_CTRL memory block.

Register	Offset	P.Array	C.Array	Bits
STAT_CTRL	0x34000	NO (0)	NO (0)	32
STAT_ACL_CNT_MODE	0x34004	NO (0)	YES (16)	1
STAT_ACL_CNT_TYPE	0x34008	NO (0)	YES (16)	1
STAT_ACL_CNT_RST	0x3400C	NO (0)	YES (32)	1
STAT_PORT_RST	0x34010	YES (7)	NO (0)	1

Register	Offset	P.Array	C.Array	Bits
STAT_RST	0x34014	NO (0)	NO (0)	32
EPON_STAT_RST	0x34018	NO (0)	NO (0)	32
RGF_VER_MIB_CTRL	0x3401C	NO (0)	NO (0)	32
RSVD_MIB_CTRL	0x34020	NO (0)	YES (16)	32

### MAC\_PON (0x35000)

All registers located at MAC\_PON memory block.

Register	Offset	P.Array	C.Array	Bits
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### EPON\_CTRL (0x36000)

All registers located at EPON\_CTRL memory block.

Register	Offset	P.Array	C.Array	Bits
EPON_FEC_CONFIG	0x36000	NO (0)	NO (0)	32
EPON_ASIC_TIMING_ADJUST1	0x36004	NO (0)	NO (0)	32
EPON_ASIC_TIMING_ADJUST2	0x36008	NO (0)	NO (0)	32
EPON_RGSTR1	0x3600C	NO (0)	NO (0)	32
EPON_RGSTR2	0x36010	NO (0)	NO (0)	32
EPON_RGSTR3	0x36014	NO (0)	NO (0)	32
EPON_DEBUG1	0x36018	NO (0)	NO (0)	32
EPON_DEBUG2	0x3601C	NO (0)	NO (0)	32
EPON_TIMER_CONFIG1	0x36020	NO (0)	NO (0)	32
EPON_INTR	0x36024	NO (0)	NO (0)	32
SYNC_TIME	0x36028	NO (0)	NO (0)	32
LASER_ON_OFF_TIME	0x3602C	NO (0)	NO (0)	32
MIN_GRANT_START	0x36030	NO (0)	NO (0)	32
MAX_GRANT_START	0x36034	NO (0)	NO (0)	32
EPON_TIME_CTRL	0x36038	NO (0)	NO (0)	32
EP_MISC	0x3603C	NO (0)	NO (0)	32
LLID_TABLE	0x36040	NO (0)	YES (8)	32
EPON_MPCP_CTR	0x36060	NO (0)	NO (0)	32
EPON_GRANT_LIST0	0x36064	NO (0)	YES (32)	32
EPON_GRANT_LIST1	0x360E4	NO (0)	YES (32)	32
EPON_GRANT_LIST2	0x36164	NO (0)	YES (32)	32
EPON_TX_CTRL	0x361E4	NO (0)	NO (0)	32
RGF_VER_EPON_CTRL	0x361E8	NO (0)	NO (0)	32
RSVD_EPON_CTRL	0x361EC	NO (0)	YES (16)	32
EPON_DECRYPT_CFG	0x3622C	NO (0)	NO (0)	32
EPON_DECRYPT_KEY0	0x36230	NO (0)	YES (8)	24
EPON_DECRYPT_KEY1	0x36250	NO (0)	YES (8)	24
EPON_MISC_CFG	0x36270	NO (0)	NO (0)	32

### TBD (0x37000)

All registers located at TBD memory block.

Register	Offset	P.Array	C.Array	Bits
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### RESERVED (0x38000)

All registers located at RESERVED memory block.

Register	Offset	P.Array	C.Array	Bits
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### GPON\_PAGE0 (0x700000)

All registers located at GPON\_PAGE0 memory block.

Register	Offset	P.Array	C.Array	Bits
GPON_INT_DLT	0x700000	NO (0)	NO (0)	32
GPON_RESET	0x70000C	NO (0)	NO (0)	32
GPON_VERSION	0x700010	NO (0)	NO (0)	32
GPON_TEST	0x700014	NO (0)	NO (0)	32
GPON_AES_BYPASS	0x700020	NO (0)	NO (0)	32
GPON_INTR_MASK	0x700040	NO (0)	NO (0)	32
GPON_INTR_STS	0x700044	NO (0)	NO (0)	32

### GPON\_PAGE1 (0x701000)

All registers located at GPON\_PAGE1 memory block.

Register	Offset	P.Array	C.Array	Bits
GPON_GTC_DS_INTR_DLT	0x701000	NO (0)	NO (0)	32
GPON_GTC_DS_INTR_MASK	0x701004	NO (0)	NO (0)	32
GPON_GTC_DS_INTR_STS	0x701008	NO (0)	NO (0)	32
GPON_GTC_DS_ONU_ID_STATUS	0x701010	NO (0)	NO (0)	32
GPON_GTC_DS_CFG	0x701014	NO (0)	NO (0)	32
GPON_GTC_DS_PLOAM_CFG	0x70101C	NO (0)	NO (0)	32
GPON_GTC_DS_LOS_CFG_STS	0x701040	NO (0)	NO (0)	32
GPON_GTC_DS_SUPERFRAME_CNT	0x701048	NO (0)	NO (0)	32
GPON_GTC_DS_PLOAM_IND	0x701080	NO (0)	NO (0)	32
GPON_GTC_DS_PLOAM_MSG	0x7010A0	NO (0)	YES (8)	32
GPON_GTC_DS_ALLOC_IND	0x7010C0	NO (0)	NO (0)	32
GPON_GTC_DS_ALLOC_WR	0x7010C4	NO (0)	NO (0)	32
GPON_GTC_DS_ALLOC_RD	0x7010CC	NO (0)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
GPON_GTC_DS_PORT_IND	0x701100	NO (0)	NO (0)	32
GPON_GTC_DS_PORT_WR	0x701104	NO (0)	NO (0)	32
GPON_GTC_DS_PORT_RD	0x70110C	NO (0)	NO (0)	32
GPON_GTC_DS_PORT_CNTR_IND	0x701140	NO (0)	NO (0)	32
GPON_GTC_DS_PORT_CNTR_STAT	0x701144	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_BIP_ERR _BLK	0x701184	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_BIP_ERR_BIT	0x701188	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_FEC_COR RECT_BIT	0x70118C	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_FEC_COR RECT_BYTE	0x701190	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_FEC_COR RECT_CW	0x701194	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_FEC_UNC OR_CW	0x701198	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_LOM	0x70119C	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_PLOAM_A CPT	0x7011A0	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_PLOAM_FAIL	0x7011A4	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_BWM_FAIL	0x7011A8	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_BWM_INV	0x7011AC	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_ACTIVE	0x7011B0	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_BWM_ACP T	0x7011B4	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_GEM_LOS	0x7011B8	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_HEC_COR RECT	0x7011BC	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_GEM_IDLE	0x7011C0	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_GEM_FAIL	0x7011C4	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_GEM_NON _IDLE	0x7011C8	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_PLEN_CO RRECT	0x7011CC	NO (0)	NO (0)	32
GPON_GTC_DS_OMCI_PTI	0x701204	NO (0)	NO (0)	32
GPON_GTC_DS_ETH_PTI	0x701208	NO (0)	NO (0)	32
GPON_GTC_DS_TRAFFIC_CFG	0x701400	NO (0)	YES (128)	32

## GPON\_PAGE2 (0x702000)

All registers located at GPON\_PAGE2 memory block.

Register	Offset	P.Array	C.Array	Bits
GPON_BWMAP_CTRL	0x70200C	NO (0)	NO (0)	32
GPON_BWMAP_STS	0x702010	NO (0)	NO (0)	32
GPON_BWMAP_DATA	0x702400	NO (0)	YES (256)	32



### GPON\_PAGE3 (0x703000)

All registers located at GPON\_PAGE3 memory block.

Register	Offset	P.Array	C.Array	Bits
GPON_AES_INTR_DLT	0x703000	NO (0)	NO (0)	32
GPON_AES_INTR_MASK	0x703004	NO (0)	NO (0)	32
GPON_AES_INTR_STS	0x703008	NO (0)	NO (0)	32
GPON_AES_KEY_SWITCH_REQ	0x703010	NO (0)	NO (0)	32
GPON_AES_KEY_SWITCH_TIME	0x703014	NO (0)	NO (0)	32
GPON_AES_KEY_WORD_IND	0x703020	NO (0)	NO (0)	32
GPON_AES_WORD_DATA	0x703024	NO (0)	NO (0)	32

### GPON\_PAGE4 (0x704000)

All registers located at GPON\_PAGE4 memory block.

Register	Offset	P.Array	C.Array	Bits
GPON_GEM_DS_RX_CNTR_IND	0x704040	NO (0)	NO (0)	32
GPON_GEM_DS_RX_CNTR_STAT	0x704044	NO (0)	NO (0)	32
GPON_GEM_DS_FWD_CNTR_IND	0x70404C	NO (0)	NO (0)	32
GPON_GEM_DS_FWD_CNTR_STAT	0x704050	NO (0)	NO (0)	32
GPON_GEM_DS_MISC_IND	0x704064	NO (0)	NO (0)	32
GPON_GEM_DS_MISC_CNTR_STAT	0x704068	NO (0)	NO (0)	32
GPON_GEM_DS_MC_CFG	0x704080	NO (0)	NO (0)	32
GPON_GEM_DS_MC_IND	0x704084	NO (0)	NO (0)	32
GPON_GEM_DS_MC_WR	0x704088	NO (0)	NO (0)	32
GPON_GEM_DS_MC_RD	0x704090	NO (0)	NO (0)	32
GPON_GEM_DS_FRM_TIMEOUT	0x704098	NO (0)	NO (0)	32
GPON_GEM_DS_MC_ADDR_PTN_IPV4	0x70409C	NO (0)	NO (0)	32
GPON_GEM_DS_MC_ADDR_PTN_IPV6	0x7040A0	NO (0)	NO (0)	32

### GPON\_PAGE5 (0x705000)

All registers located at GPON\_PAGE5 memory block.

Register	Offset	P.Array	C.Array	Bits
GPON_GTC_US_INTR_DLT	0x705000	NO (0)	NO (0)	32
GPON_GTC_US_INTR_MASK	0x705004	NO (0)	NO (0)	32
GPON_GTC_US_INTR_STS	0x705008	NO (0)	NO (0)	32
GPON_GTC_US_ONU_ID	0x705010	NO (0)	NO (0)	32
GPON_GTC_US_CFG	0x705014	NO (0)	NO (0)	32
GPON_GTC_US_WRITE_PROTECT	0x705018	NO (0)	NO (0)	32
GPON_GTC_US_TX_PATTERN_CTL	0x705020	NO (0)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
GPON_GTC_US_TX_PATTERN_BG	0x705024	NO (0)	NO (0)	32
GPON_GTC_US_TX_PATTERN_FG	0x705028	NO (0)	NO (0)	32
GPON_GTC_US_MIN_DELAY	0x705040	NO (0)	NO (0)	32
GPON_GTC_US_EQD	0x705044	NO (0)	NO (0)	32
GPON_GTC_US_LASER	0x70504C	NO (0)	NO (0)	32
GPON_GTC_US_BOH_CFG	0x705054	NO (0)	NO (0)	32
GPON_GTC_US_BOH_DATA	0x705080	NO (0)	YES (12)	32
GPON_GTC_US_PLOAM_IND	0x7050C0	NO (0)	NO (0)	32
GPON_GTC_US_PLOAM_DATA	0x7050E0	NO (0)	YES (8)	32
GPON_GTC_US_PLOAM_CFG	0x705100	NO (0)	NO (0)	32
GPON_GTC_US_MISC_CNTR_IDX	0x705140	NO (0)	NO (0)	32
GPON_GTC_US_MISC_CNTR_STAT	0x705148	NO (0)	NO (0)	32
GPON_GTC_US_RDI	0x705180	NO (0)	NO (0)	32
GPON_GTC_US_DG	0x705184	NO (0)	NO (0)	32
GPON_GTC_US_OPTIC_SD_TH	0x705188	NO (0)	NO (0)	32
GPON_GTC_US_PROC_MODE	0x705200	NO (0)	NO (0)	32

### GPON\_PAGE6 (0x706000)

All registers located at GPON\_PAGE6 memory block.

Register	Offset	P.Array	C.Array	Bits
GPON_GEM_US_INTR_DLT	0x706000	NO (0)	NO (0)	32
GPON_GEM_US_INTR_MASK	0x706004	NO (0)	NO (0)	32
GPON_GEM_US_INTR_STS	0x706008	NO (0)	NO (0)	32
GPON_GEM_US_PTI_CFG	0x706020	NO (0)	NO (0)	32
GPON_GEM_US_ETH_GEM_RX_CNTR_I DX	0x706048	NO (0)	NO (0)	32
GPON_GEM_US_ETH_GEM_RX_CNTR_S TAT	0x70604C	NO (0)	NO (0)	32
GPON_GEM_US_PTN_CTRL	0x706054	NO (0)	NO (0)	32
GPON_GEM_US_PORT_MAP	0x706400	NO (0)	YES (128)	32
GPON_GEM_US_BYTE_STAT	0x706800	NO (0)	YES (128)	64
TCONT_IDLE_BYTE_STAT	0x706C00	NO (0)	YES (32)	64

### NIC (0x710000)

All registers located at NIC memory block.

Register	Offset	P.Array	C.Array	Bits
NIC_ID_CRTL0	0x710000	NO (0)	NO (0)	32
NIC_ID_CRTL1	0x710004	NO (0)	NO (0)	32
NIC_MC_CRTL0	0x710008	NO (0)	NO (0)	32
NIC_MC_CRTL1	0x71000C	NO (0)	NO (0)	32
NIC_MIB0	0x710010	NO (0)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
NIC_MIB1	0x710014	NO (0)	NO (0)	32
NIC_MIB2	0x710018	NO (0)	NO (0)	32
NIC_MIB3	0x71001C	NO (0)	NO (0)	32
NIC_MIB4	0x710020	NO (0)	NO (0)	32
NIC_MIB5	0x710024	NO (0)	NO (0)	32
NIC_MIB6	0x710028	NO (0)	NO (0)	32
NIC_STS	0x710034	NO (0)	NO (0)	32
NIC_COM	0x710038	NO (0)	NO (0)	32
NIC_INTR	0x71003C	NO (0)	NO (0)	32
NIC_IMR0_CFG	0x710040	NO (0)	NO (0)	32
NIC_IMR1_CFG	0x710044	NO (0)	NO (0)	32
NIC_ISR1_CFG	0x710048	NO (0)	NO (0)	32
NIC_INT_ROUTE	0x71004C	NO (0)	NO (0)	32
NIC_TC	0x710050	NO (0)	NO (0)	32
NIC_RC	0x710054	NO (0)	NO (0)	32
NIC_CPUTAG	0x710058	NO (0)	NO (0)	32
NIC_CONFIG	0x71005C	NO (0)	NO (0)	32
NIC_CPUTAG1	0x710060	NO (0)	NO (0)	32
NIC_MS	0x710068	NO (0)	NO (0)	32
NIC_MIIA	0x71006C	NO (0)	NO (0)	32
NIC_SWINT	0x710070	NO (0)	NO (0)	32
NIC_VLAN	0x710074	NO (0)	NO (0)	32
NIC_LED_CR	0x710080	NO (0)	NO (0)	32

### NIC\_DMA (0x720000)

All registers located at NIC\_DMA memory block.

Register	Offset	P.Array	C.Array	Bits
NIC_TXFPD1	0x720000	NO (0)	NO (0)	32
NIC_TXCDO1	0x720004	NO (0)	NO (0)	32
NIC_TXFDP2	0x720010	NO (0)	NO (0)	32
NIC_TXCDO2	0x720014	NO (0)	NO (0)	32
NIC_TXFDP3	0x720020	NO (0)	NO (0)	32
NIC_TXCDO3	0x720024	NO (0)	NO (0)	32
NIC_TXFDP4	0x720030	NO (0)	NO (0)	32
NIC_TXCDO4	0x720034	NO (0)	NO (0)	32
NIC_TXFDP5	0x720040	NO (0)	NO (0)	32
NIC_TXCDO5	0x720044	NO (0)	NO (0)	32
NIC_RRING_ROUTING1	0x720070	NO (0)	NO (0)	32
NIC_RRING_ROUTING2	0x720074	NO (0)	NO (0)	32
NIC_RRING_ROUTING3	0x720078	NO (0)	NO (0)	32
NIC_RRING_ROUTING4	0x72007C	NO (0)	NO (0)	32
NIC_RRING_ROUTING5	0x720080	NO (0)	NO (0)	32
NIC_RRING_ROUTING6	0x720084	NO (0)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
DUMMY	0x720088	NO (0)	YES (2)	32
NIC_RXFDP2	0x720090	NO (0)	NO (0)	32
NIC_RXCDORINGRS2	0x720094	NO (0)	NO (0)	32
NIC_RX_CPU_DESN2	0x720098	NO (0)	NO (0)	32
NIC_RX_DES_THRES2	0x72009C	NO (0)	NO (0)	32
NIC_RXFDP3	0x7200A0	NO (0)	NO (0)	32
NIC_RXCDORINGRS3	0x7200A4	NO (0)	NO (0)	32
NIC_RX_CPU_DESN3	0x7200A8	NO (0)	NO (0)	32
NIC_RX_DES_THRES3	0x7200AC	NO (0)	NO (0)	32
NIC_RXFDP4	0x7200B0	NO (0)	NO (0)	32
NIC_RXCDORINGRS4	0x7200B4	NO (0)	NO (0)	32
NIC_RX_CPU_DESN4	0x7200B8	NO (0)	NO (0)	32
NIC_RX_DES_THRES4	0x7200BC	NO (0)	NO (0)	32
NIC_RXFDP5	0x7200C0	NO (0)	NO (0)	32
NIC_RXCDORINGRS5	0x7200C4	NO (0)	NO (0)	32
NIC_RX_CPU_DESN5	0x7200C8	NO (0)	NO (0)	32
NIC_RX_DES_THRES5	0x7200CC	NO (0)	NO (0)	32
NIC_RXFDP6	0x7200D0	NO (0)	NO (0)	32
NIC_RXCDORINGRS6	0x7200D4	NO (0)	NO (0)	32
NIC_RX_CPU_DESN6	0x7200D8	NO (0)	NO (0)	32
NIC_RX_DES_THRES6	0x7200DC	NO (0)	NO (0)	32
DUMMY	0x7200E0	NO (0)	YES (4)	32
NIC_RXFDP1	0x7200F0	NO (0)	NO (0)	32
NIC_RXCDORINGRS1	0x7200F4	NO (0)	NO (0)	32
DUMMY	0x7200F8	NO (0)	NO (0)	32
NIC_SMSA	0x7200FC	NO (0)	NO (0)	32
NIC_PROBE_SELECT	0x720100	NO (0)	NO (0)	32
NIC_DIAGNOSE1	0x720104	NO (0)	NO (0)	32
DUMMY	0x720108	NO (0)	YES (9)	32
NIC_RX_PSE1_TXC_OUT_SEL1	0x72012C	NO (0)	NO (0)	32
NIC_ETNRXCPU1	0x720130	NO (0)	NO (0)	32
NIC_ETN_IO_CMD	0x720134	NO (0)	NO (0)	32
NIC_ETN_IO_CMD1	0x720138	NO (0)	NO (0)	32
NIC_WOL	0x72013C	NO (0)	NO (0)	32

### NAT\_CTRL (0x800000)

All registers located at NAT\_CTRL memory block.

Register	Offset	P.Array	C.Array	Bits
NIFP	0x800000	NO (0)	NO (0)	32
NIFEP	0x800004	NO (0)	NO (0)	32
NIFVCH	0x800008	NO (0)	NO (0)	32
NIFVCL	0x80000C	NO (0)	NO (0)	32
SWTCR0	0x800010	NO (0)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
PP_AGE	0x800014	NO (0)	NO (0)	32
NB_TRF	0x800018	NO (0)	NO (0)	128
V6_BD_CTL	0x800028	NO (0)	NO (0)	32
BD_TRF	0x80002C	NO (0)	NO (0)	32
BD_CFG	0x800030	NO (0)	NO (0)	32

### NAT\_INDIR (0x800100)

All registers located at NAT\_INDIR memory block.

Register	Offset	P.Array	C.Array	Bits
NAT_TBL_ACCESS_CTRL	0x800100	NO (0)	NO (0)	32
NAT_TBL_ACCESS_CLR	0x800104	NO (0)	NO (0)	32
NAT_TBL_ACCESS_RDDATA	0x800108	NO (0)	NO (0)	160
NAT_TBL_ACCESS_WRDATA	0x80011C	NO (0)	NO (0)	160

### NAT\_HSBA (0x800200)

All registers located at NAT\_HSBA memory block.

Register	Offset	P.Array	C.Array	Bits
HSBA_CTRL	0x800200	NO (0)	NO (0)	32
HSB_DESC	0x800204	NO (0)	YES (10)	32
HSA_DESC	0x80022C	NO (0)	YES (4)	32

### NAT\_L4\_TRF0 (0x800300)

All registers located at NAT\_L4\_TRF0 memory block.

Register	Offset	P.Array	C.Array	Bits
L4_TRF0	0x800300	NO (0)	YES (2048)	1

### NAT\_L4\_TRF1 (0x800400)

All registers located at NAT\_L4\_TRF1 memory block.

Register	Offset	P.Array	C.Array	Bits
L4_TRF1	0x800400	NO (0)	YES (2048)	1

**NAT\_ARP\_TRF0 (0x800500)**

All registers located at NAT\_ARP\_TRF0 memory block.

Register	Offset	P.Array	C.Array	Bits
ARP_TRF0	0x800500	NO (0)	YES (512)	1

**NAT\_ARP\_TRF1 (0x800600)**

All registers located at NAT\_ARP\_TRF1 memory block.

Register	Offset	P.Array	C.Array	Bits
ARP_TRF1	0x800600	NO (0)	YES (512)	1

## Appendix B: Switch Feature View

Switch feature of the chip design. This section is a quick reference to all the tables and register in this datasheet.

### Interface

All registers located at Interface feature.

Register	Offset	P.Array	C.Array	Bits
DIGITAL_INTERFACE_SELECT	0x23000	NO (0)	NO (0)	32
SKIP_MII_RXER	0x0	NO (0)	NO (0)	32
EXT_RGMXF	0x4	NO (0)	NO (0)	32
I2C_CLOCK_DIV	0x23004	NO (0)	YES (2)	32
EXT_TXC_DLY	0x8	NO (0)	NO (0)	32
GPHY_IND_WD	0xC	NO (0)	NO (0)	32
GPHY_IND_CMD	0x10	NO (0)	NO (0)	32
GPHY_IND_RD	0x14	NO (0)	NO (0)	32
EFUSE_CFG	0x18	NO (0)	NO (0)	32
EFUSE_IND_WD	0x1C	NO (0)	NO (0)	32
EFUSE_IND_CMD	0x20	NO (0)	NO (0)	32
EFUSE_IND_RD	0x24	NO (0)	NO (0)	32
I2C_IND_WD	0x28	NO (0)	YES (2)	32
I2C_IND_CMD	0x30	NO (0)	YES (2)	32
I2C_IND_RD	0x38	NO (0)	YES (2)	32
REGCTRL_GLB	0x2300C	NO (0)	NO (0)	32
IOPAD_CFG	0x23010	NO (0)	NO (0)	32
IO_LED_EN	0x23014	NO (0)	NO (0)	32
IO_MODE_EN	0x23018	NO (0)	NO (0)	32
CFG_PCSXF	0x40	NO (0)	NO (0)	32
CFG_PHY_CTRL	0x44	NO (0)	NO (0)	32
CFG_PHY_POLL_CMD	0x48	NO (0)	NO (0)	32
CFG_PHY_POLL_ADR_0	0x4C	NO (0)	NO (0)	32
CFG_PHY_POLL_ADR_1	0x50	NO (0)	NO (0)	32
CFG_PHY_POLL_INV_0	0x54	NO (0)	NO (0)	32
CFG_PHY_POLL_INV_1	0x58	NO (0)	NO (0)	32
CFG_PHY_POLL_WD_0	0x5C	NO (0)	NO (0)	32
CFG_PHY_POLL_WD_1	0x60	NO (0)	NO (0)	32
CHIP_DEBUG_OUT	0x64	NO (0)	NO (0)	32

## Reset

All registers located at Reset feature.

Register	Offset	P.Array	C.Array	Bits
CHIP_RST	0x68	NO (0)	NO (0)	32
SOFTWARE_RST	0x6C	NO (0)	NO (0)	32

## Interrupt

All registers located at Interrupt feature.

Register	Offset	P.Array	C.Array	Bits
INTR_CTRL	0x1D000	NO (0)	NO (0)	32
INTR_IMR	0x1D004	NO (0)	NO (0)	32
INTR_IMS	0x1D008	NO (0)	NO (0)	32
INTR_STAT	0x1D00C	NO (0)	NO (0)	32

## BIST & BISR

All registers located at BIST & BISR feature.

Register	Offset	P.Array	C.Array	Bits
BIST_CFG19	0x31000	NO (0)	NO (0)	32
BIST_CFG18	0x31004	NO (0)	NO (0)	32
BIST_CFG17	0x31008	NO (0)	NO (0)	32
BIST_CFG16	0x3100C	NO (0)	NO (0)	32
BIST_CFG15	0x31010	NO (0)	NO (0)	32
BIST_CFG14	0x31014	NO (0)	NO (0)	32
BIST_CFG13	0x31018	NO (0)	NO (0)	32
BIST_CFG12	0x3101C	NO (0)	NO (0)	32
BIST_CFG9	0x31020	NO (0)	NO (0)	32
BIST_CFG8	0x31024	NO (0)	NO (0)	32
BIST_CFG7	0x31028	NO (0)	NO (0)	32
BIST_CFG4	0x3102C	NO (0)	NO (0)	32
BIST_CFG3	0x31030	NO (0)	NO (0)	32
BIST_CFG2	0x31034	NO (0)	NO (0)	32
BIST_CFG1	0x31038	NO (0)	NO (0)	32
BIST_CFG0	0x3103C	NO (0)	NO (0)	32
DIAG_MODE	0x31040	NO (0)	NO (0)	32
DFR_TEST_RESUME	0x31044	NO (0)	NO (0)	32
BIST_CFG	0x70	NO (0)	NO (0)	32
RAM_DVS_CFG0	0x2301C	NO (0)	NO (0)	32
RAM_DVS_CFG1	0x23020	NO (0)	NO (0)	32



Register	Offset	P.Array	C.Array	Bits
RAM_DVS_CFG2	0x23024	NO (0)	NO (0)	32
RAM_DVS_CFG3	0x23028	NO (0)	NO (0)	32
RAM_DVS_CFG4	0x2302C	NO (0)	NO (0)	32
RAM_DVS_CFG5	0x23030	NO (0)	NO (0)	32
PON_INTEGRATION	0x74	NO (0)	NO (0)	32

## CPU relative

All registers located at CPU relative feature.

Register	Offset	P.Array	C.Array	Bits
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## LED

All registers located at LED feature.

Register	Offset	P.Array	C.Array	Bits
LED_LED	0x1E000	NO (0)	NO (0)	32
DATA_LED_CFG	0x1E004	NO (0)	YES (32)	32
LED_ACTIVE_LOW_CFG	0x1E084	NO (0)	YES (17)	1
SERI_LED_ACTIVE_LOW_CFG	0x1E088	NO (0)	NO (0)	32
LED_FORCE_VALUE_CFG	0x1E08C	NO (0)	YES (32)	2
LED_BLINK_RATE_CFG	0x1E094	NO (0)	NO (0)	32
LOW_RATE_BLINK_CFG	0x1E098	NO (0)	NO (0)	32
LED_EN	0x1E0A0	NO (0)	NO (0)	32
SERI_LED_CLK_PER	0x1E0A4	NO (0)	NO (0)	32
SERI_LED_REFRESH_TIME	0x1E0A8	NO (0)	NO (0)	32

## HW Misc.

All registers located at HW Misc. feature.

Register	Offset	P.Array	C.Array	Bits
FORCE_P_DMP	0x11000	NO (0)	YES (7)	7
EN_FORCE_P_DMP	0x11008	NO (0)	NO (0)	32
GLB_MAC_MISC	0x23034	NO (0)	NO (0)	32
WRAP_GPHY_MISC	0x80	NO (0)	NO (0)	32

## Chp Information

All registers located at Chp Information feature.

Register	Offset	P.Array	C.Array	Bits
MODEL_NAME_INFO	0x10000	NO (0)	NO (0)	32
CHIP_INFO	0x10004	NO (0)	NO (0)	32
BOND_INFO	0x10008	NO (0)	NO (0)	32
MISCELLANEOUS_CONFIGURE0	0x84	NO (0)	NO (0)	32
FORCE_P_ABLTY	0x88	YES (7)	NO (0)	32
MDX_PHY_REG1	0xA4	NO (0)	NO (0)	32
UPS_CTRL2	0xA8	NO (0)	NO (0)	32
GATING_CLK_1	0xAC	NO (0)	NO (0)	32
ROUTER_UPS_CFG	0xB0	NO (0)	NO (0)	32
P_ABLTY	0xB4	YES (7)	NO (0)	32
GPIO_CTRL_0	0xD0	NO (0)	YES (72)	1
GPIO_CTRL_1	0xDC	NO (0)	YES (72)	1
GPIO_CTRL_2	0xE8	NO (0)	YES (72)	1
GPIO_CTRL_3	0xF4	NO (0)	YES (72)	1
GPIO_CTRL_4	0x100	NO (0)	YES (72)	1
RTL_OUI_CFG	0x10C	NO (0)	NO (0)	32
REVISION_CFG	0x110	NO (0)	NO (0)	32
MODEL_CFG	0x114	NO (0)	NO (0)	32
WAKELPI_SLOT_PRD	0x118	NO (0)	NO (0)	32
WAKELPI_SLOT	0x11C	YES (5)	NO (0)	5
RGM_EEE	0x120	NO (0)	NO (0)	32
ABLTY_FORCE_MODE	0x124	NO (0)	NO (0)	32
DEBUG_SEL	0x128	NO (0)	NO (0)	32
RST_SYNC_FIFO	0x12C	NO (0)	NO (0)	32
SDS_CFG	0x130	NO (0)	NO (0)	32
MAC_ACT_CFG	0x134	NO (0)	NO (0)	32
BYPSS_ABLTY_LOCK	0x138	NO (0)	NO (0)	32
FIFO_ERR_STS	0x13C	NO (0)	NO (0)	32
SDS_AN_RX_CFG	0x140	NO (0)	NO (0)	32
SDS_FIB_STATUS	0x144	NO (0)	NO (0)	32
EXT_STS	0x148	NO (0)	NO (0)	32
AFE_VER	0x14C	NO (0)	NO (0)	32
PON_MODE_CFG	0x150	NO (0)	NO (0)	32
HTRAM_DVS_CFG	0x23038	NO (0)	NO (0)	32
HWPKT_GEN_STA	0x2303C	NO (0)	NO (0)	32
ALL_PORT_LKDN_TIME	0x154	NO (0)	NO (0)	32
MODE_EXT	0x158	NO (0)	NO (0)	32
GPHY_AFE_DBG_CFG	0x15C	NO (0)	NO (0)	32
AD5_CTRL	0x160	NO (0)	NO (0)	32
PWM_CTRL1	0x164	NO (0)	NO (0)	32
PWM_CTRL2	0x168	NO (0)	NO (0)	32
TM_DLY	0x16C	NO (0)	NO (0)	32
TM_CTRL	0x170	NO (0)	NO (0)	32
TM_STS	0x174	NO (0)	NO (0)	32
AD5_ALARM	0x178	NO (0)	NO (0)	32
AD5_DATA	0x17C	NO (0)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
TM_ALARM	0x180	NO (0)	NO (0)	32
CHIP_INF_SEL	0x184	NO (0)	NO (0)	32
SLIC_INSEL_CTRL	0x188	NO (0)	NO (0)	32
SYS_PKT_BUF_CTRL	0x18C	NO (0)	NO (0)	32
DYNGASP_CTRL	0x190	NO (0)	NO (0)	32
BOND_STRAP_STS0	0x194	NO (0)	NO (0)	32
BOND_STRAP_STS1	0x198	NO (0)	NO (0)	32
BOND_STRAP_STS2	0x19C	NO (0)	NO (0)	32
MISCELLANEOUS_BONDING	0x1A0	NO (0)	NO (0)	32
MISCELLANEOUS_STRAPPING1	0x1A4	NO (0)	NO (0)	32
MISCELLANEOUS_STRAPPING0	0x1A8	NO (0)	NO (0)	32
MAC_DLYLNK	0x1AC	NO (0)	NO (0)	32
PLL_RGM_CTRL1	0x1B0	NO (0)	NO (0)	32
PLL_RGM_CTRL2	0x1B4	NO (0)	NO (0)	32
PLL_RGM_CTRL3	0x1B8	NO (0)	NO (0)	32

## MAC Control

All registers located at MAC Control feature.

Register	Offset	P.Array	C.Array	Bits
FPGA_VER_MAC	0x23040	NO (0)	NO (0)	32
MAC_CPU_TAG_CTRL	0x23044	NO (0)	NO (0)	32
MAC_CPU_TAG_AWARE_CTRL	0x23048	YES (7)	NO (0)	1
ACCEPT_MAX_LEN_CTRL	0x1100C	YES (7)	NO (0)	32
MAX_LENGTH_CFG1	0x11028	NO (0)	NO (0)	32
MAX_LENGTH_CFG0	0x2304C	NO (0)	NO (0)	32
MAX_LENGTH_LIMINT_IPG	0x23050	NO (0)	NO (0)	32
IOL_RXDROP_CFG	0x23054	NO (0)	NO (0)	32
CFG_BACKPRESSURE	0x23058	NO (0)	NO (0)	32
CFG_UNHIOL	0x2305C	NO (0)	NO (0)	32
SWITCH_MAC	0x23060	NO (0)	NO (0)	64
SWITCH_CTRL	0x23068	NO (0)	NO (0)	32
INBW_BOUND	0x2306C	NO (0)	NO (0)	32
MAX_FIFO_SIZE	0x23070	NO (0)	NO (0)	32
P_TX_ERR_CNT	0x20000	YES (7)	NO (0)	32
P_CGSTTIMER	0x20004	YES (7)	NO (0)	32
P_MISC	0x20008	YES (7)	NO (0)	32
P_CFG_FRC_RATE	0x2000C	YES (7)	NO (0)	32
P_CUR_RATE	0x20010	YES (7)	NO (0)	32
UTP_FIBER_AUTODET	0x1BC	NO (0)	NO (0)	32

## PHY & Serdes

All registers located at PHY & Serdes feature.

Register	Offset	P.Array	C.Array	Bits
WSDS_ANA_00	0x22000	NO (0)	NO (0)	32
WSDS_ANA_01	0x22004	NO (0)	NO (0)	32
WSDS_ANA_02	0x22008	NO (0)	NO (0)	32
WSDS_ANA_03	0x2200C	NO (0)	NO (0)	32
WSDS_ANA_04	0x22010	NO (0)	NO (0)	32
WSDS_ANA_05	0x22014	NO (0)	NO (0)	32
WSDS_ANA_06	0x22018	NO (0)	NO (0)	32
WSDS_ANA_07	0x2201C	NO (0)	NO (0)	32
WSDS_ANA_08	0x22020	NO (0)	NO (0)	32
WSDS_ANA_09	0x22024	NO (0)	NO (0)	32
WSDS_ANA_0A	0x22028	NO (0)	NO (0)	32
WSDS_ANA_0B	0x2202C	NO (0)	NO (0)	32
WSDS_ANA_0C	0x22030	NO (0)	NO (0)	32
WSDS_ANA_0D	0x22034	NO (0)	NO (0)	32
WSDS_ANA_0E	0x22038	NO (0)	NO (0)	32
WSDS_ANA_0F	0x2203C	NO (0)	NO (0)	32
WSDS_ANA_10	0x22040	NO (0)	NO (0)	32
WSDS_ANA_11	0x22044	NO (0)	NO (0)	32
WSDS_ANA_12	0x22048	NO (0)	NO (0)	32
WSDS_ANA_13	0x2204C	NO (0)	NO (0)	32
WSDS_ANA_14	0x22050	NO (0)	NO (0)	32
WSDS_ANA_15	0x22054	NO (0)	NO (0)	32
WSDS_ANA_16	0x22058	NO (0)	NO (0)	32
WSDS_ANA_17	0x2205C	NO (0)	NO (0)	32
WSDS_ANA_18	0x22060	NO (0)	NO (0)	32
WSDS_ANA_19	0x22064	NO (0)	NO (0)	32
WSDS_ANA_1A	0x22068	NO (0)	NO (0)	32
WSDS_ANA_1B	0x2206C	NO (0)	NO (0)	32
WSDS_ANA_1C	0x22070	NO (0)	NO (0)	32
WSDS_ANA_1D	0x22074	NO (0)	NO (0)	32
WSDS_ANA_1E	0x22078	NO (0)	NO (0)	32
WSDS_ANA_1F	0x2207C	NO (0)	NO (0)	32
WSDS_ANA_20	0x22080	NO (0)	NO (0)	32
WSDS_ANA_21	0x22084	NO (0)	NO (0)	32
WSDS_ANA_22	0x22088	NO (0)	NO (0)	32
WSDS_ANA_23	0x2208C	NO (0)	NO (0)	32
WSDS_ANA_24	0x22090	NO (0)	NO (0)	32
WSDS_ANA_25	0x22094	NO (0)	NO (0)	32
WSDS_DIG_00	0x22098	NO (0)	NO (0)	32
WSDS_DIG_01	0x2209C	NO (0)	NO (0)	32
WSDS_DIG_02	0x220A0	NO (0)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
WSDS_DIG_03	0x220A4	NO (0)	NO (0)	32
WSDS_DIG_04	0x220A8	NO (0)	NO (0)	32
WSDS_DIG_05	0x220AC	NO (0)	NO (0)	32
WSDS_DIG_06	0x220B0	NO (0)	NO (0)	32
WSDS_DIG_07	0x220B4	NO (0)	NO (0)	32
WSDS_DIG_08	0x220B8	NO (0)	NO (0)	32
WSDS_DIG_09	0x220BC	NO (0)	NO (0)	32
WSDS_DIG_0A	0x220C0	NO (0)	NO (0)	32
WSDS_DIG_0B	0x220C4	NO (0)	NO (0)	32
WSDS_DIG_0C	0x220C8	NO (0)	NO (0)	32
WSDS_DIG_0D	0x220CC	NO (0)	NO (0)	32
WSDS_DIG_0E	0x220D0	NO (0)	NO (0)	32
WSDS_DIG_0F	0x220D4	NO (0)	NO (0)	32
WSDS_DIG_10	0x220D8	NO (0)	NO (0)	32
WSDS_DIG_11	0x220DC	NO (0)	NO (0)	32
WSDS_DIG_12	0x220E0	NO (0)	NO (0)	32
WSDS_DIG_13	0x220E4	NO (0)	NO (0)	32
WSDS_DIG_14	0x220E8	NO (0)	NO (0)	32
WSDS_DIG_15	0x220EC	NO (0)	NO (0)	32
WSDS_DIG_16	0x220F0	NO (0)	NO (0)	32
WSDS_DIG_17	0x220F4	NO (0)	NO (0)	32
WSDS_DIG_18	0x220F8	NO (0)	NO (0)	32
WSDS_DIG_19	0x220FC	NO (0)	NO (0)	32
WSDS_DIG_1A	0x22100	NO (0)	NO (0)	32
WSDS_DIG_1B	0x22104	NO (0)	NO (0)	32
WSDS_DIG_1C	0x22108	NO (0)	NO (0)	32
WSDS_DIG_1D	0x2210C	NO (0)	NO (0)	32
WSDS_DIG_1E	0x22110	NO (0)	NO (0)	32
WSDS_DIG_1F	0x22114	NO (0)	NO (0)	32
WSDS_DIG_20	0x22118	NO (0)	NO (0)	32
WSDS_DIG_21	0x2211C	NO (0)	NO (0)	32
WSDS_DIG_22	0x22120	NO (0)	NO (0)	32
WSDS_DIG_23	0x22124	NO (0)	NO (0)	32
WSDS_DIG_24	0x22128	NO (0)	NO (0)	32
WSDS_DIG_25	0x2212C	NO (0)	NO (0)	32
WSDS_DIG_26	0x22130	NO (0)	NO (0)	32
WSDS_DIG_27	0x22134	NO (0)	NO (0)	32
WSDS_DIG_28	0x22138	NO (0)	NO (0)	32
WSDS_DIG_29	0x2213C	NO (0)	NO (0)	32
WSDS_DIG_2A	0x22140	NO (0)	NO (0)	32
WSDS_DIG_2B	0x22144	NO (0)	NO (0)	32
WSDS_DIG_2C	0x22148	NO (0)	NO (0)	32
SDS_REG0	0x22800	NO (0)	NO (0)	32
SDS_REG1	0x22804	NO (0)	NO (0)	32
SDS_REG2	0x22808	NO (0)	NO (0)	32
SDS_REG3	0x2280C	NO (0)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
SDS_REG4	0x22810	NO (0)	NO (0)	32
SDS_REG5	0x22814	NO (0)	NO (0)	32
SDS_REG6	0x22818	NO (0)	NO (0)	32
SDS_REG7	0x2281C	NO (0)	NO (0)	32
SDS_REG8	0x22820	NO (0)	NO (0)	32
SDS_REG9	0x22824	NO (0)	NO (0)	32
SDS_REG10	0x22828	NO (0)	NO (0)	32
SDS_REG11	0x2282C	NO (0)	NO (0)	32
SDS_REG12	0x22830	NO (0)	NO (0)	32
SDS_REG13	0x22834	NO (0)	NO (0)	32
SDS_REG14	0x22838	NO (0)	NO (0)	32
SDS_REG15	0x2283C	NO (0)	NO (0)	32
SDS_REG16	0x22840	NO (0)	NO (0)	32
SDS_REG17	0x22844	NO (0)	NO (0)	32
SDS_REG18	0x22848	NO (0)	NO (0)	32
SDS_REG19	0x2284C	NO (0)	NO (0)	32
SDS_REG20	0x22850	NO (0)	NO (0)	32
SDS_REG21	0x22854	NO (0)	NO (0)	32
SDS_REG22	0x22858	NO (0)	NO (0)	32
SDS_REG23	0x2285C	NO (0)	NO (0)	32
SDS_REG24	0x22860	NO (0)	NO (0)	32
SDS_REG25	0x22864	NO (0)	NO (0)	32
SDS_REG26	0x22868	NO (0)	NO (0)	32
SDS_REG27	0x2286C	NO (0)	NO (0)	32
SDS_REG28	0x22870	NO (0)	NO (0)	32
SDS_REG29	0x22874	NO (0)	NO (0)	32
DUMMY	0x22878	NO (0)	YES (98)	32
SDS_EXT_REG0	0x22A00	NO (0)	NO (0)	32
SDS_EXT_REG1	0x22A04	NO (0)	NO (0)	32
SDS_EXT_REG2	0x22A08	NO (0)	NO (0)	32
SDS_EXT_REG3	0x22A0C	NO (0)	NO (0)	32
SDS_EXT_REG4	0x22A10	NO (0)	NO (0)	32
SDS_EXT_REG5	0x22A14	NO (0)	NO (0)	32
SDS_EXT_REG6	0x22A18	NO (0)	NO (0)	32
SDS_EXT_REG7	0x22A1C	NO (0)	NO (0)	32
SDS_EXT_REG8	0x22A20	NO (0)	NO (0)	32
SDS_EXT_REG9	0x22A24	NO (0)	NO (0)	32
SDS_EXT_REG10	0x22A28	NO (0)	NO (0)	32
SDS_EXT_REG11	0x22A2C	NO (0)	NO (0)	32
SDS_EXT_REG12	0x22A30	NO (0)	NO (0)	32
SDS_EXT_REG13	0x22A34	NO (0)	NO (0)	32
SDS_EXT_REG14	0x22A38	NO (0)	NO (0)	32
SDS_EXT_REG15	0x22A3C	NO (0)	NO (0)	32
SDS_EXT_REG16	0x22A40	NO (0)	NO (0)	32
SDS_EXT_REG24	0x22A44	NO (0)	NO (0)	32
SDS_EXT_REG25	0x22A48	NO (0)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
SDS_EXT_REG26	0x22A4C	NO (0)	NO (0)	32
SDS_EXT_REG27	0x22A50	NO (0)	NO (0)	32
SDS_EXT_REG28	0x22A54	NO (0)	NO (0)	32
SDS_EXT_REG29	0x22A58	NO (0)	NO (0)	32
SDS_EXT_REG30	0x22A5C	NO (0)	NO (0)	32
DUMMY	0x22A60	NO (0)	YES (104)	32
FIB_REG0	0x22C00	NO (0)	NO (0)	32
FIB_REG1	0x22C04	NO (0)	NO (0)	32
FIB_REG2	0x22C08	NO (0)	NO (0)	32
FIB_REG4	0x22C0C	NO (0)	NO (0)	32
FIB_REG5	0x22C10	NO (0)	NO (0)	32
FIB_REG6	0x22C14	NO (0)	NO (0)	32
FIB_REG7	0x22C18	NO (0)	NO (0)	32
FIB_REG8	0x22C1C	NO (0)	NO (0)	32
DUMMY	0x22C20	NO (0)	YES (4)	32
FIB_REG13	0x22C30	NO (0)	NO (0)	32
FIB_REG14	0x22C34	NO (0)	NO (0)	32
DUMMY	0x22C38	NO (0)	NO (0)	32
FIB_REG16	0x22C3C	NO (0)	NO (0)	32
FIB_REG17	0x22C40	NO (0)	NO (0)	32
FIB_REG18	0x22C44	NO (0)	NO (0)	32
FIB_REG19	0x22C48	NO (0)	NO (0)	32
FIB_REG20	0x22C4C	NO (0)	NO (0)	32
FIB_REG21	0x22C50	NO (0)	NO (0)	32
FIB_REG22	0x22C54	NO (0)	NO (0)	32
FIB_REG23	0x22C58	NO (0)	NO (0)	32
FIB_REG28	0x22C5C	NO (0)	NO (0)	32
FIB_REG29	0x22C60	NO (0)	NO (0)	32
FIB_REG30	0x22C64	NO (0)	NO (0)	32
DUMMY	0x22C68	NO (0)	YES (102)	32
FIB_EXT_REG0	0x22E00	NO (0)	NO (0)	32
FIB_EXT_REG1	0x22E04	NO (0)	NO (0)	32
FIB_EXT_REG2	0x22E08	NO (0)	NO (0)	32
FIB_EXT_REG4	0x22E0C	NO (0)	NO (0)	32
FIB_EXT_REG5	0x22E10	NO (0)	NO (0)	32
FIB_EXT_REG6	0x22E14	NO (0)	NO (0)	32
FIB_EXT_REG7	0x22E18	NO (0)	NO (0)	32
FIB_EXT_REG8	0x22E1C	NO (0)	NO (0)	32
DUMMY	0x22E20	NO (0)	YES (4)	32
FIB_EXT_REG13	0x22E30	NO (0)	NO (0)	32
FIB_EXT_REG14	0x22E34	NO (0)	NO (0)	32
DUMMY	0x22E38	NO (0)	NO (0)	32
FIB_EXT_REG16	0x22E3C	NO (0)	NO (0)	32
FIB_EXT_REG17	0x22E40	NO (0)	NO (0)	32
FIB_EXT_REG18	0x22E44	NO (0)	NO (0)	32
FIB_EXT_REG19	0x22E48	NO (0)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
FIB_EXT_REG20	0x22E4C	NO (0)	NO (0)	32
FIB_EXT_REG21	0x22E50	NO (0)	NO (0)	32
FIB_EXT_REG22	0x22E54	NO (0)	NO (0)	32
FIB_EXT_REG23	0x22E58	NO (0)	NO (0)	32
FIB_EXT_REG24	0x22E5C	NO (0)	NO (0)	32
FIB_EXT_REG25	0x22E60	NO (0)	NO (0)	32
FIB_EXT_REG26	0x22E64	NO (0)	NO (0)	32
FIB_EXT_REG27	0x22E68	NO (0)	NO (0)	32
FIB_EXT_REG28	0x22E6C	NO (0)	NO (0)	32
FIB_EXT_REG29	0x22E70	NO (0)	NO (0)	32
FIB_EXT_REG30	0x22E74	NO (0)	NO (0)	32

## RTCT

All registers located at RTCT feature.

Register	Offset	P.Array	C.Array	Bits
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## Power Saving

All registers located at Power Saving feature.

Register	Offset	P.Array	C.Array	Bits
EEE_TX_SEL_CTRL	0x1C0	NO (0)	NO (0)	32
EEE_EEEP_PORT_CFG	0x20014	YES (5)	NO (0)	32
P_EEECFG	0x20018	YES (5)	NO (0)	32
P_EEETXMTR	0x2001C	YES (5)	NO (0)	32
P_EEERXMTR	0x20020	YES (5)	NO (0)	32
EEE_TX_THR_GIGA	0x23074	NO (0)	NO (0)	32
EEE_TX_THR_FE	0x23078	NO (0)	NO (0)	32
EEE_RX_FC_REG	0x2307C	NO (0)	NO (0)	32
EEE_MISC	0x23080	NO (0)	NO (0)	32
EEE_GIGA_CTRL0	0x23084	NO (0)	NO (0)	32
EEE_GIGA_CTRL1	0x23088	NO (0)	NO (0)	32
EEE_100M_CTRL0	0x2308C	NO (0)	NO (0)	32
EEE_100M_CTRL1	0x23090	NO (0)	NO (0)	32
EEE_BURSTSIZE	0x23094	NO (0)	NO (0)	32
EEE_IFG_CFG	0x23098	NO (0)	NO (0)	32
EEE_RXIDLE	0x2309C	NO (0)	NO (0)	32
EEE_DECISION_WINDOW	0x230A0	NO (0)	NO (0)	32
PS_LINKID_GATCLK_CTRL	0x230A4	NO (0)	NO (0)	32
P_EEEP_CFG	0x20024	YES (5)	NO (0)	32
EEEP_CFG	0x230A8	NO (0)	NO (0)	32
EEEP_TIMER_UNIT_CTRL	0x230AC	NO (0)	NO (0)	32



Register	Offset	P.Array	C.Array	Bits
EEEP_TX_TIMER_GIGA_CTRL	0x230B0	NO (0)	NO (0)	32
EEEP_TX_TIMER_500M_CTRL	0x230B4	NO (0)	NO (0)	32
EEEP_TX_TIMER_100M_CTRL	0x230B8	NO (0)	NO (0)	32
EEEP_TX_GIGA_CTRL	0x230BC	NO (0)	NO (0)	32
EEEP_TX_500M_CTRL	0x230C0	NO (0)	NO (0)	32
EEEP_TX_100M_CTRL	0x230C4	NO (0)	NO (0)	32
EEEP_RX_RATE_GIGA_CTRL	0x230C8	NO (0)	NO (0)	32
EEEP_RX_RATE_500M_CTRL	0x230CC	NO (0)	NO (0)	32
EEEP_RX_RATE_100M_CTRL	0x230D0	NO (0)	NO (0)	32
EEEP_RX_SLEEP_STEP_CTRL	0x230D4	NO (0)	NO (0)	32
EEEP_RX_WAKE_TIMER_GIGA_CTRL	0x230D8	NO (0)	NO (0)	32
EEEP_RX_TIMER_GIGA_CTRL	0x230DC	NO (0)	NO (0)	32
EEEP_RX_WAKE_TIMER_500M_CTRL	0x230E0	NO (0)	NO (0)	32
EEEP_RX_TIMER_500M_CTRL	0x230E4	NO (0)	NO (0)	32
EEEP_RX_WAKE_TIMER_100M_CTRL	0x230E8	NO (0)	NO (0)	32
EEEP_RX_TIMER_100M_CTRL	0x230EC	NO (0)	NO (0)	32
P_EEEPTXMTR	0x20028	YES (5)	NO (0)	32
P_EEEPRXMTR	0x2002C	YES (5)	NO (0)	32
SW_PWRSAV_CTRL	0x1C4	NO (0)	NO (0)	32

### Auto Fallback

All registers located at Auto Fallback feature.

Register	Offset	P.Array	C.Array	Bits
FB_CTRL	0x1B000	NO (0)	NO (0)	32
FB_PORT_CFG	0x1B004	YES (5)	NO (0)	32
FB_PORT_ERR_CNT	0x1B018	YES (5)	NO (0)	8
FB_PORT_MONITOR_CNT	0x1B020	YES (5)	NO (0)	28

### Address Table Lookup

All registers located at Address Table Lookup feature.

Register	Offset	P.Array	C.Array	Bits
LUT_UNMATCHED_SA_CTRL	0x1C000	YES (7)	NO (0)	2
LUT_UNKN_SA_CTRL	0x1C004	YES (7)	NO (0)	2
LUT_UNKN_UC_DA_CTRL	0x1C008	YES (7)	NO (0)	2
LUT_LEARN_OVER_CTRL	0x1C00C	YES (7)	NO (0)	2
LUT_CFG	0x17000	NO (0)	NO (0)	32
LUT_AGEOUT_CTRL	0x17004	YES (7)	NO (0)	1
LUT_LRN_LIMITNO	0x17008	YES (7)	NO (0)	12
L2_LRN_CNT	0x17018	YES (7)	NO (0)	12
L2_LRN_OVER_STS	0x1D010	YES (7)	NO (0)	1

Register	Offset	P.Array	C.Array	Bits
LUT_SYS_LRN_LIMITNO	0x17028	NO (0)	NO (0)	32
L2_SYS_LRN_OVER_STS	0x1D014	NO (0)	NO (0)	32
L2_SYS_LRN_CNT	0x1702C	NO (0)	NO (0)	32
UNKN_L2_MC	0x1C010	YES (7)	NO (0)	2
UNKN_IP4_MC	0x1C014	YES (7)	NO (0)	2
UNKN_IP6_MC	0x1C018	YES (7)	NO (0)	2
UNKN_MC_PRI	0x1C01C	NO (0)	NO (0)	32
LUT_BC_FLOOD	0x1C020	YES (7)	NO (0)	1
LUT_UNKN_MC_FLOOD	0x1C024	YES (7)	NO (0)	1
LUT_UNKN_UC_FLOOD	0x1C028	YES (7)	NO (0)	1
L2_EFID	0x17030	YES (7)	NO (0)	3
LUT_SYS_LRN_OVER_CTRL	0x17034	NO (0)	NO (0)	32

## Address Learning & Flush

All registers located at Address Learning & Flush feature.

Register	Offset	P.Array	C.Array	Bits
L2_TBL_FLUSH_CTRL	0x17038	NO (0)	NO (0)	32
L2_TBL_FLUSH_EN	0x1703C	YES (7)	NO (0)	1

## L2 & IP Multicast

All registers located at L2 & IP Multicast feature.

Register	Offset	P.Array	C.Array	Bits
L2_IPMC_VLAN_LEAKY	0x1C02C	YES (7)	NO (0)	1
L2_IPMC_ISO_LEAKY	0x1C030	YES (7)	NO (0)	1

## (IEEE802.1Q) VLAN

All registers located at (IEEE802.1Q) VLAN feature.

Register	Offset	P.Array	C.Array	Bits
VLAN_PORT_ACCEPT_FRAME_TYPE	0x13000	YES (7)	NO (0)	2
VLAN_INGRESS	0x13004	YES (7)	NO (0)	1
VLAN_EGRESS_TAG	0x20030	YES (7)	NO (0)	32
VLAN_MBR_CFG	0x13008	NO (0)	YES (32)	64
VLAN_CTRL	0x13108	NO (0)	NO (0)	32
VLAN_PB_FID	0x1310C	YES (7)	NO (0)	4
VLAN_PB_FIDEN	0x13110	YES (7)	NO (0)	1
VLAN_PB_PRI	0x1C034	YES (7)	NO (0)	3

Register	Offset	P.Array	C.Array	Bits
VLAN_PB_VIDX	0x13114	YES (7)	NO (0)	5
VLAN_EGRESS_KEEP	0x1C038	YES (7)	NO (0)	7
VLAN_EXT_VIDX	0x1311C	NO (0)	YES (5)	5

### (IEEE802.1ad) Provider Bridges/Q-in-Q

All registers located at (IEEE802.1ad) Provider Bridges/Q-in-Q feature.

Register	Offset	P.Array	C.Array	Bits
SVLAN_UPLINK_PMSK	0x230F0	YES (7)	NO (0)	1
SVLAN_LOOK_UP_TYPE	0x230F4	NO (0)	NO (0)	32
SVLAN_MC2S	0x18000	NO (0)	YES (8)	96
SVLAN_C2S	0x14000	NO (0)	YES (128)	32
SVLAN_SP2C	0x2A000	NO (0)	YES (128)	32
SVLAN_EP_DMAL_CTRL	0x14200	YES (7)	NO (0)	1
SVLAN_P_SVIDX	0x14204	YES (7)	NO (0)	6
SVLAN_CTRL	0x1420C	NO (0)	NO (0)	32
SVLAN_CFG	0x230F8	NO (0)	NO (0)	32
SVLAN_MBRCFG	0x14210	NO (0)	YES (64)	64

### (IEEE802.1v) Protocol-based VLAN

All registers located at (IEEE802.1v) Protocol-based VLAN feature.

Register	Offset	P.Array	C.Array	Bits
VLAN_PPVB_VLAN_VAL	0x13120	NO (0)	YES (4)	32
VLAN_PORT_PPVB_VLAN	0x13130	YES (7)	YES (4)	32

### Link Aggregation

All registers located at Link Aggregation feature.

Register	Offset	P.Array	C.Array	Bits
PORT_TRUNK_GROUP_EN	0x1C040	YES (4)	NO (0)	32
PORT_TRUNK_CTRL	0x1C050	NO (0)	NO (0)	32
PORT_TRUNK_HASH_MAPPING	0x1C054	NO (0)	YES (16)	2

### Spanning Tree

All registers located at Spanning Tree feature.

Register	Offset	P.Array	C.Array	Bits
MSTI_CTRL	0x17040	YES (7)	YES (16)	2

## Port Isolation

All registers located at Port Isolation feature.

Register	Offset	P.Array	C.Array	Bits
PISO_P_MODE0_CTRL	0x27000	YES (7)	NO (0)	13
PISO_P_MODE1_CTRL	0x27010	YES (7)	NO (0)	13
PISO_EXT_MODE0_CTRL	0x27020	NO (0)	YES (5)	13
PISO_EXT_MODE1_CTRL	0x2702C	NO (0)	YES (5)	13
PISO_CTRL	0x27038	NO (0)	NO (0)	32

## RMA

All registers located at RMA feature.

Register	Offset	P.Array	C.Array	Bits
RMA_CTRL00	0x1C058	NO (0)	NO (0)	32
RMA_CTRL01	0x1C05C	NO (0)	NO (0)	32
RMA_CTRL02	0x1C060	NO (0)	NO (0)	32
RMA_CTRL03	0x1C064	NO (0)	NO (0)	32
RMA_CTRL04	0x1C068	NO (0)	NO (0)	32
RMA_CTRL08	0x1C06C	NO (0)	NO (0)	32
RMA_CTRL0D	0x1C070	NO (0)	NO (0)	32
RMA_CTRL0E	0x1C074	NO (0)	NO (0)	32
RMA_CTRL10	0x1C078	NO (0)	NO (0)	32
RMA_CTRL11	0x1C07C	NO (0)	NO (0)	32
RMA_CTRL12	0x1C080	NO (0)	NO (0)	32
RMA_CTRL13	0x1C084	NO (0)	NO (0)	32
RMA_CTRL18	0x1C088	NO (0)	NO (0)	32
RMA_CTRL1A	0x1C08C	NO (0)	NO (0)	32
RMA_CTRL20	0x1C090	NO (0)	NO (0)	32
RMA_CTRL21	0x1C094	NO (0)	NO (0)	32
RMA_CTRL22	0x1C098	NO (0)	NO (0)	32
RMA_CTRL_CDP	0x1C09C	NO (0)	NO (0)	32
RMA_CTRL_SSTP	0x1C0A0	NO (0)	NO (0)	32
RMA_CFG	0x1C0A4	NO (0)	NO (0)	32
EEELDP_CTRL_0	0x1C0A8	NO (0)	NO (0)	32
EEELDP_CTRL_1	0x1C0AC	NO (0)	NO (0)	32

## L2 Misc.

All registers located at L2 Misc. feature.

Register	Offset	P.Array	C.Array	Bits
L2_SRC_PORT_PERMIT	0x1C0B0	YES (7)	NO (0)	1
L2_SRC_EXT_PERMIT	0x1C0B4	NO (0)	YES (5)	1

## NIC & DMA

All registers located at NIC & DMA feature.

Register	Offset	P.Array	C.Array	Bits
NIC_ID_CRTL0	0x710000	NO (0)	NO (0)	32
NIC_ID_CRTL1	0x710004	NO (0)	NO (0)	32
NIC_MC_CRTL0	0x710008	NO (0)	NO (0)	32
NIC_MC_CRTL1	0x71000C	NO (0)	NO (0)	32
NIC_MIB0	0x710010	NO (0)	NO (0)	32
NIC_MIB1	0x710014	NO (0)	NO (0)	32
NIC_MIB2	0x710018	NO (0)	NO (0)	32
NIC_MIB3	0x71001C	NO (0)	NO (0)	32
NIC_MIB4	0x710020	NO (0)	NO (0)	32
NIC_MIB5	0x710024	NO (0)	NO (0)	32
NIC_MIB6	0x710028	NO (0)	NO (0)	32
NIC_STS	0x710034	NO (0)	NO (0)	32
NIC_COM	0x710038	NO (0)	NO (0)	32
NIC_INTR	0x71003C	NO (0)	NO (0)	32
NIC_IMR0_CFG	0x710040	NO (0)	NO (0)	32
NIC_IMR1_CFG	0x710044	NO (0)	NO (0)	32
NIC_ISR1_CFG	0x710048	NO (0)	NO (0)	32
NIC_INT_ROUTE	0x71004C	NO (0)	NO (0)	32
NIC_TC	0x710050	NO (0)	NO (0)	32
NIC_RC	0x710054	NO (0)	NO (0)	32
NIC_CPUTAG	0x710058	NO (0)	NO (0)	32
NIC_CONFIG	0x71005C	NO (0)	NO (0)	32
NIC_CPUTAG1	0x710060	NO (0)	NO (0)	32
NIC_MS	0x710068	NO (0)	NO (0)	32
NIC_MIIA	0x71006C	NO (0)	NO (0)	32
NIC_SWINT	0x710070	NO (0)	NO (0)	32
NIC_VLAN	0x710074	NO (0)	NO (0)	32
NIC_LED_CR	0x710080	NO (0)	NO (0)	32
NIC_TXFPD1	0x720000	NO (0)	NO (0)	32
NIC_TXCDO1	0x720004	NO (0)	NO (0)	32
NIC_TXFDP2	0x720010	NO (0)	NO (0)	32
NIC_TXCDO2	0x720014	NO (0)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
NIC_TXFDP3	0x720020	NO (0)	NO (0)	32
NIC_TXCDO3	0x720024	NO (0)	NO (0)	32
NIC_TXFDP4	0x720030	NO (0)	NO (0)	32
NIC_TXCDO4	0x720034	NO (0)	NO (0)	32
NIC_TXFDP5	0x720040	NO (0)	NO (0)	32
NIC_TXCDO5	0x720044	NO (0)	NO (0)	32
NIC_RRING_ROUTING1	0x720070	NO (0)	NO (0)	32
NIC_RRING_ROUTING2	0x720074	NO (0)	NO (0)	32
NIC_RRING_ROUTING3	0x720078	NO (0)	NO (0)	32
NIC_RRING_ROUTING4	0x72007C	NO (0)	NO (0)	32
NIC_RRING_ROUTING5	0x720080	NO (0)	NO (0)	32
NIC_RRING_ROUTING6	0x720084	NO (0)	NO (0)	32
DUMMY	0x720088	NO (0)	YES (2)	32
NIC_RXFDP2	0x720090	NO (0)	NO (0)	32
NIC_RXCDORINGRS2	0x720094	NO (0)	NO (0)	32
NIC_RX_CPU_DESN2	0x720098	NO (0)	NO (0)	32
NIC_RX_DES_THRES2	0x72009C	NO (0)	NO (0)	32
NIC_RXFDP3	0x7200A0	NO (0)	NO (0)	32
NIC_RXCDORINGRS3	0x7200A4	NO (0)	NO (0)	32
NIC_RX_CPU_DESN3	0x7200A8	NO (0)	NO (0)	32
NIC_RX_DES_THRES3	0x7200AC	NO (0)	NO (0)	32
NIC_RXFDP4	0x7200B0	NO (0)	NO (0)	32
NIC_RXCDORINGRS4	0x7200B4	NO (0)	NO (0)	32
NIC_RX_CPU_DESN4	0x7200B8	NO (0)	NO (0)	32
NIC_RX_DES_THRES4	0x7200BC	NO (0)	NO (0)	32
NIC_RXFDP5	0x7200C0	NO (0)	NO (0)	32
NIC_RXCDORINGRS5	0x7200C4	NO (0)	NO (0)	32
NIC_RX_CPU_DESN5	0x7200C8	NO (0)	NO (0)	32
NIC_RX_DES_THRES5	0x7200CC	NO (0)	NO (0)	32
NIC_RXFDP6	0x7200D0	NO (0)	NO (0)	32
NIC_RXCDORINGRS6	0x7200D4	NO (0)	NO (0)	32
NIC_RX_CPU_DESN6	0x7200D8	NO (0)	NO (0)	32
NIC_RX_DES_THRES6	0x7200DC	NO (0)	NO (0)	32
DUMMY	0x7200E0	NO (0)	YES (4)	32
NIC_RXFDP1	0x7200F0	NO (0)	NO (0)	32
NIC_RXCDORINGRS1	0x7200F4	NO (0)	NO (0)	32
DUMMY	0x7200F8	NO (0)	NO (0)	32
NIC_SMSA	0x7200FC	NO (0)	NO (0)	32
NIC_PROBE_SELECT	0x720100	NO (0)	NO (0)	32
NIC_DIAGNOSE1	0x720104	NO (0)	NO (0)	32
DUMMY	0x720108	NO (0)	YES (9)	32
NIC_RX_PSE1_TXC_OUT_SEL1	0x72012C	NO (0)	NO (0)	32
NIC_ETNRXCPU1	0x720130	NO (0)	NO (0)	32
NIC_ETN_IO_CMD	0x720134	NO (0)	NO (0)	32
NIC_ETN_IO_CMD1	0x720138	NO (0)	NO (0)	32
NIC_WOL	0x72013C	NO (0)	NO (0)	32

## Storm Control (B/M/UM/DLF)

All registers located at Storm Control (B/M/UM/DLF) feature.

Register	Offset	P.Array	C.Array	Bits
STORM_CTRL_UM_CTRL	0x1705C	YES (7)	NO (0)	1
STORM_CTRL_UC_CTRL	0x17060	YES (7)	NO (0)	1
STORM_CTRL_MC_CTRL	0x17064	YES (7)	NO (0)	1
STORM_CTRL_BC_CTRL	0x17068	YES (7)	NO (0)	1
STORM_CTRL_UM_METER_IDX	0x1706C	YES (7)	NO (0)	5
STORM_CTRL_UC_METER_IDX	0x17074	YES (7)	NO (0)	5
STORM_CTRL_MC_METER_IDX	0x1707C	YES (7)	NO (0)	5
STORM_CTRL_BC_METER_IDX	0x17084	YES (7)	NO (0)	5
STORM_CTRL_ALT_TYPE_SEL	0x1708C	NO (0)	NO (0)	32

## Bandwidth Control (Ingress/Egress)

All registers located at Bandwidth Control (Ingress/Egress) feature.

Register	Offset	P.Array	C.Array	Bits
IGR_BWCTRL_P_CTRL	0x20034	YES (7)	NO (0)	32
IGR_BWCTRL_GLB_CTRL	0x1C0B8	NO (0)	NO (0)	32

## Meter Marker

All registers located at Meter Marker feature.

Register	Offset	P.Array	C.Array	Bits
METER_TB_CTRL	0x25000	NO (0)	NO (0)	32
METER_GLB_CTRL	0x25004	NO (0)	YES (32)	64
METER_LB_EXCEED_STS	0x25104	NO (0)	YES (32)	1
PON_TB_CTRL	0x25108	NO (0)	NO (0)	32
METER_PKT_RATE	0x2510C	NO (0)	NO (0)	32

## 802.1X

All registers located at 802.1X feature.

Register	Offset	P.Array	C.Array	Bits
DOT1X_CFG_0	0x1C0BC	NO (0)	NO (0)	32
DOT1X_CFG_1	0x17090	NO (0)	NO (0)	32
DOT1X_P_CTRL	0x17094	YES (7)	NO (0)	32

## Denial-of-service attack prevention

All registers located at Denial-of-service attack prevention feature.

Register	Offset	P.Array	C.Array	Bits
DOS_EN	0x26000	YES (7)	NO (0)	1
DOS_CFG	0x26004	NO (0)	NO (0)	32
DOS_SYN Flood_TH	0x26008	NO (0)	NO (0)	32
DOS_FIN Flood_TH	0x2600C	NO (0)	NO (0)	32
DOS_ICMP Flood_TH	0x26010	NO (0)	NO (0)	32

## Mirroring

All registers located at Mirroring feature.

Register	Offset	P.Array	C.Array	Bits
MIR_CTRL	0x230FC	NO (0)	NO (0)	32

## sFlow

All registers located at sFlow feature.

Register	Offset	P.Array	C.Array	Bits
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## Statistic Counters

All registers located at Statistic Counters feature.

Register	Offset	P.Array	C.Array	Bits
STAT_PRIVATE_REASON	0x1C0C0	YES (7)	NO (0)	10
STAT_ACL_REASON	0x1C0CC	NO (0)	YES (6)	8
STAT_CF_REASON	0x1C0D4	NO (0)	YES (2)	10
STAT_PORT_TX_MIB	0x32000	YES (7)	NO (0)	1024
STAT_PORT_RX_MIB	0x32400	YES (7)	NO (0)	1024
STAT_PORT_OAM_MIB	0x32800	YES (7)	NO (0)	64
STAT_BRIDGE_DOT1DTPLEARNEDENT RY-DISCARDS	0x32840	NO (0)	NO (0)	32
STAT_ACL_CNT	0x32880	NO (0)	YES (32)	32
STAT_CTRL	0x34000	NO (0)	NO (0)	32
STAT_ACL_CNT_MODE	0x34004	NO (0)	YES (16)	1
STAT_ACL_CNT_TYPE	0x34008	NO (0)	YES (16)	1
STAT_ACL_CNT_RST	0x3400C	NO (0)	YES (32)	1
STAT_PORT_RST	0x34010	YES (7)	NO (0)	1



Register	Offset	P.Array	C.Array	Bits
STAT_RST	0x34014	NO (0)	NO (0)	32
OMCI_DROP_PKT_CNT	0x32900	NO (0)	NO (0)	32
OMCI_TX_PKT_CNT	0x32904	NO (0)	NO (0)	32
OMCI_RX_PKT_CNT	0x32908	NO (0)	NO (0)	32
OMCI_TX_BYTE_CNT	0x3290C	NO (0)	NO (0)	32
OMCI_RX_BYTE_CNT	0x32910	NO (0)	NO (0)	32
OMCI_CRC_ERROR_PKT_CNT	0x32914	NO (0)	NO (0)	32
EPON_STAT_RST	0x34018	NO (0)	NO (0)	32
DOT3_Q_TX_FRAMES	0x32918	NO (0)	YES (128)	32
DOT3_MPCP_RX_DISC	0x32B18	NO (0)	NO (0)	32
DOT3_EPON_FEC_CORRECTED_BLOCK S	0x32B1C	NO (0)	NO (0)	32
DOT3_EPON_FEC_UNCORRECTED_BLO CKS	0x32B20	NO (0)	NO (0)	32
DOT3_EPON_FEC_CODING_VIO	0x32B24	NO (0)	NO (0)	32
DOT3_NOT_BROADCAST_BIT_NOT_ON U_LLID	0x32B28	NO (0)	NO (0)	32
DOT3_BROADCAST_BIT_PLUS_ONU_L LID	0x32B2C	NO (0)	NO (0)	32
DOT3_BROADCAST_NOT_ONUID	0x32B30	NO (0)	NO (0)	32
DOT3_CRC8_ERRORS	0x32B34	NO (0)	NO (0)	32
DOT3_LLID_RX_BROADCAST_DROP_F RAMES	0x32B38	NO (0)	NO (0)	32
DOT3_MPCP_TX_REPORT	0x32B3C	NO (0)	YES (8)	32
DOT3_MPCP_EX_GATE	0x32B5C	NO (0)	YES (8)	32
DOT3_ONUID_NOT_BROADCAST	0x32B7C	NO (0)	YES (8)	32
STAT_DOT3_LLIDRXFRAMESDROP	0x32B9C	NO (0)	YES (8)	32
DOT3_MPCP_TX_REG_REQ	0x32BBC	NO (0)	NO (0)	32

## Flowcontrol & Backpressure Threshold

All registers located at Flowcontrol & Backpressure Threshold feature.

Register	Offset	P.Array	C.Array	Bits
FC_CTRL	0x23100	NO (0)	NO (0)	32
FC_DROP_ALL_TH	0x23104	NO (0)	NO (0)	32
FC_PAUSE_ALL_TH	0x23108	NO (0)	NO (0)	32
FC_GLB_FCOFF_HI_TH	0x2310C	NO (0)	NO (0)	32
FC_GLB_FCOFF_LO_TH	0x23110	NO (0)	NO (0)	32
FC_GLB_HI_TH	0x23114	NO (0)	NO (0)	32
FC_GLB_LO_TH	0x23118	NO (0)	NO (0)	32
FC_P_HI_TH	0x2311C	NO (0)	NO (0)	32
FC_P_LO_TH	0x23120	NO (0)	NO (0)	32
FC_P_FCOFF_HI_TH	0x23124	NO (0)	NO (0)	32
FC_P_FCOFF_LO_TH	0x23128	NO (0)	NO (0)	32
FC_JUMBO_GLB_HI_TH	0x2312C	NO (0)	NO (0)	32
FC_JUMBO_GLB_LO_TH	0x23130	NO (0)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
FC_JUMBO_P_HI_TH	0x23134	NO (0)	NO (0)	32
FC_JUMBO_P_LO_TH	0x23138	NO (0)	NO (0)	32
FC_Q_EGR_DROP_TH	0x2D000	NO (0)	YES (8)	13
FC_P_EGR_DROP_TH	0x2D010	YES (7)	NO (0)	13
FC_Q_EGR_GAP_TH	0x2D020	NO (0)	NO (0)	32
FC_P_EGR_GAP_TH	0x2D024	NO (0)	NO (0)	32
FC_P_Q_EGR_DROP_EN	0x1C0D8	YES (7)	YES (8)	1
FC_DBG_CTRL	0x2D028	NO (0)	NO (0)	32
CLR_MAX_USED_PAGE_CNT	0x2313C	NO (0)	NO (0)	32
FC_TOTAL_PAGE_CNT	0x2D02C	NO (0)	NO (0)	32
FC_PE_USED_PAGE_CNT	0x2D030	YES (7)	NO (0)	32
FC_Q_USED_PAGE_CNT	0x2D04C	YES (6)	YES (8)	32
FC_TL_USED_PAGE_CNT	0x23140	NO (0)	NO (0)	32
FC_PUB_USED_PAGE_CNT	0x23144	NO (0)	NO (0)	32
FC_PUB_FCOFF_USED_PAGE_CNT	0x23148	NO (0)	NO (0)	32
FC_PUB_JUMBO_USED_PAGE_CNT	0x2314C	NO (0)	NO (0)	32
FC_P_USED_PAGE_CNT	0x23150	YES (7)	NO (0)	32
FC_P_DBG_PKT_PAGE_CNT	0x20038	YES (7)	NO (0)	32
FC_PON_GLB_HI_TH	0x2316C	NO (0)	NO (0)	32
FC_PON_GLB_LO_TH	0x23170	NO (0)	NO (0)	32
FC_PON_P_HI_TH	0x23174	NO (0)	NO (0)	32
FC_PON_P_LO_TH	0x23178	NO (0)	NO (0)	32
FC_PON_Q_EGR_DROP_IDX	0x2317C	NO (0)	YES (128)	3
FC_PON_Q_EGR_DROP_TH	0x231B0	NO (0)	YES (8)	13
FC_PON_Q_EGR_GAP_TH	0x231C0	NO (0)	NO (0)	32
FC_PON_Q_USED_PAGE_CTRL	0x231C4	NO (0)	NO (0)	32
FC_PON_Q_USED_PAGE_CNT	0x231C8	NO (0)	NO (0)	32
TH_TX_PREFET	0x2D10C	NO (0)	NO (0)	32
LOW_QUEUE_TH	0x2D110	NO (0)	NO (0)	32
HIGH_QUEUE_MSK	0x2D114	YES (7)	NO (0)	8

## Congestion Avoidance

All registers located at Congestion Avoidance feature.

Register	Offset	P.Array	C.Array	Bits
SC_P_CTRL_0	0x2003C	YES (7)	NO (0)	32
SC_P_CTRL_1	0x1D018	NO (0)	NO (0)	32

## Packet Aging

All registers located at Packet Aging feature.

Register	Offset	P.Array	C.Array	Bits
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## (IEEE802.1p) Priority

All registers located at (IEEE802.1p) Priority feature.

Register	Offset	P.Array	C.Array	Bits
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## Queue Management

All registers located at Queue Management feature.

Register	Offset	P.Array	C.Array	Bits
QOS_INTPRI_TO_QID	0x1C0F4	YES (4)	YES (8)	3
QOS_PORT_QMAP_CTRL	0x1C104	YES (7)	NO (0)	2
QOS_PRI_REMAP_IN_CPU	0x1C108	NO (0)	YES (8)	3

## Ingress Priority Decision

All registers located at Ingress Priority Decision feature.

Register	Offset	P.Array	C.Array	Bits
QOS_1Q_PRI_REMAP	0x1C10C	NO (0)	YES (8)	3
QOS_DSCP_REMAP	0x1C110	NO (0)	YES (64)	3
QOS_PB_PRI	0x1C12C	YES (7)	NO (0)	3
PRI_SEL_TBL_CTRL	0x1C130	NO (0)	NO (0)	32
PRI_SEL_TBL_CTRL2	0x1C134	NO (0)	NO (0)	32

## Remarking

All registers located at Remarking feature.

Register	Offset	P.Array	C.Array	Bits
RMK_DOT1Q_RMK_EN_CTRL	0x20040	YES (7)	NO (0)	32
RMK_1Q_CTRL	0x231CC	NO (0)	YES (8)	3
RMK_DSCP_RMK_EN_CTRL	0x231D0	YES (7)	NO (0)	32
RMK_DSCP_CTRL	0x1102C	NO (0)	YES (64)	6
RMK_DSCP_INT_PRI_CTRL	0x11060	NO (0)	YES (8)	6
RMK_P_DSCP_SEL	0x2A200	NO (0)	YES (7)	1

## Scheduling

All registers located at Scheduling feature.

Register	Offset	P.Array	C.Array	Bits
WFQ_CTRL	0x2D800	NO (0)	NO (0)	32
EGR_BWCTRL_P_CTRL	0x2D804	YES (7)	NO (0)	32
LINE_RATE_1G	0x2D820	NO (0)	NO (0)	32
LINE_RATE_500M	0x2D824	NO (0)	NO (0)	32
LINE_RATE_100M	0x2D828	NO (0)	NO (0)	32
LINE_RATE_10M	0x2D82C	NO (0)	NO (0)	32
OUTPUT_DROP_CFG	0x11068	NO (0)	NO (0)	32
OUTPUT_DROP_EN	0x1106C	YES (7)	NO (0)	1
WFQ_PORT_CFG0	0x2D830	YES (7)	NO (0)	16
WFQ_PORT_CFG1_7	0x2D840	YES (7)	YES (7)	10
WFQ_TYPE_PORT_CFG	0x2D894	YES (7)	YES (8)	1
APR_EN_PORT_CFG	0x2D8B0	YES (7)	YES (8)	1
CPU_PORT_RATE_CFG	0x2D8CC	NO (0)	NO (0)	32
APR_METER_PORT_CFG	0x2D8D0	YES (7)	YES (8)	3
P_QUEUE_EMPTY	0x2D11C	NO (0)	NO (0)	32
MOCIR_TH_H	0x2D8EC	NO (0)	NO (0)	32
MOCIR_TH_L	0x2D8F0	NO (0)	NO (0)	32
MOCIR_BPT	0x2D8F4	NO (0)	NO (0)	32
MOCIR_FRC_MD	0x2D8F8	NO (0)	NO (0)	32
MOCIR_FRC_VAL	0x2D8FC	NO (0)	NO (0)	32
DBG_HSA_EP	0x2A204	NO (0)	NO (0)	32

## PIE Template

All registers located at PIE Template feature.

Register	Offset	P.Array	C.Array	Bits
ACL_TEMPLATE_CTRL	0x15000	YES (4)	YES (8)	7

## Flow Classification (Flow Table)

All registers located at Flow Classification (Flow Table) feature.

Register	Offset	P.Array	C.Array	Bits
CF_OP_DS	0x15020	NO (0)	YES (512)	1
CF_OP_US	0x15060	NO (0)	YES (512)	1
CF_VALID	0x150A0	NO (0)	YES (512)	1
CF_CFG	0x150E0	NO (0)	NO (0)	32
RMK_DSCP_CF_PRI_CTRL	0x150E4	NO (0)	YES (8)	32

## Ingress ACL

All registers located at Ingress ACL feature.

Register	Offset	P.Array	C.Array	Bits
ACL_EN	0x15104	YES (7)	NO (0)	1
ACL_PERMIT	0x15108	YES (7)	NO (0)	1
ACL_ACTION	0x1510C	NO (0)	YES (128)	32
ACL_CFG	0x1530C	NO (0)	NO (0)	32

## Range Check (port/vlan/ip/L4port)

All registers located at Range Check (port/vlan/ip/L4port) feature.

Register	Offset	P.Array	C.Array	Bits
RNG_CHK_VID_RNG	0x15310	NO (0)	YES (8)	32
RNG_CHK_IP_RNG	0x15330	NO (0)	YES (8)	96
RNG_CHK_L4PORT_RNG	0x15390	NO (0)	YES (16)	64
RNG_CHK_PKTLEN_RNG	0x15410	NO (0)	YES (8)	32
RNG_CHK_IP_RNG_CF	0x15430	NO (0)	YES (8)	96
RNG_CHK_L4PORT_RNG_CF	0x15490	NO (0)	YES (8)	64

## OAM

All registers located at OAM feature.

Register	Offset	P.Array	C.Array	Bits
OAM_P_CTRL_0	0x170B0	YES (7)	NO (0)	2
OAM_P_CTRL_1	0x170B4	YES (7)	NO (0)	2
OAM_CTRL_0	0x1C138	NO (0)	NO (0)	32
OAM_CTRL_1	0x170B8	NO (0)	NO (0)	32

## UDLD

All registers located at UDLD feature.

Register	Offset	P.Array	C.Array	Bits
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## RLDP & RLPP

All registers located at RLDP & RLPP feature.

Register	Offset	P.Array	C.Array	Bits
RLDP_CTRL_0	0x231EC	NO (0)	NO (0)	32
RLDP_CTRL_1	0x1A000	NO (0)	NO (0)	32
RLDP_CHK_STS_CTRL	0x1A004	NO (0)	NO (0)	32
RLDP_LP_STS_CTRL	0x1A008	NO (0)	NO (0)	32
RLDP_RNDM_NUM	0x1A00C	NO (0)	NO (0)	64
RLDP_MAGIC_NUM	0x1A014	NO (0)	NO (0)	64
RLDP_PORT_TX_EN	0x1A01C	YES (6)	NO (0)	1
RLDP_PORT_LP_ENTER_STS	0x1A020	YES (6)	NO (0)	1
RLDP_PORT_LP_LEAVE_STS	0x1A024	YES (6)	NO (0)	1
RLDP_PORT_LP_STS	0x1A028	YES (6)	NO (0)	1
RLDP_PORT_CPU_LP_STS	0x1A02C	YES (6)	NO (0)	1
RLDP_PORT_LP_PNUM	0x1A030	YES (6)	NO (0)	3
RLPP_CTRL	0x1A034	NO (0)	NO (0)	32

## Code Protection

All registers located at Code Protection feature.

Register	Offset	P.Array	C.Array	Bits
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## Parser HSB

All registers located at Parser HSB feature.

Register	Offset	P.Array	C.Array	Bits
HSB_CTRL	0x28000	NO (0)	NO (0)	32
HSB_DATA	0x28040	NO (0)	YES (20)	32
HSB_DATA_TABLE	0x0	NO (0)	NO (0)	0

## HSM

All registers located at HSM feature.

Register	Offset	P.Array	C.Array	Bits
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## Modifier HSA

All registers located at Modifier HSA feature.

Register	Offset	P.Array	C.Array	Bits
HSA_DATA	0x280C0	NO (0)	YES (13)	32

Register	Offset	P.Array	C.Array	Bits
HSA_DATA_NAT	0x0	NO (0)	NO (0)	0
HSA_DATA_TABLE	0x0	NO (0)	NO (0)	0

## Debugging (ALE, Loopback, Drop Mechanism, FC and QM)

All registers located at Debugging (ALE, Loopback, Drop Mechanism, FC and QM) feature.

Register	Offset	P.Array	C.Array	Bits
DBG_BLK_SEL	0x1C8	NO (0)	NO (0)	32
PORT_VM_EN	0x20044	YES (7)	NO (0)	32
PORT_VM_RX	0x20048	YES (7)	NO (0)	32
PORT_VM_TX	0x2004C	YES (7)	NO (0)	32

## Smart Packet Generator

All registers located at Smart Packet Generator feature.

Register	Offset	P.Array	C.Array	Bits
SPG_GLB_CTRL	0x231F0	NO (0)	NO (0)	32
SPG_PORT_TX_GRP_CTRL	0x20050	YES (7)	NO (0)	32
SPG_PORT_STS	0x20054	YES (7)	NO (0)	32
SPG_P_TX_GRP_CTRL	0x20058	YES (7)	NO (0)	32
SPG_P_LEN_CTRL	0x2005C	YES (7)	NO (0)	32
SPG_P_TX_CNT	0x20060	YES (7)	NO (0)	32
SPG_P_SA	0x20064	YES (7)	NO (0)	64
SPG_P_DA	0x2006C	YES (7)	NO (0)	64
SPG_PAYLOAD	0x231F4	NO (0)	YES (48)	8
SPG_PORT_USER_PKT	0x20074	YES (7)	NO (0)	32

## L3 Routing

All registers located at L3 Routing feature.

Register	Offset	P.Array	C.Array	Bits
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## IGMP snooping

All registers located at IGMP snooping feature.

Register	Offset	P.Array	C.Array	Bits
IGMP_MC_GROUP	0x1C13C	NO (0)	YES (64)	64

Register	Offset	P.Array	C.Array	Bits
IGMP_GLB_CTRL	0x11070	NO (0)	NO (0)	32
IGMP_P_CTRL	0x11074	YES (7)	NO (0)	32

### L3 Misc

All registers located at L3 Misc feature.

Register	Offset	P.Array	C.Array	Bits
L34_GLB_CFG	0x11090	NO (0)	NO (0)	32
L34_IPMC_TRAN_TBL	0x2A208	NO (0)	YES (16)	32
L34_IPMC_TTL_CFG	0x2A248	NO (0)	NO (0)	32
L34_PORT_TO_WAN	0x11094	YES (7)	YES (8)	1
L34_EXTPORT_TO_WAN	0x110B0	YES (5)	YES (8)	1
L34_WAN_TO_PORT	0x110C4	YES (7)	YES (8)	1
L34_WAN_TO_EXTPORT	0x110E0	YES (5)	YES (8)	1

### Table Access

All registers located at Table Access feature.

Register	Offset	P.Array	C.Array	Bits
TBL_ACCESS_CTRL	0x12000	NO (0)	NO (0)	32
TBL_ACCESS_STS	0x12004	NO (0)	NO (0)	32
TBL_ACCESS_WR_DATA	0x12008	NO (0)	NO (0)	160
TBL_ACCESS_RD_DATA	0x1201C	NO (0)	NO (0)	160
ACL_ACTION_TABLE	0x0	NO (0)	NO (0)	0
ACL_DATA	0x0	NO (0)	NO (0)	0
ACL_DATA2	0x0	NO (0)	NO (0)	0
ACL_MASK	0x0	NO (0)	NO (0)	0
ACL_MASK2	0x0	NO (0)	NO (0)	0
CF_ACTION_DS	0x0	NO (0)	NO (0)	0
CF_ACTION_US	0x0	NO (0)	NO (0)	0
CF_MASK	0x0	NO (0)	NO (0)	0
CF_MASK_L34	0x0	NO (0)	NO (0)	0
CF_RULE	0x0	NO (0)	NO (0)	0
CF_RULE_L34	0x0	NO (0)	NO (0)	0
L2_MC_DSL	0x0	NO (0)	NO (0)	0
L2_UC	0x0	NO (0)	NO (0)	0
L3_MC_DSL	0x0	NO (0)	NO (0)	0
L3_MC_ROUTE	0x0	NO (0)	NO (0)	0
VLAN	0x0	NO (0)	NO (0)	0



## Special Trap

All registers located at Special Trap feature.

Register	Offset	P.Array	C.Array	Bits
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## Ethernet AV

All registers located at Ethernet AV feature.

Register	Offset	P.Array	C.Array	Bits
AVB_PORT_EN	0x110F4	YES (7)	NO (0)	1
AVB_PRI_REMAP	0x110F8	NO (0)	YES (8)	3

## PTP (Precision Time Protocol)

All registers located at PTP (Precision Time Protocol) feature.

Register	Offset	P.Array	C.Array	Bits
PTP_TIME_SEC	0x1B034	NO (0)	NO (0)	64
PTP_TIME_NSEC	0x1B03C	NO (0)	NO (0)	32
PTP_TIME_OFFSET_SEC	0x1B040	NO (0)	NO (0)	64
PTP_TIME_OFFSET_8NSEC	0x1B048	NO (0)	NO (0)	32
PTP_TIME_FREQ	0x1B04C	NO (0)	NO (0)	32
PTP_TIME_CTRL	0x1B050	NO (0)	NO (0)	32
PTP_TRANSPARENT_CFG	0x110FC	YES (7)	NO (0)	1
PTP_IGR_MSG_ACT	0x11100	NO (0)	YES (10)	2
PTP_EGR_MSG_ACT	0x11104	NO (0)	YES (10)	2
PTP_MEANPATH_DEALY	0x1B054	NO (0)	NO (0)	32
PTP_RX_TIME	0x11108	NO (0)	NO (0)	64
PTP_P_EN	0x11110	YES (7)	NO (0)	32

## Parser

All registers located at Parser feature.

Register	Offset	P.Array	C.Array	Bits
PARSER_FIELD_SELTOR_CTRL	0x23224	NO (0)	YES (16)	32

## PON MAC Scheduling Config

All registers located at PON MAC Scheduling Config feature.

Register	Offset	P.Array	C.Array	Bits
PON_CFG	0x2D900	NO (0)	NO (0)	32
PON_SID_TO_QID	0x1C33C	NO (0)	YES (128)	7
PON_QID_CIR_RATE	0x2D904	NO (0)	YES (128)	17
PON_QID_PIR_RATE	0x2DB04	NO (0)	YES (128)	17
PON_SCH_QMAP	0x2DD04	NO (0)	YES (32)	32
PON_WFQ_WEIGHT	0x2DD84	NO (0)	YES (128)	10
PON_WFQ_TYPE	0x2DE30	NO (0)	YES (128)	1
FC_PON_Q_EGR_DROP_EN	0x1C3BC	NO (0)	YES (128)	1
PON_TCONT_EN	0x2DE40	NO (0)	YES (32)	1
QUEUE_SEL_IND	0x2D120	NO (0)	NO (0)	32
QUEUE_SEL_IND_DATA	0x2D124	NO (0)	NO (0)	32
GPON_DPRU_RPT_PRD	0x2D128	NO (0)	NO (0)	32
PON_PIR_CIR_IFG	0x2D12C	NO (0)	NO (0)	32
PON_PORT_CTRL	0x23264	NO (0)	NO (0)	32
PONMAC_DRN_CTRL	0x23268	NO (0)	NO (0)	32
PON_OLT_BW_MTR_FULL	0x2DE44	NO (0)	NO (0)	32
PON_WFQ_IFG_CTRL	0x2DE48	NO (0)	NO (0)	32

## GPON MAC General Config

All registers located at GPON MAC General Config feature.

Register	Offset	P.Array	C.Array	Bits
GPON_INT_DLT	0x700000	NO (0)	NO (0)	32
GPON_RESET	0x70000C	NO (0)	NO (0)	32
GPON_VERSION	0x700010	NO (0)	NO (0)	32
GPON_TEST	0x700014	NO (0)	NO (0)	32
GPON_AES_BYPASS	0x700020	NO (0)	NO (0)	32
GPON_INTR_MASK	0x700040	NO (0)	NO (0)	32
GPON_INTR_STS	0x700044	NO (0)	NO (0)	32

## GTC Downstream

All registers located at GTC Downstream feature.

Register	Offset	P.Array	C.Array	Bits
GPON_GTC_DS_INTR_DLT	0x701000	NO (0)	NO (0)	32
GPON_GTC_DS_INTR_MASK	0x701004	NO (0)	NO (0)	32
GPON_GTC_DS_INTR_STS	0x701008	NO (0)	NO (0)	32
GPON_GTC_DS_ONU_ID_STATUS	0x701010	NO (0)	NO (0)	32
GPON_GTC_DS_CFG	0x701014	NO (0)	NO (0)	32
GPON_GTC_DS_PLOAM_CFG	0x70101C	NO (0)	NO (0)	32
GPON_GTC_DS_LOS_CFG_STS	0x701040	NO (0)	NO (0)	32
GPON_GTC_DS_SUPERFRAME_CNT	0x701048	NO (0)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
GPON_GTC_DS_PLOAM_IND	0x701080	NO (0)	NO (0)	32
GPON_GTC_DS_PLOAM_MSG	0x7010A0	NO (0)	YES (8)	32
GPON_GTC_DS_ALLOC_IND	0x7010C0	NO (0)	NO (0)	32
GPON_GTC_DS_ALLOC_WR	0x7010C4	NO (0)	NO (0)	32
GPON_GTC_DS_ALLOC_RD	0x7010CC	NO (0)	NO (0)	32
GPON_GTC_DS_PORT_IND	0x701100	NO (0)	NO (0)	32
GPON_GTC_DS_PORT_WR	0x701104	NO (0)	NO (0)	32
GPON_GTC_DS_PORT_RD	0x70110C	NO (0)	NO (0)	32
GPON_GTC_DS_PORT_CNTR_IND	0x701140	NO (0)	NO (0)	32
GPON_GTC_DS_PORT_CNTR_STAT	0x701144	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_BIP_ERR _BLK	0x701184	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_BIP_ERR_BIT	0x701188	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_FEC_COR RECT_BIT	0x70118C	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_FEC_COR RECT_BYTE	0x701190	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_FEC_COR RECT_CW	0x701194	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_FEC_UNC OR_CW	0x701198	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_LOM	0x70119C	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_PLOAM_A CPT	0x7011A0	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_PLOAM_FAIL	0x7011A4	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_BWM_FAIL	0x7011A8	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_BWM_INV	0x7011AC	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_ACTIVE	0x7011B0	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_BWM_ACPT	0x7011B4	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_GEM_LOS	0x7011B8	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_HEC_COR RECT	0x7011BC	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_GEM_IDLE	0x7011C0	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_GEM_FAIL	0x7011C4	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_GEM_NON _IDLE	0x7011C8	NO (0)	NO (0)	32
GPON_GTC_DS_MISC_CNTR_PLEN_CO RRECT	0x7011CC	NO (0)	NO (0)	32
GPON_GTC_DS_OMCI_PTI	0x701204	NO (0)	NO (0)	32
GPON_GTC_DS_ETH_PTI	0x701208	NO (0)	NO (0)	32
GPON_GTC_DS_TRAFFIC_CFG	0x701400	NO (0)	YES (128)	32

## BWMAP Capture

All registers located at BWMAP Capture feature.

Register	Offset	P.Array	C.Array	Bits
GPON_BWMAP_CTRL	0x70200C	NO (0)	NO (0)	32
GPON_BWMAP_STS	0x702010	NO (0)	NO (0)	32
GPON_BWMAP_DATA	0x702400	NO (0)	YES (256)	32

## AES Decrypt

All registers located at AES Decrypt feature.

Register	Offset	P.Array	C.Array	Bits
GPON_AES_INTR_DLT	0x703000	NO (0)	NO (0)	32
GPON_AES_INTR_MASK	0x703004	NO (0)	NO (0)	32
GPON_AES_INTR_STS	0x703008	NO (0)	NO (0)	32
GPON_AES_KEY_SWITCH_REQ	0x703010	NO (0)	NO (0)	32
GPON_AES_KEY_SWITCH_TIME	0x703014	NO (0)	NO (0)	32
GPON_AES_KEY_WORD_IND	0x703020	NO (0)	NO (0)	32
GPON_AES_WORD_DATA	0x703024	NO (0)	NO (0)	32

## GEM Port Downstream

All registers located at GEM Port Downstream feature.

Register	Offset	P.Array	C.Array	Bits
GPON_GEM_DS_RX_CNTR_IND	0x704040	NO (0)	NO (0)	32
GPON_GEM_DS_RX_CNTR_STAT	0x704044	NO (0)	NO (0)	32
GPON_GEM_DS_FWD_CNTR_IND	0x70404C	NO (0)	NO (0)	32
GPON_GEM_DS_FWD_CNTR_STAT	0x704050	NO (0)	NO (0)	32
GPON_GEM_DS_MISC_IND	0x704064	NO (0)	NO (0)	32
GPON_GEM_DS_MISC_CNTR_STAT	0x704068	NO (0)	NO (0)	32
GPON_GEM_DS_MC_CFG	0x704080	NO (0)	NO (0)	32
GPON_GEM_DS_MC_IND	0x704084	NO (0)	NO (0)	32
GPON_GEM_DS_MC_WR	0x704088	NO (0)	NO (0)	32
GPON_GEM_DS_MC_RD	0x704090	NO (0)	NO (0)	32
GPON_GEM_DS_FRM_TIMEOUT	0x704098	NO (0)	NO (0)	32
GPON_GEM_DS_MC_ADDR_PTN_IPV4	0x70409C	NO (0)	NO (0)	32
GPON_GEM_DS_MC_ADDR_PTN_IPV6	0x7040A0	NO (0)	NO (0)	32

## GTC Upstream

All registers located at GTC Upstream feature.

Register	Offset	P.Array	C.Array	Bits
GPON_GTC_US_INTR_DLT	0x705000	NO (0)	NO (0)	32

Register	Offset	P.Array	C.Array	Bits
GPON_GTC_US_INTR_MASK	0x705004	NO (0)	NO (0)	32
GPON_GTC_US_INTR_STS	0x705008	NO (0)	NO (0)	32
GPON_GTC_US_ONU_ID	0x705010	NO (0)	NO (0)	32
GPON_GTC_US_CFG	0x705014	NO (0)	NO (0)	32
GPON_GTC_US_WRITE_PROTECT	0x705018	NO (0)	NO (0)	32
GPON_GTC_US_TX_PATTERN_CTL	0x705020	NO (0)	NO (0)	32
GPON_GTC_US_TX_PATTERN_BG	0x705024	NO (0)	NO (0)	32
GPON_GTC_US_TX_PATTERN_FG	0x705028	NO (0)	NO (0)	32
GPON_GTC_US_MIN_DELAY	0x705040	NO (0)	NO (0)	32
GPON_GTC_US_EQD	0x705044	NO (0)	NO (0)	32
GPON_GTC_US_LASER	0x70504C	NO (0)	NO (0)	32
GPON_GTC_US_BOH_CFG	0x705054	NO (0)	NO (0)	32
GPON_GTC_US_BOH_DATA	0x705080	NO (0)	YES (12)	32
GPON_GTC_US_PLOAM_IND	0x7050C0	NO (0)	NO (0)	32
GPON_GTC_US_PLOAM_DATA	0x7050E0	NO (0)	YES (8)	32
GPON_GTC_US_PLOAM_CFG	0x705100	NO (0)	NO (0)	32
GPON_GTC_US_MISC_CNTR_IDX	0x705140	NO (0)	NO (0)	32
GPON_GTC_US_MISC_CNTR_STAT	0x705148	NO (0)	NO (0)	32
GPON_GTC_US_RDI	0x705180	NO (0)	NO (0)	32
GPON_GTC_US_DG	0x705184	NO (0)	NO (0)	32
GPON_GTC_US_OPTIC_SD_TH	0x705188	NO (0)	NO (0)	32
GPON_GTC_US_PROC_MODE	0x705200	NO (0)	NO (0)	32

## GEM Upstream

All registers located at GEM Upstream feature.

Register	Offset	P.Array	C.Array	Bits
GPON_GEM_US_INTR_DLT	0x706000	NO (0)	NO (0)	32
GPON_GEM_US_INTR_MASK	0x706004	NO (0)	NO (0)	32
GPON_GEM_US_INTR_STS	0x706008	NO (0)	NO (0)	32
GPON_GEM_US_PTI_CFG	0x706020	NO (0)	NO (0)	32
GPON_GEM_US_ETH_GEM_RX_CNTR_I DX	0x706048	NO (0)	NO (0)	32
GPON_GEM_US_ETH_GEM_RX_CNTR_S TAT	0x70604C	NO (0)	NO (0)	32
GPON_GEM_US_PTN_CTRL	0x706054	NO (0)	NO (0)	32
GPON_GEM_US_PORT_MAP	0x706400	NO (0)	YES (128)	32
GPON_GEM_US_BYTE_STAT	0x706800	NO (0)	YES (128)	64
TCONT_IDLE_BYTE_STAT	0x706C00	NO (0)	YES (32)	64

## EPON Configuration

All registers located at EPON Configuration feature.

Register	Offset	P.Array	C.Array	Bits
EPON_FEC_CONFIG	0x36000	NO (0)	NO (0)	32
EPON_ASIC_TIMING_ADJUST1	0x36004	NO (0)	NO (0)	32
EPON_ASIC_TIMING_ADJUST2	0x36008	NO (0)	NO (0)	32
EPON_RGSTR1	0x3600C	NO (0)	NO (0)	32
EPON_RGSTR2	0x36010	NO (0)	NO (0)	32
EPON_RGSTR3	0x36014	NO (0)	NO (0)	32
EPON_DEBUG1	0x36018	NO (0)	NO (0)	32
EPON_DEBUG2	0x3601C	NO (0)	NO (0)	32
EPON_TIMER_CONFIG1	0x36020	NO (0)	NO (0)	32
EPON_INTR	0x36024	NO (0)	NO (0)	32
SYNC_TIME	0x36028	NO (0)	NO (0)	32
LASER_ON_OFF_TIME	0x3602C	NO (0)	NO (0)	32
MIN_GRANT_START	0x36030	NO (0)	NO (0)	32
MAX_GRANT_START	0x36034	NO (0)	NO (0)	32
EPON_TIME_CTRL	0x36038	NO (0)	NO (0)	32
EP_MISC	0x3603C	NO (0)	NO (0)	32
LLID_TABLE	0x36040	NO (0)	YES (8)	32
EPON_MPCP_CTR	0x36060	NO (0)	NO (0)	32
EPON_GRANT_LIST0	0x36064	NO (0)	YES (32)	32
EPON_GRANT_LIST1	0x360E4	NO (0)	YES (32)	32
EPON_GRANT_LIST2	0x36164	NO (0)	YES (32)	32
EPON_TX_CTRL	0x361E4	NO (0)	NO (0)	32

## Table Access

All registers located at Table Access feature.

Register	Offset	P.Array	C.Array	Bits
NAT_TBL_ACCESS_CTRL	0x800100	NO (0)	NO (0)	32
NAT_TBL_ACCESS_CLR	0x800104	NO (0)	NO (0)	32
NAT_TBL_ACCESS_RDDATA	0x800108	NO (0)	NO (0)	160
NAT_TBL_ACCESS_WRDATA	0x80011C	NO (0)	NO (0)	160
ARP_TABLE	0x0	NO (0)	NO (0)	0
BINDING_TABLE	0x0	NO (0)	NO (0)	0
EXTERNAL_IP_TABLE	0x0	NO (0)	NO (0)	0
IPV6_ROUTING_TABLE	0x0	NO (0)	NO (0)	0
L3_ROUTING_DROP_TRAP	0x0	NO (0)	NO (0)	0
L3_ROUTING_GLOBAL_ROUTE	0x0	NO (0)	NO (0)	0
L3_ROUTING_LOCAL_ROUTE	0x0	NO (0)	NO (0)	0
NAPT_TABLE	0x0	NO (0)	NO (0)	0
NAPTR_TABLE	0x0	NO (0)	NO (0)	0
NEIGHBOR_TABLE	0x0	NO (0)	NO (0)	0
NETIF	0x0	NO (0)	NO (0)	0
NEXT_HOP_TABLE	0x0	NO (0)	NO (0)	0
PPPOE_TABLE	0x0	NO (0)	NO (0)	0

Register	Offset	P.Array	C.Array	Bits
WAN_TYPE_TABLE	0x0	NO (0)	NO (0)	0

## ALE and TM for L3L4

All registers located at ALE and TM for L3L4 feature.

Register	Offset	P.Array	C.Array	Bits
NIFP	0x800000	NO (0)	NO (0)	32
NIFEP	0x800004	NO (0)	NO (0)	32
NIFVCH	0x800008	NO (0)	NO (0)	32
NIFVCL	0x80000C	NO (0)	NO (0)	32
SWTCR0	0x800010	NO (0)	NO (0)	32
PP_AGE	0x800014	NO (0)	NO (0)	32
NB_TRF	0x800018	NO (0)	NO (0)	128
V6_BD_CTL	0x800028	NO (0)	NO (0)	32
BD_TRF	0x80002C	NO (0)	NO (0)	32
BD_CFG	0x800030	NO (0)	NO (0)	32

## NAT HSB HAS

All registers located at NAT HSB HAS feature.

Register	Offset	P.Array	C.Array	Bits
HSBA_CTRL	0x800200	NO (0)	NO (0)	32
HSB_DESC	0x800204	NO (0)	YES (10)	32
HSA_DESC	0x80022C	NO (0)	YES (4)	32
L34_HSA	0x0	NO (0)	NO (0)	0
L34_HSB	0x0	NO (0)	NO (0)	0

## L4 Traffic Table0

All registers located at L4 Traffic Table0 feature.

Register	Offset	P.Array	C.Array	Bits
L4_TRF0	0x800300	NO (0)	YES (2048)	1
L4_TRF1	0x800400	NO (0)	YES (2048)	1
ARP_TRF0	0x800500	NO (0)	YES (512)	1
ARP_TRF1	0x800600	NO (0)	YES (512)	1

## Temp Register

All registers located at Temp Register feature.

Register	Offset	P.Array	C.Array	Bits
RGF_VER_GLB_CTRL	0x1CC	NO (0)	NO (0)	32
RGF_VER_ALE_GLB	0x1112C	NO (0)	NO (0)	32
RGF_VER_ALE_ACL	0x154D0	NO (0)	NO (0)	32
RGF_VER_ALE_CVLAN	0x131A0	NO (0)	NO (0)	32
RGF_VER_ALE_DPM	0x1C3CC	NO (0)	NO (0)	32
RGF_VER_ALE_L2	0x170BC	NO (0)	NO (0)	32
RGF_VER_ALE_MLTVLAN	0x18060	NO (0)	NO (0)	32
RGF_VER_ALE_SVLAN	0x14410	NO (0)	NO (0)	32
RGF_VER_ALE_EEE_LLDP	0x19000	NO (0)	NO (0)	32
RGF_VER_ALE_RLDP	0x1A038	NO (0)	NO (0)	32
RGF_VER_ALE_EAV_AFBK	0x1B058	NO (0)	NO (0)	32
RGF_VER_INTR	0x1D01C	NO (0)	NO (0)	32
RGF_VER_LED	0x1E0C0	NO (0)	NO (0)	32
RGF_VER_PER_PORT_MAC	0x20078	YES (7)	NO (0)	32
RGF_VER_SDSREG	0x2214C	NO (0)	NO (0)	32
RGF_VER_SWCORE	0x2326C	NO (0)	NO (0)	32
RGF_VER_EPON_CTRL	0x361E8	NO (0)	NO (0)	32
RGF_VER_ALE_RMA_ATTACK	0x26014	NO (0)	NO (0)	32
RGF_VER_BIST_CTRL	0x31048	NO (0)	NO (0)	32
RGF_VER_EGR_OUTQ	0x2D130	NO (0)	NO (0)	32
RGF_VER_EGR_SCH	0x2DE4C	NO (0)	NO (0)	32
RGF_VER_ALE_HSA	0x2A24C	NO (0)	NO (0)	32
RGF_VER_ALE_METER	0x25110	NO (0)	NO (0)	32
RGF_VER_MIB_CTRL	0x3401C	NO (0)	NO (0)	32
RGF_VER_ALE_PISO	0x2703C	NO (0)	NO (0)	32
RSVD_GLB_CTRL	0x1D0	NO (0)	YES (16)	32
RSVD_ALE_GLB	0x11130	NO (0)	YES (16)	32
RSVD_ALE_ACL	0x154D4	NO (0)	YES (16)	32
RSVD_ALE_CVLAN	0x131A4	NO (0)	YES (16)	32
RSVD_ALE_DPM	0x1C3D0	NO (0)	YES (16)	32
RSVD_ALE_L2	0x170C0	NO (0)	YES (16)	32
RSVD_ALE_MLTVLAN	0x18064	NO (0)	YES (16)	32
RSVD_ALE_SVLAN	0x14414	NO (0)	YES (16)	32
RSVD_ALE_EEE_LLDP	0x19004	NO (0)	YES (16)	32
RSVD_ALE_RLDP	0x1A03C	NO (0)	YES (16)	32
RSVD_ALE_EAV_AFBK	0x1B05C	NO (0)	YES (16)	32
RSVD_INTR	0x1D020	NO (0)	YES (16)	32
RSVD_LED	0x1E0C4	NO (0)	YES (16)	32
RSVD_PER_PORT_MAC	0x2007C	YES (7)	YES (16)	32
RSVD_SDSREG	0x22150	NO (0)	YES (16)	32
RSVD_SWCORE	0x23270	NO (0)	YES (16)	32



Register	Offset	P.Array	C.Array	Bits
RSVD_EPON_CTRL	0x361EC	NO (0)	YES (16)	32
RSVD_ALE_RMA_ATTACK	0x26018	NO (0)	YES (16)	32
RSVD_BIST_CTRL	0x3104C	NO (0)	YES (16)	32
RSVD_EGR_OUTQ	0x2D134	NO (0)	YES (16)	32
RSVD_EGR_SCH	0x2DE50	NO (0)	YES (16)	32
RSVD_ALE_HSA	0x2A250	NO (0)	YES (16)	32
RSVD_ALE_METER	0x25114	NO (0)	YES (16)	32
RSVD_MIB_CTRL	0x34020	NO (0)	YES (16)	32
RSVD_ALE_PISO	0x27040	NO (0)	YES (16)	32
HSA_TX_DBG	0x2A290	NO (0)	YES (16)	32
BYTE_TOKEN_METER	0x2DE90	NO (0)	NO (0)	32
HSARAM_5_CFG	0x2A2D0	NO (0)	NO (0)	32
DBG_EP_CFG	0x2A2D4	NO (0)	NO (0)	32
TRUNK_DROP_CFG	0x2A2D8	NO (0)	NO (0)	32
PAUSE_ALL_LW_CFG	0x2A2DC	NO (0)	NO (0)	32
HYS_PUSAL_CFG	0x2A2E0	NO (0)	NO (0)	32
EPON_DECRYPT_CFG	0x3622C	NO (0)	NO (0)	32
EPON_DECRYPT_KEY0	0x36230	NO (0)	YES (8)	24
EPON_DECRYPT_KEY1	0x36250	NO (0)	YES (8)	24
EPON_MISC_CFG	0x36270	NO (0)	NO (0)	32
CHANGE_DUPLEX_CTRL	0x232B0	NO (0)	NO (0)	32
RLDP_BUZZER	0x1E104	NO (0)	NO (0)	32
PON_LED_CFG	0x1E108	NO (0)	NO (0)	32
FB_GPHY_ADDR_CTRL	0x1B09C	NO (0)	NO (0)	32
HSA_DEBUG_DATA	0x0	NO (0)	NO (0)	0



## Appendix C: Memory Map

Register memory map of the chip design. This section is a quick reference to all the tables and register in this datasheet.

**0xBB000000**

Address	Register	Len
0xBB000000	SKIP_MII_RXER.RESERVED[31:1]	31
0xBB000000	SKIP_MII_RXER.SKIP_MII_RXER[0:0]	1
0xBB000004	EXT_RGMXF.RESERVED[31:9]	23
0xBB000004	EXT_RGMXF.EXT_RGMXF_SELPLL[8:8]	1
0xBB000004	EXT_RGMXF.EXT_RGMXF_PLLDLY[7:7]	1
0xBB000004	EXT_RGMXF.EXT_RGTX_INV[6:6]	1
0xBB000004	EXT_RGMXF.EXT_RGRX_INV[5:5]	1
0xBB000004	EXT_RGMXF.EXT_RGMXF[4:0]	5
0xBB000008	EXT_TXC_DLY.RESERVED[31:6]	26
0xBB000008	EXT_TXC_DLY.EXT_GMII_TX_DELAY[5:3]	3
0xBB000008	EXT_TXC_DLY.EXT_RGMII_TX_DELAY[2:0]	3
0xBB00000C	GPHY_IND_WD.RESERVED[31:16]	16
0xBB00000C	GPHY_IND_WD.WR_DAT[15:0]	16
0xBB000010	GPHY_IND_CMD.RESERVED[31:23]	9
0xBB000010	GPHY_IND_CMD.WREN[22:22]	1
0xBB000010	GPHY_IND_CMD.CMD_EN[21:21]	1
0xBB000010	GPHY_IND_CMD.ADR[20:0]	21
0xBB000014	GPHY_IND_RD.RESERVED[31:17]	15
0xBB000014	GPHY_IND_RD.BUSY[16:16]	1
0xBB000014	GPHY_IND_RD.RD_DAT[15:0]	16
0xBB000018	EFUSE_CFG.RESERVED[31:2]	30
0xBB000018	EFUSE_CFG.EFUSE_TMRF[1:0]	2
0xBB00001C	EFUSE_IND_WD.RESERVED[31:16]	16
0xBB00001C	EFUSE_IND_WD.WR_DAT[15:0]	16
0xBB000020	EFUSE_IND_CMD.RESERVED[31:18]	14
0xBB000020	EFUSE_IND_CMD.WREN[17:17]	1
0xBB000020	EFUSE_IND_CMD.CMD_EN[16:16]	1
0xBB000020	EFUSE_IND_CMD.ADR[15:0]	16
0xBB000024	EFUSE_IND_RD.RESERVED[31:17]	15
0xBB000024	EFUSE_IND_RD.BUSY[16:16]	1

Address	Register	Len
0xBB000024	EFUSE_IND_RD.RD_DAT[15:0]	16
0xBB000028	I2C_IND_WD [0].RESERVED[31:16]	16
0xBB000028	I2C_IND_WD [0].WR_DAT[15:0]	16
0xBB00002C	I2C_IND_WD [1].RESERVED[31:16]	16
0xBB00002C	I2C_IND_WD [1].WR_DAT[15:0]	16
0xBB000030	I2C_IND_CMD [0].RESERVED[31:18]	14
0xBB000030	I2C_IND_CMD [0].WREN[17:17]	1
0xBB000030	I2C_IND_CMD [0].CMD_EN[16:16]	1
0xBB000030	I2C_IND_CMD [0].ADR[15:0]	16
0xBB000034	I2C_IND_CMD [1].RESERVED[31:18]	14
0xBB000034	I2C_IND_CMD [1].WREN[17:17]	1
0xBB000034	I2C_IND_CMD [1].CMD_EN[16:16]	1
0xBB000034	I2C_IND_CMD [1].ADR[15:0]	16
0xBB000038	I2C_IND_RD [0].RESERVED[31:17]	15
0xBB000038	I2C_IND_RD [0].BUSY[16:16]	1
0xBB000038	I2C_IND_RD [0].RD_DAT[15:0]	16
0xBB00003C	I2C_IND_RD [1].RESERVED[31:17]	15
0xBB00003C	I2C_IND_RD [1].BUSY[16:16]	1
0xBB00003C	I2C_IND_RD [1].RD_DAT[15:0]	16
0xBB000040	CFG_PCSXF.RESERVED[31:10]	22
0xBB000040	CFG_PCSXF.CFG_PCSXF[9:6]	4
0xBB000040	CFG_PCSXF.RST_RXFIFO[5:1]	5
0xBB000040	CFG_PCSXF.COL_10M[0:0]	1
0xBB000044	CFG_PHY_CTRL.RESERVED[31:11]	21
0xBB000044	CFG_PHY_CTRL.MSK_MDI[10:6]	5
0xBB000044	CFG_PHY_CTRL.BASE_PHYAD[5:1]	5
0xBB000044	CFG_PHY_CTRL.BYPS_PDPHY[0:0]	1
0xBB000048	CFG_PHY_POLL_CMD.RESERVED[31:16]	16
0xBB000048	CFG_PHY_POLL_CMD.HOTCMD_PRD_EN[15:15]	1
0xBB000048	CFG_PHY_POLL_CMD.HOTCMD_EN[14:12]	3
0xBB000048	CFG_PHY_POLL_CMD.CMD_PRD[11:8]	4
0xBB000048	CFG_PHY_POLL_CMD.CMD_RD_EN[7:4]	4
0xBB000048	CFG_PHY_POLL_CMD.CMD_WR_EN[3:0]	4
0xBB00004C	CFG_PHY_POLL_ADR_0.CMD0_ADR[31:16]	16
0xBB00004C	CFG_PHY_POLL_ADR_0.CMD1_ADR[15:0]	16
0xBB000050	CFG_PHY_POLL_ADR_1.CMD2_ADR[31:16]	16
0xBB000050	CFG_PHY_POLL_ADR_1.CMD3_ADR[15:0]	16
0xBB000054	CFG_PHY_POLL_INV_0.CMD0_INV[31:16]	16
0xBB000054	CFG_PHY_POLL_INV_0.CMD1_INV[15:0]	16
0xBB000058	CFG_PHY_POLL_INV_1.CMD2_INV[31:16]	16
0xBB000058	CFG_PHY_POLL_INV_1.CMD3_INV[15:0]	16
0xBB00005C	CFG_PHY_POLL_WD_0.CMD0_WDAT[31:16]	16
0xBB00005C	CFG_PHY_POLL_WD_0.CMD1_WDAT[15:0]	16
0xBB000060	CFG_PHY_POLL_WD_1.CMD2_WDAT[31:16]	16
0xBB000060	CFG_PHY_POLL_WD_1.CMD3_WDAT[15:0]	16
0xBB000064	CHIP_DEBUG_OUT.DBGO[31:0]	32

Address	Register	Len
0xBB000068	CHIP_RST.DUMMY[31:0]	32
0xBB00006C	SOFTWARE_RST.RESERVED[31:7]	25
0xBB00006C	SOFTWARE_RST.PONMAC_RST[6:6]	1
0xBB00006C	SOFTWARE_RST.SW_RST[5:5]	1
0xBB00006C	SOFTWARE_RST.CMD_SWSYS_RST_PS[4:4]	1
0xBB00006C	SOFTWARE_RST.CMD_CFG_RST_PS[3:3]	1
0xBB00006C	SOFTWARE_RST.CMD_CHIP_RST_PS[2:2]	1
0xBB00006C	SOFTWARE_RST.CMD_GPHY_RST_PS[1:1]	1
0xBB00006C	SOFTWARE_RST.CMD_SDS_RST_PS[0:0]	1
0xBB000070	BIST_CFG.RESERVED[31:9]	23
0xBB000070	BIST_CFG.BIST_DONE_ALL[8:8]	1
0xBB000070	BIST_CFG.BIST_PASS[7:5]	3
0xBB000070	BIST_CFG.DRF_BIST_DONE_ALL[4:4]	1
0xBB000070	BIST_CFG.DRF_START_PAUSE_ALL[3:3]	1
0xBB000070	BIST_CFG.BISR_COND_EN[2:0]	3
0xBB000074	PON_INTEGRATION.RESERVED[31:2]	30
0xBB000074	PON_INTEGRATION.DIS_EPON_BIST[1:1]	1
0xBB000074	PON_INTEGRATION.DIS_GPON_BIST[0:0]	1
0xBB000080	WRAP_GPHY_MISC.RESERVED[31:1]	31
0xBB000080	WRAP_GPHY_MISC.PATCH_PHY_DONE[0:0]	1
0xBB000084	MISCELLANEOUS_CONFIGURE0.RESERVED[31:10]	22
0xBB000084	MISCELLANEOUS_CONFIGURE0.ADCCKI_FROM_PAD[9:9]	1
0xBB000084	MISCELLANEOUS_CONFIGURE0.ADCCKI_EN[8:8]	1
0xBB000084	MISCELLANEOUS_CONFIGURE0.RESERVED[7:4]	4
0xBB000084	MISCELLANEOUS_CONFIGURE0.OLT_ENABLE[3:3]	1
0xBB000084	MISCELLANEOUS_CONFIGURE0.DIS_PWRON_TABLE_INIT[2:2]	1
0xBB000084	MISCELLANEOUS_CONFIGURE0.DIS_PWRON_BIST[1:1]	1
0xBB000084	MISCELLANEOUS_CONFIGURE0.EFUSE_EN[0:0]	1
0xBB000088	FORCE_P_ABLTY [0].RESERVED[31:12]	20
0xBB000088	FORCE_P_ABLTY [0].LPI_1000_ABLTY[11:11]	1
0xBB000088	FORCE_P_ABLTY [0].LPI_100_ABLTY[10:10]	1
0xBB000088	FORCE_P_ABLTY [0].MST_FAULT_ABLTY[9:9]	1
0xBB000088	FORCE_P_ABLTY [0].MST_MOD_ABLTY[8:8]	1
0xBB000088	FORCE_P_ABLTY [0].NWAY_ABLTY[7:7]	1
0xBB000088	FORCE_P_ABLTY [0].TXPAUSE_ABLTY[6:6]	1
0xBB000088	FORCE_P_ABLTY [0].RXPAUSE_ABLTY[5:5]	1
0xBB000088	FORCE_P_ABLTY [0].LINK_ABLTY[4:4]	1
0xBB000088	FORCE_P_ABLTY [0].FIB1G_ABLTY[3:3]	1
0xBB000088	FORCE_P_ABLTY [0].DUPLEX_ABLTY[2:2]	1
0xBB000088	FORCE_P_ABLTY [0].SPEED_ABLTY[1:0]	2
0xBB00008C	FORCE_P_ABLTY [1].RESERVED[31:12]	20
0xBB00008C	FORCE_P_ABLTY [1].LPI_1000_ABLTY[11:11]	1
0xBB00008C	FORCE_P_ABLTY [1].LPI_100_ABLTY[10:10]	1
0xBB00008C	FORCE_P_ABLTY [1].MST_FAULT_ABLTY[9:9]	1
0xBB00008C	FORCE_P_ABLTY [1].MST_MOD_ABLTY[8:8]	1
0xBB00008C	FORCE_P_ABLTY [1].NWAY_ABLTY[7:7]	1

Address	Register	Len
0xBB00008C	FORCE_P_ABLTY [1].TXPAUSE_ABLTY[6:6]	1
0xBB00008C	FORCE_P_ABLTY [1].RXPAUSE_ABLTY[5:5]	1
0xBB00008C	FORCE_P_ABLTY [1].LINK_ABLTY[4:4]	1
0xBB00008C	FORCE_P_ABLTY [1].FIB1G_ABLTY[3:3]	1
0xBB00008C	FORCE_P_ABLTY [1].DUPLEX_ABLTY[2:2]	1
0xBB00008C	FORCE_P_ABLTY [1].SPEED_ABLTY[1:0]	2
0xBB000090	FORCE_P_ABLTY [2].RESERVED[31:12]	20
0xBB000090	FORCE_P_ABLTY [2].LPI_1000_ABLTY[11:11]	1
0xBB000090	FORCE_P_ABLTY [2].LPI_100_ABLTY[10:10]	1
0xBB000090	FORCE_P_ABLTY [2].MST_FAULT_ABLTY[9:9]	1
0xBB000090	FORCE_P_ABLTY [2].MST_MOD_ABLTY[8:8]	1
0xBB000090	FORCE_P_ABLTY [2].NWAY_ABLTY[7:7]	1
0xBB000090	FORCE_P_ABLTY [2].TXPAUSE_ABLTY[6:6]	1
0xBB000090	FORCE_P_ABLTY [2].RXPAUSE_ABLTY[5:5]	1
0xBB000090	FORCE_P_ABLTY [2].LINK_ABLTY[4:4]	1
0xBB000090	FORCE_P_ABLTY [2].FIB1G_ABLTY[3:3]	1
0xBB000090	FORCE_P_ABLTY [2].DUPLEX_ABLTY[2:2]	1
0xBB000090	FORCE_P_ABLTY [2].SPEED_ABLTY[1:0]	2
0xBB000094	FORCE_P_ABLTY [3].RESERVED[31:12]	20
0xBB000094	FORCE_P_ABLTY [3].LPI_1000_ABLTY[11:11]	1
0xBB000094	FORCE_P_ABLTY [3].LPI_100_ABLTY[10:10]	1
0xBB000094	FORCE_P_ABLTY [3].MST_FAULT_ABLTY[9:9]	1
0xBB000094	FORCE_P_ABLTY [3].MST_MOD_ABLTY[8:8]	1
0xBB000094	FORCE_P_ABLTY [3].NWAY_ABLTY[7:7]	1
0xBB000094	FORCE_P_ABLTY [3].TXPAUSE_ABLTY[6:6]	1
0xBB000094	FORCE_P_ABLTY [3].RXPAUSE_ABLTY[5:5]	1
0xBB000094	FORCE_P_ABLTY [3].LINK_ABLTY[4:4]	1
0xBB000094	FORCE_P_ABLTY [3].FIB1G_ABLTY[3:3]	1
0xBB000094	FORCE_P_ABLTY [3].DUPLEX_ABLTY[2:2]	1
0xBB000094	FORCE_P_ABLTY [3].SPEED_ABLTY[1:0]	2
0xBB000098	FORCE_P_ABLTY [4].RESERVED[31:12]	20
0xBB000098	FORCE_P_ABLTY [4].LPI_1000_ABLTY[11:11]	1
0xBB000098	FORCE_P_ABLTY [4].LPI_100_ABLTY[10:10]	1
0xBB000098	FORCE_P_ABLTY [4].MST_FAULT_ABLTY[9:9]	1
0xBB000098	FORCE_P_ABLTY [4].MST_MOD_ABLTY[8:8]	1
0xBB000098	FORCE_P_ABLTY [4].NWAY_ABLTY[7:7]	1
0xBB000098	FORCE_P_ABLTY [4].TXPAUSE_ABLTY[6:6]	1
0xBB000098	FORCE_P_ABLTY [4].RXPAUSE_ABLTY[5:5]	1
0xBB000098	FORCE_P_ABLTY [4].LINK_ABLTY[4:4]	1
0xBB000098	FORCE_P_ABLTY [4].FIB1G_ABLTY[3:3]	1
0xBB000098	FORCE_P_ABLTY [4].DUPLEX_ABLTY[2:2]	1
0xBB000098	FORCE_P_ABLTY [4].SPEED_ABLTY[1:0]	2
0xBB00009C	FORCE_P_ABLTY [5].RESERVED[31:12]	20
0xBB00009C	FORCE_P_ABLTY [5].LPI_1000_ABLTY[11:11]	1
0xBB00009C	FORCE_P_ABLTY [5].LPI_100_ABLTY[10:10]	1
0xBB00009C	FORCE_P_ABLTY [5].MST_FAULT_ABLTY[9:9]	1

Address	Register	Len
0xBB00009C	FORCE_P_ABLTY [5].MST_MOD_ABLTY[8:8]	1
0xBB00009C	FORCE_P_ABLTY [5].NWAY_ABLTY[7:7]	1
0xBB00009C	FORCE_P_ABLTY [5].TXPAUSE_ABLTY[6:6]	1
0xBB00009C	FORCE_P_ABLTY [5].RXPAUSE_ABLTY[5:5]	1
0xBB00009C	FORCE_P_ABLTY [5].LINK_ABLTY[4:4]	1
0xBB00009C	FORCE_P_ABLTY [5].FIB1G_ABLTY[3:3]	1
0xBB00009C	FORCE_P_ABLTY [5].DUPLEX_ABLTY[2:2]	1
0xBB00009C	FORCE_P_ABLTY [5].SPEED_ABLTY[1:0]	2
0xBB0000A0	FORCE_P_ABLTY [6].RESERVED[31:12]	20
0xBB0000A0	FORCE_P_ABLTY [6].LPI_1000_ABLTY[11:11]	1
0xBB0000A0	FORCE_P_ABLTY [6].LPI_100_ABLTY[10:10]	1
0xBB0000A0	FORCE_P_ABLTY [6].MST_FAULT_ABLTY[9:9]	1
0xBB0000A0	FORCE_P_ABLTY [6].MST_MOD_ABLTY[8:8]	1
0xBB0000A0	FORCE_P_ABLTY [6].NWAY_ABLTY[7:7]	1
0xBB0000A0	FORCE_P_ABLTY [6].TXPAUSE_ABLTY[6:6]	1
0xBB0000A0	FORCE_P_ABLTY [6].RXPAUSE_ABLTY[5:5]	1
0xBB0000A0	FORCE_P_ABLTY [6].LINK_ABLTY[4:4]	1
0xBB0000A0	FORCE_P_ABLTY [6].FIB1G_ABLTY[3:3]	1
0xBB0000A0	FORCE_P_ABLTY [6].DUPLEX_ABLTY[2:2]	1
0xBB0000A0	FORCE_P_ABLTY [6].SPEED_ABLTY[1:0]	2
0xBB0000A4	MDX_PHY_REG1.RESERVED[31:10]	22
0xBB0000A4	MDX_PHY_REG1.PHY_BRD_MODE[9:5]	5
0xBB0000A4	MDX_PHY_REG1.BRD_PHYAD[4:0]	5
0xBB0000A8	UPS_CTRL2.RESERVED[31:16]	16
0xBB0000A8	UPS_CTRL2.IGNOE_MAC5_LINK[15:15]	1
0xBB0000A8	UPS_CTRL2.RESERVED[14:0]	15
0xBB0000AC	GATING_CLK_1.RESERVED[31:1]	31
0xBB0000AC	GATING_CLK_1.IGNOE_MAC6_LINK[0:0]	1
0xBB0000B0	ROUTER_UPS_CFG.RESERVED[31:1]	31
0xBB0000B0	ROUTER_UPS_CFG.SOFTSTART[0:0]	1
0xBB0000B4	P_ABLTY [0].RESERVED[31:12]	20
0xBB0000B4	P_ABLTY [0].LPI_1000[11:11]	1
0xBB0000B4	P_ABLTY [0].LPI_100[10:10]	1
0xBB0000B4	P_ABLTY [0].P_NWAY_FAULT[9:9]	1
0xBB0000B4	P_ABLTY [0].P_MSTR[8:8]	1
0xBB0000B4	P_ABLTY [0].P_NWAY_ABLTY[7:7]	1
0xBB0000B4	P_ABLTY [0].P_TX_FC[6:6]	1
0xBB0000B4	P_ABLTY [0].P_RX_FC[5:5]	1
0xBB0000B4	P_ABLTY [0].P_LINK_STATUS[4:4]	1
0xBB0000B4	P_ABLTY [0].P_LINK_FIB1G[3:3]	1
0xBB0000B4	P_ABLTY [0].P_DUPLEX[2:2]	1
0xBB0000B4	P_ABLTY [0].P_LINK_SPD[1:0]	2
0xBB0000B8	P_ABLTY [1].RESERVED[31:12]	20
0xBB0000B8	P_ABLTY [1].LPI_1000[11:11]	1
0xBB0000B8	P_ABLTY [1].LPI_100[10:10]	1
0xBB0000B8	P_ABLTY [1].P_NWAY_FAULT[9:9]	1

Address	Register	Len
0xBB0000B8	P_ABLTY [1].P_MSTR[8:8]	1
0xBB0000B8	P_ABLTY [1].P_NWAY_ABLTY[7:7]	1
0xBB0000B8	P_ABLTY [1].P_TX_FC[6:6]	1
0xBB0000B8	P_ABLTY [1].P_RX_FC[5:5]	1
0xBB0000B8	P_ABLTY [1].P_LINK_STATUS[4:4]	1
0xBB0000B8	P_ABLTY [1].P_LINK_FIB1G[3:3]	1
0xBB0000B8	P_ABLTY [1].P_DUPLEX[2:2]	1
0xBB0000B8	P_ABLTY [1].P_LINK_SPD[1:0]	2
0xBB0000BC	P_ABLTY [2].RESERVED[31:12]	20
0xBB0000BC	P_ABLTY [2].LPI_1000[11:11]	1
0xBB0000BC	P_ABLTY [2].LPI_100[10:10]	1
0xBB0000BC	P_ABLTY [2].P_NWAY_FAULT[9:9]	1
0xBB0000BC	P_ABLTY [2].P_MSTR[8:8]	1
0xBB0000BC	P_ABLTY [2].P_NWAY_ABLTY[7:7]	1
0xBB0000BC	P_ABLTY [2].P_TX_FC[6:6]	1
0xBB0000BC	P_ABLTY [2].P_RX_FC[5:5]	1
0xBB0000BC	P_ABLTY [2].P_LINK_STATUS[4:4]	1
0xBB0000BC	P_ABLTY [2].P_LINK_FIB1G[3:3]	1
0xBB0000BC	P_ABLTY [2].P_DUPLEX[2:2]	1
0xBB0000BC	P_ABLTY [2].P_LINK_SPD[1:0]	2
0xBB0000C0	P_ABLTY [3].RESERVED[31:12]	20
0xBB0000C0	P_ABLTY [3].LPI_1000[11:11]	1
0xBB0000C0	P_ABLTY [3].LPI_100[10:10]	1
0xBB0000C0	P_ABLTY [3].P_NWAY_FAULT[9:9]	1
0xBB0000C0	P_ABLTY [3].P_MSTR[8:8]	1
0xBB0000C0	P_ABLTY [3].P_NWAY_ABLTY[7:7]	1
0xBB0000C0	P_ABLTY [3].P_TX_FC[6:6]	1
0xBB0000C0	P_ABLTY [3].P_RX_FC[5:5]	1
0xBB0000C0	P_ABLTY [3].P_LINK_STATUS[4:4]	1
0xBB0000C0	P_ABLTY [3].P_LINK_FIB1G[3:3]	1
0xBB0000C0	P_ABLTY [3].P_DUPLEX[2:2]	1
0xBB0000C0	P_ABLTY [3].P_LINK_SPD[1:0]	2
0xBB0000C4	P_ABLTY [4].RESERVED[31:12]	20
0xBB0000C4	P_ABLTY [4].LPI_1000[11:11]	1
0xBB0000C4	P_ABLTY [4].LPI_100[10:10]	1
0xBB0000C4	P_ABLTY [4].P_NWAY_FAULT[9:9]	1
0xBB0000C4	P_ABLTY [4].P_MSTR[8:8]	1
0xBB0000C4	P_ABLTY [4].P_NWAY_ABLTY[7:7]	1
0xBB0000C4	P_ABLTY [4].P_TX_FC[6:6]	1
0xBB0000C4	P_ABLTY [4].P_RX_FC[5:5]	1
0xBB0000C4	P_ABLTY [4].P_LINK_STATUS[4:4]	1
0xBB0000C4	P_ABLTY [4].P_LINK_FIB1G[3:3]	1
0xBB0000C4	P_ABLTY [4].P_DUPLEX[2:2]	1
0xBB0000C4	P_ABLTY [4].P_LINK_SPD[1:0]	2
0xBB0000C8	P_ABLTY [5].RESERVED[31:12]	20
0xBB0000C8	P_ABLTY [5].LPI_1000[11:11]	1



Address	Register	Len
0xBB0000C8	P_ABLTY [5].LPI_100[10:10]	1
0xBB0000C8	P_ABLTY [5].P_NWAY_FAULT[9:9]	1
0xBB0000C8	P_ABLTY [5].P_MSTR[8:8]	1
0xBB0000C8	P_ABLTY [5].P_NWAY_ABLTY[7:7]	1
0xBB0000C8	P_ABLTY [5].P_TX_FC[6:6]	1
0xBB0000C8	P_ABLTY [5].P_RX_FC[5:5]	1
0xBB0000C8	P_ABLTY [5].P_LINK_STATUS[4:4]	1
0xBB0000C8	P_ABLTY [5].P_LINK_FIB1G[3:3]	1
0xBB0000C8	P_ABLTY [5].P_DUPLEX[2:2]	1
0xBB0000C8	P_ABLTY [5].P_LINK_SPD[1:0]	2
0xBB0000CC	P_ABLTY [6].RESERVED[31:12]	20
0xBB0000CC	P_ABLTY [6].LPI_1000[11:11]	1
0xBB0000CC	P_ABLTY [6].LPI_100[10:10]	1
0xBB0000CC	P_ABLTY [6].P_NWAY_FAULT[9:9]	1
0xBB0000CC	P_ABLTY [6].P_MSTR[8:8]	1
0xBB0000CC	P_ABLTY [6].P_NWAY_ABLTY[7:7]	1
0xBB0000CC	P_ABLTY [6].P_TX_FC[6:6]	1
0xBB0000CC	P_ABLTY [6].P_RX_FC[5:5]	1
0xBB0000CC	P_ABLTY [6].P_LINK_STATUS[4:4]	1
0xBB0000CC	P_ABLTY [6].P_LINK_FIB1G[3:3]	1
0xBB0000CC	P_ABLTY [6].P_DUPLEX[2:2]	1
0xBB0000CC	P_ABLTY [6].P_LINK_SPD[1:0]	2
0xBB0000D0	GPIO_CTRL_0 [0].CTRL_GPIO[0:0]	1
0xBB0000D0	GPIO_CTRL_0 [1].CTRL_GPIO[1:1]	1
0xBB0000D0	GPIO_CTRL_0 [2].CTRL_GPIO[2:2]	1
0xBB0000D0	GPIO_CTRL_0 [3].CTRL_GPIO[3:3]	1
0xBB0000D0	GPIO_CTRL_0 [4].CTRL_GPIO[4:4]	1
0xBB0000D0	GPIO_CTRL_0 [5].CTRL_GPIO[5:5]	1
0xBB0000D0	GPIO_CTRL_0 [6].CTRL_GPIO[6:6]	1
0xBB0000D0	GPIO_CTRL_0 [7].CTRL_GPIO[7:7]	1
0xBB0000D0	GPIO_CTRL_0 [8].CTRL_GPIO[8:8]	1
0xBB0000D0	GPIO_CTRL_0 [9].CTRL_GPIO[9:9]	1
0xBB0000D0	GPIO_CTRL_0 [10].CTRL_GPIO[10:10]	1
0xBB0000D0	GPIO_CTRL_0 [11].CTRL_GPIO[11:11]	1
0xBB0000D0	GPIO_CTRL_0 [12].CTRL_GPIO[12:12]	1
0xBB0000D0	GPIO_CTRL_0 [13].CTRL_GPIO[13:13]	1
0xBB0000D0	GPIO_CTRL_0 [14].CTRL_GPIO[14:14]	1
0xBB0000D0	GPIO_CTRL_0 [15].CTRL_GPIO[15:15]	1
0xBB0000D0	GPIO_CTRL_0 [16].CTRL_GPIO[16:16]	1
0xBB0000D0	GPIO_CTRL_0 [17].CTRL_GPIO[17:17]	1
0xBB0000D0	GPIO_CTRL_0 [18].CTRL_GPIO[18:18]	1
0xBB0000D0	GPIO_CTRL_0 [19].CTRL_GPIO[19:19]	1
0xBB0000D0	GPIO_CTRL_0 [20].CTRL_GPIO[20:20]	1
0xBB0000D0	GPIO_CTRL_0 [21].CTRL_GPIO[21:21]	1
0xBB0000D0	GPIO_CTRL_0 [22].CTRL_GPIO[22:22]	1
0xBB0000D0	GPIO_CTRL_0 [23].CTRL_GPIO[23:23]	1

Address	Register	Len
0xBB0000D0	GPIO_CTRL_0 [24].CTRL_GPIO[24:24]	1
0xBB0000D0	GPIO_CTRL_0 [25].CTRL_GPIO[25:25]	1
0xBB0000D0	GPIO_CTRL_0 [26].CTRL_GPIO[26:26]	1
0xBB0000D0	GPIO_CTRL_0 [27].CTRL_GPIO[27:27]	1
0xBB0000D0	GPIO_CTRL_0 [28].CTRL_GPIO[28:28]	1
0xBB0000D0	GPIO_CTRL_0 [29].CTRL_GPIO[29:29]	1
0xBB0000D0	GPIO_CTRL_0 [30].CTRL_GPIO[30:30]	1
0xBB0000D0	GPIO_CTRL_0 [31].CTRL_GPIO[31:31]	1
0xBB0000D4	GPIO_CTRL_0 [32].CTRL_GPIO[0:0]	1
0xBB0000D4	GPIO_CTRL_0 [33].CTRL_GPIO[1:1]	1
0xBB0000D4	GPIO_CTRL_0 [34].CTRL_GPIO[2:2]	1
0xBB0000D4	GPIO_CTRL_0 [35].CTRL_GPIO[3:3]	1
0xBB0000D4	GPIO_CTRL_0 [36].CTRL_GPIO[4:4]	1
0xBB0000D4	GPIO_CTRL_0 [37].CTRL_GPIO[5:5]	1
0xBB0000D4	GPIO_CTRL_0 [38].CTRL_GPIO[6:6]	1
0xBB0000D4	GPIO_CTRL_0 [39].CTRL_GPIO[7:7]	1
0xBB0000D4	GPIO_CTRL_0 [40].CTRL_GPIO[8:8]	1
0xBB0000D4	GPIO_CTRL_0 [41].CTRL_GPIO[9:9]	1
0xBB0000D4	GPIO_CTRL_0 [42].CTRL_GPIO[10:10]	1
0xBB0000D4	GPIO_CTRL_0 [43].CTRL_GPIO[11:11]	1
0xBB0000D4	GPIO_CTRL_0 [44].CTRL_GPIO[12:12]	1
0xBB0000D4	GPIO_CTRL_0 [45].CTRL_GPIO[13:13]	1
0xBB0000D4	GPIO_CTRL_0 [46].CTRL_GPIO[14:14]	1
0xBB0000D4	GPIO_CTRL_0 [47].CTRL_GPIO[15:15]	1
0xBB0000D4	GPIO_CTRL_0 [48].CTRL_GPIO[16:16]	1
0xBB0000D4	GPIO_CTRL_0 [49].CTRL_GPIO[17:17]	1
0xBB0000D4	GPIO_CTRL_0 [50].CTRL_GPIO[18:18]	1
0xBB0000D4	GPIO_CTRL_0 [51].CTRL_GPIO[19:19]	1
0xBB0000D4	GPIO_CTRL_0 [52].CTRL_GPIO[20:20]	1
0xBB0000D4	GPIO_CTRL_0 [53].CTRL_GPIO[21:21]	1
0xBB0000D4	GPIO_CTRL_0 [54].CTRL_GPIO[22:22]	1
0xBB0000D4	GPIO_CTRL_0 [55].CTRL_GPIO[23:23]	1
0xBB0000D4	GPIO_CTRL_0 [56].CTRL_GPIO[24:24]	1
0xBB0000D4	GPIO_CTRL_0 [57].CTRL_GPIO[25:25]	1
0xBB0000D4	GPIO_CTRL_0 [58].CTRL_GPIO[26:26]	1
0xBB0000D4	GPIO_CTRL_0 [59].CTRL_GPIO[27:27]	1
0xBB0000D4	GPIO_CTRL_0 [60].CTRL_GPIO[28:28]	1
0xBB0000D4	GPIO_CTRL_0 [61].CTRL_GPIO[29:29]	1
0xBB0000D4	GPIO_CTRL_0 [62].CTRL_GPIO[30:30]	1
0xBB0000D4	GPIO_CTRL_0 [63].CTRL_GPIO[31:31]	1
0xBB0000D8	GPIO_CTRL_0 [64].CTRL_GPIO[0:0]	1
0xBB0000D8	GPIO_CTRL_0 [65].CTRL_GPIO[1:1]	1
0xBB0000D8	GPIO_CTRL_0 [66].CTRL_GPIO[2:2]	1
0xBB0000D8	GPIO_CTRL_0 [67].CTRL_GPIO[3:3]	1
0xBB0000D8	GPIO_CTRL_0 [68].CTRL_GPIO[4:4]	1
0xBB0000D8	GPIO_CTRL_0 [69].CTRL_GPIO[5:5]	1

Address	Register	Len
0xBB0000D8	GPIO_CTRL_0 [70].CTRL_GPIO[6:6]	1
0xBB0000D8	GPIO_CTRL_0 [71].CTRL_GPIO[7:7]	1
0xBB0000DC	GPIO_CTRL_1 [0].STS_GPIO[0:0]	1
0xBB0000DC	GPIO_CTRL_1 [1].STS_GPIO[1:1]	1
0xBB0000DC	GPIO_CTRL_1 [2].STS_GPIO[2:2]	1
0xBB0000DC	GPIO_CTRL_1 [3].STS_GPIO[3:3]	1
0xBB0000DC	GPIO_CTRL_1 [4].STS_GPIO[4:4]	1
0xBB0000DC	GPIO_CTRL_1 [5].STS_GPIO[5:5]	1
0xBB0000DC	GPIO_CTRL_1 [6].STS_GPIO[6:6]	1
0xBB0000DC	GPIO_CTRL_1 [7].STS_GPIO[7:7]	1
0xBB0000DC	GPIO_CTRL_1 [8].STS_GPIO[8:8]	1
0xBB0000DC	GPIO_CTRL_1 [9].STS_GPIO[9:9]	1
0xBB0000DC	GPIO_CTRL_1 [10].STS_GPIO[10:10]	1
0xBB0000DC	GPIO_CTRL_1 [11].STS_GPIO[11:11]	1
0xBB0000DC	GPIO_CTRL_1 [12].STS_GPIO[12:12]	1
0xBB0000DC	GPIO_CTRL_1 [13].STS_GPIO[13:13]	1
0xBB0000DC	GPIO_CTRL_1 [14].STS_GPIO[14:14]	1
0xBB0000DC	GPIO_CTRL_1 [15].STS_GPIO[15:15]	1
0xBB0000DC	GPIO_CTRL_1 [16].STS_GPIO[16:16]	1
0xBB0000DC	GPIO_CTRL_1 [17].STS_GPIO[17:17]	1
0xBB0000DC	GPIO_CTRL_1 [18].STS_GPIO[18:18]	1
0xBB0000DC	GPIO_CTRL_1 [19].STS_GPIO[19:19]	1
0xBB0000DC	GPIO_CTRL_1 [20].STS_GPIO[20:20]	1
0xBB0000DC	GPIO_CTRL_1 [21].STS_GPIO[21:21]	1
0xBB0000DC	GPIO_CTRL_1 [22].STS_GPIO[22:22]	1
0xBB0000DC	GPIO_CTRL_1 [23].STS_GPIO[23:23]	1
0xBB0000DC	GPIO_CTRL_1 [24].STS_GPIO[24:24]	1
0xBB0000DC	GPIO_CTRL_1 [25].STS_GPIO[25:25]	1
0xBB0000DC	GPIO_CTRL_1 [26].STS_GPIO[26:26]	1
0xBB0000DC	GPIO_CTRL_1 [27].STS_GPIO[27:27]	1
0xBB0000DC	GPIO_CTRL_1 [28].STS_GPIO[28:28]	1
0xBB0000DC	GPIO_CTRL_1 [29].STS_GPIO[29:29]	1
0xBB0000DC	GPIO_CTRL_1 [30].STS_GPIO[30:30]	1
0xBB0000DC	GPIO_CTRL_1 [31].STS_GPIO[31:31]	1
0xBB0000E0	GPIO_CTRL_1 [32].STS_GPIO[0:0]	1
0xBB0000E0	GPIO_CTRL_1 [33].STS_GPIO[1:1]	1
0xBB0000E0	GPIO_CTRL_1 [34].STS_GPIO[2:2]	1
0xBB0000E0	GPIO_CTRL_1 [35].STS_GPIO[3:3]	1
0xBB0000E0	GPIO_CTRL_1 [36].STS_GPIO[4:4]	1
0xBB0000E0	GPIO_CTRL_1 [37].STS_GPIO[5:5]	1
0xBB0000E0	GPIO_CTRL_1 [38].STS_GPIO[6:6]	1
0xBB0000E0	GPIO_CTRL_1 [39].STS_GPIO[7:7]	1
0xBB0000E0	GPIO_CTRL_1 [40].STS_GPIO[8:8]	1
0xBB0000E0	GPIO_CTRL_1 [41].STS_GPIO[9:9]	1
0xBB0000E0	GPIO_CTRL_1 [42].STS_GPIO[10:10]	1
0xBB0000E0	GPIO_CTRL_1 [43].STS_GPIO[11:11]	1

Address	Register	Len
0xBB0000E0	GPIO_CTRL_1 [44].STS_GPIO[12:12]	1
0xBB0000E0	GPIO_CTRL_1 [45].STS_GPIO[13:13]	1
0xBB0000E0	GPIO_CTRL_1 [46].STS_GPIO[14:14]	1
0xBB0000E0	GPIO_CTRL_1 [47].STS_GPIO[15:15]	1
0xBB0000E0	GPIO_CTRL_1 [48].STS_GPIO[16:16]	1
0xBB0000E0	GPIO_CTRL_1 [49].STS_GPIO[17:17]	1
0xBB0000E0	GPIO_CTRL_1 [50].STS_GPIO[18:18]	1
0xBB0000E0	GPIO_CTRL_1 [51].STS_GPIO[19:19]	1
0xBB0000E0	GPIO_CTRL_1 [52].STS_GPIO[20:20]	1
0xBB0000E0	GPIO_CTRL_1 [53].STS_GPIO[21:21]	1
0xBB0000E0	GPIO_CTRL_1 [54].STS_GPIO[22:22]	1
0xBB0000E0	GPIO_CTRL_1 [55].STS_GPIO[23:23]	1
0xBB0000E0	GPIO_CTRL_1 [56].STS_GPIO[24:24]	1
0xBB0000E0	GPIO_CTRL_1 [57].STS_GPIO[25:25]	1
0xBB0000E0	GPIO_CTRL_1 [58].STS_GPIO[26:26]	1
0xBB0000E0	GPIO_CTRL_1 [59].STS_GPIO[27:27]	1
0xBB0000E0	GPIO_CTRL_1 [60].STS_GPIO[28:28]	1
0xBB0000E0	GPIO_CTRL_1 [61].STS_GPIO[29:29]	1
0xBB0000E0	GPIO_CTRL_1 [62].STS_GPIO[30:30]	1
0xBB0000E0	GPIO_CTRL_1 [63].STS_GPIO[31:31]	1
0xBB0000E4	GPIO_CTRL_1 [64].STS_GPIO[0:0]	1
0xBB0000E4	GPIO_CTRL_1 [65].STS_GPIO[1:1]	1
0xBB0000E4	GPIO_CTRL_1 [66].STS_GPIO[2:2]	1
0xBB0000E4	GPIO_CTRL_1 [67].STS_GPIO[3:3]	1
0xBB0000E4	GPIO_CTRL_1 [68].STS_GPIO[4:4]	1
0xBB0000E4	GPIO_CTRL_1 [69].STS_GPIO[5:5]	1
0xBB0000E4	GPIO_CTRL_1 [70].STS_GPIO[6:6]	1
0xBB0000E4	GPIO_CTRL_1 [71].STS_GPIO[7:7]	1
0xBB0000E8	GPIO_CTRL_2 [0].EN_GPIO[0:0]	1
0xBB0000E8	GPIO_CTRL_2 [1].EN_GPIO[1:1]	1
0xBB0000E8	GPIO_CTRL_2 [2].EN_GPIO[2:2]	1
0xBB0000E8	GPIO_CTRL_2 [3].EN_GPIO[3:3]	1
0xBB0000E8	GPIO_CTRL_2 [4].EN_GPIO[4:4]	1
0xBB0000E8	GPIO_CTRL_2 [5].EN_GPIO[5:5]	1
0xBB0000E8	GPIO_CTRL_2 [6].EN_GPIO[6:6]	1
0xBB0000E8	GPIO_CTRL_2 [7].EN_GPIO[7:7]	1
0xBB0000E8	GPIO_CTRL_2 [8].EN_GPIO[8:8]	1
0xBB0000E8	GPIO_CTRL_2 [9].EN_GPIO[9:9]	1
0xBB0000E8	GPIO_CTRL_2 [10].EN_GPIO[10:10]	1
0xBB0000E8	GPIO_CTRL_2 [11].EN_GPIO[11:11]	1
0xBB0000E8	GPIO_CTRL_2 [12].EN_GPIO[12:12]	1
0xBB0000E8	GPIO_CTRL_2 [13].EN_GPIO[13:13]	1
0xBB0000E8	GPIO_CTRL_2 [14].EN_GPIO[14:14]	1
0xBB0000E8	GPIO_CTRL_2 [15].EN_GPIO[15:15]	1
0xBB0000E8	GPIO_CTRL_2 [16].EN_GPIO[16:16]	1
0xBB0000E8	GPIO_CTRL_2 [17].EN_GPIO[17:17]	1

Address	Register	Len
0xBB0000E8	GPIO_CTRL_2 [18].EN_GPIO[18:18]	1
0xBB0000E8	GPIO_CTRL_2 [19].EN_GPIO[19:19]	1
0xBB0000E8	GPIO_CTRL_2 [20].EN_GPIO[20:20]	1
0xBB0000E8	GPIO_CTRL_2 [21].EN_GPIO[21:21]	1
0xBB0000E8	GPIO_CTRL_2 [22].EN_GPIO[22:22]	1
0xBB0000E8	GPIO_CTRL_2 [23].EN_GPIO[23:23]	1
0xBB0000E8	GPIO_CTRL_2 [24].EN_GPIO[24:24]	1
0xBB0000E8	GPIO_CTRL_2 [25].EN_GPIO[25:25]	1
0xBB0000E8	GPIO_CTRL_2 [26].EN_GPIO[26:26]	1
0xBB0000E8	GPIO_CTRL_2 [27].EN_GPIO[27:27]	1
0xBB0000E8	GPIO_CTRL_2 [28].EN_GPIO[28:28]	1
0xBB0000E8	GPIO_CTRL_2 [29].EN_GPIO[29:29]	1
0xBB0000E8	GPIO_CTRL_2 [30].EN_GPIO[30:30]	1
0xBB0000E8	GPIO_CTRL_2 [31].EN_GPIO[31:31]	1
0xBB0000EC	GPIO_CTRL_2 [32].EN_GPIO[0:0]	1
0xBB0000EC	GPIO_CTRL_2 [33].EN_GPIO[1:1]	1
0xBB0000EC	GPIO_CTRL_2 [34].EN_GPIO[2:2]	1
0xBB0000EC	GPIO_CTRL_2 [35].EN_GPIO[3:3]	1
0xBB0000EC	GPIO_CTRL_2 [36].EN_GPIO[4:4]	1
0xBB0000EC	GPIO_CTRL_2 [37].EN_GPIO[5:5]	1
0xBB0000EC	GPIO_CTRL_2 [38].EN_GPIO[6:6]	1
0xBB0000EC	GPIO_CTRL_2 [39].EN_GPIO[7:7]	1
0xBB0000EC	GPIO_CTRL_2 [40].EN_GPIO[8:8]	1
0xBB0000EC	GPIO_CTRL_2 [41].EN_GPIO[9:9]	1
0xBB0000EC	GPIO_CTRL_2 [42].EN_GPIO[10:10]	1
0xBB0000EC	GPIO_CTRL_2 [43].EN_GPIO[11:11]	1
0xBB0000EC	GPIO_CTRL_2 [44].EN_GPIO[12:12]	1
0xBB0000EC	GPIO_CTRL_2 [45].EN_GPIO[13:13]	1
0xBB0000EC	GPIO_CTRL_2 [46].EN_GPIO[14:14]	1
0xBB0000EC	GPIO_CTRL_2 [47].EN_GPIO[15:15]	1
0xBB0000EC	GPIO_CTRL_2 [48].EN_GPIO[16:16]	1
0xBB0000EC	GPIO_CTRL_2 [49].EN_GPIO[17:17]	1
0xBB0000EC	GPIO_CTRL_2 [50].EN_GPIO[18:18]	1
0xBB0000EC	GPIO_CTRL_2 [51].EN_GPIO[19:19]	1
0xBB0000EC	GPIO_CTRL_2 [52].EN_GPIO[20:20]	1
0xBB0000EC	GPIO_CTRL_2 [53].EN_GPIO[21:21]	1
0xBB0000EC	GPIO_CTRL_2 [54].EN_GPIO[22:22]	1
0xBB0000EC	GPIO_CTRL_2 [55].EN_GPIO[23:23]	1
0xBB0000EC	GPIO_CTRL_2 [56].EN_GPIO[24:24]	1
0xBB0000EC	GPIO_CTRL_2 [57].EN_GPIO[25:25]	1
0xBB0000EC	GPIO_CTRL_2 [58].EN_GPIO[26:26]	1
0xBB0000EC	GPIO_CTRL_2 [59].EN_GPIO[27:27]	1
0xBB0000EC	GPIO_CTRL_2 [60].EN_GPIO[28:28]	1
0xBB0000EC	GPIO_CTRL_2 [61].EN_GPIO[29:29]	1
0xBB0000EC	GPIO_CTRL_2 [62].EN_GPIO[30:30]	1
0xBB0000EC	GPIO_CTRL_2 [63].EN_GPIO[31:31]	1

Address	Register	Len
0xBB0000F0	GPIO_CTRL_2 [64].EN_GPIO[0:0]	1
0xBB0000F0	GPIO_CTRL_2 [65].EN_GPIO[1:1]	1
0xBB0000F0	GPIO_CTRL_2 [66].EN_GPIO[2:2]	1
0xBB0000F0	GPIO_CTRL_2 [67].EN_GPIO[3:3]	1
0xBB0000F0	GPIO_CTRL_2 [68].EN_GPIO[4:4]	1
0xBB0000F0	GPIO_CTRL_2 [69].EN_GPIO[5:5]	1
0xBB0000F0	GPIO_CTRL_2 [70].EN_GPIO[6:6]	1
0xBB0000F0	GPIO_CTRL_2 [71].EN_GPIO[7:7]	1
0xBB0000F4	GPIO_CTRL_3 [0].DUMMY[0:0]	1
0xBB0000F4	GPIO_CTRL_3 [1].DUMMY[1:1]	1
0xBB0000F4	GPIO_CTRL_3 [2].DUMMY[2:2]	1
0xBB0000F4	GPIO_CTRL_3 [3].DUMMY[3:3]	1
0xBB0000F4	GPIO_CTRL_3 [4].DUMMY[4:4]	1
0xBB0000F4	GPIO_CTRL_3 [5].DUMMY[5:5]	1
0xBB0000F4	GPIO_CTRL_3 [6].DUMMY[6:6]	1
0xBB0000F4	GPIO_CTRL_3 [7].DUMMY[7:7]	1
0xBB0000F4	GPIO_CTRL_3 [8].DUMMY[8:8]	1
0xBB0000F4	GPIO_CTRL_3 [9].DUMMY[9:9]	1
0xBB0000F4	GPIO_CTRL_3 [10].DUMMY[10:10]	1
0xBB0000F4	GPIO_CTRL_3 [11].DUMMY[11:11]	1
0xBB0000F4	GPIO_CTRL_3 [12].DUMMY[12:12]	1
0xBB0000F4	GPIO_CTRL_3 [13].DUMMY[13:13]	1
0xBB0000F4	GPIO_CTRL_3 [14].DUMMY[14:14]	1
0xBB0000F4	GPIO_CTRL_3 [15].DUMMY[15:15]	1
0xBB0000F4	GPIO_CTRL_3 [16].DUMMY[16:16]	1
0xBB0000F4	GPIO_CTRL_3 [17].DUMMY[17:17]	1
0xBB0000F4	GPIO_CTRL_3 [18].DUMMY[18:18]	1
0xBB0000F4	GPIO_CTRL_3 [19].DUMMY[19:19]	1
0xBB0000F4	GPIO_CTRL_3 [20].DUMMY[20:20]	1
0xBB0000F4	GPIO_CTRL_3 [21].DUMMY[21:21]	1
0xBB0000F4	GPIO_CTRL_3 [22].DUMMY[22:22]	1
0xBB0000F4	GPIO_CTRL_3 [23].DUMMY[23:23]	1
0xBB0000F4	GPIO_CTRL_3 [24].DUMMY[24:24]	1
0xBB0000F4	GPIO_CTRL_3 [25].DUMMY[25:25]	1
0xBB0000F4	GPIO_CTRL_3 [26].DUMMY[26:26]	1
0xBB0000F4	GPIO_CTRL_3 [27].DUMMY[27:27]	1
0xBB0000F4	GPIO_CTRL_3 [28].DUMMY[28:28]	1
0xBB0000F4	GPIO_CTRL_3 [29].DUMMY[29:29]	1
0xBB0000F4	GPIO_CTRL_3 [30].DUMMY[30:30]	1
0xBB0000F4	GPIO_CTRL_3 [31].DUMMY[31:31]	1
0xBB0000F8	GPIO_CTRL_3 [32].DUMMY[0:0]	1
0xBB0000F8	GPIO_CTRL_3 [33].DUMMY[1:1]	1
0xBB0000F8	GPIO_CTRL_3 [34].DUMMY[2:2]	1
0xBB0000F8	GPIO_CTRL_3 [35].DUMMY[3:3]	1
0xBB0000F8	GPIO_CTRL_3 [36].DUMMY[4:4]	1
0xBB0000F8	GPIO_CTRL_3 [37].DUMMY[5:5]	1

Address	Register	Len
0xBB0000F8	GPIO_CTRL_3 [38].DUMMY[6:6]	1
0xBB0000F8	GPIO_CTRL_3 [39].DUMMY[7:7]	1
0xBB0000F8	GPIO_CTRL_3 [40].DUMMY[8:8]	1
0xBB0000F8	GPIO_CTRL_3 [41].DUMMY[9:9]	1
0xBB0000F8	GPIO_CTRL_3 [42].DUMMY[10:10]	1
0xBB0000F8	GPIO_CTRL_3 [43].DUMMY[11:11]	1
0xBB0000F8	GPIO_CTRL_3 [44].DUMMY[12:12]	1
0xBB0000F8	GPIO_CTRL_3 [45].DUMMY[13:13]	1
0xBB0000F8	GPIO_CTRL_3 [46].DUMMY[14:14]	1
0xBB0000F8	GPIO_CTRL_3 [47].DUMMY[15:15]	1
0xBB0000F8	GPIO_CTRL_3 [48].DUMMY[16:16]	1
0xBB0000F8	GPIO_CTRL_3 [49].DUMMY[17:17]	1
0xBB0000F8	GPIO_CTRL_3 [50].DUMMY[18:18]	1
0xBB0000F8	GPIO_CTRL_3 [51].DUMMY[19:19]	1
0xBB0000F8	GPIO_CTRL_3 [52].DUMMY[20:20]	1
0xBB0000F8	GPIO_CTRL_3 [53].DUMMY[21:21]	1
0xBB0000F8	GPIO_CTRL_3 [54].DUMMY[22:22]	1
0xBB0000F8	GPIO_CTRL_3 [55].DUMMY[23:23]	1
0xBB0000F8	GPIO_CTRL_3 [56].DUMMY[24:24]	1
0xBB0000F8	GPIO_CTRL_3 [57].DUMMY[25:25]	1
0xBB0000F8	GPIO_CTRL_3 [58].DUMMY[26:26]	1
0xBB0000F8	GPIO_CTRL_3 [59].DUMMY[27:27]	1
0xBB0000F8	GPIO_CTRL_3 [60].DUMMY[28:28]	1
0xBB0000F8	GPIO_CTRL_3 [61].DUMMY[29:29]	1
0xBB0000F8	GPIO_CTRL_3 [62].DUMMY[30:30]	1
0xBB0000F8	GPIO_CTRL_3 [63].DUMMY[31:31]	1
0xBB0000FC	GPIO_CTRL_3 [64].DUMMY[0:0]	1
0xBB0000FC	GPIO_CTRL_3 [65].DUMMY[1:1]	1
0xBB0000FC	GPIO_CTRL_3 [66].DUMMY[2:2]	1
0xBB0000FC	GPIO_CTRL_3 [67].DUMMY[3:3]	1
0xBB0000FC	GPIO_CTRL_3 [68].DUMMY[4:4]	1
0xBB0000FC	GPIO_CTRL_3 [69].DUMMY[5:5]	1
0xBB0000FC	GPIO_CTRL_3 [70].DUMMY[6:6]	1
0xBB0000FC	GPIO_CTRL_3 [71].DUMMY[7:7]	1
0xBB000100	GPIO_CTRL_4 [0].SEL_GPIO[0:0]	1
0xBB000100	GPIO_CTRL_4 [1].SEL_GPIO[1:1]	1
0xBB000100	GPIO_CTRL_4 [2].SEL_GPIO[2:2]	1
0xBB000100	GPIO_CTRL_4 [3].SEL_GPIO[3:3]	1
0xBB000100	GPIO_CTRL_4 [4].SEL_GPIO[4:4]	1
0xBB000100	GPIO_CTRL_4 [5].SEL_GPIO[5:5]	1
0xBB000100	GPIO_CTRL_4 [6].SEL_GPIO[6:6]	1
0xBB000100	GPIO_CTRL_4 [7].SEL_GPIO[7:7]	1
0xBB000100	GPIO_CTRL_4 [8].SEL_GPIO[8:8]	1
0xBB000100	GPIO_CTRL_4 [9].SEL_GPIO[9:9]	1
0xBB000100	GPIO_CTRL_4 [10].SEL_GPIO[10:10]	1
0xBB000100	GPIO_CTRL_4 [11].SEL_GPIO[11:11]	1

Address	Register	Len
0xBB000100	GPIO_CTRL_4 [12].SEL_GPIO[12:12]	1
0xBB000100	GPIO_CTRL_4 [13].SEL_GPIO[13:13]	1
0xBB000100	GPIO_CTRL_4 [14].SEL_GPIO[14:14]	1
0xBB000100	GPIO_CTRL_4 [15].SEL_GPIO[15:15]	1
0xBB000100	GPIO_CTRL_4 [16].SEL_GPIO[16:16]	1
0xBB000100	GPIO_CTRL_4 [17].SEL_GPIO[17:17]	1
0xBB000100	GPIO_CTRL_4 [18].SEL_GPIO[18:18]	1
0xBB000100	GPIO_CTRL_4 [19].SEL_GPIO[19:19]	1
0xBB000100	GPIO_CTRL_4 [20].SEL_GPIO[20:20]	1
0xBB000100	GPIO_CTRL_4 [21].SEL_GPIO[21:21]	1
0xBB000100	GPIO_CTRL_4 [22].SEL_GPIO[22:22]	1
0xBB000100	GPIO_CTRL_4 [23].SEL_GPIO[23:23]	1
0xBB000100	GPIO_CTRL_4 [24].SEL_GPIO[24:24]	1
0xBB000100	GPIO_CTRL_4 [25].SEL_GPIO[25:25]	1
0xBB000100	GPIO_CTRL_4 [26].SEL_GPIO[26:26]	1
0xBB000100	GPIO_CTRL_4 [27].SEL_GPIO[27:27]	1
0xBB000100	GPIO_CTRL_4 [28].SEL_GPIO[28:28]	1
0xBB000100	GPIO_CTRL_4 [29].SEL_GPIO[29:29]	1
0xBB000100	GPIO_CTRL_4 [30].SEL_GPIO[30:30]	1
0xBB000100	GPIO_CTRL_4 [31].SEL_GPIO[31:31]	1
0xBB000104	GPIO_CTRL_4 [32].SEL_GPIO[0:0]	1
0xBB000104	GPIO_CTRL_4 [33].SEL_GPIO[1:1]	1
0xBB000104	GPIO_CTRL_4 [34].SEL_GPIO[2:2]	1
0xBB000104	GPIO_CTRL_4 [35].SEL_GPIO[3:3]	1
0xBB000104	GPIO_CTRL_4 [36].SEL_GPIO[4:4]	1
0xBB000104	GPIO_CTRL_4 [37].SEL_GPIO[5:5]	1
0xBB000104	GPIO_CTRL_4 [38].SEL_GPIO[6:6]	1
0xBB000104	GPIO_CTRL_4 [39].SEL_GPIO[7:7]	1
0xBB000104	GPIO_CTRL_4 [40].SEL_GPIO[8:8]	1
0xBB000104	GPIO_CTRL_4 [41].SEL_GPIO[9:9]	1
0xBB000104	GPIO_CTRL_4 [42].SEL_GPIO[10:10]	1
0xBB000104	GPIO_CTRL_4 [43].SEL_GPIO[11:11]	1
0xBB000104	GPIO_CTRL_4 [44].SEL_GPIO[12:12]	1
0xBB000104	GPIO_CTRL_4 [45].SEL_GPIO[13:13]	1
0xBB000104	GPIO_CTRL_4 [46].SEL_GPIO[14:14]	1
0xBB000104	GPIO_CTRL_4 [47].SEL_GPIO[15:15]	1
0xBB000104	GPIO_CTRL_4 [48].SEL_GPIO[16:16]	1
0xBB000104	GPIO_CTRL_4 [49].SEL_GPIO[17:17]	1
0xBB000104	GPIO_CTRL_4 [50].SEL_GPIO[18:18]	1
0xBB000104	GPIO_CTRL_4 [51].SEL_GPIO[19:19]	1
0xBB000104	GPIO_CTRL_4 [52].SEL_GPIO[20:20]	1
0xBB000104	GPIO_CTRL_4 [53].SEL_GPIO[21:21]	1
0xBB000104	GPIO_CTRL_4 [54].SEL_GPIO[22:22]	1
0xBB000104	GPIO_CTRL_4 [55].SEL_GPIO[23:23]	1
0xBB000104	GPIO_CTRL_4 [56].SEL_GPIO[24:24]	1
0xBB000104	GPIO_CTRL_4 [57].SEL_GPIO[25:25]	1



Address	Register	Len
0xBB000104	GPIO_CTRL_4 [58].SEL_GPIO[26:26]	1
0xBB000104	GPIO_CTRL_4 [59].SEL_GPIO[27:27]	1
0xBB000104	GPIO_CTRL_4 [60].SEL_GPIO[28:28]	1
0xBB000104	GPIO_CTRL_4 [61].SEL_GPIO[29:29]	1
0xBB000104	GPIO_CTRL_4 [62].SEL_GPIO[30:30]	1
0xBB000104	GPIO_CTRL_4 [63].SEL_GPIO[31:31]	1
0xBB000108	GPIO_CTRL_4 [64].SEL_GPIO[0:0]	1
0xBB000108	GPIO_CTRL_4 [65].SEL_GPIO[1:1]	1
0xBB000108	GPIO_CTRL_4 [66].SEL_GPIO[2:2]	1
0xBB000108	GPIO_CTRL_4 [67].SEL_GPIO[3:3]	1
0xBB000108	GPIO_CTRL_4 [68].SEL_GPIO[4:4]	1
0xBB000108	GPIO_CTRL_4 [69].SEL_GPIO[5:5]	1
0xBB000108	GPIO_CTRL_4 [70].SEL_GPIO[6:6]	1
0xBB000108	GPIO_CTRL_4 [71].SEL_GPIO[7:7]	1
0xBB00010C	RTL_OUI_CFG.RESERVED[31:24]	8
0xBB00010C	RTL_OUI_CFG.OUI_CFG[23:0]	24
0xBB000110	REVISION_CFG.RESERVED[31:4]	28
0xBB000110	REVISION_CFG.REVISIOIN_CFG[3:0]	4
0xBB000114	MODEL_CFG.RESERVED[31:6]	26
0xBB000114	MODEL_CFG.MODEL_CFG[5:0]	6
0xBB000118	WAKELPI_SLOT_PRD.RESERVED[31:5]	27
0xBB000118	WAKELPI_SLOT_PRD.WAKE_LPI_SLOT_PRD[4:0]	5
0xBB00011C	WAKELPI_SLOT [0].WAKELPI_SLOT_PORT[4:0]	5
0xBB00011C	WAKELPI_SLOT [1].WAKELPI_SLOT_PORT[9:5]	5
0xBB00011C	WAKELPI_SLOT [2].WAKELPI_SLOT_PORT[14:10]	5
0xBB00011C	WAKELPI_SLOT [3].WAKELPI_SLOT_PORT[19:15]	5
0xBB00011C	WAKELPI_SLOT [4].WAKELPI_SLOT_PORT[24:20]	5
0xBB000120	RGM_EEE.RESERVED[31:5]	27
0xBB000120	RGM_EEE.EXT_PAD_STOP_EN[4:4]	1
0xBB000120	RGM_EEE.EXT_CYCLE_PAD[3:0]	4
0xBB000124	ABLTY_FORCE_MODE.RESERVED[31:7]	25
0xBB000124	ABLTY_FORCE_MODE.ABLTY_FORCE_MODE[6:0]	7
0xBB000128	DEBUG_SEL.RESERVED[31:26]	6
0xBB000128	DEBUG_SEL.DBGEN_BY_REG[25:25]	1
0xBB000128	DEBUG_SEL.DBG_BY_SPI[24:24]	1
0xBB000128	DEBUG_SEL.DBG_BY_OEM[23:22]	2
0xBB000128	DEBUG_SEL.DBG_BY_SLIC[21:21]	1
0xBB000128	DEBUG_SEL.DBG_BY_EXT[20:20]	1
0xBB000128	DEBUG_SEL.CFG_DBGGO_SHIFT[19:16]	4
0xBB000128	DEBUG_SEL.DBGO_SEL[15:0]	16
0xBB00012C	RST_SYNC_FIFO.RESERVED[31:4]	28
0xBB00012C	RST_SYNC_FIFO.CFG_SYNC_FIFO_TX[3:3]	1
0xBB00012C	RST_SYNC_FIFO.CFG_SYNC_FIFO_RX[2:2]	1
0xBB00012C	RST_SYNC_FIFO.CFG_STOP_GLI_CLK_EN[1:1]	1
0xBB00012C	RST_SYNC_FIFO.CFG_STOP_CLK_PORT_EN[0:0]	1
0xBB000130	SDS_CFG.RESERVED[31:5]	27

Address	Register	Len
0xBB000130	SDS_CFG.CFG_SDS_MODE[4:0]	5
0xBB000134	MAC_ACT_CFG.RESERVED[31:17]	15
0xBB000134	MAC_ACT_CFG.CFG_MAC_ACTIVE[16:9]	8
0xBB000134	MAC_ACT_CFG.CFG_LINK_DOWN_TIME_EN[8:8]	1
0xBB000134	MAC_ACT_CFG.CFG_LINK_DOWN_TIME[7:0]	8
0xBB000138	BYPS_ABLTY_LOCK.RESERVED[31:7]	25
0xBB000138	BYPS_ABLTY_LOCK.BYPS_ABLTY_LOCK[6:0]	7
0xBB00013C	FIFO_ERR_STS.RESERVED[31:7]	25
0xBB00013C	FIFO_ERR_STS.STS_SYNC_FIFO_TX_ERR[6:6]	1
0xBB00013C	FIFO_ERR_STS.STS_SYNC_FIFO_RX_ERR[5:0]	6
0xBB000140	SDS_AN_RX_CFG.RESERVED[31:16]	16
0xBB000140	SDS_AN_RX_CFG.RX_CFG_REG_SDS[15:0]	16
0xBB000144	SDS_FIB_STATUS.RESERVED[31:17]	15
0xBB000144	SDS_FIB_STATUS.FIBER_ABLTY[16:5]	12
0xBB000144	SDS_FIB_STATUS.SDS_LINK_OK[4:4]	1
0xBB000144	SDS_FIB_STATUS.SDS_INTB[3:3]	1
0xBB000144	SDS_FIB_STATUS.SDS_ANFAULT[2:2]	1
0xBB000144	SDS_FIB_STATUS.FIB_ISO[1:1]	1
0xBB000144	SDS_FIB_STATUS.FIB100_DET[0:0]	1
0xBB000148	EXT_STS.RESERVED[31:16]	16
0xBB000148	EXT_STS.EXT_STS_EXTXF[15:0]	16
0xBB00014C	AFE_VER.RESERVED[31:1]	31
0xBB00014C	AFE_VER.AFE_VERSION[0:0]	1
0xBB000150	PON_MODE_CFG.RESERVED[31:2]	30
0xBB000150	PON_MODE_CFG.EPON_EN[1:1]	1
0xBB000150	PON_MODE_CFG.GPON_EN[0:0]	1
0xBB000154	ALL_PORT_LKDN_TIME.DUMMY[31:0]	32
0xBB000158	MODE_EXT.RESERVED[31:4]	28
0xBB000158	MODE_EXT.MODE_EXT[3:0]	4
0xBB00015C	GPHY_AFE_DBG_CFG.RESERVED[31:6]	26
0xBB00015C	GPHY_AFE_DBG_CFG.REG_ANA[5:2]	4
0xBB00015C	GPHY_AFE_DBG_CFG.EN_RTT2[1:1]	1
0xBB00015C	GPHY_AFE_DBG_CFG.EN_RTT1[0:0]	1
0xBB000160	AD5_CTRL.RESERVED[31:10]	22
0xBB000160	AD5_CTRL.ISET_AD5[9:7]	3
0xBB000160	AD5_CTRL.AVSET_AD5[6:4]	3
0xBB000160	AD5_CTRL.VICM_AD5[3:1]	3
0xBB000160	AD5_CTRL.VINSEL_AD5[0:0]	1
0xBB000164	PWM_CTRL1.RESERVED[31:14]	18
0xBB000164	PWM_CTRL1.BYPASS_PWM[13:13]	1
0xBB000164	PWM_CTRL1.ENC_S_PWM[12:12]	1
0xBB000164	PWM_CTRL1.ENSS_PWM[11:11]	1
0xBB000164	PWM_CTRL1.EN_PWM[10:10]	1
0xBB000164	PWM_CTRL1.FCK_PWM[9:7]	3
0xBB000164	PWM_CTRL1.IB20UTO5U_PWM[6:5]	2
0xBB000164	PWM_CTRL1.IOS_PWM[4:4]	1

Address	Register	Len
0xBB000164	PWM_CTRL1.LATCH_PWM[3:3]	1
0xBB000164	PWM_CTRL1.OCPT_PWM[2:0]	3
0xBB000168	PWM_CTRL2.RESERVED[31:30]	2
0xBB000168	PWM_CTRL2.OVPT_PWM[29:27]	3
0xBB000168	PWM_CTRL2.OOS_PWM[26:26]	1
0xBB000168	PWM_CTRL2.OSC_PWM[25:24]	2
0xBB000168	PWM_CTRL2.OVPWIN_PWM[23:22]	2
0xBB000168	PWM_CTRL2.PWM[21:21]	1
0xBB000168	PWM_CTRL2.SAWFREQ_PWM[20:17]	4
0xBB000168	PWM_CTRL2.SELOS_PWM[16:16]	1
0xBB000168	PWM_CTRL2.SSCLK_PWM[15:13]	3
0xBB000168	PWM_CTRL2.VCMOCP_PWM[12:10]	3
0xBB000168	PWM_CTRL2.VREF09_PWM[9:7]	3
0xBB000168	PWM_CTRL2.VREFOCP_PWM[6:3]	4
0xBB000168	PWM_CTRL2.VREFOVP_PWM[2:0]	3
0xBB00016C	TM_DLY.CMPDLY_TM[31:16]	16
0xBB00016C	TM_DLY.PONDLY_TM[15:0]	16
0xBB000170	TM_CTRL.RESERVED[31:18]	14
0xBB000170	TM_CTRL.ENABLE_TM[17:17]	1
0xBB000170	TM_CTRL.REVERSE_TM[16:16]	1
0xBB000170	TM_CTRL.SMPDLY_TM[15:0]	16
0xBB000174	TM_STS.RESERVED[31:7]	25
0xBB000174	TM_STS.DATAVLD_TM[6:6]	1
0xBB000174	TM_STS.DATAOUT_TM[5:0]	6
0xBB000178	AD5_ALARM.RESERVED[31:5]	27
0xBB000178	AD5_ALARM.AD5_ALARM_TH[4:0]	5
0xBB00017C	AD5_DATA.RESERVED[31:5]	27
0xBB00017C	AD5_DATA.AD5_DATAOUT[4:0]	5
0xBB000180	TM_ALARM.RESERVED[31:6]	26
0xBB000180	TM_ALARM.TM_ALARM_TH[5:0]	6
0xBB000184	CHIP_INF_SEL.RESERVED[31:2]	30
0xBB000184	CHIP_INF_SEL.PHY4_EN[1:1]	1
0xBB000188	SLIC_INSEL_CTRL.RESERVED[31:3]	29
0xBB000188	SLIC_INSEL_CTRL.SLIC_EN[2:2]	1
0xBB000188	SLIC_INSEL_CTRL.SLIC_INFSEL[1:0]	2
0xBB00018C	SYS_PKT_BUF_CTRL.RESERVED[31:1]	31
0xBB00018C	SYS_PKT_BUF_CTRL.PB_3M[0:0]	1
0xBB000190	DYNGASP_CTRL.RESERVED[31:12]	20
0xBB000190	DYNGASP_CTRL.DYNGASP_EN[11:11]	1
0xBB000190	DYNGASP_CTRL.DYNGASP_IDX[10:4]	7
0xBB000190	DYNGASP_CTRL.DYNGASP_CMP_INV[3:3]	1
0xBB000190	DYNGASP_CTRL.DYNGASP_OUT_INV[2:2]	1
0xBB000190	DYNGASP_CTRL.DYNGASP_OUT_EN[1:1]	1
0xBB000190	DYNGASP_CTRL.DYNGASP_OUT_PULL[0:0]	1
0xBB000194	BOND_STRAP_STS0.BOND_STRAP_STS0[31:0]	32
0xBB000198	BOND_STRAP_STS1.BOND_STRAP_STS1[31:0]	32

Address	Register	Len
0xBB00019C	BOND_STRAP_STS2.BOND_STRAP_STS2[31:0]	32
0xBB0001A0	MISCELLANEOUS_BONDING.IN_EXT_CLK_CLK_LX[31:31]	1
0xBB0001A0	MISCELLANEOUS_BONDING.IN_EXT_CLK_CLK_M90[30:30]	1
0xBB0001A0	MISCELLANEOUS_BONDING.IN_EXT_CLK_CLK_M[29:29]	1
0xBB0001A0	MISCELLANEOUS_BONDING.IN_EXT_CLK_OCP2[28:28]	1
0xBB0001A0	MISCELLANEOUS_BONDING.IN_EXT_CLK_OCP1[27:27]	1
0xBB0001A0	MISCELLANEOUS_BONDING.IN_EXT_CLK_SW[26:26]	1
0xBB0001A0	MISCELLANEOUS_BONDING.BOND_PHY_EN[25:25]	1
0xBB0001A0	MISCELLANEOUS_BONDING.BOND_DUMMY2[24:24]	1
0xBB0001A0	MISCELLANEOUS_BONDING.BOND_DUMMY1[23:23]	1
0xBB0001A0	MISCELLANEOUS_BONDING.BOND_DUMMY0[22:22]	1
0xBB0001A0	MISCELLANEOUS_BONDING.BOND_CKSELB[21:21]	1
0xBB0001A0	MISCELLANEOUS_BONDING.BOND_CKSEL_ENB[20:20]	1
0xBB0001A0	MISCELLANEOUS_BONDING.BOND_DDR_FREQ_DIV[19:18]	2
0xBB0001A0	MISCELLANEOUS_BONDING.BOND_DDR_PLL_FREQ[17:14]	4
0xBB0001A0	MISCELLANEOUS_BONDING.BOND_VOIP_MODE[13:12]	2
0xBB0001A0	MISCELLANEOUS_BONDING.BOND_AFE_POR_EN[11:11]	1
0xBB0001A0	MISCELLANEOUS_BONDING.EXT_CLK_LX[10:10]	1
0xBB0001A0	MISCELLANEOUS_BONDING.EXT_CLK_M90[9:9]	1
0xBB0001A0	MISCELLANEOUS_BONDING.EXT_CLK_M[8:8]	1
0xBB0001A0	MISCELLANEOUS_BONDING.EXT_CLK_OCP2[7:7]	1
0xBB0001A0	MISCELLANEOUS_BONDING.EXT_CLK_OCP1[6:6]	1
0xBB0001A0	MISCELLANEOUS_BONDING.EXT_CLK_SW[5:5]	1
0xBB0001A0	MISCELLANEOUS_BONDING.PAD_BOND_BISR_REMAP_EN[4:4]	1
0xBB0001A0	MISCELLANEOUS_BONDING.PAD_BOND_NFBI_ENB[3:3]	1
0xBB0001A0	MISCELLANEOUS_BONDING.PAD_BOND_NF_MUX_SEL[2:2]	1
0xBB0001A0	MISCELLANEOUS_BONDING.PAD_BOND_TEST_EN[1:1]	1
0xBB0001A0	MISCELLANEOUS_BONDING.PAD_DBG_EN[0:0]	1
0xBB0001A4	MISCELLANEOUS_STRAPPING1.RESERVED[31:6]	26
0xBB0001A4	MISCELLANEOUS_STRAPPING1.BOND_PON_BIST_EN[5:5]	1
0xBB0001A4	MISCELLANEOUS_STRAPPING1.BOND_EFUSE_ENB[4:4]	1
0xBB0001A4	MISCELLANEOUS_STRAPPING1.BOND_NAT_ENB[3:3]	1
0xBB0001A4	MISCELLANEOUS_STRAPPING1.BOND_PON_SEL[2:1]	2
0xBB0001A4	MISCELLANEOUS_STRAPPING1.BOND_PON_TAB_INIT_EN[0:0]	1
0xBB0001A8	MISCELLANEOUS_STRAPPING0.RESERVED[31:12]	20
0xBB0001A8	MISCELLANEOUS_STRAPPING0.EN_SMI_SLAVE[11:11]	1
0xBB0001A8	MISCELLANEOUS_STRAPPING0.SYS_CLK_SEL[10:10]	1
0xBB0001A8	MISCELLANEOUS_STRAPPING0.DIS_JTAG[9:9]	1
0xBB0001A8	MISCELLANEOUS_STRAPPING0.SPIF4BEN[8:8]	1
0xBB0001A8	MISCELLANEOUS_STRAPPING0.NAFC_RC[7:7]	1
0xBB0001A8	MISCELLANEOUS_STRAPPING0.NAF_AC1[6:6]	1
0xBB0001A8	MISCELLANEOUS_STRAPPING0.NAF_AC0[5:5]	1
0xBB0001A8	MISCELLANEOUS_STRAPPING0.BTUP_TYP1[4:4]	1
0xBB0001A8	MISCELLANEOUS_STRAPPING0.BTUP_TYP0[3:3]	1
0xBB0001A8	MISCELLANEOUS_STRAPPING0.DRAM_TYP1[2:2]	1
0xBB0001A8	MISCELLANEOUS_STRAPPING0.DRAM_TYP0[1:1]	1

Address	Register	Len
0xBB0001A8	MISCELLANEOUS_STRAPPING0.EN_CPU[0:0]	1
0xBB0001AC	MAC_DLYLNK.RESERVED[31:6]	26
0xBB0001AC	MAC_DLYLNK.MACRX_DUPDET_EN[5:5]	1
0xBB0001AC	MAC_DLYLNK.MAC_LNKUP_DELAY_EN[4:4]	1
0xBB0001AC	MAC_DLYLNK.GE_100M_LNKUP_DELAY[3:2]	2
0xBB0001AC	MAC_DLYLNK.LNKUP_10M_DELAY[1:0]	2
0xBB0001B0	PLL_RGM_CTRL1.RESERVED[31:28]	4
0xBB0001B0	PLL_RGM_CTRL1.PLL_RGM_PSEN[27:27]	1
0xBB0001B0	PLL_RGM_CTRL1.PLL_RGM_OEB[26:26]	1
0xBB0001B0	PLL_RGM_CTRL1.PLL_RGM_FUPDN[25:25]	1
0xBB0001B0	PLL_RGM_CTRL1.PLL_RGM_PWRDN[24:24]	1
0xBB0001B0	PLL_RGM_CTRL1.PLL_RGM_SSC_TMODE[23:22]	2
0xBB0001B0	PLL_RGM_CTRL1.PLL_RGM_SSC_OFFS[21:14]	8
0xBB0001B0	PLL_RGM_CTRL1.PLL_RGM_SSC_STEP[13:8]	6
0xBB0001B0	PLL_RGM_CTRL1.PLL_RGM_SSC_PERIOD[7:1]	7
0xBB0001B0	PLL_RGM_CTRL1.PLL_RGM_SSC_EN[0:0]	1
0xBB0001B4	PLL_RGM_CTRL2.PLL_RGM_PI_COMP_DLY_L[31:31]	1
0xBB0001B4	PLL_RGM_CTRL2.PLL_RGM_PI_BIAS[30:29]	2
0xBB0001B4	PLL_RGM_CTRL2.PLL_RGM_PI_RS[28:27]	2
0xBB0001B4	PLL_RGM_CTRL2.PLL_RGM_PI_RL[26:25]	2
0xBB0001B4	PLL_RGM_CTRL2.PLL_RGM_PSTST[24:24]	1
0xBB0001B4	PLL_RGM_CTRL2.PLL_RGM_C3[23:22]	2
0xBB0001B4	PLL_RGM_CTRL2.PLL_RGM_R3[21:19]	3
0xBB0001B4	PLL_RGM_CTRL2.PLL_RGM_CP[18:17]	2
0xBB0001B4	PLL_RGM_CTRL2.PLL_RGM_CS[16:15]	2
0xBB0001B4	PLL_RGM_CTRL2.PLL_RGM_RS[14:12]	3
0xBB0001B4	PLL_RGM_CTRL2.PLL_RGM_IP[11:9]	3
0xBB0001B4	PLL_RGM_CTRL2.PLL_RGM_DIV[8:2]	7
0xBB0001B4	PLL_RGM_CTRL2.PLL_RGM_LDO[1:0]	2
0xBB0001B8	PLL_RGM_CTRL3.RESERVED[31:24]	8
0xBB0001B8	PLL_RGM_CTRL3.PLL_RGM_RSVD[23:18]	6
0xBB0001B8	PLL_RGM_CTRL3.PLL_RGM_WDMODE[17:16]	2
0xBB0001B8	PLL_RGM_CTRL3.PLL_RGM_EN_PI16[15:15]	1
0xBB0001B8	PLL_RGM_CTRL3.PLL_RGM_PI16_BIAS[14:13]	2
0xBB0001B8	PLL_RGM_CTRL3.PLL_RGM_PI16_RS[12:11]	2
0xBB0001B8	PLL_RGM_CTRL3.PLL_RGM_PI16_RL[10:9]	2
0xBB0001B8	PLL_RGM_CTRL3.PLL_RGM_REG_CK0[8:5]	4
0xBB0001B8	PLL_RGM_CTRL3.PLL_RGM_PHS_H[4:1]	4
0xBB0001B8	PLL_RGM_CTRL3.PLL_RGM_PI_COMP_DLY_H[0:0]	1
0xBB0001BC	UTP_FIBER_AUTODET.RESERVED[31:9]	23
0xBB0001BC	UTP_FIBER_AUTODET.PHY4_SDET[8:8]	1
0xBB0001BC	UTP_FIBER_AUTODET.FIB_SDET[7:7]	1
0xBB0001BC	UTP_FIBER_AUTODET.PHY4_DIS_RX[6:6]	1
0xBB0001BC	UTP_FIBER_AUTODET.PHY4_FRC_LKDN[5:5]	1
0xBB0001BC	UTP_FIBER_AUTODET.SDS_PWR_GATING[4:4]	1
0xBB0001BC	UTP_FIBER_AUTODET.SDS_RX_DISABLE[3:3]	1

Address	Register	Len
0xBB0001BC	UTP_FIBER_AUTODET.SDS_TX_DISABLE[2:2]	1
0xBB0001BC	UTP_FIBER_AUTODET.SDS_FRC_LD[1:1]	1
0xBB0001BC	UTP_FIBER_AUTODET.CKGPHY_SEL[0:0]	1
0xBB0001C0	EEE_TX_SEL_CTRL.DUMMY[31:0]	32
0xBB0001C4	SW_PWRSABV_CTRL.RESERVED[31:19]	13
0xBB0001C4	SW_PWRSABV_CTRL.SLOW_DOWN_PLL_EN[18:18]	1
0xBB0001C4	SW_PWRSABV_CTRL.SLOW_DOWN_CLK_EN[17:17]	1
0xBB0001C4	SW_PWRSABV_CTRL.FRC_MAC_ACTIVE[16:16]	1
0xBB0001C4	SW_PWRSABV_CTRL.SLOW_CLK_TGL_RATE[15:12]	4
0xBB0001C4	SW_PWRSABV_CTRL.GPHY_MDX_MDC_DIV[11:2]	10
0xBB0001C4	SW_PWRSABV_CTRL.WAIT_FOR_AGREEMENT[1:1]	1
0xBB0001C4	SW_PWRSABV_CTRL.AGREE_SLEEP[0:0]	1
0xBB0001C8	DBG_BLK_SEL.RESERVED[31:16]	16
0xBB0001C8	DBG_BLK_SEL.DBG_BLK_SEL[15:0]	16
0xBB0001CC	RGF_VER_GLB_CTRL.REGFILE_VER[31:0]	32
0xBB0001D0	RSVD_GLB_CTRL [0].RSVD_MEM[31:0]	32
0xBB0001D4	RSVD_GLB_CTRL [1].RSVD_MEM[31:0]	32
0xBB0001D8	RSVD_GLB_CTRL [2].RSVD_MEM[31:0]	32
0xBB0001DC	RSVD_GLB_CTRL [3].RSVD_MEM[31:0]	32
0xBB0001E0	RSVD_GLB_CTRL [4].RSVD_MEM[31:0]	32
0xBB0001E4	RSVD_GLB_CTRL [5].RSVD_MEM[31:0]	32
0xBB0001E8	RSVD_GLB_CTRL [6].RSVD_MEM[31:0]	32
0xBB0001EC	RSVD_GLB_CTRL [7].RSVD_MEM[31:0]	32
0xBB0001F0	RSVD_GLB_CTRL [8].RSVD_MEM[31:0]	32
0xBB0001F4	RSVD_GLB_CTRL [9].RSVD_MEM[31:0]	32
0xBB0001F8	RSVD_GLB_CTRL [10].RSVD_MEM[31:0]	32
0xBB0001FC	RSVD_GLB_CTRL [11].RSVD_MEM[31:0]	32
0xBB000200	RSVD_GLB_CTRL [12].RSVD_MEM[31:0]	32
0xBB000204	RSVD_GLB_CTRL [13].RSVD_MEM[31:0]	32
0xBB000208	RSVD_GLB_CTRL [14].RSVD_MEM[31:0]	32
0xBB00020C	RSVD_GLB_CTRL [15].RSVD_MEM[31:0]	32
0xBB010000	MODEL_NAME_INFO.RTL_ID[31:16]	16
0xBB010000	MODEL_NAME_INFO.MODEL_CHAR_1ST[15:11]	5
0xBB010000	MODEL_NAME_INFO.MODEL_CHAR_2ND[10:6]	5
0xBB010000	MODEL_NAME_INFO.MODEL_CHAR_3RD[5:1]	5
0xBB010000	MODEL_NAME_INFO.RESERVED[0:0]	1
0xBB010004	CHIP_INFO.CHIP_INFO_EN[31:28]	4
0xBB010004	CHIP_INFO.RESERVED[27:21]	7
0xBB010004	CHIP_INFO.CHIP_VER[20:16]	5
0xBB010004	CHIP_INFO.RL_ID[15:0]	16
0xBB010008	BOND_INFO.BOND_INFO_EN[31:28]	4
0xBB010008	BOND_INFO.RESERVED[27:5]	23
0xBB010008	BOND_INFO.BOND_CHIP_MODE[4:0]	5
0xBB011000	FORCE_P_DMP [0].FORCE_PROT_MASK[6:0]	7
0xBB011000	FORCE_P_DMP [1].FORCE_PROT_MASK[13:7]	7
0xBB011000	FORCE_P_DMP [2].FORCE_PROT_MASK[20:14]	7

Address	Register	Len
0xBB011000	FORCE_P_DMP [3].FORCE_PROT_MASK[27:21]	7
0xBB011004	FORCE_P_DMP [4].FORCE_PROT_MASK[6:0]	7
0xBB011004	FORCE_P_DMP [5].FORCE_PROT_MASK[13:7]	7
0xBB011004	FORCE_P_DMP [6].FORCE_PROT_MASK[20:14]	7
0xBB011008	EN_FORCE_P_DMP.RESERVED[31:1]	31
0xBB011008	EN_FORCE_P_DMP.FORCE_MODE[0:0]	1
0xBB01100C	ACCEPT_MAX_LEN_CTRL [0].RESERVED[31:2]	30
0xBB01100C	ACCEPT_MAX_LEN_CTRL [0].MAX_LENGTH_GIGA[1:1]	1
0xBB01100C	ACCEPT_MAX_LEN_CTRL [0].MAX_LENGTH_10_100[0:0]	1
0xBB011010	ACCEPT_MAX_LEN_CTRL [1].RESERVED[31:2]	30
0xBB011010	ACCEPT_MAX_LEN_CTRL [1].MAX_LENGTH_GIGA[1:1]	1
0xBB011010	ACCEPT_MAX_LEN_CTRL [1].MAX_LENGTH_10_100[0:0]	1
0xBB011014	ACCEPT_MAX_LEN_CTRL [2].RESERVED[31:2]	30
0xBB011014	ACCEPT_MAX_LEN_CTRL [2].MAX_LENGTH_GIGA[1:1]	1
0xBB011014	ACCEPT_MAX_LEN_CTRL [2].MAX_LENGTH_10_100[0:0]	1
0xBB011018	ACCEPT_MAX_LEN_CTRL [3].RESERVED[31:2]	30
0xBB011018	ACCEPT_MAX_LEN_CTRL [3].MAX_LENGTH_GIGA[1:1]	1
0xBB011018	ACCEPT_MAX_LEN_CTRL [3].MAX_LENGTH_10_100[0:0]	1
0xBB01101C	ACCEPT_MAX_LEN_CTRL [4].RESERVED[31:2]	30
0xBB01101C	ACCEPT_MAX_LEN_CTRL [4].MAX_LENGTH_GIGA[1:1]	1
0xBB01101C	ACCEPT_MAX_LEN_CTRL [4].MAX_LENGTH_10_100[0:0]	1
0xBB011020	ACCEPT_MAX_LEN_CTRL [5].RESERVED[31:2]	30
0xBB011020	ACCEPT_MAX_LEN_CTRL [5].MAX_LENGTH_GIGA[1:1]	1
0xBB011020	ACCEPT_MAX_LEN_CTRL [5].MAX_LENGTH_10_100[0:0]	1
0xBB011024	ACCEPT_MAX_LEN_CTRL [6].RESERVED[31:2]	30
0xBB011024	ACCEPT_MAX_LEN_CTRL [6].MAX_LENGTH_GIGA[1:1]	1
0xBB011024	ACCEPT_MAX_LEN_CTRL [6].MAX_LENGTH_10_100[0:0]	1
0xBB011028	MAX_LENGTH_CFG1.RESERVED[31:14]	18
0xBB011028	MAX_LENGTH_CFG1.ACCEPT_MAX_LENTH_CFG1[13:0]	14
0xBB01102C	RMK_DSCP_CTRL [0].INTPRI_DSCP[5:0]	6
0xBB01102C	RMK_DSCP_CTRL [1].INTPRI_DSCP[11:6]	6
0xBB01102C	RMK_DSCP_CTRL [2].INTPRI_DSCP[17:12]	6
0xBB01102C	RMK_DSCP_CTRL [3].INTPRI_DSCP[23:18]	6
0xBB01102C	RMK_DSCP_CTRL [4].INTPRI_DSCP[29:24]	6
0xBB011030	RMK_DSCP_CTRL [5].INTPRI_DSCP[5:0]	6
0xBB011030	RMK_DSCP_CTRL [6].INTPRI_DSCP[11:6]	6
0xBB011030	RMK_DSCP_CTRL [7].INTPRI_DSCP[17:12]	6
0xBB011030	RMK_DSCP_CTRL [8].INTPRI_DSCP[23:18]	6
0xBB011030	RMK_DSCP_CTRL [9].INTPRI_DSCP[29:24]	6
0xBB011034	RMK_DSCP_CTRL [10].INTPRI_DSCP[5:0]	6
0xBB011034	RMK_DSCP_CTRL [11].INTPRI_DSCP[11:6]	6
0xBB011034	RMK_DSCP_CTRL [12].INTPRI_DSCP[17:12]	6
0xBB011034	RMK_DSCP_CTRL [13].INTPRI_DSCP[23:18]	6
0xBB011034	RMK_DSCP_CTRL [14].INTPRI_DSCP[29:24]	6
0xBB011038	RMK_DSCP_CTRL [15].INTPRI_DSCP[5:0]	6
0xBB011038	RMK_DSCP_CTRL [16].INTPRI_DSCP[11:6]	6



Address	Register	Len
0xBB011038	RMK_DSCP_CTRL [17].INTPRI_DSCP[17:12]	6
0xBB011038	RMK_DSCP_CTRL [18].INTPRI_DSCP[23:18]	6
0xBB011038	RMK_DSCP_CTRL [19].INTPRI_DSCP[29:24]	6
0xBB01103C	RMK_DSCP_CTRL [20].INTPRI_DSCP[5:0]	6
0xBB01103C	RMK_DSCP_CTRL [21].INTPRI_DSCP[11:6]	6
0xBB01103C	RMK_DSCP_CTRL [22].INTPRI_DSCP[17:12]	6
0xBB01103C	RMK_DSCP_CTRL [23].INTPRI_DSCP[23:18]	6
0xBB01103C	RMK_DSCP_CTRL [24].INTPRI_DSCP[29:24]	6
0xBB011040	RMK_DSCP_CTRL [25].INTPRI_DSCP[5:0]	6
0xBB011040	RMK_DSCP_CTRL [26].INTPRI_DSCP[11:6]	6
0xBB011040	RMK_DSCP_CTRL [27].INTPRI_DSCP[17:12]	6
0xBB011040	RMK_DSCP_CTRL [28].INTPRI_DSCP[23:18]	6
0xBB011040	RMK_DSCP_CTRL [29].INTPRI_DSCP[29:24]	6
0xBB011044	RMK_DSCP_CTRL [30].INTPRI_DSCP[5:0]	6
0xBB011044	RMK_DSCP_CTRL [31].INTPRI_DSCP[11:6]	6
0xBB011044	RMK_DSCP_CTRL [32].INTPRI_DSCP[17:12]	6
0xBB011044	RMK_DSCP_CTRL [33].INTPRI_DSCP[23:18]	6
0xBB011044	RMK_DSCP_CTRL [34].INTPRI_DSCP[29:24]	6
0xBB011048	RMK_DSCP_CTRL [35].INTPRI_DSCP[5:0]	6
0xBB011048	RMK_DSCP_CTRL [36].INTPRI_DSCP[11:6]	6
0xBB011048	RMK_DSCP_CTRL [37].INTPRI_DSCP[17:12]	6
0xBB011048	RMK_DSCP_CTRL [38].INTPRI_DSCP[23:18]	6
0xBB011048	RMK_DSCP_CTRL [39].INTPRI_DSCP[29:24]	6
0xBB01104C	RMK_DSCP_CTRL [40].INTPRI_DSCP[5:0]	6
0xBB01104C	RMK_DSCP_CTRL [41].INTPRI_DSCP[11:6]	6
0xBB01104C	RMK_DSCP_CTRL [42].INTPRI_DSCP[17:12]	6
0xBB01104C	RMK_DSCP_CTRL [43].INTPRI_DSCP[23:18]	6
0xBB01104C	RMK_DSCP_CTRL [44].INTPRI_DSCP[29:24]	6
0xBB011050	RMK_DSCP_CTRL [45].INTPRI_DSCP[5:0]	6
0xBB011050	RMK_DSCP_CTRL [46].INTPRI_DSCP[11:6]	6
0xBB011050	RMK_DSCP_CTRL [47].INTPRI_DSCP[17:12]	6
0xBB011050	RMK_DSCP_CTRL [48].INTPRI_DSCP[23:18]	6
0xBB011050	RMK_DSCP_CTRL [49].INTPRI_DSCP[29:24]	6
0xBB011054	RMK_DSCP_CTRL [50].INTPRI_DSCP[5:0]	6
0xBB011054	RMK_DSCP_CTRL [51].INTPRI_DSCP[11:6]	6
0xBB011054	RMK_DSCP_CTRL [52].INTPRI_DSCP[17:12]	6
0xBB011054	RMK_DSCP_CTRL [53].INTPRI_DSCP[23:18]	6
0xBB011054	RMK_DSCP_CTRL [54].INTPRI_DSCP[29:24]	6
0xBB011058	RMK_DSCP_CTRL [55].INTPRI_DSCP[5:0]	6
0xBB011058	RMK_DSCP_CTRL [56].INTPRI_DSCP[11:6]	6
0xBB011058	RMK_DSCP_CTRL [57].INTPRI_DSCP[17:12]	6
0xBB011058	RMK_DSCP_CTRL [58].INTPRI_DSCP[23:18]	6
0xBB011058	RMK_DSCP_CTRL [59].INTPRI_DSCP[29:24]	6
0xBB01105C	RMK_DSCP_CTRL [60].INTPRI_DSCP[5:0]	6
0xBB01105C	RMK_DSCP_CTRL [61].INTPRI_DSCP[11:6]	6
0xBB01105C	RMK_DSCP_CTRL [62].INTPRI_DSCP[17:12]	6



Address	Register	Len
0xBB01105C	RMK_DSCP_CTRL [63].INTPRI_DSCP[23:18]	6
0xBB011060	RMK_DSCP_INT_PRI_CTRL [0].INTPRI_DSCP[5:0]	6
0xBB011060	RMK_DSCP_INT_PRI_CTRL [1].INTPRI_DSCP[11:6]	6
0xBB011060	RMK_DSCP_INT_PRI_CTRL [2].INTPRI_DSCP[17:12]	6
0xBB011060	RMK_DSCP_INT_PRI_CTRL [3].INTPRI_DSCP[23:18]	6
0xBB011060	RMK_DSCP_INT_PRI_CTRL [4].INTPRI_DSCP[29:24]	6
0xBB011064	RMK_DSCP_INT_PRI_CTRL [5].INTPRI_DSCP[5:0]	6
0xBB011064	RMK_DSCP_INT_PRI_CTRL [6].INTPRI_DSCP[11:6]	6
0xBB011064	RMK_DSCP_INT_PRI_CTRL [7].INTPRI_DSCP[17:12]	6
0xBB011068	OUTPUT_DROP_CFG.RESERVED[31:3]	29
0xBB011068	OUTPUT_DROP_CFG.OD_BC_SEL[2:2]	1
0xBB011068	OUTPUT_DROP_CFG.OD_MC_SEL[1:1]	1
0xBB011068	OUTPUT_DROP_CFG.OD_UC_SEL[0:0]	1
0xBB01106C	OUTPUT_DROP_EN [0].EN[0:0]	1
0xBB01106C	OUTPUT_DROP_EN [1].EN[1:1]	1
0xBB01106C	OUTPUT_DROP_EN [2].EN[2:2]	1
0xBB01106C	OUTPUT_DROP_EN [3].EN[3:3]	1
0xBB01106C	OUTPUT_DROP_EN [4].EN[4:4]	1
0xBB01106C	OUTPUT_DROP_EN [5].EN[5:5]	1
0xBB01106C	OUTPUT_DROP_EN [6].EN[6:6]	1
0xBB011070	IGMP_GLB_CTRL.RESERVED[31:8]	24
0xBB011070	IGMP_GLB_CTRL.TRAP_PRIORITY[7:5]	3
0xBB011070	IGMP_GLB_CTRL.PISO_LEAKY[4:4]	1
0xBB011070	IGMP_GLB_CTRL.VLAN_LEAKY[3:3]	1
0xBB011070	IGMP_GLB_CTRL.DISC_STORM_FILTER[2:2]	1
0xBB011070	IGMP_GLB_CTRL.CKS_ERR_OP[1:0]	2
0xBB011074	IGMP_P_CTRL [0].RESERVED[31:11]	21
0xBB011074	IGMP_P_CTRL [0].ALLOW_MC_DATA[10:10]	1
0xBB011074	IGMP_P_CTRL [0].MLDV2_OP[9:8]	2
0xBB011074	IGMP_P_CTRL [0].MLDV1_OP[7:6]	2
0xBB011074	IGMP_P_CTRL [0].IGMPV3_OP[5:4]	2
0xBB011074	IGMP_P_CTRL [0].IGMPV2_OP[3:2]	2
0xBB011074	IGMP_P_CTRL [0].IGMPV1_OP[1:0]	2
0xBB011078	IGMP_P_CTRL [1].RESERVED[31:11]	21
0xBB011078	IGMP_P_CTRL [1].ALLOW_MC_DATA[10:10]	1
0xBB011078	IGMP_P_CTRL [1].MLDV2_OP[9:8]	2
0xBB011078	IGMP_P_CTRL [1].MLDV1_OP[7:6]	2
0xBB011078	IGMP_P_CTRL [1].IGMPV3_OP[5:4]	2
0xBB011078	IGMP_P_CTRL [1].IGMPV2_OP[3:2]	2
0xBB011078	IGMP_P_CTRL [1].IGMPV1_OP[1:0]	2
0xBB01107C	IGMP_P_CTRL [2].RESERVED[31:11]	21
0xBB01107C	IGMP_P_CTRL [2].ALLOW_MC_DATA[10:10]	1
0xBB01107C	IGMP_P_CTRL [2].MLDV2_OP[9:8]	2
0xBB01107C	IGMP_P_CTRL [2].MLDV1_OP[7:6]	2
0xBB01107C	IGMP_P_CTRL [2].IGMPV3_OP[5:4]	2
0xBB01107C	IGMP_P_CTRL [2].IGMPV2_OP[3:2]	2

Address	Register	Len
0xBB01107C	IGMP_P_CTRL [2].IGMPV1_OP[1:0]	2
0xBB011080	IGMP_P_CTRL [3].RESERVED[31:11]	21
0xBB011080	IGMP_P_CTRL [3].ALLOW_MC_DATA[10:10]	1
0xBB011080	IGMP_P_CTRL [3].MLDV2_OP[9:8]	2
0xBB011080	IGMP_P_CTRL [3].MLDV1_OP[7:6]	2
0xBB011080	IGMP_P_CTRL [3].IGMPV3_OP[5:4]	2
0xBB011080	IGMP_P_CTRL [3].IGMPV2_OP[3:2]	2
0xBB011080	IGMP_P_CTRL [3].IGMPV1_OP[1:0]	2
0xBB011084	IGMP_P_CTRL [4].RESERVED[31:11]	21
0xBB011084	IGMP_P_CTRL [4].ALLOW_MC_DATA[10:10]	1
0xBB011084	IGMP_P_CTRL [4].MLDV2_OP[9:8]	2
0xBB011084	IGMP_P_CTRL [4].MLDV1_OP[7:6]	2
0xBB011084	IGMP_P_CTRL [4].IGMPV3_OP[5:4]	2
0xBB011084	IGMP_P_CTRL [4].IGMPV2_OP[3:2]	2
0xBB011084	IGMP_P_CTRL [4].IGMPV1_OP[1:0]	2
0xBB011088	IGMP_P_CTRL [5].RESERVED[31:11]	21
0xBB011088	IGMP_P_CTRL [5].ALLOW_MC_DATA[10:10]	1
0xBB011088	IGMP_P_CTRL [5].MLDV2_OP[9:8]	2
0xBB011088	IGMP_P_CTRL [5].MLDV1_OP[7:6]	2
0xBB011088	IGMP_P_CTRL [5].IGMPV3_OP[5:4]	2
0xBB011088	IGMP_P_CTRL [5].IGMPV2_OP[3:2]	2
0xBB011088	IGMP_P_CTRL [5].IGMPV1_OP[1:0]	2
0xBB01108C	IGMP_P_CTRL [6].RESERVED[31:11]	21
0xBB01108C	IGMP_P_CTRL [6].ALLOW_MC_DATA[10:10]	1
0xBB01108C	IGMP_P_CTRL [6].MLDV2_OP[9:8]	2
0xBB01108C	IGMP_P_CTRL [6].MLDV1_OP[7:6]	2
0xBB01108C	IGMP_P_CTRL [6].IGMPV3_OP[5:4]	2
0xBB01108C	IGMP_P_CTRL [6].IGMPV2_OP[3:2]	2
0xBB01108C	IGMP_P_CTRL [6].IGMPV1_OP[1:0]	2
0xBB011090	L34_GLB_CFG.RESERVED[31:3]	29
0xBB011090	L34_GLB_CFG.L34_L2_LOOKUP_MISS_ACT[2:2]	1
0xBB011090	L34_GLB_CFG.RESERVED[1:1]	1
0xBB011090	L34_GLB_CFG.L34_GLOBAL_CFG[0:0]	1
0xBB011094	L34_PORT_TO_WAN [0][0].PORT_TO_WAN_PERMIT[0:0]	1
0xBB011094	L34_PORT_TO_WAN [0][1].PORT_TO_WAN_PERMIT[1:1]	1
0xBB011094	L34_PORT_TO_WAN [0][2].PORT_TO_WAN_PERMIT[2:2]	1
0xBB011094	L34_PORT_TO_WAN [0][3].PORT_TO_WAN_PERMIT[3:3]	1
0xBB011094	L34_PORT_TO_WAN [0][4].PORT_TO_WAN_PERMIT[4:4]	1
0xBB011094	L34_PORT_TO_WAN [0][5].PORT_TO_WAN_PERMIT[5:5]	1
0xBB011094	L34_PORT_TO_WAN [0][6].PORT_TO_WAN_PERMIT[6:6]	1
0xBB011094	L34_PORT_TO_WAN [0][7].PORT_TO_WAN_PERMIT[7:7]	1
0xBB011098	L34_PORT_TO_WAN [1][0].PORT_TO_WAN_PERMIT[0:0]	1
0xBB011098	L34_PORT_TO_WAN [1][1].PORT_TO_WAN_PERMIT[1:1]	1
0xBB011098	L34_PORT_TO_WAN [1][2].PORT_TO_WAN_PERMIT[2:2]	1
0xBB011098	L34_PORT_TO_WAN [1][3].PORT_TO_WAN_PERMIT[3:3]	1
0xBB011098	L34_PORT_TO_WAN [1][4].PORT_TO_WAN_PERMIT[4:4]	1

Address	Register	Len
0xBB011098	L34_PORT_TO_WAN [1][5].PORT_TO_WAN_PERMIT[5:5]	1
0xBB011098	L34_PORT_TO_WAN [1][6].PORT_TO_WAN_PERMIT[6:6]	1
0xBB011098	L34_PORT_TO_WAN [1][7].PORT_TO_WAN_PERMIT[7:7]	1
0xBB01109C	L34_PORT_TO_WAN [2][0].PORT_TO_WAN_PERMIT[0:0]	1
0xBB01109C	L34_PORT_TO_WAN [2][1].PORT_TO_WAN_PERMIT[1:1]	1
0xBB01109C	L34_PORT_TO_WAN [2][2].PORT_TO_WAN_PERMIT[2:2]	1
0xBB01109C	L34_PORT_TO_WAN [2][3].PORT_TO_WAN_PERMIT[3:3]	1
0xBB01109C	L34_PORT_TO_WAN [2][4].PORT_TO_WAN_PERMIT[4:4]	1
0xBB01109C	L34_PORT_TO_WAN [2][5].PORT_TO_WAN_PERMIT[5:5]	1
0xBB01109C	L34_PORT_TO_WAN [2][6].PORT_TO_WAN_PERMIT[6:6]	1
0xBB01109C	L34_PORT_TO_WAN [2][7].PORT_TO_WAN_PERMIT[7:7]	1
0xBB0110A0	L34_PORT_TO_WAN [3][0].PORT_TO_WAN_PERMIT[0:0]	1
0xBB0110A0	L34_PORT_TO_WAN [3][1].PORT_TO_WAN_PERMIT[1:1]	1
0xBB0110A0	L34_PORT_TO_WAN [3][2].PORT_TO_WAN_PERMIT[2:2]	1
0xBB0110A0	L34_PORT_TO_WAN [3][3].PORT_TO_WAN_PERMIT[3:3]	1
0xBB0110A0	L34_PORT_TO_WAN [3][4].PORT_TO_WAN_PERMIT[4:4]	1
0xBB0110A0	L34_PORT_TO_WAN [3][5].PORT_TO_WAN_PERMIT[5:5]	1
0xBB0110A0	L34_PORT_TO_WAN [3][6].PORT_TO_WAN_PERMIT[6:6]	1
0xBB0110A0	L34_PORT_TO_WAN [3][7].PORT_TO_WAN_PERMIT[7:7]	1
0xBB0110A4	L34_PORT_TO_WAN [4][0].PORT_TO_WAN_PERMIT[0:0]	1
0xBB0110A4	L34_PORT_TO_WAN [4][1].PORT_TO_WAN_PERMIT[1:1]	1
0xBB0110A4	L34_PORT_TO_WAN [4][2].PORT_TO_WAN_PERMIT[2:2]	1
0xBB0110A4	L34_PORT_TO_WAN [4][3].PORT_TO_WAN_PERMIT[3:3]	1
0xBB0110A4	L34_PORT_TO_WAN [4][4].PORT_TO_WAN_PERMIT[4:4]	1
0xBB0110A4	L34_PORT_TO_WAN [4][5].PORT_TO_WAN_PERMIT[5:5]	1
0xBB0110A4	L34_PORT_TO_WAN [4][6].PORT_TO_WAN_PERMIT[6:6]	1
0xBB0110A4	L34_PORT_TO_WAN [4][7].PORT_TO_WAN_PERMIT[7:7]	1
0xBB0110A8	L34_PORT_TO_WAN [5][0].PORT_TO_WAN_PERMIT[0:0]	1
0xBB0110A8	L34_PORT_TO_WAN [5][1].PORT_TO_WAN_PERMIT[1:1]	1
0xBB0110A8	L34_PORT_TO_WAN [5][2].PORT_TO_WAN_PERMIT[2:2]	1
0xBB0110A8	L34_PORT_TO_WAN [5][3].PORT_TO_WAN_PERMIT[3:3]	1
0xBB0110A8	L34_PORT_TO_WAN [5][4].PORT_TO_WAN_PERMIT[4:4]	1
0xBB0110A8	L34_PORT_TO_WAN [5][5].PORT_TO_WAN_PERMIT[5:5]	1
0xBB0110A8	L34_PORT_TO_WAN [5][6].PORT_TO_WAN_PERMIT[6:6]	1
0xBB0110A8	L34_PORT_TO_WAN [5][7].PORT_TO_WAN_PERMIT[7:7]	1
0xBB0110AC	L34_PORT_TO_WAN [6][0].PORT_TO_WAN_PERMIT[0:0]	1
0xBB0110AC	L34_PORT_TO_WAN [6][1].PORT_TO_WAN_PERMIT[1:1]	1
0xBB0110AC	L34_PORT_TO_WAN [6][2].PORT_TO_WAN_PERMIT[2:2]	1
0xBB0110AC	L34_PORT_TO_WAN [6][3].PORT_TO_WAN_PERMIT[3:3]	1
0xBB0110AC	L34_PORT_TO_WAN [6][4].PORT_TO_WAN_PERMIT[4:4]	1
0xBB0110AC	L34_PORT_TO_WAN [6][5].PORT_TO_WAN_PERMIT[5:5]	1
0xBB0110AC	L34_PORT_TO_WAN [6][6].PORT_TO_WAN_PERMIT[6:6]	1
0xBB0110AC	L34_PORT_TO_WAN [6][7].PORT_TO_WAN_PERMIT[7:7]	1
0xBB0110B0	L34_EXTPORT_TO_WAN [0][0].EXTPORT_TO_WAN_PERMIT[0:0]	1
0xBB0110B0	L34_EXTPORT_TO_WAN [0][1].EXTPORT_TO_WAN_PERMIT[1:1]	1
0xBB0110B0	L34_EXTPORT_TO_WAN [0][2].EXTPORT_TO_WAN_PERMIT[2:2]	1

Address	Register	Len
0xBB0110B0	L34_EXTPORT_TO_WAN [0][3].EXTPORT_TO_WAN_PERMIT[3:3]	1
0xBB0110B0	L34_EXTPORT_TO_WAN [0][4].EXTPORT_TO_WAN_PERMIT[4:4]	1
0xBB0110B0	L34_EXTPORT_TO_WAN [0][5].EXTPORT_TO_WAN_PERMIT[5:5]	1
0xBB0110B0	L34_EXTPORT_TO_WAN [0][6].EXTPORT_TO_WAN_PERMIT[6:6]	1
0xBB0110B0	L34_EXTPORT_TO_WAN [0][7].EXTPORT_TO_WAN_PERMIT[7:7]	1
0xBB0110B4	L34_EXTPORT_TO_WAN [1][0].EXTPORT_TO_WAN_PERMIT[0:0]	1
0xBB0110B4	L34_EXTPORT_TO_WAN [1][1].EXTPORT_TO_WAN_PERMIT[1:1]	1
0xBB0110B4	L34_EXTPORT_TO_WAN [1][2].EXTPORT_TO_WAN_PERMIT[2:2]	1
0xBB0110B4	L34_EXTPORT_TO_WAN [1][3].EXTPORT_TO_WAN_PERMIT[3:3]	1
0xBB0110B4	L34_EXTPORT_TO_WAN [1][4].EXTPORT_TO_WAN_PERMIT[4:4]	1
0xBB0110B4	L34_EXTPORT_TO_WAN [1][5].EXTPORT_TO_WAN_PERMIT[5:5]	1
0xBB0110B4	L34_EXTPORT_TO_WAN [1][6].EXTPORT_TO_WAN_PERMIT[6:6]	1
0xBB0110B4	L34_EXTPORT_TO_WAN [1][7].EXTPORT_TO_WAN_PERMIT[7:7]	1
0xBB0110B8	L34_EXTPORT_TO_WAN [2][0].EXTPORT_TO_WAN_PERMIT[0:0]	1
0xBB0110B8	L34_EXTPORT_TO_WAN [2][1].EXTPORT_TO_WAN_PERMIT[1:1]	1
0xBB0110B8	L34_EXTPORT_TO_WAN [2][2].EXTPORT_TO_WAN_PERMIT[2:2]	1
0xBB0110B8	L34_EXTPORT_TO_WAN [2][3].EXTPORT_TO_WAN_PERMIT[3:3]	1
0xBB0110B8	L34_EXTPORT_TO_WAN [2][4].EXTPORT_TO_WAN_PERMIT[4:4]	1
0xBB0110B8	L34_EXTPORT_TO_WAN [2][5].EXTPORT_TO_WAN_PERMIT[5:5]	1
0xBB0110B8	L34_EXTPORT_TO_WAN [2][6].EXTPORT_TO_WAN_PERMIT[6:6]	1
0xBB0110B8	L34_EXTPORT_TO_WAN [2][7].EXTPORT_TO_WAN_PERMIT[7:7]	1
0xBB0110BC	L34_EXTPORT_TO_WAN [3][0].EXTPORT_TO_WAN_PERMIT[0:0]	1
0xBB0110BC	L34_EXTPORT_TO_WAN [3][1].EXTPORT_TO_WAN_PERMIT[1:1]	1
0xBB0110BC	L34_EXTPORT_TO_WAN [3][2].EXTPORT_TO_WAN_PERMIT[2:2]	1
0xBB0110BC	L34_EXTPORT_TO_WAN [3][3].EXTPORT_TO_WAN_PERMIT[3:3]	1
0xBB0110BC	L34_EXTPORT_TO_WAN [3][4].EXTPORT_TO_WAN_PERMIT[4:4]	1
0xBB0110BC	L34_EXTPORT_TO_WAN [3][5].EXTPORT_TO_WAN_PERMIT[5:5]	1
0xBB0110BC	L34_EXTPORT_TO_WAN [3][6].EXTPORT_TO_WAN_PERMIT[6:6]	1
0xBB0110BC	L34_EXTPORT_TO_WAN [3][7].EXTPORT_TO_WAN_PERMIT[7:7]	1
0xBB0110C0	L34_EXTPORT_TO_WAN [4][0].EXTPORT_TO_WAN_PERMIT[0:0]	1
0xBB0110C0	L34_EXTPORT_TO_WAN [4][1].EXTPORT_TO_WAN_PERMIT[1:1]	1
0xBB0110C0	L34_EXTPORT_TO_WAN [4][2].EXTPORT_TO_WAN_PERMIT[2:2]	1
0xBB0110C0	L34_EXTPORT_TO_WAN [4][3].EXTPORT_TO_WAN_PERMIT[3:3]	1
0xBB0110C0	L34_EXTPORT_TO_WAN [4][4].EXTPORT_TO_WAN_PERMIT[4:4]	1
0xBB0110C0	L34_EXTPORT_TO_WAN [4][5].EXTPORT_TO_WAN_PERMIT[5:5]	1
0xBB0110C0	L34_EXTPORT_TO_WAN [4][6].EXTPORT_TO_WAN_PERMIT[6:6]	1
0xBB0110C0	L34_EXTPORT_TO_WAN [4][7].EXTPORT_TO_WAN_PERMIT[7:7]	1
0xBB0110C4	L34_WAN_TO_PORT [0][0].WAN_TO_PORT_PERMIT[0:0]	1
0xBB0110C4	L34_WAN_TO_PORT [0][1].WAN_TO_PORT_PERMIT[1:1]	1
0xBB0110C4	L34_WAN_TO_PORT [0][2].WAN_TO_PORT_PERMIT[2:2]	1
0xBB0110C4	L34_WAN_TO_PORT [0][3].WAN_TO_PORT_PERMIT[3:3]	1
0xBB0110C4	L34_WAN_TO_PORT [0][4].WAN_TO_PORT_PERMIT[4:4]	1
0xBB0110C4	L34_WAN_TO_PORT [0][5].WAN_TO_PORT_PERMIT[5:5]	1
0xBB0110C4	L34_WAN_TO_PORT [0][6].WAN_TO_PORT_PERMIT[6:6]	1
0xBB0110C4	L34_WAN_TO_PORT [0][7].WAN_TO_PORT_PERMIT[7:7]	1
0xBB0110C8	L34_WAN_TO_PORT [1][0].WAN_TO_PORT_PERMIT[0:0]	1

Address	Register	Len
0xBB0110C8	L34_WAN_TO_PORT [1][1].WAN_TO_PORT_PERMIT[1:1]	1
0xBB0110C8	L34_WAN_TO_PORT [1][2].WAN_TO_PORT_PERMIT[2:2]	1
0xBB0110C8	L34_WAN_TO_PORT [1][3].WAN_TO_PORT_PERMIT[3:3]	1
0xBB0110C8	L34_WAN_TO_PORT [1][4].WAN_TO_PORT_PERMIT[4:4]	1
0xBB0110C8	L34_WAN_TO_PORT [1][5].WAN_TO_PORT_PERMIT[5:5]	1
0xBB0110C8	L34_WAN_TO_PORT [1][6].WAN_TO_PORT_PERMIT[6:6]	1
0xBB0110C8	L34_WAN_TO_PORT [1][7].WAN_TO_PORT_PERMIT[7:7]	1
0xBB0110CC	L34_WAN_TO_PORT [2][0].WAN_TO_PORT_PERMIT[0:0]	1
0xBB0110CC	L34_WAN_TO_PORT [2][1].WAN_TO_PORT_PERMIT[1:1]	1
0xBB0110CC	L34_WAN_TO_PORT [2][2].WAN_TO_PORT_PERMIT[2:2]	1
0xBB0110CC	L34_WAN_TO_PORT [2][3].WAN_TO_PORT_PERMIT[3:3]	1
0xBB0110CC	L34_WAN_TO_PORT [2][4].WAN_TO_PORT_PERMIT[4:4]	1
0xBB0110CC	L34_WAN_TO_PORT [2][5].WAN_TO_PORT_PERMIT[5:5]	1
0xBB0110CC	L34_WAN_TO_PORT [2][6].WAN_TO_PORT_PERMIT[6:6]	1
0xBB0110CC	L34_WAN_TO_PORT [2][7].WAN_TO_PORT_PERMIT[7:7]	1
0xBB0110D0	L34_WAN_TO_PORT [3][0].WAN_TO_PORT_PERMIT[0:0]	1
0xBB0110D0	L34_WAN_TO_PORT [3][1].WAN_TO_PORT_PERMIT[1:1]	1
0xBB0110D0	L34_WAN_TO_PORT [3][2].WAN_TO_PORT_PERMIT[2:2]	1
0xBB0110D0	L34_WAN_TO_PORT [3][3].WAN_TO_PORT_PERMIT[3:3]	1
0xBB0110D0	L34_WAN_TO_PORT [3][4].WAN_TO_PORT_PERMIT[4:4]	1
0xBB0110D0	L34_WAN_TO_PORT [3][5].WAN_TO_PORT_PERMIT[5:5]	1
0xBB0110D0	L34_WAN_TO_PORT [3][6].WAN_TO_PORT_PERMIT[6:6]	1
0xBB0110D0	L34_WAN_TO_PORT [3][7].WAN_TO_PORT_PERMIT[7:7]	1
0xBB0110D4	L34_WAN_TO_PORT [4][0].WAN_TO_PORT_PERMIT[0:0]	1
0xBB0110D4	L34_WAN_TO_PORT [4][1].WAN_TO_PORT_PERMIT[1:1]	1
0xBB0110D4	L34_WAN_TO_PORT [4][2].WAN_TO_PORT_PERMIT[2:2]	1
0xBB0110D4	L34_WAN_TO_PORT [4][3].WAN_TO_PORT_PERMIT[3:3]	1
0xBB0110D4	L34_WAN_TO_PORT [4][4].WAN_TO_PORT_PERMIT[4:4]	1
0xBB0110D4	L34_WAN_TO_PORT [4][5].WAN_TO_PORT_PERMIT[5:5]	1
0xBB0110D4	L34_WAN_TO_PORT [4][6].WAN_TO_PORT_PERMIT[6:6]	1
0xBB0110D4	L34_WAN_TO_PORT [4][7].WAN_TO_PORT_PERMIT[7:7]	1
0xBB0110D8	L34_WAN_TO_PORT [5][0].WAN_TO_PORT_PERMIT[0:0]	1
0xBB0110D8	L34_WAN_TO_PORT [5][1].WAN_TO_PORT_PERMIT[1:1]	1
0xBB0110D8	L34_WAN_TO_PORT [5][2].WAN_TO_PORT_PERMIT[2:2]	1
0xBB0110D8	L34_WAN_TO_PORT [5][3].WAN_TO_PORT_PERMIT[3:3]	1
0xBB0110D8	L34_WAN_TO_PORT [5][4].WAN_TO_PORT_PERMIT[4:4]	1
0xBB0110D8	L34_WAN_TO_PORT [5][5].WAN_TO_PORT_PERMIT[5:5]	1
0xBB0110D8	L34_WAN_TO_PORT [5][6].WAN_TO_PORT_PERMIT[6:6]	1
0xBB0110D8	L34_WAN_TO_PORT [5][7].WAN_TO_PORT_PERMIT[7:7]	1
0xBB0110DC	L34_WAN_TO_PORT [6][0].WAN_TO_PORT_PERMIT[0:0]	1
0xBB0110DC	L34_WAN_TO_PORT [6][1].WAN_TO_PORT_PERMIT[1:1]	1
0xBB0110DC	L34_WAN_TO_PORT [6][2].WAN_TO_PORT_PERMIT[2:2]	1
0xBB0110DC	L34_WAN_TO_PORT [6][3].WAN_TO_PORT_PERMIT[3:3]	1
0xBB0110DC	L34_WAN_TO_PORT [6][4].WAN_TO_PORT_PERMIT[4:4]	1
0xBB0110DC	L34_WAN_TO_PORT [6][5].WAN_TO_PORT_PERMIT[5:5]	1
0xBB0110DC	L34_WAN_TO_PORT [6][6].WAN_TO_PORT_PERMIT[6:6]	1

Address	Register	Len
0xBB0110DC	L34_WAN_TO_PORT [6][7].WAN_TO_PORT_PERMIT[7:7]	1
0xBB0110E0	L34_WAN_TO_EXTPORT [0][0].WAN_TO_EXTPORT_PERMIT[0:0]	1
0xBB0110E0	L34_WAN_TO_EXTPORT [0][1].WAN_TO_EXTPORT_PERMIT[1:1]	1
0xBB0110E0	L34_WAN_TO_EXTPORT [0][2].WAN_TO_EXTPORT_PERMIT[2:2]	1
0xBB0110E0	L34_WAN_TO_EXTPORT [0][3].WAN_TO_EXTPORT_PERMIT[3:3]	1
0xBB0110E0	L34_WAN_TO_EXTPORT [0][4].WAN_TO_EXTPORT_PERMIT[4:4]	1
0xBB0110E0	L34_WAN_TO_EXTPORT [0][5].WAN_TO_EXTPORT_PERMIT[5:5]	1
0xBB0110E0	L34_WAN_TO_EXTPORT [0][6].WAN_TO_EXTPORT_PERMIT[6:6]	1
0xBB0110E0	L34_WAN_TO_EXTPORT [0][7].WAN_TO_EXTPORT_PERMIT[7:7]	1
0xBB0110E4	L34_WAN_TO_EXTPORT [1][0].WAN_TO_EXTPORT_PERMIT[0:0]	1
0xBB0110E4	L34_WAN_TO_EXTPORT [1][1].WAN_TO_EXTPORT_PERMIT[1:1]	1
0xBB0110E4	L34_WAN_TO_EXTPORT [1][2].WAN_TO_EXTPORT_PERMIT[2:2]	1
0xBB0110E4	L34_WAN_TO_EXTPORT [1][3].WAN_TO_EXTPORT_PERMIT[3:3]	1
0xBB0110E4	L34_WAN_TO_EXTPORT [1][4].WAN_TO_EXTPORT_PERMIT[4:4]	1
0xBB0110E4	L34_WAN_TO_EXTPORT [1][5].WAN_TO_EXTPORT_PERMIT[5:5]	1
0xBB0110E4	L34_WAN_TO_EXTPORT [1][6].WAN_TO_EXTPORT_PERMIT[6:6]	1
0xBB0110E4	L34_WAN_TO_EXTPORT [1][7].WAN_TO_EXTPORT_PERMIT[7:7]	1
0xBB0110E8	L34_WAN_TO_EXTPORT [2][0].WAN_TO_EXTPORT_PERMIT[0:0]	1
0xBB0110E8	L34_WAN_TO_EXTPORT [2][1].WAN_TO_EXTPORT_PERMIT[1:1]	1
0xBB0110E8	L34_WAN_TO_EXTPORT [2][2].WAN_TO_EXTPORT_PERMIT[2:2]	1
0xBB0110E8	L34_WAN_TO_EXTPORT [2][3].WAN_TO_EXTPORT_PERMIT[3:3]	1
0xBB0110E8	L34_WAN_TO_EXTPORT [2][4].WAN_TO_EXTPORT_PERMIT[4:4]	1
0xBB0110E8	L34_WAN_TO_EXTPORT [2][5].WAN_TO_EXTPORT_PERMIT[5:5]	1
0xBB0110E8	L34_WAN_TO_EXTPORT [2][6].WAN_TO_EXTPORT_PERMIT[6:6]	1
0xBB0110E8	L34_WAN_TO_EXTPORT [2][7].WAN_TO_EXTPORT_PERMIT[7:7]	1
0xBB0110EC	L34_WAN_TO_EXTPORT [3][0].WAN_TO_EXTPORT_PERMIT[0:0]	1
0xBB0110EC	L34_WAN_TO_EXTPORT [3][1].WAN_TO_EXTPORT_PERMIT[1:1]	1
0xBB0110EC	L34_WAN_TO_EXTPORT [3][2].WAN_TO_EXTPORT_PERMIT[2:2]	1
0xBB0110EC	L34_WAN_TO_EXTPORT [3][3].WAN_TO_EXTPORT_PERMIT[3:3]	1
0xBB0110EC	L34_WAN_TO_EXTPORT [3][4].WAN_TO_EXTPORT_PERMIT[4:4]	1
0xBB0110EC	L34_WAN_TO_EXTPORT [3][5].WAN_TO_EXTPORT_PERMIT[5:5]	1
0xBB0110EC	L34_WAN_TO_EXTPORT [3][6].WAN_TO_EXTPORT_PERMIT[6:6]	1
0xBB0110EC	L34_WAN_TO_EXTPORT [3][7].WAN_TO_EXTPORT_PERMIT[7:7]	1
0xBB0110F0	L34_WAN_TO_EXTPORT [4][0].WAN_TO_EXTPORT_PERMIT[0:0]	1
0xBB0110F0	L34_WAN_TO_EXTPORT [4][1].WAN_TO_EXTPORT_PERMIT[1:1]	1
0xBB0110F0	L34_WAN_TO_EXTPORT [4][2].WAN_TO_EXTPORT_PERMIT[2:2]	1
0xBB0110F0	L34_WAN_TO_EXTPORT [4][3].WAN_TO_EXTPORT_PERMIT[3:3]	1
0xBB0110F0	L34_WAN_TO_EXTPORT [4][4].WAN_TO_EXTPORT_PERMIT[4:4]	1
0xBB0110F0	L34_WAN_TO_EXTPORT [4][5].WAN_TO_EXTPORT_PERMIT[5:5]	1
0xBB0110F0	L34_WAN_TO_EXTPORT [4][6].WAN_TO_EXTPORT_PERMIT[6:6]	1
0xBB0110F0	L34_WAN_TO_EXTPORT [4][7].WAN_TO_EXTPORT_PERMIT[7:7]	1
0xBB0110F4	AVB_PORT_EN [0].EN[0:0]	1
0xBB0110F4	AVB_PORT_EN [1].EN[1:1]	1
0xBB0110F4	AVB_PORT_EN [2].EN[2:2]	1
0xBB0110F4	AVB_PORT_EN [3].EN[3:3]	1
0xBB0110F4	AVB_PORT_EN [4].EN[4:4]	1

Address	Register	Len
0xBB0110F4	AVB_PORT_EN [5].EN[5:5]	1
0xBB0110F4	AVB_PORT_EN [6].EN[6:6]	1
0xBB0110F8	AVB_PRI_REMAP [0].PRI[2:0]	3
0xBB0110F8	AVB_PRI_REMAP [1].PRI[5:3]	3
0xBB0110F8	AVB_PRI_REMAP [2].PRI[8:6]	3
0xBB0110F8	AVB_PRI_REMAP [3].PRI[11:9]	3
0xBB0110F8	AVB_PRI_REMAP [4].PRI[14:12]	3
0xBB0110F8	AVB_PRI_REMAP [5].PRI[17:15]	3
0xBB0110F8	AVB_PRI_REMAP [6].PRI[20:18]	3
0xBB0110F8	AVB_PRI_REMAP [7].PRI[23:21]	3
0xBB0110FC	PTP_TRANSPARENT_CFG [0].TRANSPARENT_PORT[0:0]	1
0xBB0110FC	PTP_TRANSPARENT_CFG [1].TRANSPARENT_PORT[1:1]	1
0xBB0110FC	PTP_TRANSPARENT_CFG [2].TRANSPARENT_PORT[2:2]	1
0xBB0110FC	PTP_TRANSPARENT_CFG [3].TRANSPARENT_PORT[3:3]	1
0xBB0110FC	PTP_TRANSPARENT_CFG [4].TRANSPARENT_PORT[4:4]	1
0xBB0110FC	PTP_TRANSPARENT_CFG [5].TRANSPARENT_PORT[5:5]	1
0xBB0110FC	PTP_TRANSPARENT_CFG [6].TRANSPARENT_PORT[6:6]	1
0xBB011100	PTP_IGR_MSG_ACT [0].ACT[1:0]	2
0xBB011100	PTP_IGR_MSG_ACT [1].ACT[3:2]	2
0xBB011100	PTP_IGR_MSG_ACT [2].ACT[5:4]	2
0xBB011100	PTP_IGR_MSG_ACT [3].ACT[7:6]	2
0xBB011100	PTP_IGR_MSG_ACT [4].ACT[9:8]	2
0xBB011100	PTP_IGR_MSG_ACT [5].ACT[11:10]	2
0xBB011100	PTP_IGR_MSG_ACT [6].ACT[13:12]	2
0xBB011100	PTP_IGR_MSG_ACT [7].ACT[15:14]	2
0xBB011100	PTP_IGR_MSG_ACT [8].ACT[17:16]	2
0xBB011100	PTP_IGR_MSG_ACT [9].ACT[19:18]	2
0xBB011104	PTP_EGR_MSG_ACT [0].ACT[1:0]	2
0xBB011104	PTP_EGR_MSG_ACT [1].ACT[3:2]	2
0xBB011104	PTP_EGR_MSG_ACT [2].ACT[5:4]	2
0xBB011104	PTP_EGR_MSG_ACT [3].ACT[7:6]	2
0xBB011104	PTP_EGR_MSG_ACT [4].ACT[9:8]	2
0xBB011104	PTP_EGR_MSG_ACT [5].ACT[11:10]	2
0xBB011104	PTP_EGR_MSG_ACT [6].ACT[13:12]	2
0xBB011104	PTP_EGR_MSG_ACT [7].ACT[15:14]	2
0xBB011104	PTP_EGR_MSG_ACT [8].ACT[17:16]	2
0xBB011104	PTP_EGR_MSG_ACT [9].ACT[19:18]	2
0xBB011108	PTP_RX_TIME.RESERVED[31:3]	29
0xBB011108	PTP_RX_TIME.SEC_2_0[2:0]	3
0xBB01110C	PTP_RX_TIME.RESERVED[31:30]	2
0xBB01110C	PTP_RX_TIME.NSEC_UNIT[29:3]	27
0xBB01110C	PTP_RX_TIME.RESERVED[2:0]	3
0xBB011110	PTP_P_EN [0].RESERVED[31:1]	31
0xBB011110	PTP_P_EN [0].PTP_EN[0:0]	1
0xBB011114	PTP_P_EN [1].RESERVED[31:1]	31
0xBB011114	PTP_P_EN [1].PTP_EN[0:0]	1



Address	Register	Len
0xBB011118	PTP_P_EN [2].RESERVED[31:1]	31
0xBB011118	PTP_P_EN [2].PTP_EN[0:0]	1
0xBB01111C	PTP_P_EN [3].RESERVED[31:1]	31
0xBB01111C	PTP_P_EN [3].PTP_EN[0:0]	1
0xBB011120	PTP_P_EN [4].RESERVED[31:1]	31
0xBB011120	PTP_P_EN [4].PTP_EN[0:0]	1
0xBB011124	PTP_P_EN [5].RESERVED[31:1]	31
0xBB011124	PTP_P_EN [5].PTP_EN[0:0]	1
0xBB011128	PTP_P_EN [6].RESERVED[31:1]	31
0xBB011128	PTP_P_EN [6].PTP_EN[0:0]	1
0xBB01112C	RGF_VER_ALE_GLB.REGFILE_VER[31:0]	32
0xBB011130	RSVD_ALE_GLB [0].RSVD_MEM[31:0]	32
0xBB011134	RSVD_ALE_GLB [1].RSVD_MEM[31:0]	32
0xBB011138	RSVD_ALE_GLB [2].RSVD_MEM[31:0]	32
0xBB01113C	RSVD_ALE_GLB [3].RSVD_MEM[31:0]	32
0xBB011140	RSVD_ALE_GLB [4].RSVD_MEM[31:0]	32
0xBB011144	RSVD_ALE_GLB [5].RSVD_MEM[31:0]	32
0xBB011148	RSVD_ALE_GLB [6].RSVD_MEM[31:0]	32
0xBB01114C	RSVD_ALE_GLB [7].RSVD_MEM[31:0]	32
0xBB011150	RSVD_ALE_GLB [8].RSVD_MEM[31:0]	32
0xBB011154	RSVD_ALE_GLB [9].RSVD_MEM[31:0]	32
0xBB011158	RSVD_ALE_GLB [10].RSVD_MEM[31:0]	32
0xBB01115C	RSVD_ALE_GLB [11].RSVD_MEM[31:0]	32
0xBB011160	RSVD_ALE_GLB [12].RSVD_MEM[31:0]	32
0xBB011164	RSVD_ALE_GLB [13].RSVD_MEM[31:0]	32
0xBB011168	RSVD_ALE_GLB [14].RSVD_MEM[31:0]	32
0xBB01116C	RSVD_ALE_GLB [15].RSVD_MEM[31:0]	32
0xBB012000	TBL_ACCESS_CTRL.RESERVED[31:22]	10
0xBB012000	TBL_ACCESS_CTRL.ADDR[21:10]	12
0xBB012000	TBL_ACCESS_CTRL.SPA[9:7]	3
0xBB012000	TBL_ACCESS_CTRL.ACCESS_METHOD[6:4]	3
0xBB012000	TBL_ACCESS_CTRL.CMD_TYPE[3:3]	1
0xBB012000	TBL_ACCESS_CTRL.TBL_TYPE[2:0]	3
0xBB012004	TBL_ACCESS_STS.RESERVED[31:14]	18
0xBB012004	TBL_ACCESS_STS.BUSY_FLAG[13:13]	1
0xBB012004	TBL_ACCESS_STS.HIT_STATUS[12:12]	1
0xBB012004	TBL_ACCESS_STS.TYPE[11:11]	1
0xBB012004	TBL_ACCESS_STS.ADDR[10:0]	11
0xBB012008	TBL_ACCESS_WR_DATA.DATA4[31:0]	32
0xBB01200C	TBL_ACCESS_WR_DATA.DATA3[31:0]	32
0xBB012010	TBL_ACCESS_WR_DATA.DATA2[31:0]	32
0xBB012014	TBL_ACCESS_WR_DATA.DATA1[31:0]	32
0xBB012018	TBL_ACCESS_WR_DATA.DATA0[31:0]	32
0xBB01201C	TBL_ACCESS_RD_DATA.DATA4[31:0]	32
0xBB012020	TBL_ACCESS_RD_DATA.DATA3[31:0]	32
0xBB012024	TBL_ACCESS_RD_DATA.DATA2[31:0]	32



Address	Register	Len
0xBB012028	TBL_ACCESS_RD_DATA.DATA1[31:0]	32
0xBB01202C	TBL_ACCESS_RD_DATA.DATA0[31:0]	32
0xBB013000	VLAN_PORT_ACCEPT_FRAME_TYPE [0].FRAME_TYPE[1:0]	2
0xBB013000	VLAN_PORT_ACCEPT_FRAME_TYPE [1].FRAME_TYPE[3:2]	2
0xBB013000	VLAN_PORT_ACCEPT_FRAME_TYPE [2].FRAME_TYPE[5:4]	2
0xBB013000	VLAN_PORT_ACCEPT_FRAME_TYPE [3].FRAME_TYPE[7:6]	2
0xBB013000	VLAN_PORT_ACCEPT_FRAME_TYPE [4].FRAME_TYPE[9:8]	2
0xBB013000	VLAN_PORT_ACCEPT_FRAME_TYPE [5].FRAME_TYPE[11:10]	2
0xBB013000	VLAN_PORT_ACCEPT_FRAME_TYPE [6].FRAME_TYPE[13:12]	2
0xBB013004	VLAN_INGRESS [0].INGRESS[0:0]	1
0xBB013004	VLAN_INGRESS [1].INGRESS[1:1]	1
0xBB013004	VLAN_INGRESS [2].INGRESS[2:2]	1
0xBB013004	VLAN_INGRESS [3].INGRESS[3:3]	1
0xBB013004	VLAN_INGRESS [4].INGRESS[4:4]	1
0xBB013004	VLAN_INGRESS [5].INGRESS[5:5]	1
0xBB013004	VLAN_INGRESS [6].INGRESS[6:6]	1
0xBB013008	VLAN_MBR_CFG [0].RESERVED[31:27]	5
0xBB013008	VLAN_MBR_CFG [0].EVID[26:14]	13
0xBB013008	VLAN_MBR_CFG [0].METERIDX[13:9]	5
0xBB013008	VLAN_MBR_CFG [0].ENVLANPOL[8:8]	1
0xBB013008	VLAN_MBR_CFG [0].VBPRI[7:5]	3
0xBB013008	VLAN_MBR_CFG [0].VBPEN[4:4]	1
0xBB013008	VLAN_MBR_CFG [0].FID_MSTI[3:0]	4
0xBB01300C	VLAN_MBR_CFG [0].RESERVED[31:29]	3
0xBB01300C	VLAN_MBR_CFG [0].EXT_MBR[28:23]	6
0xBB01300C	VLAN_MBR_CFG [0].RESERVED[22:7]	16
0xBB01300C	VLAN_MBR_CFG [0].MBR[6:0]	7
0xBB013010	VLAN_MBR_CFG [1].RESERVED[31:27]	5
0xBB013010	VLAN_MBR_CFG [1].EVID[26:14]	13
0xBB013010	VLAN_MBR_CFG [1].METERIDX[13:9]	5
0xBB013010	VLAN_MBR_CFG [1].ENVLANPOL[8:8]	1
0xBB013010	VLAN_MBR_CFG [1].VBPRI[7:5]	3
0xBB013010	VLAN_MBR_CFG [1].VBPEN[4:4]	1
0xBB013010	VLAN_MBR_CFG [1].FID_MSTI[3:0]	4
0xBB013014	VLAN_MBR_CFG [1].RESERVED[31:29]	3
0xBB013014	VLAN_MBR_CFG [1].EXT_MBR[28:23]	6
0xBB013014	VLAN_MBR_CFG [1].RESERVED[22:7]	16
0xBB013014	VLAN_MBR_CFG [1].MBR[6:0]	7
0xBB013018	VLAN_MBR_CFG [2].RESERVED[31:27]	5
0xBB013018	VLAN_MBR_CFG [2].EVID[26:14]	13
0xBB013018	VLAN_MBR_CFG [2].METERIDX[13:9]	5
0xBB013018	VLAN_MBR_CFG [2].ENVLANPOL[8:8]	1
0xBB013018	VLAN_MBR_CFG [2].VBPRI[7:5]	3
0xBB013018	VLAN_MBR_CFG [2].VBPEN[4:4]	1
0xBB013018	VLAN_MBR_CFG [2].FID_MSTI[3:0]	4
0xBB01301C	VLAN_MBR_CFG [2].RESERVED[31:29]	3

Address	Register	Len
0xBB01301C	VLAN_MBR_CFG [2].EXT_MBR[28:23]	6
0xBB01301C	VLAN_MBR_CFG [2].RESERVED[22:7]	16
0xBB01301C	VLAN_MBR_CFG [2].MBR[6:0]	7
0xBB013020	VLAN_MBR_CFG [3].RESERVED[31:27]	5
0xBB013020	VLAN_MBR_CFG [3].EVID[26:14]	13
0xBB013020	VLAN_MBR_CFG [3].METERIDX[13:9]	5
0xBB013020	VLAN_MBR_CFG [3].ENVLANPOL[8:8]	1
0xBB013020	VLAN_MBR_CFG [3].VBPRI[7:5]	3
0xBB013020	VLAN_MBR_CFG [3].VBPEN[4:4]	1
0xBB013020	VLAN_MBR_CFG [3].FID_MSTI[3:0]	4
0xBB013024	VLAN_MBR_CFG [3].RESERVED[31:29]	3
0xBB013024	VLAN_MBR_CFG [3].EXT_MBR[28:23]	6
0xBB013024	VLAN_MBR_CFG [3].RESERVED[22:7]	16
0xBB013024	VLAN_MBR_CFG [3].MBR[6:0]	7
0xBB013028	VLAN_MBR_CFG [4].RESERVED[31:27]	5
0xBB013028	VLAN_MBR_CFG [4].EVID[26:14]	13
0xBB013028	VLAN_MBR_CFG [4].METERIDX[13:9]	5
0xBB013028	VLAN_MBR_CFG [4].ENVLANPOL[8:8]	1
0xBB013028	VLAN_MBR_CFG [4].VBPRI[7:5]	3
0xBB013028	VLAN_MBR_CFG [4].VBPEN[4:4]	1
0xBB013028	VLAN_MBR_CFG [4].FID_MSTI[3:0]	4
0xBB01302C	VLAN_MBR_CFG [4].RESERVED[31:29]	3
0xBB01302C	VLAN_MBR_CFG [4].EXT_MBR[28:23]	6
0xBB01302C	VLAN_MBR_CFG [4].RESERVED[22:7]	16
0xBB01302C	VLAN_MBR_CFG [4].MBR[6:0]	7
0xBB013030	VLAN_MBR_CFG [5].RESERVED[31:27]	5
0xBB013030	VLAN_MBR_CFG [5].EVID[26:14]	13
0xBB013030	VLAN_MBR_CFG [5].METERIDX[13:9]	5
0xBB013030	VLAN_MBR_CFG [5].ENVLANPOL[8:8]	1
0xBB013030	VLAN_MBR_CFG [5].VBPRI[7:5]	3
0xBB013030	VLAN_MBR_CFG [5].VBPEN[4:4]	1
0xBB013030	VLAN_MBR_CFG [5].FID_MSTI[3:0]	4
0xBB013034	VLAN_MBR_CFG [5].RESERVED[31:29]	3
0xBB013034	VLAN_MBR_CFG [5].EXT_MBR[28:23]	6
0xBB013034	VLAN_MBR_CFG [5].RESERVED[22:7]	16
0xBB013034	VLAN_MBR_CFG [5].MBR[6:0]	7
0xBB013038	VLAN_MBR_CFG [6].RESERVED[31:27]	5
0xBB013038	VLAN_MBR_CFG [6].EVID[26:14]	13
0xBB013038	VLAN_MBR_CFG [6].METERIDX[13:9]	5
0xBB013038	VLAN_MBR_CFG [6].ENVLANPOL[8:8]	1
0xBB013038	VLAN_MBR_CFG [6].VBPRI[7:5]	3
0xBB013038	VLAN_MBR_CFG [6].VBPEN[4:4]	1
0xBB013038	VLAN_MBR_CFG [6].FID_MSTI[3:0]	4
0xBB01303C	VLAN_MBR_CFG [6].RESERVED[31:29]	3
0xBB01303C	VLAN_MBR_CFG [6].EXT_MBR[28:23]	6
0xBB01303C	VLAN_MBR_CFG [6].RESERVED[22:7]	16

Address	Register	Len
0xBB01303C	VLAN_MBR_CFG [6].MBR[6:0]	7
0xBB013040	VLAN_MBR_CFG [7].RESERVED[31:27]	5
0xBB013040	VLAN_MBR_CFG [7].EVID[26:14]	13
0xBB013040	VLAN_MBR_CFG [7].METERIDX[13:9]	5
0xBB013040	VLAN_MBR_CFG [7].ENVLANPOL[8:8]	1
0xBB013040	VLAN_MBR_CFG [7].VBPRI[7:5]	3
0xBB013040	VLAN_MBR_CFG [7].VBPEN[4:4]	1
0xBB013040	VLAN_MBR_CFG [7].FID_MSTI[3:0]	4
0xBB013044	VLAN_MBR_CFG [7].RESERVED[31:29]	3
0xBB013044	VLAN_MBR_CFG [7].EXT_MBR[28:23]	6
0xBB013044	VLAN_MBR_CFG [7].RESERVED[22:7]	16
0xBB013044	VLAN_MBR_CFG [7].MBR[6:0]	7
0xBB013048	VLAN_MBR_CFG [8].RESERVED[31:27]	5
0xBB013048	VLAN_MBR_CFG [8].EVID[26:14]	13
0xBB013048	VLAN_MBR_CFG [8].METERIDX[13:9]	5
0xBB013048	VLAN_MBR_CFG [8].ENVLANPOL[8:8]	1
0xBB013048	VLAN_MBR_CFG [8].VBPRI[7:5]	3
0xBB013048	VLAN_MBR_CFG [8].VBPEN[4:4]	1
0xBB013048	VLAN_MBR_CFG [8].FID_MSTI[3:0]	4
0xBB01304C	VLAN_MBR_CFG [8].RESERVED[31:29]	3
0xBB01304C	VLAN_MBR_CFG [8].EXT_MBR[28:23]	6
0xBB01304C	VLAN_MBR_CFG [8].RESERVED[22:7]	16
0xBB01304C	VLAN_MBR_CFG [8].MBR[6:0]	7
0xBB013050	VLAN_MBR_CFG [9].RESERVED[31:27]	5
0xBB013050	VLAN_MBR_CFG [9].EVID[26:14]	13
0xBB013050	VLAN_MBR_CFG [9].METERIDX[13:9]	5
0xBB013050	VLAN_MBR_CFG [9].ENVLANPOL[8:8]	1
0xBB013050	VLAN_MBR_CFG [9].VBPRI[7:5]	3
0xBB013050	VLAN_MBR_CFG [9].VBPEN[4:4]	1
0xBB013050	VLAN_MBR_CFG [9].FID_MSTI[3:0]	4
0xBB013054	VLAN_MBR_CFG [9].RESERVED[31:29]	3
0xBB013054	VLAN_MBR_CFG [9].EXT_MBR[28:23]	6
0xBB013054	VLAN_MBR_CFG [9].RESERVED[22:7]	16
0xBB013054	VLAN_MBR_CFG [9].MBR[6:0]	7
0xBB013058	VLAN_MBR_CFG [10].RESERVED[31:27]	5
0xBB013058	VLAN_MBR_CFG [10].EVID[26:14]	13
0xBB013058	VLAN_MBR_CFG [10].METERIDX[13:9]	5
0xBB013058	VLAN_MBR_CFG [10].ENVLANPOL[8:8]	1
0xBB013058	VLAN_MBR_CFG [10].VBPRI[7:5]	3
0xBB013058	VLAN_MBR_CFG [10].VBPEN[4:4]	1
0xBB013058	VLAN_MBR_CFG [10].FID_MSTI[3:0]	4
0xBB01305C	VLAN_MBR_CFG [10].RESERVED[31:29]	3
0xBB01305C	VLAN_MBR_CFG [10].EXT_MBR[28:23]	6
0xBB01305C	VLAN_MBR_CFG [10].RESERVED[22:7]	16
0xBB01305C	VLAN_MBR_CFG [10].MBR[6:0]	7
0xBB013060	VLAN_MBR_CFG [11].RESERVED[31:27]	5

Address	Register	Len
0xBB013060	VLAN_MBR_CFG [11].EVID[26:14]	13
0xBB013060	VLAN_MBR_CFG [11].METERIDX[13:9]	5
0xBB013060	VLAN_MBR_CFG [11].ENVLANPOL[8:8]	1
0xBB013060	VLAN_MBR_CFG [11].VBPRI[7:5]	3
0xBB013060	VLAN_MBR_CFG [11].VBPEN[4:4]	1
0xBB013060	VLAN_MBR_CFG [11].FID_MSTI[3:0]	4
0xBB013064	VLAN_MBR_CFG [11].RESERVED[31:29]	3
0xBB013064	VLAN_MBR_CFG [11].EXT_MBR[28:23]	6
0xBB013064	VLAN_MBR_CFG [11].RESERVED[22:7]	16
0xBB013064	VLAN_MBR_CFG [11].MBR[6:0]	7
0xBB013068	VLAN_MBR_CFG [12].RESERVED[31:27]	5
0xBB013068	VLAN_MBR_CFG [12].EVID[26:14]	13
0xBB013068	VLAN_MBR_CFG [12].METERIDX[13:9]	5
0xBB013068	VLAN_MBR_CFG [12].ENVLANPOL[8:8]	1
0xBB013068	VLAN_MBR_CFG [12].VBPRI[7:5]	3
0xBB013068	VLAN_MBR_CFG [12].VBPEN[4:4]	1
0xBB013068	VLAN_MBR_CFG [12].FID_MSTI[3:0]	4
0xBB01306C	VLAN_MBR_CFG [12].RESERVED[31:29]	3
0xBB01306C	VLAN_MBR_CFG [12].EXT_MBR[28:23]	6
0xBB01306C	VLAN_MBR_CFG [12].RESERVED[22:7]	16
0xBB01306C	VLAN_MBR_CFG [12].MBR[6:0]	7
0xBB013070	VLAN_MBR_CFG [13].RESERVED[31:27]	5
0xBB013070	VLAN_MBR_CFG [13].EVID[26:14]	13
0xBB013070	VLAN_MBR_CFG [13].METERIDX[13:9]	5
0xBB013070	VLAN_MBR_CFG [13].ENVLANPOL[8:8]	1
0xBB013070	VLAN_MBR_CFG [13].VBPRI[7:5]	3
0xBB013070	VLAN_MBR_CFG [13].VBPEN[4:4]	1
0xBB013070	VLAN_MBR_CFG [13].FID_MSTI[3:0]	4
0xBB013074	VLAN_MBR_CFG [13].RESERVED[31:29]	3
0xBB013074	VLAN_MBR_CFG [13].EXT_MBR[28:23]	6
0xBB013074	VLAN_MBR_CFG [13].RESERVED[22:7]	16
0xBB013074	VLAN_MBR_CFG [13].MBR[6:0]	7
0xBB013078	VLAN_MBR_CFG [14].RESERVED[31:27]	5
0xBB013078	VLAN_MBR_CFG [14].EVID[26:14]	13
0xBB013078	VLAN_MBR_CFG [14].METERIDX[13:9]	5
0xBB013078	VLAN_MBR_CFG [14].ENVLANPOL[8:8]	1
0xBB013078	VLAN_MBR_CFG [14].VBPRI[7:5]	3
0xBB013078	VLAN_MBR_CFG [14].VBPEN[4:4]	1
0xBB013078	VLAN_MBR_CFG [14].FID_MSTI[3:0]	4
0xBB01307C	VLAN_MBR_CFG [14].RESERVED[31:29]	3
0xBB01307C	VLAN_MBR_CFG [14].EXT_MBR[28:23]	6
0xBB01307C	VLAN_MBR_CFG [14].RESERVED[22:7]	16
0xBB01307C	VLAN_MBR_CFG [14].MBR[6:0]	7
0xBB013080	VLAN_MBR_CFG [15].RESERVED[31:27]	5
0xBB013080	VLAN_MBR_CFG [15].EVID[26:14]	13
0xBB013080	VLAN_MBR_CFG [15].METERIDX[13:9]	5

Address	Register	Len
0xBB013080	VLAN_MBR_CFG [15].ENVLANPOL[8:8]	1
0xBB013080	VLAN_MBR_CFG [15].VBPRI[7:5]	3
0xBB013080	VLAN_MBR_CFG [15].VBPEN[4:4]	1
0xBB013080	VLAN_MBR_CFG [15].FID_MSTI[3:0]	4
0xBB013084	VLAN_MBR_CFG [15].RESERVED[31:29]	3
0xBB013084	VLAN_MBR_CFG [15].EXT_MBR[28:23]	6
0xBB013084	VLAN_MBR_CFG [15].RESERVED[22:7]	16
0xBB013084	VLAN_MBR_CFG [15].MBR[6:0]	7
0xBB013088	VLAN_MBR_CFG [16].RESERVED[31:27]	5
0xBB013088	VLAN_MBR_CFG [16].EVID[26:14]	13
0xBB013088	VLAN_MBR_CFG [16].METERIDX[13:9]	5
0xBB013088	VLAN_MBR_CFG [16].ENVLANPOL[8:8]	1
0xBB013088	VLAN_MBR_CFG [16].VBPRI[7:5]	3
0xBB013088	VLAN_MBR_CFG [16].VBPEN[4:4]	1
0xBB013088	VLAN_MBR_CFG [16].FID_MSTI[3:0]	4
0xBB01308C	VLAN_MBR_CFG [16].RESERVED[31:29]	3
0xBB01308C	VLAN_MBR_CFG [16].EXT_MBR[28:23]	6
0xBB01308C	VLAN_MBR_CFG [16].RESERVED[22:7]	16
0xBB01308C	VLAN_MBR_CFG [16].MBR[6:0]	7
0xBB013090	VLAN_MBR_CFG [17].RESERVED[31:27]	5
0xBB013090	VLAN_MBR_CFG [17].EVID[26:14]	13
0xBB013090	VLAN_MBR_CFG [17].METERIDX[13:9]	5
0xBB013090	VLAN_MBR_CFG [17].ENVLANPOL[8:8]	1
0xBB013090	VLAN_MBR_CFG [17].VBPRI[7:5]	3
0xBB013090	VLAN_MBR_CFG [17].VBPEN[4:4]	1
0xBB013090	VLAN_MBR_CFG [17].FID_MSTI[3:0]	4
0xBB013094	VLAN_MBR_CFG [17].RESERVED[31:29]	3
0xBB013094	VLAN_MBR_CFG [17].EXT_MBR[28:23]	6
0xBB013094	VLAN_MBR_CFG [17].RESERVED[22:7]	16
0xBB013094	VLAN_MBR_CFG [17].MBR[6:0]	7
0xBB013098	VLAN_MBR_CFG [18].RESERVED[31:27]	5
0xBB013098	VLAN_MBR_CFG [18].EVID[26:14]	13
0xBB013098	VLAN_MBR_CFG [18].METERIDX[13:9]	5
0xBB013098	VLAN_MBR_CFG [18].ENVLANPOL[8:8]	1
0xBB013098	VLAN_MBR_CFG [18].VBPRI[7:5]	3
0xBB013098	VLAN_MBR_CFG [18].VBPEN[4:4]	1
0xBB013098	VLAN_MBR_CFG [18].FID_MSTI[3:0]	4
0xBB01309C	VLAN_MBR_CFG [18].RESERVED[31:29]	3
0xBB01309C	VLAN_MBR_CFG [18].EXT_MBR[28:23]	6
0xBB01309C	VLAN_MBR_CFG [18].RESERVED[22:7]	16
0xBB01309C	VLAN_MBR_CFG [18].MBR[6:0]	7
0xBB0130A0	VLAN_MBR_CFG [19].RESERVED[31:27]	5
0xBB0130A0	VLAN_MBR_CFG [19].EVID[26:14]	13
0xBB0130A0	VLAN_MBR_CFG [19].METERIDX[13:9]	5
0xBB0130A0	VLAN_MBR_CFG [19].ENVLANPOL[8:8]	1
0xBB0130A0	VLAN_MBR_CFG [19].VBPRI[7:5]	3

Address	Register	Len
0xBB0130A0	VLAN_MBR_CFG [19].VBPEN[4:4]	1
0xBB0130A0	VLAN_MBR_CFG [19].FID_MSTI[3:0]	4
0xBB0130A4	VLAN_MBR_CFG [19].RESERVED[31:29]	3
0xBB0130A4	VLAN_MBR_CFG [19].EXT_MBR[28:23]	6
0xBB0130A4	VLAN_MBR_CFG [19].RESERVED[22:7]	16
0xBB0130A4	VLAN_MBR_CFG [19].MBR[6:0]	7
0xBB0130A8	VLAN_MBR_CFG [20].RESERVED[31:27]	5
0xBB0130A8	VLAN_MBR_CFG [20].EVID[26:14]	13
0xBB0130A8	VLAN_MBR_CFG [20].METERIDX[13:9]	5
0xBB0130A8	VLAN_MBR_CFG [20].ENVLANPOL[8:8]	1
0xBB0130A8	VLAN_MBR_CFG [20].VBPRI[7:5]	3
0xBB0130A8	VLAN_MBR_CFG [20].VBPEN[4:4]	1
0xBB0130A8	VLAN_MBR_CFG [20].FID_MSTI[3:0]	4
0xBB0130AC	VLAN_MBR_CFG [20].RESERVED[31:29]	3
0xBB0130AC	VLAN_MBR_CFG [20].EXT_MBR[28:23]	6
0xBB0130AC	VLAN_MBR_CFG [20].RESERVED[22:7]	16
0xBB0130AC	VLAN_MBR_CFG [20].MBR[6:0]	7
0xBB0130B0	VLAN_MBR_CFG [21].RESERVED[31:27]	5
0xBB0130B0	VLAN_MBR_CFG [21].EVID[26:14]	13
0xBB0130B0	VLAN_MBR_CFG [21].METERIDX[13:9]	5
0xBB0130B0	VLAN_MBR_CFG [21].ENVLANPOL[8:8]	1
0xBB0130B0	VLAN_MBR_CFG [21].VBPRI[7:5]	3
0xBB0130B0	VLAN_MBR_CFG [21].VBPEN[4:4]	1
0xBB0130B0	VLAN_MBR_CFG [21].FID_MSTI[3:0]	4
0xBB0130B4	VLAN_MBR_CFG [21].RESERVED[31:29]	3
0xBB0130B4	VLAN_MBR_CFG [21].EXT_MBR[28:23]	6
0xBB0130B4	VLAN_MBR_CFG [21].RESERVED[22:7]	16
0xBB0130B4	VLAN_MBR_CFG [21].MBR[6:0]	7
0xBB0130B8	VLAN_MBR_CFG [22].RESERVED[31:27]	5
0xBB0130B8	VLAN_MBR_CFG [22].EVID[26:14]	13
0xBB0130B8	VLAN_MBR_CFG [22].METERIDX[13:9]	5
0xBB0130B8	VLAN_MBR_CFG [22].ENVLANPOL[8:8]	1
0xBB0130B8	VLAN_MBR_CFG [22].VBPRI[7:5]	3
0xBB0130B8	VLAN_MBR_CFG [22].VBPEN[4:4]	1
0xBB0130B8	VLAN_MBR_CFG [22].FID_MSTI[3:0]	4
0xBB0130BC	VLAN_MBR_CFG [22].RESERVED[31:29]	3
0xBB0130BC	VLAN_MBR_CFG [22].EXT_MBR[28:23]	6
0xBB0130BC	VLAN_MBR_CFG [22].RESERVED[22:7]	16
0xBB0130BC	VLAN_MBR_CFG [22].MBR[6:0]	7
0xBB0130C0	VLAN_MBR_CFG [23].RESERVED[31:27]	5
0xBB0130C0	VLAN_MBR_CFG [23].EVID[26:14]	13
0xBB0130C0	VLAN_MBR_CFG [23].METERIDX[13:9]	5
0xBB0130C0	VLAN_MBR_CFG [23].ENVLANPOL[8:8]	1
0xBB0130C0	VLAN_MBR_CFG [23].VBPRI[7:5]	3
0xBB0130C0	VLAN_MBR_CFG [23].VBPEN[4:4]	1
0xBB0130C0	VLAN_MBR_CFG [23].FID_MSTI[3:0]	4

Address	Register	Len
0xBB0130C4	VLAN_MBR_CFG [23].RESERVED[31:29]	3
0xBB0130C4	VLAN_MBR_CFG [23].EXT_MBR[28:23]	6
0xBB0130C4	VLAN_MBR_CFG [23].RESERVED[22:7]	16
0xBB0130C4	VLAN_MBR_CFG [23].MBR[6:0]	7
0xBB0130C8	VLAN_MBR_CFG [24].RESERVED[31:27]	5
0xBB0130C8	VLAN_MBR_CFG [24].EVID[26:14]	13
0xBB0130C8	VLAN_MBR_CFG [24].METERIDX[13:9]	5
0xBB0130C8	VLAN_MBR_CFG [24].ENVLANPOL[8:8]	1
0xBB0130C8	VLAN_MBR_CFG [24].VBPRI[7:5]	3
0xBB0130C8	VLAN_MBR_CFG [24].VBPEN[4:4]	1
0xBB0130C8	VLAN_MBR_CFG [24].FID_MSTI[3:0]	4
0xBB0130CC	VLAN_MBR_CFG [24].RESERVED[31:29]	3
0xBB0130CC	VLAN_MBR_CFG [24].EXT_MBR[28:23]	6
0xBB0130CC	VLAN_MBR_CFG [24].RESERVED[22:7]	16
0xBB0130CC	VLAN_MBR_CFG [24].MBR[6:0]	7
0xBB0130D0	VLAN_MBR_CFG [25].RESERVED[31:27]	5
0xBB0130D0	VLAN_MBR_CFG [25].EVID[26:14]	13
0xBB0130D0	VLAN_MBR_CFG [25].METERIDX[13:9]	5
0xBB0130D0	VLAN_MBR_CFG [25].ENVLANPOL[8:8]	1
0xBB0130D0	VLAN_MBR_CFG [25].VBPRI[7:5]	3
0xBB0130D0	VLAN_MBR_CFG [25].VBPEN[4:4]	1
0xBB0130D0	VLAN_MBR_CFG [25].FID_MSTI[3:0]	4
0xBB0130D4	VLAN_MBR_CFG [25].RESERVED[31:29]	3
0xBB0130D4	VLAN_MBR_CFG [25].EXT_MBR[28:23]	6
0xBB0130D4	VLAN_MBR_CFG [25].RESERVED[22:7]	16
0xBB0130D4	VLAN_MBR_CFG [25].MBR[6:0]	7
0xBB0130D8	VLAN_MBR_CFG [26].RESERVED[31:27]	5
0xBB0130D8	VLAN_MBR_CFG [26].EVID[26:14]	13
0xBB0130D8	VLAN_MBR_CFG [26].METERIDX[13:9]	5
0xBB0130D8	VLAN_MBR_CFG [26].ENVLANPOL[8:8]	1
0xBB0130D8	VLAN_MBR_CFG [26].VBPRI[7:5]	3
0xBB0130D8	VLAN_MBR_CFG [26].VBPEN[4:4]	1
0xBB0130D8	VLAN_MBR_CFG [26].FID_MSTI[3:0]	4
0xBB0130DC	VLAN_MBR_CFG [26].RESERVED[31:29]	3
0xBB0130DC	VLAN_MBR_CFG [26].EXT_MBR[28:23]	6
0xBB0130DC	VLAN_MBR_CFG [26].RESERVED[22:7]	16
0xBB0130DC	VLAN_MBR_CFG [26].MBR[6:0]	7
0xBB0130E0	VLAN_MBR_CFG [27].RESERVED[31:27]	5
0xBB0130E0	VLAN_MBR_CFG [27].EVID[26:14]	13
0xBB0130E0	VLAN_MBR_CFG [27].METERIDX[13:9]	5
0xBB0130E0	VLAN_MBR_CFG [27].ENVLANPOL[8:8]	1
0xBB0130E0	VLAN_MBR_CFG [27].VBPRI[7:5]	3
0xBB0130E0	VLAN_MBR_CFG [27].VBPEN[4:4]	1
0xBB0130E0	VLAN_MBR_CFG [27].FID_MSTI[3:0]	4
0xBB0130E4	VLAN_MBR_CFG [27].RESERVED[31:29]	3
0xBB0130E4	VLAN_MBR_CFG [27].EXT_MBR[28:23]	6



Address	Register	Len
0xBB0130E4	VLAN_MBR_CFG [27].RESERVED[22:7]	16
0xBB0130E4	VLAN_MBR_CFG [27].MBR[6:0]	7
0xBB0130E8	VLAN_MBR_CFG [28].RESERVED[31:27]	5
0xBB0130E8	VLAN_MBR_CFG [28].EVID[26:14]	13
0xBB0130E8	VLAN_MBR_CFG [28].METERIDX[13:9]	5
0xBB0130E8	VLAN_MBR_CFG [28].ENVLANPOL[8:8]	1
0xBB0130E8	VLAN_MBR_CFG [28].VBPRI[7:5]	3
0xBB0130E8	VLAN_MBR_CFG [28].VBPEN[4:4]	1
0xBB0130E8	VLAN_MBR_CFG [28].FID_MSTI[3:0]	4
0xBB0130EC	VLAN_MBR_CFG [28].RESERVED[31:29]	3
0xBB0130EC	VLAN_MBR_CFG [28].EXT_MBR[28:23]	6
0xBB0130EC	VLAN_MBR_CFG [28].RESERVED[22:7]	16
0xBB0130EC	VLAN_MBR_CFG [28].MBR[6:0]	7
0xBB0130F0	VLAN_MBR_CFG [29].RESERVED[31:27]	5
0xBB0130F0	VLAN_MBR_CFG [29].EVID[26:14]	13
0xBB0130F0	VLAN_MBR_CFG [29].METERIDX[13:9]	5
0xBB0130F0	VLAN_MBR_CFG [29].ENVLANPOL[8:8]	1
0xBB0130F0	VLAN_MBR_CFG [29].VBPRI[7:5]	3
0xBB0130F0	VLAN_MBR_CFG [29].VBPEN[4:4]	1
0xBB0130F0	VLAN_MBR_CFG [29].FID_MSTI[3:0]	4
0xBB0130F4	VLAN_MBR_CFG [29].RESERVED[31:29]	3
0xBB0130F4	VLAN_MBR_CFG [29].EXT_MBR[28:23]	6
0xBB0130F4	VLAN_MBR_CFG [29].RESERVED[22:7]	16
0xBB0130F4	VLAN_MBR_CFG [29].MBR[6:0]	7
0xBB0130F8	VLAN_MBR_CFG [30].RESERVED[31:27]	5
0xBB0130F8	VLAN_MBR_CFG [30].EVID[26:14]	13
0xBB0130F8	VLAN_MBR_CFG [30].METERIDX[13:9]	5
0xBB0130F8	VLAN_MBR_CFG [30].ENVLANPOL[8:8]	1
0xBB0130F8	VLAN_MBR_CFG [30].VBPRI[7:5]	3
0xBB0130F8	VLAN_MBR_CFG [30].VBPEN[4:4]	1
0xBB0130F8	VLAN_MBR_CFG [30].FID_MSTI[3:0]	4
0xBB0130FC	VLAN_MBR_CFG [30].RESERVED[31:29]	3
0xBB0130FC	VLAN_MBR_CFG [30].EXT_MBR[28:23]	6
0xBB0130FC	VLAN_MBR_CFG [30].RESERVED[22:7]	16
0xBB0130FC	VLAN_MBR_CFG [30].MBR[6:0]	7
0xBB013100	VLAN_MBR_CFG [31].RESERVED[31:27]	5
0xBB013100	VLAN_MBR_CFG [31].EVID[26:14]	13
0xBB013100	VLAN_MBR_CFG [31].METERIDX[13:9]	5
0xBB013100	VLAN_MBR_CFG [31].ENVLANPOL[8:8]	1
0xBB013100	VLAN_MBR_CFG [31].VBPRI[7:5]	3
0xBB013100	VLAN_MBR_CFG [31].VBPEN[4:4]	1
0xBB013100	VLAN_MBR_CFG [31].FID_MSTI[3:0]	4
0xBB013104	VLAN_MBR_CFG [31].RESERVED[31:29]	3
0xBB013104	VLAN_MBR_CFG [31].EXT_MBR[28:23]	6
0xBB013104	VLAN_MBR_CFG [31].RESERVED[22:7]	16
0xBB013104	VLAN_MBR_CFG [31].MBR[6:0]	7



Address	Register	Len
0xBB013108	VLAN_CTRL.RESERVED[31:5]	27
0xBB013108	VLAN_CTRL.VID_4095_TYPE[4:4]	1
0xBB013108	VLAN_CTRL.VID_0_TYPE[3:3]	1
0xBB013108	VLAN_CTRL.CFI_KEEP[2:2]	1
0xBB013108	VLAN_CTRL.TRANSPARENT_EN[1:1]	1
0xBB013108	VLAN_CTRL.VLAN_FILTERING[0:0]	1
0xBB01310C	VLAN_PB_FID [0].PBFID[3:0]	4
0xBB01310C	VLAN_PB_FID [1].PBFID[7:4]	4
0xBB01310C	VLAN_PB_FID [2].PBFID[11:8]	4
0xBB01310C	VLAN_PB_FID [3].PBFID[15:12]	4
0xBB01310C	VLAN_PB_FID [4].PBFID[19:16]	4
0xBB01310C	VLAN_PB_FID [5].PBFID[23:20]	4
0xBB01310C	VLAN_PB_FID [6].PBFID[27:24]	4
0xBB013110	VLAN_PB_FIDEN [0].PBFIDEN[0:0]	1
0xBB013110	VLAN_PB_FIDEN [1].PBFIDEN[1:1]	1
0xBB013110	VLAN_PB_FIDEN [2].PBFIDEN[2:2]	1
0xBB013110	VLAN_PB_FIDEN [3].PBFIDEN[3:3]	1
0xBB013110	VLAN_PB_FIDEN [4].PBFIDEN[4:4]	1
0xBB013110	VLAN_PB_FIDEN [5].PBFIDEN[5:5]	1
0xBB013110	VLAN_PB_FIDEN [6].PBFIDEN[6:6]	1
0xBB013114	VLAN_PB_VIDX [0].VIDX[4:0]	5
0xBB013114	VLAN_PB_VIDX [1].VIDX[9:5]	5
0xBB013114	VLAN_PB_VIDX [2].VIDX[14:10]	5
0xBB013114	VLAN_PB_VIDX [3].VIDX[19:15]	5
0xBB013114	VLAN_PB_VIDX [4].VIDX[24:20]	5
0xBB013114	VLAN_PB_VIDX [5].VIDX[29:25]	5
0xBB013118	VLAN_PB_VIDX [6].VIDX[4:0]	5
0xBB01311C	VLAN_EXT_VIDX [0].VIDX[4:0]	5
0xBB01311C	VLAN_EXT_VIDX [1].VIDX[9:5]	5
0xBB01311C	VLAN_EXT_VIDX [2].VIDX[14:10]	5
0xBB01311C	VLAN_EXT_VIDX [3].VIDX[19:15]	5
0xBB01311C	VLAN_EXT_VIDX [4].VIDX[24:20]	5
0xBB013120	VLAN_PPB_VLAN_VAL [0].RESERVED[31:18]	14
0xBB013120	VLAN_PPB_VLAN_VAL [0].ETHER_TYPE[17:2]	16
0xBB013120	VLAN_PPB_VLAN_VAL [0].FRAME_TYPE[1:0]	2
0xBB013124	VLAN_PPB_VLAN_VAL [1].RESERVED[31:18]	14
0xBB013124	VLAN_PPB_VLAN_VAL [1].ETHER_TYPE[17:2]	16
0xBB013124	VLAN_PPB_VLAN_VAL [1].FRAME_TYPE[1:0]	2
0xBB013128	VLAN_PPB_VLAN_VAL [2].RESERVED[31:18]	14
0xBB013128	VLAN_PPB_VLAN_VAL [2].ETHER_TYPE[17:2]	16
0xBB013128	VLAN_PPB_VLAN_VAL [2].FRAME_TYPE[1:0]	2
0xBB01312C	VLAN_PPB_VLAN_VAL [3].RESERVED[31:18]	14
0xBB01312C	VLAN_PPB_VLAN_VAL [3].ETHER_TYPE[17:2]	16
0xBB01312C	VLAN_PPB_VLAN_VAL [3].FRAME_TYPE[1:0]	2
0xBB013130	VLAN_PORT_PPB_VLAN [0][0].RESERVED[31:16]	16
0xBB013130	VLAN_PORT_PPB_VLAN [0][0].PPB_PRI[15:13]	3

Address	Register	Len
0xBB013130	VLAN_PORT_PPB_VLAN [0][0].RESERVED[12:6]	7
0xBB013130	VLAN_PORT_PPB_VLAN [0][0].PPB_VIDX[5:1]	5
0xBB013130	VLAN_PORT_PPB_VLAN [0][0].VALID[0:0]	1
0xBB013134	VLAN_PORT_PPB_VLAN [0][1].RESERVED[31:16]	16
0xBB013134	VLAN_PORT_PPB_VLAN [0][1].PPB_PRI[15:13]	3
0xBB013134	VLAN_PORT_PPB_VLAN [0][1].RESERVED[12:6]	7
0xBB013134	VLAN_PORT_PPB_VLAN [0][1].PPB_VIDX[5:1]	5
0xBB013134	VLAN_PORT_PPB_VLAN [0][1].VALID[0:0]	1
0xBB013138	VLAN_PORT_PPB_VLAN [0][2].RESERVED[31:16]	16
0xBB013138	VLAN_PORT_PPB_VLAN [0][2].PPB_PRI[15:13]	3
0xBB013138	VLAN_PORT_PPB_VLAN [0][2].RESERVED[12:6]	7
0xBB013138	VLAN_PORT_PPB_VLAN [0][2].PPB_VIDX[5:1]	5
0xBB013138	VLAN_PORT_PPB_VLAN [0][2].VALID[0:0]	1
0xBB01313C	VLAN_PORT_PPB_VLAN [0][3].RESERVED[31:16]	16
0xBB01313C	VLAN_PORT_PPB_VLAN [0][3].PPB_PRI[15:13]	3
0xBB01313C	VLAN_PORT_PPB_VLAN [0][3].RESERVED[12:6]	7
0xBB01313C	VLAN_PORT_PPB_VLAN [0][3].PPB_VIDX[5:1]	5
0xBB01313C	VLAN_PORT_PPB_VLAN [0][3].VALID[0:0]	1
0xBB013140	VLAN_PORT_PPB_VLAN [1][0].RESERVED[31:16]	16
0xBB013140	VLAN_PORT_PPB_VLAN [1][0].PPB_PRI[15:13]	3
0xBB013140	VLAN_PORT_PPB_VLAN [1][0].RESERVED[12:6]	7
0xBB013140	VLAN_PORT_PPB_VLAN [1][0].PPB_VIDX[5:1]	5
0xBB013140	VLAN_PORT_PPB_VLAN [1][0].VALID[0:0]	1
0xBB013144	VLAN_PORT_PPB_VLAN [1][1].RESERVED[31:16]	16
0xBB013144	VLAN_PORT_PPB_VLAN [1][1].PPB_PRI[15:13]	3
0xBB013144	VLAN_PORT_PPB_VLAN [1][1].RESERVED[12:6]	7
0xBB013144	VLAN_PORT_PPB_VLAN [1][1].PPB_VIDX[5:1]	5
0xBB013144	VLAN_PORT_PPB_VLAN [1][1].VALID[0:0]	1
0xBB013148	VLAN_PORT_PPB_VLAN [1][2].RESERVED[31:16]	16
0xBB013148	VLAN_PORT_PPB_VLAN [1][2].PPB_PRI[15:13]	3
0xBB013148	VLAN_PORT_PPB_VLAN [1][2].RESERVED[12:6]	7
0xBB013148	VLAN_PORT_PPB_VLAN [1][2].PPB_VIDX[5:1]	5
0xBB013148	VLAN_PORT_PPB_VLAN [1][2].VALID[0:0]	1
0xBB01314C	VLAN_PORT_PPB_VLAN [1][3].RESERVED[31:16]	16
0xBB01314C	VLAN_PORT_PPB_VLAN [1][3].PPB_PRI[15:13]	3
0xBB01314C	VLAN_PORT_PPB_VLAN [1][3].RESERVED[12:6]	7
0xBB01314C	VLAN_PORT_PPB_VLAN [1][3].PPB_VIDX[5:1]	5
0xBB01314C	VLAN_PORT_PPB_VLAN [1][3].VALID[0:0]	1
0xBB013150	VLAN_PORT_PPB_VLAN [2][0].RESERVED[31:16]	16
0xBB013150	VLAN_PORT_PPB_VLAN [2][0].PPB_PRI[15:13]	3
0xBB013150	VLAN_PORT_PPB_VLAN [2][0].RESERVED[12:6]	7
0xBB013150	VLAN_PORT_PPB_VLAN [2][0].PPB_VIDX[5:1]	5
0xBB013150	VLAN_PORT_PPB_VLAN [2][0].VALID[0:0]	1
0xBB013154	VLAN_PORT_PPB_VLAN [2][1].RESERVED[31:16]	16
0xBB013154	VLAN_PORT_PPB_VLAN [2][1].PPB_PRI[15:13]	3
0xBB013154	VLAN_PORT_PPB_VLAN [2][1].RESERVED[12:6]	7

Address	Register	Len
0xBB013154	VLAN_PORT_PPB_VLAN [2][1].PPB_VIDX[5:1]	5
0xBB013154	VLAN_PORT_PPB_VLAN [2][1].VALID[0:0]	1
0xBB013158	VLAN_PORT_PPB_VLAN [2][2].RESERVED[31:16]	16
0xBB013158	VLAN_PORT_PPB_VLAN [2][2].PPB_PRI[15:13]	3
0xBB013158	VLAN_PORT_PPB_VLAN [2][2].RESERVED[12:6]	7
0xBB013158	VLAN_PORT_PPB_VLAN [2][2].PPB_VIDX[5:1]	5
0xBB013158	VLAN_PORT_PPB_VLAN [2][2].VALID[0:0]	1
0xBB01315C	VLAN_PORT_PPB_VLAN [2][3].RESERVED[31:16]	16
0xBB01315C	VLAN_PORT_PPB_VLAN [2][3].PPB_PRI[15:13]	3
0xBB01315C	VLAN_PORT_PPB_VLAN [2][3].RESERVED[12:6]	7
0xBB01315C	VLAN_PORT_PPB_VLAN [2][3].PPB_VIDX[5:1]	5
0xBB01315C	VLAN_PORT_PPB_VLAN [2][3].VALID[0:0]	1
0xBB013160	VLAN_PORT_PPB_VLAN [3][0].RESERVED[31:16]	16
0xBB013160	VLAN_PORT_PPB_VLAN [3][0].PPB_PRI[15:13]	3
0xBB013160	VLAN_PORT_PPB_VLAN [3][0].RESERVED[12:6]	7
0xBB013160	VLAN_PORT_PPB_VLAN [3][0].PPB_VIDX[5:1]	5
0xBB013160	VLAN_PORT_PPB_VLAN [3][0].VALID[0:0]	1
0xBB013164	VLAN_PORT_PPB_VLAN [3][1].RESERVED[31:16]	16
0xBB013164	VLAN_PORT_PPB_VLAN [3][1].PPB_PRI[15:13]	3
0xBB013164	VLAN_PORT_PPB_VLAN [3][1].RESERVED[12:6]	7
0xBB013164	VLAN_PORT_PPB_VLAN [3][1].PPB_VIDX[5:1]	5
0xBB013164	VLAN_PORT_PPB_VLAN [3][1].VALID[0:0]	1
0xBB013168	VLAN_PORT_PPB_VLAN [3][2].RESERVED[31:16]	16
0xBB013168	VLAN_PORT_PPB_VLAN [3][2].PPB_PRI[15:13]	3
0xBB013168	VLAN_PORT_PPB_VLAN [3][2].RESERVED[12:6]	7
0xBB013168	VLAN_PORT_PPB_VLAN [3][2].PPB_VIDX[5:1]	5
0xBB013168	VLAN_PORT_PPB_VLAN [3][2].VALID[0:0]	1
0xBB01316C	VLAN_PORT_PPB_VLAN [3][3].RESERVED[31:16]	16
0xBB01316C	VLAN_PORT_PPB_VLAN [3][3].PPB_PRI[15:13]	3
0xBB01316C	VLAN_PORT_PPB_VLAN [3][3].RESERVED[12:6]	7
0xBB01316C	VLAN_PORT_PPB_VLAN [3][3].PPB_VIDX[5:1]	5
0xBB01316C	VLAN_PORT_PPB_VLAN [3][3].VALID[0:0]	1
0xBB013170	VLAN_PORT_PPB_VLAN [4][0].RESERVED[31:16]	16
0xBB013170	VLAN_PORT_PPB_VLAN [4][0].PPB_PRI[15:13]	3
0xBB013170	VLAN_PORT_PPB_VLAN [4][0].RESERVED[12:6]	7
0xBB013170	VLAN_PORT_PPB_VLAN [4][0].PPB_VIDX[5:1]	5
0xBB013170	VLAN_PORT_PPB_VLAN [4][0].VALID[0:0]	1
0xBB013174	VLAN_PORT_PPB_VLAN [4][1].RESERVED[31:16]	16
0xBB013174	VLAN_PORT_PPB_VLAN [4][1].PPB_PRI[15:13]	3
0xBB013174	VLAN_PORT_PPB_VLAN [4][1].RESERVED[12:6]	7
0xBB013174	VLAN_PORT_PPB_VLAN [4][1].PPB_VIDX[5:1]	5
0xBB013174	VLAN_PORT_PPB_VLAN [4][1].VALID[0:0]	1
0xBB013178	VLAN_PORT_PPB_VLAN [4][2].RESERVED[31:16]	16
0xBB013178	VLAN_PORT_PPB_VLAN [4][2].PPB_PRI[15:13]	3
0xBB013178	VLAN_PORT_PPB_VLAN [4][2].RESERVED[12:6]	7
0xBB013178	VLAN_PORT_PPB_VLAN [4][2].PPB_VIDX[5:1]	5

Address	Register	Len
0xBB013178	VLAN_PORT_PPB_VLAN [4][2].VALID[0:0]	1
0xBB01317C	VLAN_PORT_PPB_VLAN [4][3].RESERVED[31:16]	16
0xBB01317C	VLAN_PORT_PPB_VLAN [4][3].PPB_PRI[15:13]	3
0xBB01317C	VLAN_PORT_PPB_VLAN [4][3].RESERVED[12:6]	7
0xBB01317C	VLAN_PORT_PPB_VLAN [4][3].PPB_VIDX[5:1]	5
0xBB01317C	VLAN_PORT_PPB_VLAN [4][3].VALID[0:0]	1
0xBB013180	VLAN_PORT_PPB_VLAN [5][0].RESERVED[31:16]	16
0xBB013180	VLAN_PORT_PPB_VLAN [5][0].PPB_PRI[15:13]	3
0xBB013180	VLAN_PORT_PPB_VLAN [5][0].RESERVED[12:6]	7
0xBB013180	VLAN_PORT_PPB_VLAN [5][0].PPB_VIDX[5:1]	5
0xBB013180	VLAN_PORT_PPB_VLAN [5][0].VALID[0:0]	1
0xBB013184	VLAN_PORT_PPB_VLAN [5][1].RESERVED[31:16]	16
0xBB013184	VLAN_PORT_PPB_VLAN [5][1].PPB_PRI[15:13]	3
0xBB013184	VLAN_PORT_PPB_VLAN [5][1].RESERVED[12:6]	7
0xBB013184	VLAN_PORT_PPB_VLAN [5][1].PPB_VIDX[5:1]	5
0xBB013184	VLAN_PORT_PPB_VLAN [5][1].VALID[0:0]	1
0xBB013188	VLAN_PORT_PPB_VLAN [5][2].RESERVED[31:16]	16
0xBB013188	VLAN_PORT_PPB_VLAN [5][2].PPB_PRI[15:13]	3
0xBB013188	VLAN_PORT_PPB_VLAN [5][2].RESERVED[12:6]	7
0xBB013188	VLAN_PORT_PPB_VLAN [5][2].PPB_VIDX[5:1]	5
0xBB013188	VLAN_PORT_PPB_VLAN [5][2].VALID[0:0]	1
0xBB01318C	VLAN_PORT_PPB_VLAN [5][3].RESERVED[31:16]	16
0xBB01318C	VLAN_PORT_PPB_VLAN [5][3].PPB_PRI[15:13]	3
0xBB01318C	VLAN_PORT_PPB_VLAN [5][3].RESERVED[12:6]	7
0xBB01318C	VLAN_PORT_PPB_VLAN [5][3].PPB_VIDX[5:1]	5
0xBB01318C	VLAN_PORT_PPB_VLAN [5][3].VALID[0:0]	1
0xBB013190	VLAN_PORT_PPB_VLAN [6][0].RESERVED[31:16]	16
0xBB013190	VLAN_PORT_PPB_VLAN [6][0].PPB_PRI[15:13]	3
0xBB013190	VLAN_PORT_PPB_VLAN [6][0].RESERVED[12:6]	7
0xBB013190	VLAN_PORT_PPB_VLAN [6][0].PPB_VIDX[5:1]	5
0xBB013190	VLAN_PORT_PPB_VLAN [6][0].VALID[0:0]	1
0xBB013194	VLAN_PORT_PPB_VLAN [6][1].RESERVED[31:16]	16
0xBB013194	VLAN_PORT_PPB_VLAN [6][1].PPB_PRI[15:13]	3
0xBB013194	VLAN_PORT_PPB_VLAN [6][1].RESERVED[12:6]	7
0xBB013194	VLAN_PORT_PPB_VLAN [6][1].PPB_VIDX[5:1]	5
0xBB013194	VLAN_PORT_PPB_VLAN [6][1].VALID[0:0]	1
0xBB013198	VLAN_PORT_PPB_VLAN [6][2].RESERVED[31:16]	16
0xBB013198	VLAN_PORT_PPB_VLAN [6][2].PPB_PRI[15:13]	3
0xBB013198	VLAN_PORT_PPB_VLAN [6][2].RESERVED[12:6]	7
0xBB013198	VLAN_PORT_PPB_VLAN [6][2].PPB_VIDX[5:1]	5
0xBB013198	VLAN_PORT_PPB_VLAN [6][2].VALID[0:0]	1
0xBB01319C	VLAN_PORT_PPB_VLAN [6][3].RESERVED[31:16]	16
0xBB01319C	VLAN_PORT_PPB_VLAN [6][3].PPB_PRI[15:13]	3
0xBB01319C	VLAN_PORT_PPB_VLAN [6][3].RESERVED[12:6]	7
0xBB01319C	VLAN_PORT_PPB_VLAN [6][3].PPB_VIDX[5:1]	5
0xBB01319C	VLAN_PORT_PPB_VLAN [6][3].VALID[0:0]	1

Address	Register	Len
0xBB0131A0	RGF_VER_ALE_CVLAN.REGFILE_VER[31:0]	32
0xBB0131A4	RSVD_ALE_CVLAN [0].RSVD_MEM[31:0]	32
0xBB0131A8	RSVD_ALE_CVLAN [1].RSVD_MEM[31:0]	32
0xBB0131AC	RSVD_ALE_CVLAN [2].RSVD_MEM[31:0]	32
0xBB0131B0	RSVD_ALE_CVLAN [3].RSVD_MEM[31:0]	32
0xBB0131B4	RSVD_ALE_CVLAN [4].RSVD_MEM[31:0]	32
0xBB0131B8	RSVD_ALE_CVLAN [5].RSVD_MEM[31:0]	32
0xBB0131BC	RSVD_ALE_CVLAN [6].RSVD_MEM[31:0]	32
0xBB0131C0	RSVD_ALE_CVLAN [7].RSVD_MEM[31:0]	32
0xBB0131C4	RSVD_ALE_CVLAN [8].RSVD_MEM[31:0]	32
0xBB0131C8	RSVD_ALE_CVLAN [9].RSVD_MEM[31:0]	32
0xBB0131CC	RSVD_ALE_CVLAN [10].RSVD_MEM[31:0]	32
0xBB0131D0	RSVD_ALE_CVLAN [11].RSVD_MEM[31:0]	32
0xBB0131D4	RSVD_ALE_CVLAN [12].RSVD_MEM[31:0]	32
0xBB0131D8	RSVD_ALE_CVLAN [13].RSVD_MEM[31:0]	32
0xBB0131DC	RSVD_ALE_CVLAN [14].RSVD_MEM[31:0]	32
0xBB0131E0	RSVD_ALE_CVLAN [15].RSVD_MEM[31:0]	32
0xBB014000	SVLAN_C2S [0].RESERVED[31:26]	6
0xBB014000	SVLAN_C2S [0].EVID[25:13]	13
0xBB014000	SVLAN_C2S [0].C2SENPMASK[12:6]	7
0xBB014000	SVLAN_C2S [0].SVIDX[5:0]	6
0xBB014004	SVLAN_C2S [1].RESERVED[31:26]	6
0xBB014004	SVLAN_C2S [1].EVID[25:13]	13
0xBB014004	SVLAN_C2S [1].C2SENPMASK[12:6]	7
0xBB014004	SVLAN_C2S [1].SVIDX[5:0]	6
0xBB014008	SVLAN_C2S [2].RESERVED[31:26]	6
0xBB014008	SVLAN_C2S [2].EVID[25:13]	13
0xBB014008	SVLAN_C2S [2].C2SENPMASK[12:6]	7
0xBB014008	SVLAN_C2S [2].SVIDX[5:0]	6
0xBB01400C	SVLAN_C2S [3].RESERVED[31:26]	6
0xBB01400C	SVLAN_C2S [3].EVID[25:13]	13
0xBB01400C	SVLAN_C2S [3].C2SENPMASK[12:6]	7
0xBB01400C	SVLAN_C2S [3].SVIDX[5:0]	6
0xBB014010	SVLAN_C2S [4].RESERVED[31:26]	6
0xBB014010	SVLAN_C2S [4].EVID[25:13]	13
0xBB014010	SVLAN_C2S [4].C2SENPMASK[12:6]	7
0xBB014010	SVLAN_C2S [4].SVIDX[5:0]	6
0xBB014014	SVLAN_C2S [5].RESERVED[31:26]	6
0xBB014014	SVLAN_C2S [5].EVID[25:13]	13
0xBB014014	SVLAN_C2S [5].C2SENPMASK[12:6]	7
0xBB014014	SVLAN_C2S [5].SVIDX[5:0]	6
0xBB014018	SVLAN_C2S [6].RESERVED[31:26]	6
0xBB014018	SVLAN_C2S [6].EVID[25:13]	13
0xBB014018	SVLAN_C2S [6].C2SENPMASK[12:6]	7
0xBB014018	SVLAN_C2S [6].SVIDX[5:0]	6
0xBB01401C	SVLAN_C2S [7].RESERVED[31:26]	6

Address	Register	Len
0xBB01401C	SVLAN_C2S [7].EVID[25:13]	13
0xBB01401C	SVLAN_C2S [7].C2SENPMASK[12:6]	7
0xBB01401C	SVLAN_C2S [7].SVIDX[5:0]	6
0xBB014020	SVLAN_C2S [8].RESERVED[31:26]	6
0xBB014020	SVLAN_C2S [8].EVID[25:13]	13
0xBB014020	SVLAN_C2S [8].C2SENPMASK[12:6]	7
0xBB014020	SVLAN_C2S [8].SVIDX[5:0]	6
0xBB014024	SVLAN_C2S [9].RESERVED[31:26]	6
0xBB014024	SVLAN_C2S [9].EVID[25:13]	13
0xBB014024	SVLAN_C2S [9].C2SENPMASK[12:6]	7
0xBB014024	SVLAN_C2S [9].SVIDX[5:0]	6
0xBB014028	SVLAN_C2S [10].RESERVED[31:26]	6
0xBB014028	SVLAN_C2S [10].EVID[25:13]	13
0xBB014028	SVLAN_C2S [10].C2SENPMASK[12:6]	7
0xBB014028	SVLAN_C2S [10].SVIDX[5:0]	6
0xBB01402C	SVLAN_C2S [11].RESERVED[31:26]	6
0xBB01402C	SVLAN_C2S [11].EVID[25:13]	13
0xBB01402C	SVLAN_C2S [11].C2SENPMASK[12:6]	7
0xBB01402C	SVLAN_C2S [11].SVIDX[5:0]	6
0xBB014030	SVLAN_C2S [12].RESERVED[31:26]	6
0xBB014030	SVLAN_C2S [12].EVID[25:13]	13
0xBB014030	SVLAN_C2S [12].C2SENPMASK[12:6]	7
0xBB014030	SVLAN_C2S [12].SVIDX[5:0]	6
0xBB014034	SVLAN_C2S [13].RESERVED[31:26]	6
0xBB014034	SVLAN_C2S [13].EVID[25:13]	13
0xBB014034	SVLAN_C2S [13].C2SENPMASK[12:6]	7
0xBB014034	SVLAN_C2S [13].SVIDX[5:0]	6
0xBB014038	SVLAN_C2S [14].RESERVED[31:26]	6
0xBB014038	SVLAN_C2S [14].EVID[25:13]	13
0xBB014038	SVLAN_C2S [14].C2SENPMASK[12:6]	7
0xBB014038	SVLAN_C2S [14].SVIDX[5:0]	6
0xBB01403C	SVLAN_C2S [15].RESERVED[31:26]	6
0xBB01403C	SVLAN_C2S [15].EVID[25:13]	13
0xBB01403C	SVLAN_C2S [15].C2SENPMASK[12:6]	7
0xBB01403C	SVLAN_C2S [15].SVIDX[5:0]	6
0xBB014040	SVLAN_C2S [16].RESERVED[31:26]	6
0xBB014040	SVLAN_C2S [16].EVID[25:13]	13
0xBB014040	SVLAN_C2S [16].C2SENPMASK[12:6]	7
0xBB014040	SVLAN_C2S [16].SVIDX[5:0]	6
0xBB014044	SVLAN_C2S [17].RESERVED[31:26]	6
0xBB014044	SVLAN_C2S [17].EVID[25:13]	13
0xBB014044	SVLAN_C2S [17].C2SENPMASK[12:6]	7
0xBB014044	SVLAN_C2S [17].SVIDX[5:0]	6
0xBB014048	SVLAN_C2S [18].RESERVED[31:26]	6
0xBB014048	SVLAN_C2S [18].EVID[25:13]	13
0xBB014048	SVLAN_C2S [18].C2SENPMASK[12:6]	7

Address	Register	Len
0xBB014048	SVLAN_C2S [18].SVIDX[5:0]	6
0xBB01404C	SVLAN_C2S [19].RESERVED[31:26]	6
0xBB01404C	SVLAN_C2S [19].EVID[25:13]	13
0xBB01404C	SVLAN_C2S [19].C2SENPMASK[12:6]	7
0xBB01404C	SVLAN_C2S [19].SVIDX[5:0]	6
0xBB014050	SVLAN_C2S [20].RESERVED[31:26]	6
0xBB014050	SVLAN_C2S [20].EVID[25:13]	13
0xBB014050	SVLAN_C2S [20].C2SENPMASK[12:6]	7
0xBB014050	SVLAN_C2S [20].SVIDX[5:0]	6
0xBB014054	SVLAN_C2S [21].RESERVED[31:26]	6
0xBB014054	SVLAN_C2S [21].EVID[25:13]	13
0xBB014054	SVLAN_C2S [21].C2SENPMASK[12:6]	7
0xBB014054	SVLAN_C2S [21].SVIDX[5:0]	6
0xBB014058	SVLAN_C2S [22].RESERVED[31:26]	6
0xBB014058	SVLAN_C2S [22].EVID[25:13]	13
0xBB014058	SVLAN_C2S [22].C2SENPMASK[12:6]	7
0xBB014058	SVLAN_C2S [22].SVIDX[5:0]	6
0xBB01405C	SVLAN_C2S [23].RESERVED[31:26]	6
0xBB01405C	SVLAN_C2S [23].EVID[25:13]	13
0xBB01405C	SVLAN_C2S [23].C2SENPMASK[12:6]	7
0xBB01405C	SVLAN_C2S [23].SVIDX[5:0]	6
0xBB014060	SVLAN_C2S [24].RESERVED[31:26]	6
0xBB014060	SVLAN_C2S [24].EVID[25:13]	13
0xBB014060	SVLAN_C2S [24].C2SENPMASK[12:6]	7
0xBB014060	SVLAN_C2S [24].SVIDX[5:0]	6
0xBB014064	SVLAN_C2S [25].RESERVED[31:26]	6
0xBB014064	SVLAN_C2S [25].EVID[25:13]	13
0xBB014064	SVLAN_C2S [25].C2SENPMASK[12:6]	7
0xBB014064	SVLAN_C2S [25].SVIDX[5:0]	6
0xBB014068	SVLAN_C2S [26].RESERVED[31:26]	6
0xBB014068	SVLAN_C2S [26].EVID[25:13]	13
0xBB014068	SVLAN_C2S [26].C2SENPMASK[12:6]	7
0xBB014068	SVLAN_C2S [26].SVIDX[5:0]	6
0xBB01406C	SVLAN_C2S [27].RESERVED[31:26]	6
0xBB01406C	SVLAN_C2S [27].EVID[25:13]	13
0xBB01406C	SVLAN_C2S [27].C2SENPMASK[12:6]	7
0xBB01406C	SVLAN_C2S [27].SVIDX[5:0]	6
0xBB014070	SVLAN_C2S [28].RESERVED[31:26]	6
0xBB014070	SVLAN_C2S [28].EVID[25:13]	13
0xBB014070	SVLAN_C2S [28].C2SENPMASK[12:6]	7
0xBB014070	SVLAN_C2S [28].SVIDX[5:0]	6
0xBB014074	SVLAN_C2S [29].RESERVED[31:26]	6
0xBB014074	SVLAN_C2S [29].EVID[25:13]	13
0xBB014074	SVLAN_C2S [29].C2SENPMASK[12:6]	7
0xBB014074	SVLAN_C2S [29].SVIDX[5:0]	6
0xBB014078	SVLAN_C2S [30].RESERVED[31:26]	6



Address	Register	Len
0xBB014078	SVLAN_C2S [30].EVID[25:13]	13
0xBB014078	SVLAN_C2S [30].C2SENPMASK[12:6]	7
0xBB014078	SVLAN_C2S [30].SVIDX[5:0]	6
0xBB01407C	SVLAN_C2S [31].RESERVED[31:26]	6
0xBB01407C	SVLAN_C2S [31].EVID[25:13]	13
0xBB01407C	SVLAN_C2S [31].C2SENPMASK[12:6]	7
0xBB01407C	SVLAN_C2S [31].SVIDX[5:0]	6
0xBB014080	SVLAN_C2S [32].RESERVED[31:26]	6
0xBB014080	SVLAN_C2S [32].EVID[25:13]	13
0xBB014080	SVLAN_C2S [32].C2SENPMASK[12:6]	7
0xBB014080	SVLAN_C2S [32].SVIDX[5:0]	6
0xBB014084	SVLAN_C2S [33].RESERVED[31:26]	6
0xBB014084	SVLAN_C2S [33].EVID[25:13]	13
0xBB014084	SVLAN_C2S [33].C2SENPMASK[12:6]	7
0xBB014084	SVLAN_C2S [33].SVIDX[5:0]	6
0xBB014088	SVLAN_C2S [34].RESERVED[31:26]	6
0xBB014088	SVLAN_C2S [34].EVID[25:13]	13
0xBB014088	SVLAN_C2S [34].C2SENPMASK[12:6]	7
0xBB014088	SVLAN_C2S [34].SVIDX[5:0]	6
0xBB01408C	SVLAN_C2S [35].RESERVED[31:26]	6
0xBB01408C	SVLAN_C2S [35].EVID[25:13]	13
0xBB01408C	SVLAN_C2S [35].C2SENPMASK[12:6]	7
0xBB01408C	SVLAN_C2S [35].SVIDX[5:0]	6
0xBB014090	SVLAN_C2S [36].RESERVED[31:26]	6
0xBB014090	SVLAN_C2S [36].EVID[25:13]	13
0xBB014090	SVLAN_C2S [36].C2SENPMASK[12:6]	7
0xBB014090	SVLAN_C2S [36].SVIDX[5:0]	6
0xBB014094	SVLAN_C2S [37].RESERVED[31:26]	6
0xBB014094	SVLAN_C2S [37].EVID[25:13]	13
0xBB014094	SVLAN_C2S [37].C2SENPMASK[12:6]	7
0xBB014094	SVLAN_C2S [37].SVIDX[5:0]	6
0xBB014098	SVLAN_C2S [38].RESERVED[31:26]	6
0xBB014098	SVLAN_C2S [38].EVID[25:13]	13
0xBB014098	SVLAN_C2S [38].C2SENPMASK[12:6]	7
0xBB014098	SVLAN_C2S [38].SVIDX[5:0]	6
0xBB01409C	SVLAN_C2S [39].RESERVED[31:26]	6
0xBB01409C	SVLAN_C2S [39].EVID[25:13]	13
0xBB01409C	SVLAN_C2S [39].C2SENPMASK[12:6]	7
0xBB01409C	SVLAN_C2S [39].SVIDX[5:0]	6
0xBB0140A0	SVLAN_C2S [40].RESERVED[31:26]	6
0xBB0140A0	SVLAN_C2S [40].EVID[25:13]	13
0xBB0140A0	SVLAN_C2S [40].C2SENPMASK[12:6]	7
0xBB0140A0	SVLAN_C2S [40].SVIDX[5:0]	6
0xBB0140A4	SVLAN_C2S [41].RESERVED[31:26]	6
0xBB0140A4	SVLAN_C2S [41].EVID[25:13]	13
0xBB0140A4	SVLAN_C2S [41].C2SENPMASK[12:6]	7



Address	Register	Len
0xBB0140A4	SVLAN_C2S [41].SVIDX[5:0]	6
0xBB0140A8	SVLAN_C2S [42].RESERVED[31:26]	6
0xBB0140A8	SVLAN_C2S [42].EVID[25:13]	13
0xBB0140A8	SVLAN_C2S [42].C2SENPMASK[12:6]	7
0xBB0140A8	SVLAN_C2S [42].SVIDX[5:0]	6
0xBB0140AC	SVLAN_C2S [43].RESERVED[31:26]	6
0xBB0140AC	SVLAN_C2S [43].EVID[25:13]	13
0xBB0140AC	SVLAN_C2S [43].C2SENPMASK[12:6]	7
0xBB0140AC	SVLAN_C2S [43].SVIDX[5:0]	6
0xBB0140B0	SVLAN_C2S [44].RESERVED[31:26]	6
0xBB0140B0	SVLAN_C2S [44].EVID[25:13]	13
0xBB0140B0	SVLAN_C2S [44].C2SENPMASK[12:6]	7
0xBB0140B0	SVLAN_C2S [44].SVIDX[5:0]	6
0xBB0140B4	SVLAN_C2S [45].RESERVED[31:26]	6
0xBB0140B4	SVLAN_C2S [45].EVID[25:13]	13
0xBB0140B4	SVLAN_C2S [45].C2SENPMASK[12:6]	7
0xBB0140B4	SVLAN_C2S [45].SVIDX[5:0]	6
0xBB0140B8	SVLAN_C2S [46].RESERVED[31:26]	6
0xBB0140B8	SVLAN_C2S [46].EVID[25:13]	13
0xBB0140B8	SVLAN_C2S [46].C2SENPMASK[12:6]	7
0xBB0140B8	SVLAN_C2S [46].SVIDX[5:0]	6
0xBB0140BC	SVLAN_C2S [47].RESERVED[31:26]	6
0xBB0140BC	SVLAN_C2S [47].EVID[25:13]	13
0xBB0140BC	SVLAN_C2S [47].C2SENPMASK[12:6]	7
0xBB0140BC	SVLAN_C2S [47].SVIDX[5:0]	6
0xBB0140C0	SVLAN_C2S [48].RESERVED[31:26]	6
0xBB0140C0	SVLAN_C2S [48].EVID[25:13]	13
0xBB0140C0	SVLAN_C2S [48].C2SENPMASK[12:6]	7
0xBB0140C0	SVLAN_C2S [48].SVIDX[5:0]	6
0xBB0140C4	SVLAN_C2S [49].RESERVED[31:26]	6
0xBB0140C4	SVLAN_C2S [49].EVID[25:13]	13
0xBB0140C4	SVLAN_C2S [49].C2SENPMASK[12:6]	7
0xBB0140C4	SVLAN_C2S [49].SVIDX[5:0]	6
0xBB0140C8	SVLAN_C2S [50].RESERVED[31:26]	6
0xBB0140C8	SVLAN_C2S [50].EVID[25:13]	13
0xBB0140C8	SVLAN_C2S [50].C2SENPMASK[12:6]	7
0xBB0140C8	SVLAN_C2S [50].SVIDX[5:0]	6
0xBB0140CC	SVLAN_C2S [51].RESERVED[31:26]	6
0xBB0140CC	SVLAN_C2S [51].EVID[25:13]	13
0xBB0140CC	SVLAN_C2S [51].C2SENPMASK[12:6]	7
0xBB0140CC	SVLAN_C2S [51].SVIDX[5:0]	6
0xBB0140D0	SVLAN_C2S [52].RESERVED[31:26]	6
0xBB0140D0	SVLAN_C2S [52].EVID[25:13]	13
0xBB0140D0	SVLAN_C2S [52].C2SENPMASK[12:6]	7
0xBB0140D0	SVLAN_C2S [52].SVIDX[5:0]	6
0xBB0140D4	SVLAN_C2S [53].RESERVED[31:26]	6

Address	Register	Len
0xBB0140D4	SVLAN_C2S [53].EVID[25:13]	13
0xBB0140D4	SVLAN_C2S [53].C2SENPMASK[12:6]	7
0xBB0140D4	SVLAN_C2S [53].SVIDX[5:0]	6
0xBB0140D8	SVLAN_C2S [54].RESERVED[31:26]	6
0xBB0140D8	SVLAN_C2S [54].EVID[25:13]	13
0xBB0140D8	SVLAN_C2S [54].C2SENPMASK[12:6]	7
0xBB0140D8	SVLAN_C2S [54].SVIDX[5:0]	6
0xBB0140DC	SVLAN_C2S [55].RESERVED[31:26]	6
0xBB0140DC	SVLAN_C2S [55].EVID[25:13]	13
0xBB0140DC	SVLAN_C2S [55].C2SENPMASK[12:6]	7
0xBB0140DC	SVLAN_C2S [55].SVIDX[5:0]	6
0xBB0140E0	SVLAN_C2S [56].RESERVED[31:26]	6
0xBB0140E0	SVLAN_C2S [56].EVID[25:13]	13
0xBB0140E0	SVLAN_C2S [56].C2SENPMASK[12:6]	7
0xBB0140E0	SVLAN_C2S [56].SVIDX[5:0]	6
0xBB0140E4	SVLAN_C2S [57].RESERVED[31:26]	6
0xBB0140E4	SVLAN_C2S [57].EVID[25:13]	13
0xBB0140E4	SVLAN_C2S [57].C2SENPMASK[12:6]	7
0xBB0140E4	SVLAN_C2S [57].SVIDX[5:0]	6
0xBB0140E8	SVLAN_C2S [58].RESERVED[31:26]	6
0xBB0140E8	SVLAN_C2S [58].EVID[25:13]	13
0xBB0140E8	SVLAN_C2S [58].C2SENPMASK[12:6]	7
0xBB0140E8	SVLAN_C2S [58].SVIDX[5:0]	6
0xBB0140EC	SVLAN_C2S [59].RESERVED[31:26]	6
0xBB0140EC	SVLAN_C2S [59].EVID[25:13]	13
0xBB0140EC	SVLAN_C2S [59].C2SENPMASK[12:6]	7
0xBB0140EC	SVLAN_C2S [59].SVIDX[5:0]	6
0xBB0140F0	SVLAN_C2S [60].RESERVED[31:26]	6
0xBB0140F0	SVLAN_C2S [60].EVID[25:13]	13
0xBB0140F0	SVLAN_C2S [60].C2SENPMASK[12:6]	7
0xBB0140F0	SVLAN_C2S [60].SVIDX[5:0]	6
0xBB0140F4	SVLAN_C2S [61].RESERVED[31:26]	6
0xBB0140F4	SVLAN_C2S [61].EVID[25:13]	13
0xBB0140F4	SVLAN_C2S [61].C2SENPMASK[12:6]	7
0xBB0140F4	SVLAN_C2S [61].SVIDX[5:0]	6
0xBB0140F8	SVLAN_C2S [62].RESERVED[31:26]	6
0xBB0140F8	SVLAN_C2S [62].EVID[25:13]	13
0xBB0140F8	SVLAN_C2S [62].C2SENPMASK[12:6]	7
0xBB0140F8	SVLAN_C2S [62].SVIDX[5:0]	6
0xBB0140FC	SVLAN_C2S [63].RESERVED[31:26]	6
0xBB0140FC	SVLAN_C2S [63].EVID[25:13]	13
0xBB0140FC	SVLAN_C2S [63].C2SENPMASK[12:6]	7
0xBB0140FC	SVLAN_C2S [63].SVIDX[5:0]	6
0xBB014100	SVLAN_C2S [64].RESERVED[31:26]	6
0xBB014100	SVLAN_C2S [64].EVID[25:13]	13
0xBB014100	SVLAN_C2S [64].C2SENPMASK[12:6]	7

Address	Register	Len
0xBB014100	SVLAN_C2S [64].SVIDX[5:0]	6
0xBB014104	SVLAN_C2S [65].RESERVED[31:26]	6
0xBB014104	SVLAN_C2S [65].EVID[25:13]	13
0xBB014104	SVLAN_C2S [65].C2SENPMASK[12:6]	7
0xBB014104	SVLAN_C2S [65].SVIDX[5:0]	6
0xBB014108	SVLAN_C2S [66].RESERVED[31:26]	6
0xBB014108	SVLAN_C2S [66].EVID[25:13]	13
0xBB014108	SVLAN_C2S [66].C2SENPMASK[12:6]	7
0xBB014108	SVLAN_C2S [66].SVIDX[5:0]	6
0xBB01410C	SVLAN_C2S [67].RESERVED[31:26]	6
0xBB01410C	SVLAN_C2S [67].EVID[25:13]	13
0xBB01410C	SVLAN_C2S [67].C2SENPMASK[12:6]	7
0xBB01410C	SVLAN_C2S [67].SVIDX[5:0]	6
0xBB014110	SVLAN_C2S [68].RESERVED[31:26]	6
0xBB014110	SVLAN_C2S [68].EVID[25:13]	13
0xBB014110	SVLAN_C2S [68].C2SENPMASK[12:6]	7
0xBB014110	SVLAN_C2S [68].SVIDX[5:0]	6
0xBB014114	SVLAN_C2S [69].RESERVED[31:26]	6
0xBB014114	SVLAN_C2S [69].EVID[25:13]	13
0xBB014114	SVLAN_C2S [69].C2SENPMASK[12:6]	7
0xBB014114	SVLAN_C2S [69].SVIDX[5:0]	6
0xBB014118	SVLAN_C2S [70].RESERVED[31:26]	6
0xBB014118	SVLAN_C2S [70].EVID[25:13]	13
0xBB014118	SVLAN_C2S [70].C2SENPMASK[12:6]	7
0xBB014118	SVLAN_C2S [70].SVIDX[5:0]	6
0xBB01411C	SVLAN_C2S [71].RESERVED[31:26]	6
0xBB01411C	SVLAN_C2S [71].EVID[25:13]	13
0xBB01411C	SVLAN_C2S [71].C2SENPMASK[12:6]	7
0xBB01411C	SVLAN_C2S [71].SVIDX[5:0]	6
0xBB014120	SVLAN_C2S [72].RESERVED[31:26]	6
0xBB014120	SVLAN_C2S [72].EVID[25:13]	13
0xBB014120	SVLAN_C2S [72].C2SENPMASK[12:6]	7
0xBB014120	SVLAN_C2S [72].SVIDX[5:0]	6
0xBB014124	SVLAN_C2S [73].RESERVED[31:26]	6
0xBB014124	SVLAN_C2S [73].EVID[25:13]	13
0xBB014124	SVLAN_C2S [73].C2SENPMASK[12:6]	7
0xBB014124	SVLAN_C2S [73].SVIDX[5:0]	6
0xBB014128	SVLAN_C2S [74].RESERVED[31:26]	6
0xBB014128	SVLAN_C2S [74].EVID[25:13]	13
0xBB014128	SVLAN_C2S [74].C2SENPMASK[12:6]	7
0xBB014128	SVLAN_C2S [74].SVIDX[5:0]	6
0xBB01412C	SVLAN_C2S [75].RESERVED[31:26]	6
0xBB01412C	SVLAN_C2S [75].EVID[25:13]	13
0xBB01412C	SVLAN_C2S [75].C2SENPMASK[12:6]	7
0xBB01412C	SVLAN_C2S [75].SVIDX[5:0]	6
0xBB014130	SVLAN_C2S [76].RESERVED[31:26]	6

Address	Register	Len
0xBB014130	SVLAN_C2S [76].EVID[25:13]	13
0xBB014130	SVLAN_C2S [76].C2SENPMASK[12:6]	7
0xBB014130	SVLAN_C2S [76].SVIDX[5:0]	6
0xBB014134	SVLAN_C2S [77].RESERVED[31:26]	6
0xBB014134	SVLAN_C2S [77].EVID[25:13]	13
0xBB014134	SVLAN_C2S [77].C2SENPMASK[12:6]	7
0xBB014134	SVLAN_C2S [77].SVIDX[5:0]	6
0xBB014138	SVLAN_C2S [78].RESERVED[31:26]	6
0xBB014138	SVLAN_C2S [78].EVID[25:13]	13
0xBB014138	SVLAN_C2S [78].C2SENPMASK[12:6]	7
0xBB014138	SVLAN_C2S [78].SVIDX[5:0]	6
0xBB01413C	SVLAN_C2S [79].RESERVED[31:26]	6
0xBB01413C	SVLAN_C2S [79].EVID[25:13]	13
0xBB01413C	SVLAN_C2S [79].C2SENPMASK[12:6]	7
0xBB01413C	SVLAN_C2S [79].SVIDX[5:0]	6
0xBB014140	SVLAN_C2S [80].RESERVED[31:26]	6
0xBB014140	SVLAN_C2S [80].EVID[25:13]	13
0xBB014140	SVLAN_C2S [80].C2SENPMASK[12:6]	7
0xBB014140	SVLAN_C2S [80].SVIDX[5:0]	6
0xBB014144	SVLAN_C2S [81].RESERVED[31:26]	6
0xBB014144	SVLAN_C2S [81].EVID[25:13]	13
0xBB014144	SVLAN_C2S [81].C2SENPMASK[12:6]	7
0xBB014144	SVLAN_C2S [81].SVIDX[5:0]	6
0xBB014148	SVLAN_C2S [82].RESERVED[31:26]	6
0xBB014148	SVLAN_C2S [82].EVID[25:13]	13
0xBB014148	SVLAN_C2S [82].C2SENPMASK[12:6]	7
0xBB014148	SVLAN_C2S [82].SVIDX[5:0]	6
0xBB01414C	SVLAN_C2S [83].RESERVED[31:26]	6
0xBB01414C	SVLAN_C2S [83].EVID[25:13]	13
0xBB01414C	SVLAN_C2S [83].C2SENPMASK[12:6]	7
0xBB01414C	SVLAN_C2S [83].SVIDX[5:0]	6
0xBB014150	SVLAN_C2S [84].RESERVED[31:26]	6
0xBB014150	SVLAN_C2S [84].EVID[25:13]	13
0xBB014150	SVLAN_C2S [84].C2SENPMASK[12:6]	7
0xBB014150	SVLAN_C2S [84].SVIDX[5:0]	6
0xBB014154	SVLAN_C2S [85].RESERVED[31:26]	6
0xBB014154	SVLAN_C2S [85].EVID[25:13]	13
0xBB014154	SVLAN_C2S [85].C2SENPMASK[12:6]	7
0xBB014154	SVLAN_C2S [85].SVIDX[5:0]	6
0xBB014158	SVLAN_C2S [86].RESERVED[31:26]	6
0xBB014158	SVLAN_C2S [86].EVID[25:13]	13
0xBB014158	SVLAN_C2S [86].C2SENPMASK[12:6]	7
0xBB014158	SVLAN_C2S [86].SVIDX[5:0]	6
0xBB01415C	SVLAN_C2S [87].RESERVED[31:26]	6
0xBB01415C	SVLAN_C2S [87].EVID[25:13]	13
0xBB01415C	SVLAN_C2S [87].C2SENPMASK[12:6]	7

Address	Register	Len
0xBB01415C	SVLAN_C2S [87].SVIDX[5:0]	6
0xBB014160	SVLAN_C2S [88].RESERVED[31:26]	6
0xBB014160	SVLAN_C2S [88].EVID[25:13]	13
0xBB014160	SVLAN_C2S [88].C2SENPMASK[12:6]	7
0xBB014160	SVLAN_C2S [88].SVIDX[5:0]	6
0xBB014164	SVLAN_C2S [89].RESERVED[31:26]	6
0xBB014164	SVLAN_C2S [89].EVID[25:13]	13
0xBB014164	SVLAN_C2S [89].C2SENPMASK[12:6]	7
0xBB014164	SVLAN_C2S [89].SVIDX[5:0]	6
0xBB014168	SVLAN_C2S [90].RESERVED[31:26]	6
0xBB014168	SVLAN_C2S [90].EVID[25:13]	13
0xBB014168	SVLAN_C2S [90].C2SENPMASK[12:6]	7
0xBB014168	SVLAN_C2S [90].SVIDX[5:0]	6
0xBB01416C	SVLAN_C2S [91].RESERVED[31:26]	6
0xBB01416C	SVLAN_C2S [91].EVID[25:13]	13
0xBB01416C	SVLAN_C2S [91].C2SENPMASK[12:6]	7
0xBB01416C	SVLAN_C2S [91].SVIDX[5:0]	6
0xBB014170	SVLAN_C2S [92].RESERVED[31:26]	6
0xBB014170	SVLAN_C2S [92].EVID[25:13]	13
0xBB014170	SVLAN_C2S [92].C2SENPMASK[12:6]	7
0xBB014170	SVLAN_C2S [92].SVIDX[5:0]	6
0xBB014174	SVLAN_C2S [93].RESERVED[31:26]	6
0xBB014174	SVLAN_C2S [93].EVID[25:13]	13
0xBB014174	SVLAN_C2S [93].C2SENPMASK[12:6]	7
0xBB014174	SVLAN_C2S [93].SVIDX[5:0]	6
0xBB014178	SVLAN_C2S [94].RESERVED[31:26]	6
0xBB014178	SVLAN_C2S [94].EVID[25:13]	13
0xBB014178	SVLAN_C2S [94].C2SENPMASK[12:6]	7
0xBB014178	SVLAN_C2S [94].SVIDX[5:0]	6
0xBB01417C	SVLAN_C2S [95].RESERVED[31:26]	6
0xBB01417C	SVLAN_C2S [95].EVID[25:13]	13
0xBB01417C	SVLAN_C2S [95].C2SENPMASK[12:6]	7
0xBB01417C	SVLAN_C2S [95].SVIDX[5:0]	6
0xBB014180	SVLAN_C2S [96].RESERVED[31:26]	6
0xBB014180	SVLAN_C2S [96].EVID[25:13]	13
0xBB014180	SVLAN_C2S [96].C2SENPMASK[12:6]	7
0xBB014180	SVLAN_C2S [96].SVIDX[5:0]	6
0xBB014184	SVLAN_C2S [97].RESERVED[31:26]	6
0xBB014184	SVLAN_C2S [97].EVID[25:13]	13
0xBB014184	SVLAN_C2S [97].C2SENPMASK[12:6]	7
0xBB014184	SVLAN_C2S [97].SVIDX[5:0]	6
0xBB014188	SVLAN_C2S [98].RESERVED[31:26]	6
0xBB014188	SVLAN_C2S [98].EVID[25:13]	13
0xBB014188	SVLAN_C2S [98].C2SENPMASK[12:6]	7
0xBB014188	SVLAN_C2S [98].SVIDX[5:0]	6
0xBB01418C	SVLAN_C2S [99].RESERVED[31:26]	6

Address	Register	Len
0xBB01418C	SVLAN_C2S [99].EVID[25:13]	13
0xBB01418C	SVLAN_C2S [99].C2SENPMASK[12:6]	7
0xBB01418C	SVLAN_C2S [99].SVIDX[5:0]	6
0xBB014190	SVLAN_C2S [100].RESERVED[31:26]	6
0xBB014190	SVLAN_C2S [100].EVID[25:13]	13
0xBB014190	SVLAN_C2S [100].C2SENPMASK[12:6]	7
0xBB014190	SVLAN_C2S [100].SVIDX[5:0]	6
0xBB014194	SVLAN_C2S [101].RESERVED[31:26]	6
0xBB014194	SVLAN_C2S [101].EVID[25:13]	13
0xBB014194	SVLAN_C2S [101].C2SENPMASK[12:6]	7
0xBB014194	SVLAN_C2S [101].SVIDX[5:0]	6
0xBB014198	SVLAN_C2S [102].RESERVED[31:26]	6
0xBB014198	SVLAN_C2S [102].EVID[25:13]	13
0xBB014198	SVLAN_C2S [102].C2SENPMASK[12:6]	7
0xBB014198	SVLAN_C2S [102].SVIDX[5:0]	6
0xBB01419C	SVLAN_C2S [103].RESERVED[31:26]	6
0xBB01419C	SVLAN_C2S [103].EVID[25:13]	13
0xBB01419C	SVLAN_C2S [103].C2SENPMASK[12:6]	7
0xBB01419C	SVLAN_C2S [103].SVIDX[5:0]	6
0xBB0141A0	SVLAN_C2S [104].RESERVED[31:26]	6
0xBB0141A0	SVLAN_C2S [104].EVID[25:13]	13
0xBB0141A0	SVLAN_C2S [104].C2SENPMASK[12:6]	7
0xBB0141A0	SVLAN_C2S [104].SVIDX[5:0]	6
0xBB0141A4	SVLAN_C2S [105].RESERVED[31:26]	6
0xBB0141A4	SVLAN_C2S [105].EVID[25:13]	13
0xBB0141A4	SVLAN_C2S [105].C2SENPMASK[12:6]	7
0xBB0141A4	SVLAN_C2S [105].SVIDX[5:0]	6
0xBB0141A8	SVLAN_C2S [106].RESERVED[31:26]	6
0xBB0141A8	SVLAN_C2S [106].EVID[25:13]	13
0xBB0141A8	SVLAN_C2S [106].C2SENPMASK[12:6]	7
0xBB0141A8	SVLAN_C2S [106].SVIDX[5:0]	6
0xBB0141AC	SVLAN_C2S [107].RESERVED[31:26]	6
0xBB0141AC	SVLAN_C2S [107].EVID[25:13]	13
0xBB0141AC	SVLAN_C2S [107].C2SENPMASK[12:6]	7
0xBB0141AC	SVLAN_C2S [107].SVIDX[5:0]	6
0xBB0141B0	SVLAN_C2S [108].RESERVED[31:26]	6
0xBB0141B0	SVLAN_C2S [108].EVID[25:13]	13
0xBB0141B0	SVLAN_C2S [108].C2SENPMASK[12:6]	7
0xBB0141B0	SVLAN_C2S [108].SVIDX[5:0]	6
0xBB0141B4	SVLAN_C2S [109].RESERVED[31:26]	6
0xBB0141B4	SVLAN_C2S [109].EVID[25:13]	13
0xBB0141B4	SVLAN_C2S [109].C2SENPMASK[12:6]	7
0xBB0141B4	SVLAN_C2S [109].SVIDX[5:0]	6
0xBB0141B8	SVLAN_C2S [110].RESERVED[31:26]	6
0xBB0141B8	SVLAN_C2S [110].EVID[25:13]	13
0xBB0141B8	SVLAN_C2S [110].C2SENPMASK[12:6]	7

Address	Register	Len
0xBB0141B8	SVLAN_C2S [110].SVIDX[5:0]	6
0xBB0141BC	SVLAN_C2S [111].RESERVED[31:26]	6
0xBB0141BC	SVLAN_C2S [111].EVID[25:13]	13
0xBB0141BC	SVLAN_C2S [111].C2SENPMASK[12:6]	7
0xBB0141BC	SVLAN_C2S [111].SVIDX[5:0]	6
0xBB0141C0	SVLAN_C2S [112].RESERVED[31:26]	6
0xBB0141C0	SVLAN_C2S [112].EVID[25:13]	13
0xBB0141C0	SVLAN_C2S [112].C2SENPMASK[12:6]	7
0xBB0141C0	SVLAN_C2S [112].SVIDX[5:0]	6
0xBB0141C4	SVLAN_C2S [113].RESERVED[31:26]	6
0xBB0141C4	SVLAN_C2S [113].EVID[25:13]	13
0xBB0141C4	SVLAN_C2S [113].C2SENPMASK[12:6]	7
0xBB0141C4	SVLAN_C2S [113].SVIDX[5:0]	6
0xBB0141C8	SVLAN_C2S [114].RESERVED[31:26]	6
0xBB0141C8	SVLAN_C2S [114].EVID[25:13]	13
0xBB0141C8	SVLAN_C2S [114].C2SENPMASK[12:6]	7
0xBB0141C8	SVLAN_C2S [114].SVIDX[5:0]	6
0xBB0141CC	SVLAN_C2S [115].RESERVED[31:26]	6
0xBB0141CC	SVLAN_C2S [115].EVID[25:13]	13
0xBB0141CC	SVLAN_C2S [115].C2SENPMASK[12:6]	7
0xBB0141CC	SVLAN_C2S [115].SVIDX[5:0]	6
0xBB0141D0	SVLAN_C2S [116].RESERVED[31:26]	6
0xBB0141D0	SVLAN_C2S [116].EVID[25:13]	13
0xBB0141D0	SVLAN_C2S [116].C2SENPMASK[12:6]	7
0xBB0141D0	SVLAN_C2S [116].SVIDX[5:0]	6
0xBB0141D4	SVLAN_C2S [117].RESERVED[31:26]	6
0xBB0141D4	SVLAN_C2S [117].EVID[25:13]	13
0xBB0141D4	SVLAN_C2S [117].C2SENPMASK[12:6]	7
0xBB0141D4	SVLAN_C2S [117].SVIDX[5:0]	6
0xBB0141D8	SVLAN_C2S [118].RESERVED[31:26]	6
0xBB0141D8	SVLAN_C2S [118].EVID[25:13]	13
0xBB0141D8	SVLAN_C2S [118].C2SENPMASK[12:6]	7
0xBB0141D8	SVLAN_C2S [118].SVIDX[5:0]	6
0xBB0141DC	SVLAN_C2S [119].RESERVED[31:26]	6
0xBB0141DC	SVLAN_C2S [119].EVID[25:13]	13
0xBB0141DC	SVLAN_C2S [119].C2SENPMASK[12:6]	7
0xBB0141DC	SVLAN_C2S [119].SVIDX[5:0]	6
0xBB0141E0	SVLAN_C2S [120].RESERVED[31:26]	6
0xBB0141E0	SVLAN_C2S [120].EVID[25:13]	13
0xBB0141E0	SVLAN_C2S [120].C2SENPMASK[12:6]	7
0xBB0141E0	SVLAN_C2S [120].SVIDX[5:0]	6
0xBB0141E4	SVLAN_C2S [121].RESERVED[31:26]	6
0xBB0141E4	SVLAN_C2S [121].EVID[25:13]	13
0xBB0141E4	SVLAN_C2S [121].C2SENPMASK[12:6]	7
0xBB0141E4	SVLAN_C2S [121].SVIDX[5:0]	6
0xBB0141E8	SVLAN_C2S [122].RESERVED[31:26]	6

Address	Register	Len
0xBB0141E8	SVLAN_C2S [122].EVID[25:13]	13
0xBB0141E8	SVLAN_C2S [122].C2SENPMASK[12:6]	7
0xBB0141E8	SVLAN_C2S [122].SVIDX[5:0]	6
0xBB0141EC	SVLAN_C2S [123].RESERVED[31:26]	6
0xBB0141EC	SVLAN_C2S [123].EVID[25:13]	13
0xBB0141EC	SVLAN_C2S [123].C2SENPMASK[12:6]	7
0xBB0141EC	SVLAN_C2S [123].SVIDX[5:0]	6
0xBB0141F0	SVLAN_C2S [124].RESERVED[31:26]	6
0xBB0141F0	SVLAN_C2S [124].EVID[25:13]	13
0xBB0141F0	SVLAN_C2S [124].C2SENPMASK[12:6]	7
0xBB0141F0	SVLAN_C2S [124].SVIDX[5:0]	6
0xBB0141F4	SVLAN_C2S [125].RESERVED[31:26]	6
0xBB0141F4	SVLAN_C2S [125].EVID[25:13]	13
0xBB0141F4	SVLAN_C2S [125].C2SENPMASK[12:6]	7
0xBB0141F4	SVLAN_C2S [125].SVIDX[5:0]	6
0xBB0141F8	SVLAN_C2S [126].RESERVED[31:26]	6
0xBB0141F8	SVLAN_C2S [126].EVID[25:13]	13
0xBB0141F8	SVLAN_C2S [126].C2SENPMASK[12:6]	7
0xBB0141F8	SVLAN_C2S [126].SVIDX[5:0]	6
0xBB0141FC	SVLAN_C2S [127].RESERVED[31:26]	6
0xBB0141FC	SVLAN_C2S [127].EVID[25:13]	13
0xBB0141FC	SVLAN_C2S [127].C2SENPMASK[12:6]	7
0xBB0141FC	SVLAN_C2S [127].SVIDX[5:0]	6
0xBB014200	SVLAN_EP_DMAC_CTRL [0].EN[0:0]	1
0xBB014200	SVLAN_EP_DMAC_CTRL [1].EN[1:1]	1
0xBB014200	SVLAN_EP_DMAC_CTRL [2].EN[2:2]	1
0xBB014200	SVLAN_EP_DMAC_CTRL [3].EN[3:3]	1
0xBB014200	SVLAN_EP_DMAC_CTRL [4].EN[4:4]	1
0xBB014200	SVLAN_EP_DMAC_CTRL [5].EN[5:5]	1
0xBB014200	SVLAN_EP_DMAC_CTRL [6].EN[6:6]	1
0xBB014204	SVLAN_P_SVIDX [0].SVIDX[5:0]	6
0xBB014204	SVLAN_P_SVIDX [1].SVIDX[11:6]	6
0xBB014204	SVLAN_P_SVIDX [2].SVIDX[17:12]	6
0xBB014204	SVLAN_P_SVIDX [3].SVIDX[23:18]	6
0xBB014204	SVLAN_P_SVIDX [4].SVIDX[29:24]	6
0xBB014208	SVLAN_P_SVIDX [5].SVIDX[5:0]	6
0xBB014208	SVLAN_P_SVIDX [6].SVIDX[11:6]	6
0xBB01420C	SVLAN_CTRL.RESERVED[31:23]	9
0xBB01420C	SVLAN_CTRL.VS_SP2C_UNMAT[22:22]	1
0xBB01420C	SVLAN_CTRL.VS_DEI_KEEP[21:21]	1
0xBB01420C	SVLAN_CTRL.VS_PRI[20:18]	3
0xBB01420C	SVLAN_CTRL.VS_UNTAG_SVIDX[17:12]	6
0xBB01420C	SVLAN_CTRL.VS_UNMAT_SVIDX[11:6]	6
0xBB01420C	SVLAN_CTRL.VS_UNMAT[5:4]	2
0xBB01420C	SVLAN_CTRL.VS_UNTAG[3:2]	2
0xBB01420C	SVLAN_CTRL.VS_SPRISEL[1:0]	2



Address	Register	Len
0xBB014210	SVLAN_MBRCFG [0].RESERVED[31:16]	16
0xBB014210	SVLAN_MBRCFG [0].EFID[15:13]	3
0xBB014210	SVLAN_MBRCFG [0].EFIDEN[12:12]	1
0xBB014210	SVLAN_MBRCFG [0].SVID[11:0]	12
0xBB014214	SVLAN_MBRCFG [0].RESERVED[31:24]	8
0xBB014214	SVLAN_MBRCFG [0].FIDEN[23:23]	1
0xBB014214	SVLAN_MBRCFG [0].SPR[22:20]	3
0xBB014214	SVLAN_MBRCFG [0].FID_MSTI[19:16]	4
0xBB014214	SVLAN_MBRCFG [0].RESERVED[15:15]	1
0xBB014214	SVLAN_MBRCFG [0].UNTAGSET[14:8]	7
0xBB014214	SVLAN_MBRCFG [0].RESERVED[7:7]	1
0xBB014214	SVLAN_MBRCFG [0].MBR[6:0]	7
0xBB014218	SVLAN_MBRCFG [1].RESERVED[31:16]	16
0xBB014218	SVLAN_MBRCFG [1].EFID[15:13]	3
0xBB014218	SVLAN_MBRCFG [1].EFIDEN[12:12]	1
0xBB014218	SVLAN_MBRCFG [1].SVID[11:0]	12
0xBB01421C	SVLAN_MBRCFG [1].RESERVED[31:24]	8
0xBB01421C	SVLAN_MBRCFG [1].FIDEN[23:23]	1
0xBB01421C	SVLAN_MBRCFG [1].SPR[22:20]	3
0xBB01421C	SVLAN_MBRCFG [1].FID_MSTI[19:16]	4
0xBB01421C	SVLAN_MBRCFG [1].RESERVED[15:15]	1
0xBB01421C	SVLAN_MBRCFG [1].UNTAGSET[14:8]	7
0xBB01421C	SVLAN_MBRCFG [1].RESERVED[7:7]	1
0xBB01421C	SVLAN_MBRCFG [1].MBR[6:0]	7
0xBB014220	SVLAN_MBRCFG [2].RESERVED[31:16]	16
0xBB014220	SVLAN_MBRCFG [2].EFID[15:13]	3
0xBB014220	SVLAN_MBRCFG [2].EFIDEN[12:12]	1
0xBB014220	SVLAN_MBRCFG [2].SVID[11:0]	12
0xBB014224	SVLAN_MBRCFG [2].RESERVED[31:24]	8
0xBB014224	SVLAN_MBRCFG [2].FIDEN[23:23]	1
0xBB014224	SVLAN_MBRCFG [2].SPR[22:20]	3
0xBB014224	SVLAN_MBRCFG [2].FID_MSTI[19:16]	4
0xBB014224	SVLAN_MBRCFG [2].RESERVED[15:15]	1
0xBB014224	SVLAN_MBRCFG [2].UNTAGSET[14:8]	7
0xBB014224	SVLAN_MBRCFG [2].RESERVED[7:7]	1
0xBB014224	SVLAN_MBRCFG [2].MBR[6:0]	7
0xBB014228	SVLAN_MBRCFG [3].RESERVED[31:16]	16
0xBB014228	SVLAN_MBRCFG [3].EFID[15:13]	3
0xBB014228	SVLAN_MBRCFG [3].EFIDEN[12:12]	1
0xBB014228	SVLAN_MBRCFG [3].SVID[11:0]	12
0xBB01422C	SVLAN_MBRCFG [3].RESERVED[31:24]	8
0xBB01422C	SVLAN_MBRCFG [3].FIDEN[23:23]	1
0xBB01422C	SVLAN_MBRCFG [3].SPR[22:20]	3
0xBB01422C	SVLAN_MBRCFG [3].FID_MSTI[19:16]	4
0xBB01422C	SVLAN_MBRCFG [3].RESERVED[15:15]	1
0xBB01422C	SVLAN_MBRCFG [3].UNTAGSET[14:8]	7

Address	Register	Len
0xBB01422C	SVLAN_MBRCFG [3].RESERVED[7:7]	1
0xBB01422C	SVLAN_MBRCFG [3].MBR[6:0]	7
0xBB014230	SVLAN_MBRCFG [4].RESERVED[31:16]	16
0xBB014230	SVLAN_MBRCFG [4].EFID[15:13]	3
0xBB014230	SVLAN_MBRCFG [4].EFIDEN[12:12]	1
0xBB014230	SVLAN_MBRCFG [4].SVID[11:0]	12
0xBB014234	SVLAN_MBRCFG [4].RESERVED[31:24]	8
0xBB014234	SVLAN_MBRCFG [4].FIDEN[23:23]	1
0xBB014234	SVLAN_MBRCFG [4].SPR[22:20]	3
0xBB014234	SVLAN_MBRCFG [4].FID_MSTI[19:16]	4
0xBB014234	SVLAN_MBRCFG [4].RESERVED[15:15]	1
0xBB014234	SVLAN_MBRCFG [4].UNTAGSET[14:8]	7
0xBB014234	SVLAN_MBRCFG [4].RESERVED[7:7]	1
0xBB014234	SVLAN_MBRCFG [4].MBR[6:0]	7
0xBB014238	SVLAN_MBRCFG [5].RESERVED[31:16]	16
0xBB014238	SVLAN_MBRCFG [5].EFID[15:13]	3
0xBB014238	SVLAN_MBRCFG [5].EFIDEN[12:12]	1
0xBB014238	SVLAN_MBRCFG [5].SVID[11:0]	12
0xBB01423C	SVLAN_MBRCFG [5].RESERVED[31:24]	8
0xBB01423C	SVLAN_MBRCFG [5].FIDEN[23:23]	1
0xBB01423C	SVLAN_MBRCFG [5].SPR[22:20]	3
0xBB01423C	SVLAN_MBRCFG [5].FID_MSTI[19:16]	4
0xBB01423C	SVLAN_MBRCFG [5].RESERVED[15:15]	1
0xBB01423C	SVLAN_MBRCFG [5].UNTAGSET[14:8]	7
0xBB01423C	SVLAN_MBRCFG [5].RESERVED[7:7]	1
0xBB01423C	SVLAN_MBRCFG [5].MBR[6:0]	7
0xBB014240	SVLAN_MBRCFG [6].RESERVED[31:16]	16
0xBB014240	SVLAN_MBRCFG [6].EFID[15:13]	3
0xBB014240	SVLAN_MBRCFG [6].EFIDEN[12:12]	1
0xBB014240	SVLAN_MBRCFG [6].SVID[11:0]	12
0xBB014244	SVLAN_MBRCFG [6].RESERVED[31:24]	8
0xBB014244	SVLAN_MBRCFG [6].FIDEN[23:23]	1
0xBB014244	SVLAN_MBRCFG [6].SPR[22:20]	3
0xBB014244	SVLAN_MBRCFG [6].FID_MSTI[19:16]	4
0xBB014244	SVLAN_MBRCFG [6].RESERVED[15:15]	1
0xBB014244	SVLAN_MBRCFG [6].UNTAGSET[14:8]	7
0xBB014244	SVLAN_MBRCFG [6].RESERVED[7:7]	1
0xBB014244	SVLAN_MBRCFG [6].MBR[6:0]	7
0xBB014248	SVLAN_MBRCFG [7].RESERVED[31:16]	16
0xBB014248	SVLAN_MBRCFG [7].EFID[15:13]	3
0xBB014248	SVLAN_MBRCFG [7].EFIDEN[12:12]	1
0xBB014248	SVLAN_MBRCFG [7].SVID[11:0]	12
0xBB01424C	SVLAN_MBRCFG [7].RESERVED[31:24]	8
0xBB01424C	SVLAN_MBRCFG [7].FIDEN[23:23]	1
0xBB01424C	SVLAN_MBRCFG [7].SPR[22:20]	3
0xBB01424C	SVLAN_MBRCFG [7].FID_MSTI[19:16]	4

Address	Register	Len
0xBB01424C	SVLAN_MBRCFG [7].RESERVED[15:15]	1
0xBB01424C	SVLAN_MBRCFG [7].UNTAGSET[14:8]	7
0xBB01424C	SVLAN_MBRCFG [7].RESERVED[7:7]	1
0xBB01424C	SVLAN_MBRCFG [7].MBR[6:0]	7
0xBB014250	SVLAN_MBRCFG [8].RESERVED[31:16]	16
0xBB014250	SVLAN_MBRCFG [8].EFID[15:13]	3
0xBB014250	SVLAN_MBRCFG [8].EFIDEN[12:12]	1
0xBB014250	SVLAN_MBRCFG [8].SVID[11:0]	12
0xBB014254	SVLAN_MBRCFG [8].RESERVED[31:24]	8
0xBB014254	SVLAN_MBRCFG [8].FIDEN[23:23]	1
0xBB014254	SVLAN_MBRCFG [8].SPR[22:20]	3
0xBB014254	SVLAN_MBRCFG [8].FID_MSTI[19:16]	4
0xBB014254	SVLAN_MBRCFG [8].RESERVED[15:15]	1
0xBB014254	SVLAN_MBRCFG [8].UNTAGSET[14:8]	7
0xBB014254	SVLAN_MBRCFG [8].RESERVED[7:7]	1
0xBB014254	SVLAN_MBRCFG [8].MBR[6:0]	7
0xBB014258	SVLAN_MBRCFG [9].RESERVED[31:16]	16
0xBB014258	SVLAN_MBRCFG [9].EFID[15:13]	3
0xBB014258	SVLAN_MBRCFG [9].EFIDEN[12:12]	1
0xBB014258	SVLAN_MBRCFG [9].SVID[11:0]	12
0xBB01425C	SVLAN_MBRCFG [9].RESERVED[31:24]	8
0xBB01425C	SVLAN_MBRCFG [9].FIDEN[23:23]	1
0xBB01425C	SVLAN_MBRCFG [9].SPR[22:20]	3
0xBB01425C	SVLAN_MBRCFG [9].FID_MSTI[19:16]	4
0xBB01425C	SVLAN_MBRCFG [9].RESERVED[15:15]	1
0xBB01425C	SVLAN_MBRCFG [9].UNTAGSET[14:8]	7
0xBB01425C	SVLAN_MBRCFG [9].RESERVED[7:7]	1
0xBB01425C	SVLAN_MBRCFG [9].MBR[6:0]	7
0xBB014260	SVLAN_MBRCFG [10].RESERVED[31:16]	16
0xBB014260	SVLAN_MBRCFG [10].EFID[15:13]	3
0xBB014260	SVLAN_MBRCFG [10].EFIDEN[12:12]	1
0xBB014260	SVLAN_MBRCFG [10].SVID[11:0]	12
0xBB014264	SVLAN_MBRCFG [10].RESERVED[31:24]	8
0xBB014264	SVLAN_MBRCFG [10].FIDEN[23:23]	1
0xBB014264	SVLAN_MBRCFG [10].SPR[22:20]	3
0xBB014264	SVLAN_MBRCFG [10].FID_MSTI[19:16]	4
0xBB014264	SVLAN_MBRCFG [10].RESERVED[15:15]	1
0xBB014264	SVLAN_MBRCFG [10].UNTAGSET[14:8]	7
0xBB014264	SVLAN_MBRCFG [10].RESERVED[7:7]	1
0xBB014264	SVLAN_MBRCFG [10].MBR[6:0]	7
0xBB014268	SVLAN_MBRCFG [11].RESERVED[31:16]	16
0xBB014268	SVLAN_MBRCFG [11].EFID[15:13]	3
0xBB014268	SVLAN_MBRCFG [11].EFIDEN[12:12]	1
0xBB014268	SVLAN_MBRCFG [11].SVID[11:0]	12
0xBB01426C	SVLAN_MBRCFG [11].RESERVED[31:24]	8
0xBB01426C	SVLAN_MBRCFG [11].FIDEN[23:23]	1

Address	Register	Len
0xBB01426C	SVLAN_MBRCFG [11].SPR[22:20]	3
0xBB01426C	SVLAN_MBRCFG [11].FID_MSTI[19:16]	4
0xBB01426C	SVLAN_MBRCFG [11].RESERVED[15:15]	1
0xBB01426C	SVLAN_MBRCFG [11].UNTAGSET[14:8]	7
0xBB01426C	SVLAN_MBRCFG [11].RESERVED[7:7]	1
0xBB01426C	SVLAN_MBRCFG [11].MBR[6:0]	7
0xBB014270	SVLAN_MBRCFG [12].RESERVED[31:16]	16
0xBB014270	SVLAN_MBRCFG [12].EFID[15:13]	3
0xBB014270	SVLAN_MBRCFG [12].EFIDEN[12:12]	1
0xBB014270	SVLAN_MBRCFG [12].SVID[11:0]	12
0xBB014274	SVLAN_MBRCFG [12].RESERVED[31:24]	8
0xBB014274	SVLAN_MBRCFG [12].FIDEN[23:23]	1
0xBB014274	SVLAN_MBRCFG [12].SPR[22:20]	3
0xBB014274	SVLAN_MBRCFG [12].FID_MSTI[19:16]	4
0xBB014274	SVLAN_MBRCFG [12].RESERVED[15:15]	1
0xBB014274	SVLAN_MBRCFG [12].UNTAGSET[14:8]	7
0xBB014274	SVLAN_MBRCFG [12].RESERVED[7:7]	1
0xBB014274	SVLAN_MBRCFG [12].MBR[6:0]	7
0xBB014278	SVLAN_MBRCFG [13].RESERVED[31:16]	16
0xBB014278	SVLAN_MBRCFG [13].EFID[15:13]	3
0xBB014278	SVLAN_MBRCFG [13].EFIDEN[12:12]	1
0xBB014278	SVLAN_MBRCFG [13].SVID[11:0]	12
0xBB01427C	SVLAN_MBRCFG [13].RESERVED[31:24]	8
0xBB01427C	SVLAN_MBRCFG [13].FIDEN[23:23]	1
0xBB01427C	SVLAN_MBRCFG [13].SPR[22:20]	3
0xBB01427C	SVLAN_MBRCFG [13].FID_MSTI[19:16]	4
0xBB01427C	SVLAN_MBRCFG [13].RESERVED[15:15]	1
0xBB01427C	SVLAN_MBRCFG [13].UNTAGSET[14:8]	7
0xBB01427C	SVLAN_MBRCFG [13].RESERVED[7:7]	1
0xBB01427C	SVLAN_MBRCFG [13].MBR[6:0]	7
0xBB014280	SVLAN_MBRCFG [14].RESERVED[31:16]	16
0xBB014280	SVLAN_MBRCFG [14].EFID[15:13]	3
0xBB014280	SVLAN_MBRCFG [14].EFIDEN[12:12]	1
0xBB014280	SVLAN_MBRCFG [14].SVID[11:0]	12
0xBB014284	SVLAN_MBRCFG [14].RESERVED[31:24]	8
0xBB014284	SVLAN_MBRCFG [14].FIDEN[23:23]	1
0xBB014284	SVLAN_MBRCFG [14].SPR[22:20]	3
0xBB014284	SVLAN_MBRCFG [14].FID_MSTI[19:16]	4
0xBB014284	SVLAN_MBRCFG [14].RESERVED[15:15]	1
0xBB014284	SVLAN_MBRCFG [14].UNTAGSET[14:8]	7
0xBB014284	SVLAN_MBRCFG [14].RESERVED[7:7]	1
0xBB014284	SVLAN_MBRCFG [14].MBR[6:0]	7
0xBB014288	SVLAN_MBRCFG [15].RESERVED[31:16]	16
0xBB014288	SVLAN_MBRCFG [15].EFID[15:13]	3
0xBB014288	SVLAN_MBRCFG [15].EFIDEN[12:12]	1
0xBB014288	SVLAN_MBRCFG [15].SVID[11:0]	12

Address	Register	Len
0xBB01428C	SVLAN_MBRCFG [15].RESERVED[31:24]	8
0xBB01428C	SVLAN_MBRCFG [15].FIDEN[23:23]	1
0xBB01428C	SVLAN_MBRCFG [15].SPR[22:20]	3
0xBB01428C	SVLAN_MBRCFG [15].FID_MSTI[19:16]	4
0xBB01428C	SVLAN_MBRCFG [15].RESERVED[15:15]	1
0xBB01428C	SVLAN_MBRCFG [15].UNTAGSET[14:8]	7
0xBB01428C	SVLAN_MBRCFG [15].RESERVED[7:7]	1
0xBB01428C	SVLAN_MBRCFG [15].MBR[6:0]	7
0xBB014290	SVLAN_MBRCFG [16].RESERVED[31:16]	16
0xBB014290	SVLAN_MBRCFG [16].EFID[15:13]	3
0xBB014290	SVLAN_MBRCFG [16].EFIDEN[12:12]	1
0xBB014290	SVLAN_MBRCFG [16].SVID[11:0]	12
0xBB014294	SVLAN_MBRCFG [16].RESERVED[31:24]	8
0xBB014294	SVLAN_MBRCFG [16].FIDEN[23:23]	1
0xBB014294	SVLAN_MBRCFG [16].SPR[22:20]	3
0xBB014294	SVLAN_MBRCFG [16].FID_MSTI[19:16]	4
0xBB014294	SVLAN_MBRCFG [16].RESERVED[15:15]	1
0xBB014294	SVLAN_MBRCFG [16].UNTAGSET[14:8]	7
0xBB014294	SVLAN_MBRCFG [16].RESERVED[7:7]	1
0xBB014294	SVLAN_MBRCFG [16].MBR[6:0]	7
0xBB014298	SVLAN_MBRCFG [17].RESERVED[31:16]	16
0xBB014298	SVLAN_MBRCFG [17].EFID[15:13]	3
0xBB014298	SVLAN_MBRCFG [17].EFIDEN[12:12]	1
0xBB014298	SVLAN_MBRCFG [17].SVID[11:0]	12
0xBB01429C	SVLAN_MBRCFG [17].RESERVED[31:24]	8
0xBB01429C	SVLAN_MBRCFG [17].FIDEN[23:23]	1
0xBB01429C	SVLAN_MBRCFG [17].SPR[22:20]	3
0xBB01429C	SVLAN_MBRCFG [17].FID_MSTI[19:16]	4
0xBB01429C	SVLAN_MBRCFG [17].RESERVED[15:15]	1
0xBB01429C	SVLAN_MBRCFG [17].UNTAGSET[14:8]	7
0xBB01429C	SVLAN_MBRCFG [17].RESERVED[7:7]	1
0xBB01429C	SVLAN_MBRCFG [17].MBR[6:0]	7
0xBB0142A0	SVLAN_MBRCFG [18].RESERVED[31:16]	16
0xBB0142A0	SVLAN_MBRCFG [18].EFID[15:13]	3
0xBB0142A0	SVLAN_MBRCFG [18].EFIDEN[12:12]	1
0xBB0142A0	SVLAN_MBRCFG [18].SVID[11:0]	12
0xBB0142A4	SVLAN_MBRCFG [18].RESERVED[31:24]	8
0xBB0142A4	SVLAN_MBRCFG [18].FIDEN[23:23]	1
0xBB0142A4	SVLAN_MBRCFG [18].SPR[22:20]	3
0xBB0142A4	SVLAN_MBRCFG [18].FID_MSTI[19:16]	4
0xBB0142A4	SVLAN_MBRCFG [18].RESERVED[15:15]	1
0xBB0142A4	SVLAN_MBRCFG [18].UNTAGSET[14:8]	7
0xBB0142A4	SVLAN_MBRCFG [18].RESERVED[7:7]	1
0xBB0142A4	SVLAN_MBRCFG [18].MBR[6:0]	7
0xBB0142A8	SVLAN_MBRCFG [19].RESERVED[31:16]	16
0xBB0142A8	SVLAN_MBRCFG [19].EFID[15:13]	3

Address	Register	Len
0xBB0142A8	SVLAN_MBRCFG [19].EFIDEN[12:12]	1
0xBB0142A8	SVLAN_MBRCFG [19].SVID[11:0]	12
0xBB0142AC	SVLAN_MBRCFG [19].RESERVED[31:24]	8
0xBB0142AC	SVLAN_MBRCFG [19].FIDEN[23:23]	1
0xBB0142AC	SVLAN_MBRCFG [19].SPR[22:20]	3
0xBB0142AC	SVLAN_MBRCFG [19].FID_MSTI[19:16]	4
0xBB0142AC	SVLAN_MBRCFG [19].RESERVED[15:15]	1
0xBB0142AC	SVLAN_MBRCFG [19].UNTAGSET[14:8]	7
0xBB0142AC	SVLAN_MBRCFG [19].RESERVED[7:7]	1
0xBB0142AC	SVLAN_MBRCFG [19].MBR[6:0]	7
0xBB0142B0	SVLAN_MBRCFG [20].RESERVED[31:16]	16
0xBB0142B0	SVLAN_MBRCFG [20].EFID[15:13]	3
0xBB0142B0	SVLAN_MBRCFG [20].EFIDEN[12:12]	1
0xBB0142B0	SVLAN_MBRCFG [20].SVID[11:0]	12
0xBB0142B4	SVLAN_MBRCFG [20].RESERVED[31:24]	8
0xBB0142B4	SVLAN_MBRCFG [20].FIDEN[23:23]	1
0xBB0142B4	SVLAN_MBRCFG [20].SPR[22:20]	3
0xBB0142B4	SVLAN_MBRCFG [20].FID_MSTI[19:16]	4
0xBB0142B4	SVLAN_MBRCFG [20].RESERVED[15:15]	1
0xBB0142B4	SVLAN_MBRCFG [20].UNTAGSET[14:8]	7
0xBB0142B4	SVLAN_MBRCFG [20].RESERVED[7:7]	1
0xBB0142B4	SVLAN_MBRCFG [20].MBR[6:0]	7
0xBB0142B8	SVLAN_MBRCFG [21].RESERVED[31:16]	16
0xBB0142B8	SVLAN_MBRCFG [21].EFID[15:13]	3
0xBB0142B8	SVLAN_MBRCFG [21].EFIDEN[12:12]	1
0xBB0142B8	SVLAN_MBRCFG [21].SVID[11:0]	12
0xBB0142BC	SVLAN_MBRCFG [21].RESERVED[31:24]	8
0xBB0142BC	SVLAN_MBRCFG [21].FIDEN[23:23]	1
0xBB0142BC	SVLAN_MBRCFG [21].SPR[22:20]	3
0xBB0142BC	SVLAN_MBRCFG [21].FID_MSTI[19:16]	4
0xBB0142BC	SVLAN_MBRCFG [21].RESERVED[15:15]	1
0xBB0142BC	SVLAN_MBRCFG [21].UNTAGSET[14:8]	7
0xBB0142BC	SVLAN_MBRCFG [21].RESERVED[7:7]	1
0xBB0142BC	SVLAN_MBRCFG [21].MBR[6:0]	7
0xBB0142C0	SVLAN_MBRCFG [22].RESERVED[31:16]	16
0xBB0142C0	SVLAN_MBRCFG [22].EFID[15:13]	3
0xBB0142C0	SVLAN_MBRCFG [22].EFIDEN[12:12]	1
0xBB0142C0	SVLAN_MBRCFG [22].SVID[11:0]	12
0xBB0142C4	SVLAN_MBRCFG [22].RESERVED[31:24]	8
0xBB0142C4	SVLAN_MBRCFG [22].FIDEN[23:23]	1
0xBB0142C4	SVLAN_MBRCFG [22].SPR[22:20]	3
0xBB0142C4	SVLAN_MBRCFG [22].FID_MSTI[19:16]	4
0xBB0142C4	SVLAN_MBRCFG [22].RESERVED[15:15]	1
0xBB0142C4	SVLAN_MBRCFG [22].UNTAGSET[14:8]	7
0xBB0142C4	SVLAN_MBRCFG [22].RESERVED[7:7]	1
0xBB0142C4	SVLAN_MBRCFG [22].MBR[6:0]	7

Address	Register	Len
0xBB0142C8	SVLAN_MBRCFG [23].RESERVED[31:16]	16
0xBB0142C8	SVLAN_MBRCFG [23].EFID[15:13]	3
0xBB0142C8	SVLAN_MBRCFG [23].EFIDEN[12:12]	1
0xBB0142C8	SVLAN_MBRCFG [23].SVID[11:0]	12
0xBB0142CC	SVLAN_MBRCFG [23].RESERVED[31:24]	8
0xBB0142CC	SVLAN_MBRCFG [23].FIDEN[23:23]	1
0xBB0142CC	SVLAN_MBRCFG [23].SPR[22:20]	3
0xBB0142CC	SVLAN_MBRCFG [23].FID_MSTI[19:16]	4
0xBB0142CC	SVLAN_MBRCFG [23].RESERVED[15:15]	1
0xBB0142CC	SVLAN_MBRCFG [23].UNTAGSET[14:8]	7
0xBB0142CC	SVLAN_MBRCFG [23].RESERVED[7:7]	1
0xBB0142CC	SVLAN_MBRCFG [23].MBR[6:0]	7
0xBB0142D0	SVLAN_MBRCFG [24].RESERVED[31:16]	16
0xBB0142D0	SVLAN_MBRCFG [24].EFID[15:13]	3
0xBB0142D0	SVLAN_MBRCFG [24].EFIDEN[12:12]	1
0xBB0142D0	SVLAN_MBRCFG [24].SVID[11:0]	12
0xBB0142D4	SVLAN_MBRCFG [24].RESERVED[31:24]	8
0xBB0142D4	SVLAN_MBRCFG [24].FIDEN[23:23]	1
0xBB0142D4	SVLAN_MBRCFG [24].SPR[22:20]	3
0xBB0142D4	SVLAN_MBRCFG [24].FID_MSTI[19:16]	4
0xBB0142D4	SVLAN_MBRCFG [24].RESERVED[15:15]	1
0xBB0142D4	SVLAN_MBRCFG [24].UNTAGSET[14:8]	7
0xBB0142D4	SVLAN_MBRCFG [24].RESERVED[7:7]	1
0xBB0142D4	SVLAN_MBRCFG [24].MBR[6:0]	7
0xBB0142D8	SVLAN_MBRCFG [25].RESERVED[31:16]	16
0xBB0142D8	SVLAN_MBRCFG [25].EFID[15:13]	3
0xBB0142D8	SVLAN_MBRCFG [25].EFIDEN[12:12]	1
0xBB0142D8	SVLAN_MBRCFG [25].SVID[11:0]	12
0xBB0142DC	SVLAN_MBRCFG [25].RESERVED[31:24]	8
0xBB0142DC	SVLAN_MBRCFG [25].FIDEN[23:23]	1
0xBB0142DC	SVLAN_MBRCFG [25].SPR[22:20]	3
0xBB0142DC	SVLAN_MBRCFG [25].FID_MSTI[19:16]	4
0xBB0142DC	SVLAN_MBRCFG [25].RESERVED[15:15]	1
0xBB0142DC	SVLAN_MBRCFG [25].UNTAGSET[14:8]	7
0xBB0142DC	SVLAN_MBRCFG [25].RESERVED[7:7]	1
0xBB0142DC	SVLAN_MBRCFG [25].MBR[6:0]	7
0xBB0142E0	SVLAN_MBRCFG [26].RESERVED[31:16]	16
0xBB0142E0	SVLAN_MBRCFG [26].EFID[15:13]	3
0xBB0142E0	SVLAN_MBRCFG [26].EFIDEN[12:12]	1
0xBB0142E0	SVLAN_MBRCFG [26].SVID[11:0]	12
0xBB0142E4	SVLAN_MBRCFG [26].RESERVED[31:24]	8
0xBB0142E4	SVLAN_MBRCFG [26].FIDEN[23:23]	1
0xBB0142E4	SVLAN_MBRCFG [26].SPR[22:20]	3
0xBB0142E4	SVLAN_MBRCFG [26].FID_MSTI[19:16]	4
0xBB0142E4	SVLAN_MBRCFG [26].RESERVED[15:15]	1
0xBB0142E4	SVLAN_MBRCFG [26].UNTAGSET[14:8]	7



Address	Register	Len
0xBB0142E4	SVLAN_MBRCFG [26].RESERVED[7:7]	1
0xBB0142E4	SVLAN_MBRCFG [26].MBR[6:0]	7
0xBB0142E8	SVLAN_MBRCFG [27].RESERVED[31:16]	16
0xBB0142E8	SVLAN_MBRCFG [27].EFID[15:13]	3
0xBB0142E8	SVLAN_MBRCFG [27].EFIDEN[12:12]	1
0xBB0142E8	SVLAN_MBRCFG [27].SVID[11:0]	12
0xBB0142EC	SVLAN_MBRCFG [27].RESERVED[31:24]	8
0xBB0142EC	SVLAN_MBRCFG [27].FIDEN[23:23]	1
0xBB0142EC	SVLAN_MBRCFG [27].SPR[22:20]	3
0xBB0142EC	SVLAN_MBRCFG [27].FID_MSTI[19:16]	4
0xBB0142EC	SVLAN_MBRCFG [27].RESERVED[15:15]	1
0xBB0142EC	SVLAN_MBRCFG [27].UNTAGSET[14:8]	7
0xBB0142EC	SVLAN_MBRCFG [27].RESERVED[7:7]	1
0xBB0142EC	SVLAN_MBRCFG [27].MBR[6:0]	7
0xBB0142F0	SVLAN_MBRCFG [28].RESERVED[31:16]	16
0xBB0142F0	SVLAN_MBRCFG [28].EFID[15:13]	3
0xBB0142F0	SVLAN_MBRCFG [28].EFIDEN[12:12]	1
0xBB0142F0	SVLAN_MBRCFG [28].SVID[11:0]	12
0xBB0142F4	SVLAN_MBRCFG [28].RESERVED[31:24]	8
0xBB0142F4	SVLAN_MBRCFG [28].FIDEN[23:23]	1
0xBB0142F4	SVLAN_MBRCFG [28].SPR[22:20]	3
0xBB0142F4	SVLAN_MBRCFG [28].FID_MSTI[19:16]	4
0xBB0142F4	SVLAN_MBRCFG [28].RESERVED[15:15]	1
0xBB0142F4	SVLAN_MBRCFG [28].UNTAGSET[14:8]	7
0xBB0142F4	SVLAN_MBRCFG [28].RESERVED[7:7]	1
0xBB0142F4	SVLAN_MBRCFG [28].MBR[6:0]	7
0xBB0142F8	SVLAN_MBRCFG [29].RESERVED[31:16]	16
0xBB0142F8	SVLAN_MBRCFG [29].EFID[15:13]	3
0xBB0142F8	SVLAN_MBRCFG [29].EFIDEN[12:12]	1
0xBB0142F8	SVLAN_MBRCFG [29].SVID[11:0]	12
0xBB0142FC	SVLAN_MBRCFG [29].RESERVED[31:24]	8
0xBB0142FC	SVLAN_MBRCFG [29].FIDEN[23:23]	1
0xBB0142FC	SVLAN_MBRCFG [29].SPR[22:20]	3
0xBB0142FC	SVLAN_MBRCFG [29].FID_MSTI[19:16]	4
0xBB0142FC	SVLAN_MBRCFG [29].RESERVED[15:15]	1
0xBB0142FC	SVLAN_MBRCFG [29].UNTAGSET[14:8]	7
0xBB0142FC	SVLAN_MBRCFG [29].RESERVED[7:7]	1
0xBB0142FC	SVLAN_MBRCFG [29].MBR[6:0]	7
0xBB014300	SVLAN_MBRCFG [30].RESERVED[31:16]	16
0xBB014300	SVLAN_MBRCFG [30].EFID[15:13]	3
0xBB014300	SVLAN_MBRCFG [30].EFIDEN[12:12]	1
0xBB014300	SVLAN_MBRCFG [30].SVID[11:0]	12
0xBB014304	SVLAN_MBRCFG [30].RESERVED[31:24]	8
0xBB014304	SVLAN_MBRCFG [30].FIDEN[23:23]	1
0xBB014304	SVLAN_MBRCFG [30].SPR[22:20]	3
0xBB014304	SVLAN_MBRCFG [30].FID_MSTI[19:16]	4



Address	Register	Len
0xBB014304	SVLAN_MBRCFG [30].RESERVED[15:15]	1
0xBB014304	SVLAN_MBRCFG [30].UNTAGSET[14:8]	7
0xBB014304	SVLAN_MBRCFG [30].RESERVED[7:7]	1
0xBB014304	SVLAN_MBRCFG [30].MBR[6:0]	7
0xBB014308	SVLAN_MBRCFG [31].RESERVED[31:16]	16
0xBB014308	SVLAN_MBRCFG [31].EFID[15:13]	3
0xBB014308	SVLAN_MBRCFG [31].EFIDEN[12:12]	1
0xBB014308	SVLAN_MBRCFG [31].SVID[11:0]	12
0xBB01430C	SVLAN_MBRCFG [31].RESERVED[31:24]	8
0xBB01430C	SVLAN_MBRCFG [31].FIDEN[23:23]	1
0xBB01430C	SVLAN_MBRCFG [31].SPR[22:20]	3
0xBB01430C	SVLAN_MBRCFG [31].FID_MSTI[19:16]	4
0xBB01430C	SVLAN_MBRCFG [31].RESERVED[15:15]	1
0xBB01430C	SVLAN_MBRCFG [31].UNTAGSET[14:8]	7
0xBB01430C	SVLAN_MBRCFG [31].RESERVED[7:7]	1
0xBB01430C	SVLAN_MBRCFG [31].MBR[6:0]	7
0xBB014310	SVLAN_MBRCFG [32].RESERVED[31:16]	16
0xBB014310	SVLAN_MBRCFG [32].EFID[15:13]	3
0xBB014310	SVLAN_MBRCFG [32].EFIDEN[12:12]	1
0xBB014310	SVLAN_MBRCFG [32].SVID[11:0]	12
0xBB014314	SVLAN_MBRCFG [32].RESERVED[31:24]	8
0xBB014314	SVLAN_MBRCFG [32].FIDEN[23:23]	1
0xBB014314	SVLAN_MBRCFG [32].SPR[22:20]	3
0xBB014314	SVLAN_MBRCFG [32].FID_MSTI[19:16]	4
0xBB014314	SVLAN_MBRCFG [32].RESERVED[15:15]	1
0xBB014314	SVLAN_MBRCFG [32].UNTAGSET[14:8]	7
0xBB014314	SVLAN_MBRCFG [32].RESERVED[7:7]	1
0xBB014314	SVLAN_MBRCFG [32].MBR[6:0]	7
0xBB014318	SVLAN_MBRCFG [33].RESERVED[31:16]	16
0xBB014318	SVLAN_MBRCFG [33].EFID[15:13]	3
0xBB014318	SVLAN_MBRCFG [33].EFIDEN[12:12]	1
0xBB014318	SVLAN_MBRCFG [33].SVID[11:0]	12
0xBB01431C	SVLAN_MBRCFG [33].RESERVED[31:24]	8
0xBB01431C	SVLAN_MBRCFG [33].FIDEN[23:23]	1
0xBB01431C	SVLAN_MBRCFG [33].SPR[22:20]	3
0xBB01431C	SVLAN_MBRCFG [33].FID_MSTI[19:16]	4
0xBB01431C	SVLAN_MBRCFG [33].RESERVED[15:15]	1
0xBB01431C	SVLAN_MBRCFG [33].UNTAGSET[14:8]	7
0xBB01431C	SVLAN_MBRCFG [33].RESERVED[7:7]	1
0xBB01431C	SVLAN_MBRCFG [33].MBR[6:0]	7
0xBB014320	SVLAN_MBRCFG [34].RESERVED[31:16]	16
0xBB014320	SVLAN_MBRCFG [34].EFID[15:13]	3
0xBB014320	SVLAN_MBRCFG [34].EFIDEN[12:12]	1
0xBB014320	SVLAN_MBRCFG [34].SVID[11:0]	12
0xBB014324	SVLAN_MBRCFG [34].RESERVED[31:24]	8
0xBB014324	SVLAN_MBRCFG [34].FIDEN[23:23]	1

Address	Register	Len
0xBB014324	SVLAN_MBRCFG [34].SPR[22:20]	3
0xBB014324	SVLAN_MBRCFG [34].FID_MSTI[19:16]	4
0xBB014324	SVLAN_MBRCFG [34].RESERVED[15:15]	1
0xBB014324	SVLAN_MBRCFG [34].UNTAGSET[14:8]	7
0xBB014324	SVLAN_MBRCFG [34].RESERVED[7:7]	1
0xBB014324	SVLAN_MBRCFG [34].MBR[6:0]	7
0xBB014328	SVLAN_MBRCFG [35].RESERVED[31:16]	16
0xBB014328	SVLAN_MBRCFG [35].EFID[15:13]	3
0xBB014328	SVLAN_MBRCFG [35].EFIDEN[12:12]	1
0xBB014328	SVLAN_MBRCFG [35].SVID[11:0]	12
0xBB01432C	SVLAN_MBRCFG [35].RESERVED[31:24]	8
0xBB01432C	SVLAN_MBRCFG [35].FIDEN[23:23]	1
0xBB01432C	SVLAN_MBRCFG [35].SPR[22:20]	3
0xBB01432C	SVLAN_MBRCFG [35].FID_MSTI[19:16]	4
0xBB01432C	SVLAN_MBRCFG [35].RESERVED[15:15]	1
0xBB01432C	SVLAN_MBRCFG [35].UNTAGSET[14:8]	7
0xBB01432C	SVLAN_MBRCFG [35].RESERVED[7:7]	1
0xBB01432C	SVLAN_MBRCFG [35].MBR[6:0]	7
0xBB014330	SVLAN_MBRCFG [36].RESERVED[31:16]	16
0xBB014330	SVLAN_MBRCFG [36].EFID[15:13]	3
0xBB014330	SVLAN_MBRCFG [36].EFIDEN[12:12]	1
0xBB014330	SVLAN_MBRCFG [36].SVID[11:0]	12
0xBB014334	SVLAN_MBRCFG [36].RESERVED[31:24]	8
0xBB014334	SVLAN_MBRCFG [36].FIDEN[23:23]	1
0xBB014334	SVLAN_MBRCFG [36].SPR[22:20]	3
0xBB014334	SVLAN_MBRCFG [36].FID_MSTI[19:16]	4
0xBB014334	SVLAN_MBRCFG [36].RESERVED[15:15]	1
0xBB014334	SVLAN_MBRCFG [36].UNTAGSET[14:8]	7
0xBB014334	SVLAN_MBRCFG [36].RESERVED[7:7]	1
0xBB014334	SVLAN_MBRCFG [36].MBR[6:0]	7
0xBB014338	SVLAN_MBRCFG [37].RESERVED[31:16]	16
0xBB014338	SVLAN_MBRCFG [37].EFID[15:13]	3
0xBB014338	SVLAN_MBRCFG [37].EFIDEN[12:12]	1
0xBB014338	SVLAN_MBRCFG [37].SVID[11:0]	12
0xBB01433C	SVLAN_MBRCFG [37].RESERVED[31:24]	8
0xBB01433C	SVLAN_MBRCFG [37].FIDEN[23:23]	1
0xBB01433C	SVLAN_MBRCFG [37].SPR[22:20]	3
0xBB01433C	SVLAN_MBRCFG [37].FID_MSTI[19:16]	4
0xBB01433C	SVLAN_MBRCFG [37].RESERVED[15:15]	1
0xBB01433C	SVLAN_MBRCFG [37].UNTAGSET[14:8]	7
0xBB01433C	SVLAN_MBRCFG [37].RESERVED[7:7]	1
0xBB01433C	SVLAN_MBRCFG [37].MBR[6:0]	7
0xBB014340	SVLAN_MBRCFG [38].RESERVED[31:16]	16
0xBB014340	SVLAN_MBRCFG [38].EFID[15:13]	3
0xBB014340	SVLAN_MBRCFG [38].EFIDEN[12:12]	1
0xBB014340	SVLAN_MBRCFG [38].SVID[11:0]	12

Address	Register	Len
0xBB014344	SVLAN_MBRCFG [38].RESERVED[31:24]	8
0xBB014344	SVLAN_MBRCFG [38].FIDEN[23:23]	1
0xBB014344	SVLAN_MBRCFG [38].SPR[22:20]	3
0xBB014344	SVLAN_MBRCFG [38].FID_MSTI[19:16]	4
0xBB014344	SVLAN_MBRCFG [38].RESERVED[15:15]	1
0xBB014344	SVLAN_MBRCFG [38].UNTAGSET[14:8]	7
0xBB014344	SVLAN_MBRCFG [38].RESERVED[7:7]	1
0xBB014344	SVLAN_MBRCFG [38].MBR[6:0]	7
0xBB014348	SVLAN_MBRCFG [39].RESERVED[31:16]	16
0xBB014348	SVLAN_MBRCFG [39].EFID[15:13]	3
0xBB014348	SVLAN_MBRCFG [39].EFIDEN[12:12]	1
0xBB014348	SVLAN_MBRCFG [39].SVID[11:0]	12
0xBB01434C	SVLAN_MBRCFG [39].RESERVED[31:24]	8
0xBB01434C	SVLAN_MBRCFG [39].FIDEN[23:23]	1
0xBB01434C	SVLAN_MBRCFG [39].SPR[22:20]	3
0xBB01434C	SVLAN_MBRCFG [39].FID_MSTI[19:16]	4
0xBB01434C	SVLAN_MBRCFG [39].RESERVED[15:15]	1
0xBB01434C	SVLAN_MBRCFG [39].UNTAGSET[14:8]	7
0xBB01434C	SVLAN_MBRCFG [39].RESERVED[7:7]	1
0xBB01434C	SVLAN_MBRCFG [39].MBR[6:0]	7
0xBB014350	SVLAN_MBRCFG [40].RESERVED[31:16]	16
0xBB014350	SVLAN_MBRCFG [40].EFID[15:13]	3
0xBB014350	SVLAN_MBRCFG [40].EFIDEN[12:12]	1
0xBB014350	SVLAN_MBRCFG [40].SVID[11:0]	12
0xBB014354	SVLAN_MBRCFG [40].RESERVED[31:24]	8
0xBB014354	SVLAN_MBRCFG [40].FIDEN[23:23]	1
0xBB014354	SVLAN_MBRCFG [40].SPR[22:20]	3
0xBB014354	SVLAN_MBRCFG [40].FID_MSTI[19:16]	4
0xBB014354	SVLAN_MBRCFG [40].RESERVED[15:15]	1
0xBB014354	SVLAN_MBRCFG [40].UNTAGSET[14:8]	7
0xBB014354	SVLAN_MBRCFG [40].RESERVED[7:7]	1
0xBB014354	SVLAN_MBRCFG [40].MBR[6:0]	7
0xBB014358	SVLAN_MBRCFG [41].RESERVED[31:16]	16
0xBB014358	SVLAN_MBRCFG [41].EFID[15:13]	3
0xBB014358	SVLAN_MBRCFG [41].EFIDEN[12:12]	1
0xBB014358	SVLAN_MBRCFG [41].SVID[11:0]	12
0xBB01435C	SVLAN_MBRCFG [41].RESERVED[31:24]	8
0xBB01435C	SVLAN_MBRCFG [41].FIDEN[23:23]	1
0xBB01435C	SVLAN_MBRCFG [41].SPR[22:20]	3
0xBB01435C	SVLAN_MBRCFG [41].FID_MSTI[19:16]	4
0xBB01435C	SVLAN_MBRCFG [41].RESERVED[15:15]	1
0xBB01435C	SVLAN_MBRCFG [41].UNTAGSET[14:8]	7
0xBB01435C	SVLAN_MBRCFG [41].RESERVED[7:7]	1
0xBB01435C	SVLAN_MBRCFG [41].MBR[6:0]	7
0xBB014360	SVLAN_MBRCFG [42].RESERVED[31:16]	16
0xBB014360	SVLAN_MBRCFG [42].EFID[15:13]	3

Address	Register	Len
0xBB014360	SVLAN_MBRCFG [42].EFIDEN[12:12]	1
0xBB014360	SVLAN_MBRCFG [42].SVID[11:0]	12
0xBB014364	SVLAN_MBRCFG [42].RESERVED[31:24]	8
0xBB014364	SVLAN_MBRCFG [42].FIDEN[23:23]	1
0xBB014364	SVLAN_MBRCFG [42].SPR[22:20]	3
0xBB014364	SVLAN_MBRCFG [42].FID_MSTI[19:16]	4
0xBB014364	SVLAN_MBRCFG [42].RESERVED[15:15]	1
0xBB014364	SVLAN_MBRCFG [42].UNTAGSET[14:8]	7
0xBB014364	SVLAN_MBRCFG [42].RESERVED[7:7]	1
0xBB014364	SVLAN_MBRCFG [42].MBR[6:0]	7
0xBB014368	SVLAN_MBRCFG [43].RESERVED[31:16]	16
0xBB014368	SVLAN_MBRCFG [43].EFID[15:13]	3
0xBB014368	SVLAN_MBRCFG [43].EFIDEN[12:12]	1
0xBB014368	SVLAN_MBRCFG [43].SVID[11:0]	12
0xBB01436C	SVLAN_MBRCFG [43].RESERVED[31:24]	8
0xBB01436C	SVLAN_MBRCFG [43].FIDEN[23:23]	1
0xBB01436C	SVLAN_MBRCFG [43].SPR[22:20]	3
0xBB01436C	SVLAN_MBRCFG [43].FID_MSTI[19:16]	4
0xBB01436C	SVLAN_MBRCFG [43].RESERVED[15:15]	1
0xBB01436C	SVLAN_MBRCFG [43].UNTAGSET[14:8]	7
0xBB01436C	SVLAN_MBRCFG [43].RESERVED[7:7]	1
0xBB01436C	SVLAN_MBRCFG [43].MBR[6:0]	7
0xBB014370	SVLAN_MBRCFG [44].RESERVED[31:16]	16
0xBB014370	SVLAN_MBRCFG [44].EFID[15:13]	3
0xBB014370	SVLAN_MBRCFG [44].EFIDEN[12:12]	1
0xBB014370	SVLAN_MBRCFG [44].SVID[11:0]	12
0xBB014374	SVLAN_MBRCFG [44].RESERVED[31:24]	8
0xBB014374	SVLAN_MBRCFG [44].FIDEN[23:23]	1
0xBB014374	SVLAN_MBRCFG [44].SPR[22:20]	3
0xBB014374	SVLAN_MBRCFG [44].FID_MSTI[19:16]	4
0xBB014374	SVLAN_MBRCFG [44].RESERVED[15:15]	1
0xBB014374	SVLAN_MBRCFG [44].UNTAGSET[14:8]	7
0xBB014374	SVLAN_MBRCFG [44].RESERVED[7:7]	1
0xBB014374	SVLAN_MBRCFG [44].MBR[6:0]	7
0xBB014378	SVLAN_MBRCFG [45].RESERVED[31:16]	16
0xBB014378	SVLAN_MBRCFG [45].EFID[15:13]	3
0xBB014378	SVLAN_MBRCFG [45].EFIDEN[12:12]	1
0xBB014378	SVLAN_MBRCFG [45].SVID[11:0]	12
0xBB01437C	SVLAN_MBRCFG [45].RESERVED[31:24]	8
0xBB01437C	SVLAN_MBRCFG [45].FIDEN[23:23]	1
0xBB01437C	SVLAN_MBRCFG [45].SPR[22:20]	3
0xBB01437C	SVLAN_MBRCFG [45].FID_MSTI[19:16]	4
0xBB01437C	SVLAN_MBRCFG [45].RESERVED[15:15]	1
0xBB01437C	SVLAN_MBRCFG [45].UNTAGSET[14:8]	7
0xBB01437C	SVLAN_MBRCFG [45].RESERVED[7:7]	1
0xBB01437C	SVLAN_MBRCFG [45].MBR[6:0]	7

Address	Register	Len
0xBB014380	SVLAN_MBRCFG [46].RESERVED[31:16]	16
0xBB014380	SVLAN_MBRCFG [46].EFID[15:13]	3
0xBB014380	SVLAN_MBRCFG [46].EFIDEN[12:12]	1
0xBB014380	SVLAN_MBRCFG [46].SVID[11:0]	12
0xBB014384	SVLAN_MBRCFG [46].RESERVED[31:24]	8
0xBB014384	SVLAN_MBRCFG [46].FIDEN[23:23]	1
0xBB014384	SVLAN_MBRCFG [46].SPR[22:20]	3
0xBB014384	SVLAN_MBRCFG [46].FID_MSTI[19:16]	4
0xBB014384	SVLAN_MBRCFG [46].RESERVED[15:15]	1
0xBB014384	SVLAN_MBRCFG [46].UNTAGSET[14:8]	7
0xBB014384	SVLAN_MBRCFG [46].RESERVED[7:7]	1
0xBB014384	SVLAN_MBRCFG [46].MBR[6:0]	7
0xBB014388	SVLAN_MBRCFG [47].RESERVED[31:16]	16
0xBB014388	SVLAN_MBRCFG [47].EFID[15:13]	3
0xBB014388	SVLAN_MBRCFG [47].EFIDEN[12:12]	1
0xBB014388	SVLAN_MBRCFG [47].SVID[11:0]	12
0xBB01438C	SVLAN_MBRCFG [47].RESERVED[31:24]	8
0xBB01438C	SVLAN_MBRCFG [47].FIDEN[23:23]	1
0xBB01438C	SVLAN_MBRCFG [47].SPR[22:20]	3
0xBB01438C	SVLAN_MBRCFG [47].FID_MSTI[19:16]	4
0xBB01438C	SVLAN_MBRCFG [47].RESERVED[15:15]	1
0xBB01438C	SVLAN_MBRCFG [47].UNTAGSET[14:8]	7
0xBB01438C	SVLAN_MBRCFG [47].RESERVED[7:7]	1
0xBB01438C	SVLAN_MBRCFG [47].MBR[6:0]	7
0xBB014390	SVLAN_MBRCFG [48].RESERVED[31:16]	16
0xBB014390	SVLAN_MBRCFG [48].EFID[15:13]	3
0xBB014390	SVLAN_MBRCFG [48].EFIDEN[12:12]	1
0xBB014390	SVLAN_MBRCFG [48].SVID[11:0]	12
0xBB014394	SVLAN_MBRCFG [48].RESERVED[31:24]	8
0xBB014394	SVLAN_MBRCFG [48].FIDEN[23:23]	1
0xBB014394	SVLAN_MBRCFG [48].SPR[22:20]	3
0xBB014394	SVLAN_MBRCFG [48].FID_MSTI[19:16]	4
0xBB014394	SVLAN_MBRCFG [48].RESERVED[15:15]	1
0xBB014394	SVLAN_MBRCFG [48].UNTAGSET[14:8]	7
0xBB014394	SVLAN_MBRCFG [48].RESERVED[7:7]	1
0xBB014394	SVLAN_MBRCFG [48].MBR[6:0]	7
0xBB014398	SVLAN_MBRCFG [49].RESERVED[31:16]	16
0xBB014398	SVLAN_MBRCFG [49].EFID[15:13]	3
0xBB014398	SVLAN_MBRCFG [49].EFIDEN[12:12]	1
0xBB014398	SVLAN_MBRCFG [49].SVID[11:0]	12
0xBB01439C	SVLAN_MBRCFG [49].RESERVED[31:24]	8
0xBB01439C	SVLAN_MBRCFG [49].FIDEN[23:23]	1
0xBB01439C	SVLAN_MBRCFG [49].SPR[22:20]	3
0xBB01439C	SVLAN_MBRCFG [49].FID_MSTI[19:16]	4
0xBB01439C	SVLAN_MBRCFG [49].RESERVED[15:15]	1
0xBB01439C	SVLAN_MBRCFG [49].UNTAGSET[14:8]	7

Address	Register	Len
0xBB01439C	SVLAN_MBRCFG [49].RESERVED[7:7]	1
0xBB01439C	SVLAN_MBRCFG [49].MBR[6:0]	7
0xBB0143A0	SVLAN_MBRCFG [50].RESERVED[31:16]	16
0xBB0143A0	SVLAN_MBRCFG [50].EFID[15:13]	3
0xBB0143A0	SVLAN_MBRCFG [50].EFIDEN[12:12]	1
0xBB0143A0	SVLAN_MBRCFG [50].SVID[11:0]	12
0xBB0143A4	SVLAN_MBRCFG [50].RESERVED[31:24]	8
0xBB0143A4	SVLAN_MBRCFG [50].FIDEN[23:23]	1
0xBB0143A4	SVLAN_MBRCFG [50].SPR[22:20]	3
0xBB0143A4	SVLAN_MBRCFG [50].FID_MSTI[19:16]	4
0xBB0143A4	SVLAN_MBRCFG [50].RESERVED[15:15]	1
0xBB0143A4	SVLAN_MBRCFG [50].UNTAGSET[14:8]	7
0xBB0143A4	SVLAN_MBRCFG [50].RESERVED[7:7]	1
0xBB0143A4	SVLAN_MBRCFG [50].MBR[6:0]	7
0xBB0143A8	SVLAN_MBRCFG [51].RESERVED[31:16]	16
0xBB0143A8	SVLAN_MBRCFG [51].EFID[15:13]	3
0xBB0143A8	SVLAN_MBRCFG [51].EFIDEN[12:12]	1
0xBB0143A8	SVLAN_MBRCFG [51].SVID[11:0]	12
0xBB0143AC	SVLAN_MBRCFG [51].RESERVED[31:24]	8
0xBB0143AC	SVLAN_MBRCFG [51].FIDEN[23:23]	1
0xBB0143AC	SVLAN_MBRCFG [51].SPR[22:20]	3
0xBB0143AC	SVLAN_MBRCFG [51].FID_MSTI[19:16]	4
0xBB0143AC	SVLAN_MBRCFG [51].RESERVED[15:15]	1
0xBB0143AC	SVLAN_MBRCFG [51].UNTAGSET[14:8]	7
0xBB0143AC	SVLAN_MBRCFG [51].RESERVED[7:7]	1
0xBB0143AC	SVLAN_MBRCFG [51].MBR[6:0]	7
0xBB0143B0	SVLAN_MBRCFG [52].RESERVED[31:16]	16
0xBB0143B0	SVLAN_MBRCFG [52].EFID[15:13]	3
0xBB0143B0	SVLAN_MBRCFG [52].EFIDEN[12:12]	1
0xBB0143B0	SVLAN_MBRCFG [52].SVID[11:0]	12
0xBB0143B4	SVLAN_MBRCFG [52].RESERVED[31:24]	8
0xBB0143B4	SVLAN_MBRCFG [52].FIDEN[23:23]	1
0xBB0143B4	SVLAN_MBRCFG [52].SPR[22:20]	3
0xBB0143B4	SVLAN_MBRCFG [52].FID_MSTI[19:16]	4
0xBB0143B4	SVLAN_MBRCFG [52].RESERVED[15:15]	1
0xBB0143B4	SVLAN_MBRCFG [52].UNTAGSET[14:8]	7
0xBB0143B4	SVLAN_MBRCFG [52].RESERVED[7:7]	1
0xBB0143B4	SVLAN_MBRCFG [52].MBR[6:0]	7
0xBB0143B8	SVLAN_MBRCFG [53].RESERVED[31:16]	16
0xBB0143B8	SVLAN_MBRCFG [53].EFID[15:13]	3
0xBB0143B8	SVLAN_MBRCFG [53].EFIDEN[12:12]	1
0xBB0143B8	SVLAN_MBRCFG [53].SVID[11:0]	12
0xBB0143BC	SVLAN_MBRCFG [53].RESERVED[31:24]	8
0xBB0143BC	SVLAN_MBRCFG [53].FIDEN[23:23]	1
0xBB0143BC	SVLAN_MBRCFG [53].SPR[22:20]	3
0xBB0143BC	SVLAN_MBRCFG [53].FID_MSTI[19:16]	4

Address	Register	Len
0xBB0143BC	SVLAN_MBRCFG [53].RESERVED[15:15]	1
0xBB0143BC	SVLAN_MBRCFG [53].UNTAGSET[14:8]	7
0xBB0143BC	SVLAN_MBRCFG [53].RESERVED[7:7]	1
0xBB0143BC	SVLAN_MBRCFG [53].MBR[6:0]	7
0xBB0143C0	SVLAN_MBRCFG [54].RESERVED[31:16]	16
0xBB0143C0	SVLAN_MBRCFG [54].EFID[15:13]	3
0xBB0143C0	SVLAN_MBRCFG [54].EFIDEN[12:12]	1
0xBB0143C0	SVLAN_MBRCFG [54].SVID[11:0]	12
0xBB0143C4	SVLAN_MBRCFG [54].RESERVED[31:24]	8
0xBB0143C4	SVLAN_MBRCFG [54].FIDEN[23:23]	1
0xBB0143C4	SVLAN_MBRCFG [54].SPR[22:20]	3
0xBB0143C4	SVLAN_MBRCFG [54].FID_MSTI[19:16]	4
0xBB0143C4	SVLAN_MBRCFG [54].RESERVED[15:15]	1
0xBB0143C4	SVLAN_MBRCFG [54].UNTAGSET[14:8]	7
0xBB0143C4	SVLAN_MBRCFG [54].RESERVED[7:7]	1
0xBB0143C4	SVLAN_MBRCFG [54].MBR[6:0]	7
0xBB0143C8	SVLAN_MBRCFG [55].RESERVED[31:16]	16
0xBB0143C8	SVLAN_MBRCFG [55].EFID[15:13]	3
0xBB0143C8	SVLAN_MBRCFG [55].EFIDEN[12:12]	1
0xBB0143C8	SVLAN_MBRCFG [55].SVID[11:0]	12
0xBB0143CC	SVLAN_MBRCFG [55].RESERVED[31:24]	8
0xBB0143CC	SVLAN_MBRCFG [55].FIDEN[23:23]	1
0xBB0143CC	SVLAN_MBRCFG [55].SPR[22:20]	3
0xBB0143CC	SVLAN_MBRCFG [55].FID_MSTI[19:16]	4
0xBB0143CC	SVLAN_MBRCFG [55].RESERVED[15:15]	1
0xBB0143CC	SVLAN_MBRCFG [55].UNTAGSET[14:8]	7
0xBB0143CC	SVLAN_MBRCFG [55].RESERVED[7:7]	1
0xBB0143CC	SVLAN_MBRCFG [55].MBR[6:0]	7
0xBB0143D0	SVLAN_MBRCFG [56].RESERVED[31:16]	16
0xBB0143D0	SVLAN_MBRCFG [56].EFID[15:13]	3
0xBB0143D0	SVLAN_MBRCFG [56].EFIDEN[12:12]	1
0xBB0143D0	SVLAN_MBRCFG [56].SVID[11:0]	12
0xBB0143D4	SVLAN_MBRCFG [56].RESERVED[31:24]	8
0xBB0143D4	SVLAN_MBRCFG [56].FIDEN[23:23]	1
0xBB0143D4	SVLAN_MBRCFG [56].SPR[22:20]	3
0xBB0143D4	SVLAN_MBRCFG [56].FID_MSTI[19:16]	4
0xBB0143D4	SVLAN_MBRCFG [56].RESERVED[15:15]	1
0xBB0143D4	SVLAN_MBRCFG [56].UNTAGSET[14:8]	7
0xBB0143D4	SVLAN_MBRCFG [56].RESERVED[7:7]	1
0xBB0143D4	SVLAN_MBRCFG [56].MBR[6:0]	7
0xBB0143D8	SVLAN_MBRCFG [57].RESERVED[31:16]	16
0xBB0143D8	SVLAN_MBRCFG [57].EFID[15:13]	3
0xBB0143D8	SVLAN_MBRCFG [57].EFIDEN[12:12]	1
0xBB0143D8	SVLAN_MBRCFG [57].SVID[11:0]	12
0xBB0143DC	SVLAN_MBRCFG [57].RESERVED[31:24]	8
0xBB0143DC	SVLAN_MBRCFG [57].FIDEN[23:23]	1



Address	Register	Len
0xBB0143DC	SVLAN_MBRCFG [57].SPR[22:20]	3
0xBB0143DC	SVLAN_MBRCFG [57].FID_MSTI[19:16]	4
0xBB0143DC	SVLAN_MBRCFG [57].RESERVED[15:15]	1
0xBB0143DC	SVLAN_MBRCFG [57].UNTAGSET[14:8]	7
0xBB0143DC	SVLAN_MBRCFG [57].RESERVED[7:7]	1
0xBB0143DC	SVLAN_MBRCFG [57].MBR[6:0]	7
0xBB0143E0	SVLAN_MBRCFG [58].RESERVED[31:16]	16
0xBB0143E0	SVLAN_MBRCFG [58].EFID[15:13]	3
0xBB0143E0	SVLAN_MBRCFG [58].EFIDEN[12:12]	1
0xBB0143E0	SVLAN_MBRCFG [58].SVID[11:0]	12
0xBB0143E4	SVLAN_MBRCFG [58].RESERVED[31:24]	8
0xBB0143E4	SVLAN_MBRCFG [58].FIDEN[23:23]	1
0xBB0143E4	SVLAN_MBRCFG [58].SPR[22:20]	3
0xBB0143E4	SVLAN_MBRCFG [58].FID_MSTI[19:16]	4
0xBB0143E4	SVLAN_MBRCFG [58].RESERVED[15:15]	1
0xBB0143E4	SVLAN_MBRCFG [58].UNTAGSET[14:8]	7
0xBB0143E4	SVLAN_MBRCFG [58].RESERVED[7:7]	1
0xBB0143E4	SVLAN_MBRCFG [58].MBR[6:0]	7
0xBB0143E8	SVLAN_MBRCFG [59].RESERVED[31:16]	16
0xBB0143E8	SVLAN_MBRCFG [59].EFID[15:13]	3
0xBB0143E8	SVLAN_MBRCFG [59].EFIDEN[12:12]	1
0xBB0143E8	SVLAN_MBRCFG [59].SVID[11:0]	12
0xBB0143EC	SVLAN_MBRCFG [59].RESERVED[31:24]	8
0xBB0143EC	SVLAN_MBRCFG [59].FIDEN[23:23]	1
0xBB0143EC	SVLAN_MBRCFG [59].SPR[22:20]	3
0xBB0143EC	SVLAN_MBRCFG [59].FID_MSTI[19:16]	4
0xBB0143EC	SVLAN_MBRCFG [59].RESERVED[15:15]	1
0xBB0143EC	SVLAN_MBRCFG [59].UNTAGSET[14:8]	7
0xBB0143EC	SVLAN_MBRCFG [59].RESERVED[7:7]	1
0xBB0143EC	SVLAN_MBRCFG [59].MBR[6:0]	7
0xBB0143F0	SVLAN_MBRCFG [60].RESERVED[31:16]	16
0xBB0143F0	SVLAN_MBRCFG [60].EFID[15:13]	3
0xBB0143F0	SVLAN_MBRCFG [60].EFIDEN[12:12]	1
0xBB0143F0	SVLAN_MBRCFG [60].SVID[11:0]	12
0xBB0143F4	SVLAN_MBRCFG [60].RESERVED[31:24]	8
0xBB0143F4	SVLAN_MBRCFG [60].FIDEN[23:23]	1
0xBB0143F4	SVLAN_MBRCFG [60].SPR[22:20]	3
0xBB0143F4	SVLAN_MBRCFG [60].FID_MSTI[19:16]	4
0xBB0143F4	SVLAN_MBRCFG [60].RESERVED[15:15]	1
0xBB0143F4	SVLAN_MBRCFG [60].UNTAGSET[14:8]	7
0xBB0143F4	SVLAN_MBRCFG [60].RESERVED[7:7]	1
0xBB0143F4	SVLAN_MBRCFG [60].MBR[6:0]	7
0xBB0143F8	SVLAN_MBRCFG [61].RESERVED[31:16]	16
0xBB0143F8	SVLAN_MBRCFG [61].EFID[15:13]	3
0xBB0143F8	SVLAN_MBRCFG [61].EFIDEN[12:12]	1
0xBB0143F8	SVLAN_MBRCFG [61].SVID[11:0]	12



Address	Register	Len
0xBB0143FC	SVLAN_MBRCFG [61].RESERVED[31:24]	8
0xBB0143FC	SVLAN_MBRCFG [61].FIDEN[23:23]	1
0xBB0143FC	SVLAN_MBRCFG [61].SPR[22:20]	3
0xBB0143FC	SVLAN_MBRCFG [61].FID_MSTI[19:16]	4
0xBB0143FC	SVLAN_MBRCFG [61].RESERVED[15:15]	1
0xBB0143FC	SVLAN_MBRCFG [61].UNTAGSET[14:8]	7
0xBB0143FC	SVLAN_MBRCFG [61].RESERVED[7:7]	1
0xBB0143FC	SVLAN_MBRCFG [61].MBR[6:0]	7
0xBB014400	SVLAN_MBRCFG [62].RESERVED[31:16]	16
0xBB014400	SVLAN_MBRCFG [62].EFID[15:13]	3
0xBB014400	SVLAN_MBRCFG [62].EFIDEN[12:12]	1
0xBB014400	SVLAN_MBRCFG [62].SVID[11:0]	12
0xBB014404	SVLAN_MBRCFG [62].RESERVED[31:24]	8
0xBB014404	SVLAN_MBRCFG [62].FIDEN[23:23]	1
0xBB014404	SVLAN_MBRCFG [62].SPR[22:20]	3
0xBB014404	SVLAN_MBRCFG [62].FID_MSTI[19:16]	4
0xBB014404	SVLAN_MBRCFG [62].RESERVED[15:15]	1
0xBB014404	SVLAN_MBRCFG [62].UNTAGSET[14:8]	7
0xBB014404	SVLAN_MBRCFG [62].RESERVED[7:7]	1
0xBB014404	SVLAN_MBRCFG [62].MBR[6:0]	7
0xBB014408	SVLAN_MBRCFG [63].RESERVED[31:16]	16
0xBB014408	SVLAN_MBRCFG [63].EFID[15:13]	3
0xBB014408	SVLAN_MBRCFG [63].EFIDEN[12:12]	1
0xBB014408	SVLAN_MBRCFG [63].SVID[11:0]	12
0xBB01440C	SVLAN_MBRCFG [63].RESERVED[31:24]	8
0xBB01440C	SVLAN_MBRCFG [63].FIDEN[23:23]	1
0xBB01440C	SVLAN_MBRCFG [63].SPR[22:20]	3
0xBB01440C	SVLAN_MBRCFG [63].FID_MSTI[19:16]	4
0xBB01440C	SVLAN_MBRCFG [63].RESERVED[15:15]	1
0xBB01440C	SVLAN_MBRCFG [63].UNTAGSET[14:8]	7
0xBB01440C	SVLAN_MBRCFG [63].RESERVED[7:7]	1
0xBB01440C	SVLAN_MBRCFG [63].MBR[6:0]	7
0xBB014410	RGF_VER_ALE_SVLAN.REGFILE_VER[31:0]	32
0xBB014414	RSVD_ALE_SVLAN [0].RSVD_MEM[31:0]	32
0xBB014418	RSVD_ALE_SVLAN [1].RSVD_MEM[31:0]	32
0xBB01441C	RSVD_ALE_SVLAN [2].RSVD_MEM[31:0]	32
0xBB014420	RSVD_ALE_SVLAN [3].RSVD_MEM[31:0]	32
0xBB014424	RSVD_ALE_SVLAN [4].RSVD_MEM[31:0]	32
0xBB014428	RSVD_ALE_SVLAN [5].RSVD_MEM[31:0]	32
0xBB01442C	RSVD_ALE_SVLAN [6].RSVD_MEM[31:0]	32
0xBB014430	RSVD_ALE_SVLAN [7].RSVD_MEM[31:0]	32
0xBB014434	RSVD_ALE_SVLAN [8].RSVD_MEM[31:0]	32
0xBB014438	RSVD_ALE_SVLAN [9].RSVD_MEM[31:0]	32
0xBB01443C	RSVD_ALE_SVLAN [10].RSVD_MEM[31:0]	32
0xBB014440	RSVD_ALE_SVLAN [11].RSVD_MEM[31:0]	32
0xBB014444	RSVD_ALE_SVLAN [12].RSVD_MEM[31:0]	32

Address	Register	Len
0xBB014448	RSVD_ALE_SVLAN [13].RSVD_MEM[31:0]	32
0xBB01444C	RSVD_ALE_SVLAN [14].RSVD_MEM[31:0]	32
0xBB014450	RSVD_ALE_SVLAN [15].RSVD_MEM[31:0]	32
0xBB015000	ACL_TEMPLATE_CTRL [0][0].FIELD[6:0]	7
0xBB015000	ACL_TEMPLATE_CTRL [0][1].FIELD[13:7]	7
0xBB015000	ACL_TEMPLATE_CTRL [0][2].FIELD[20:14]	7
0xBB015000	ACL_TEMPLATE_CTRL [0][3].FIELD[27:21]	7
0xBB015004	ACL_TEMPLATE_CTRL [0][4].FIELD[6:0]	7
0xBB015004	ACL_TEMPLATE_CTRL [0][5].FIELD[13:7]	7
0xBB015004	ACL_TEMPLATE_CTRL [0][6].FIELD[20:14]	7
0xBB015004	ACL_TEMPLATE_CTRL [0][7].FIELD[27:21]	7
0xBB015008	ACL_TEMPLATE_CTRL [1][0].FIELD[6:0]	7
0xBB015008	ACL_TEMPLATE_CTRL [1][1].FIELD[13:7]	7
0xBB015008	ACL_TEMPLATE_CTRL [1][2].FIELD[20:14]	7
0xBB015008	ACL_TEMPLATE_CTRL [1][3].FIELD[27:21]	7
0xBB01500C	ACL_TEMPLATE_CTRL [1][4].FIELD[6:0]	7
0xBB01500C	ACL_TEMPLATE_CTRL [1][5].FIELD[13:7]	7
0xBB01500C	ACL_TEMPLATE_CTRL [1][6].FIELD[20:14]	7
0xBB01500C	ACL_TEMPLATE_CTRL [1][7].FIELD[27:21]	7
0xBB015010	ACL_TEMPLATE_CTRL [2][0].FIELD[6:0]	7
0xBB015010	ACL_TEMPLATE_CTRL [2][1].FIELD[13:7]	7
0xBB015010	ACL_TEMPLATE_CTRL [2][2].FIELD[20:14]	7
0xBB015010	ACL_TEMPLATE_CTRL [2][3].FIELD[27:21]	7
0xBB015014	ACL_TEMPLATE_CTRL [2][4].FIELD[6:0]	7
0xBB015014	ACL_TEMPLATE_CTRL [2][5].FIELD[13:7]	7
0xBB015014	ACL_TEMPLATE_CTRL [2][6].FIELD[20:14]	7
0xBB015014	ACL_TEMPLATE_CTRL [2][7].FIELD[27:21]	7
0xBB015018	ACL_TEMPLATE_CTRL [3][0].FIELD[6:0]	7
0xBB015018	ACL_TEMPLATE_CTRL [3][1].FIELD[13:7]	7
0xBB015018	ACL_TEMPLATE_CTRL [3][2].FIELD[20:14]	7
0xBB015018	ACL_TEMPLATE_CTRL [3][3].FIELD[27:21]	7
0xBB01501C	ACL_TEMPLATE_CTRL [3][4].FIELD[6:0]	7
0xBB01501C	ACL_TEMPLATE_CTRL [3][5].FIELD[13:7]	7
0xBB01501C	ACL_TEMPLATE_CTRL [3][6].FIELD[20:14]	7
0xBB01501C	ACL_TEMPLATE_CTRL [3][7].FIELD[27:21]	7
0xBB015020	CF_OP_DS [0].NOT_DS[0:0]	1
0xBB015020	CF_OP_DS [1].NOT_DS[1:1]	1
0xBB015020	CF_OP_DS [2].NOT_DS[2:2]	1
0xBB015020	CF_OP_DS [3].NOT_DS[3:3]	1
0xBB015020	CF_OP_DS [4].NOT_DS[4:4]	1
0xBB015020	CF_OP_DS [5].NOT_DS[5:5]	1
0xBB015020	CF_OP_DS [6].NOT_DS[6:6]	1
0xBB015020	CF_OP_DS [7].NOT_DS[7:7]	1
0xBB015020	CF_OP_DS [8].NOT_DS[8:8]	1
0xBB015020	CF_OP_DS [9].NOT_DS[9:9]	1
0xBB015020	CF_OP_DS [10].NOT_DS[10:10]	1

Address	Register	Len
0xBB015020	CF_OP_DS [11].NOT_DS[11:11]	1
0xBB015020	CF_OP_DS [12].NOT_DS[12:12]	1
0xBB015020	CF_OP_DS [13].NOT_DS[13:13]	1
0xBB015020	CF_OP_DS [14].NOT_DS[14:14]	1
0xBB015020	CF_OP_DS [15].NOT_DS[15:15]	1
0xBB015020	CF_OP_DS [16].NOT_DS[16:16]	1
0xBB015020	CF_OP_DS [17].NOT_DS[17:17]	1
0xBB015020	CF_OP_DS [18].NOT_DS[18:18]	1
0xBB015020	CF_OP_DS [19].NOT_DS[19:19]	1
0xBB015020	CF_OP_DS [20].NOT_DS[20:20]	1
0xBB015020	CF_OP_DS [21].NOT_DS[21:21]	1
0xBB015020	CF_OP_DS [22].NOT_DS[22:22]	1
0xBB015020	CF_OP_DS [23].NOT_DS[23:23]	1
0xBB015020	CF_OP_DS [24].NOT_DS[24:24]	1
0xBB015020	CF_OP_DS [25].NOT_DS[25:25]	1
0xBB015020	CF_OP_DS [26].NOT_DS[26:26]	1
0xBB015020	CF_OP_DS [27].NOT_DS[27:27]	1
0xBB015020	CF_OP_DS [28].NOT_DS[28:28]	1
0xBB015020	CF_OP_DS [29].NOT_DS[29:29]	1
0xBB015020	CF_OP_DS [30].NOT_DS[30:30]	1
0xBB015020	CF_OP_DS [31].NOT_DS[31:31]	1
0xBB015024	CF_OP_DS [32].NOT_DS[0:0]	1
0xBB015024	CF_OP_DS [33].NOT_DS[1:1]	1
0xBB015024	CF_OP_DS [34].NOT_DS[2:2]	1
0xBB015024	CF_OP_DS [35].NOT_DS[3:3]	1
0xBB015024	CF_OP_DS [36].NOT_DS[4:4]	1
0xBB015024	CF_OP_DS [37].NOT_DS[5:5]	1
0xBB015024	CF_OP_DS [38].NOT_DS[6:6]	1
0xBB015024	CF_OP_DS [39].NOT_DS[7:7]	1
0xBB015024	CF_OP_DS [40].NOT_DS[8:8]	1
0xBB015024	CF_OP_DS [41].NOT_DS[9:9]	1
0xBB015024	CF_OP_DS [42].NOT_DS[10:10]	1
0xBB015024	CF_OP_DS [43].NOT_DS[11:11]	1
0xBB015024	CF_OP_DS [44].NOT_DS[12:12]	1
0xBB015024	CF_OP_DS [45].NOT_DS[13:13]	1
0xBB015024	CF_OP_DS [46].NOT_DS[14:14]	1
0xBB015024	CF_OP_DS [47].NOT_DS[15:15]	1
0xBB015024	CF_OP_DS [48].NOT_DS[16:16]	1
0xBB015024	CF_OP_DS [49].NOT_DS[17:17]	1
0xBB015024	CF_OP_DS [50].NOT_DS[18:18]	1
0xBB015024	CF_OP_DS [51].NOT_DS[19:19]	1
0xBB015024	CF_OP_DS [52].NOT_DS[20:20]	1
0xBB015024	CF_OP_DS [53].NOT_DS[21:21]	1
0xBB015024	CF_OP_DS [54].NOT_DS[22:22]	1
0xBB015024	CF_OP_DS [55].NOT_DS[23:23]	1
0xBB015024	CF_OP_DS [56].NOT_DS[24:24]	1

Address	Register	Len
0xBB015024	CF_OP_DS [57].NOT_DS[25:25]	1
0xBB015024	CF_OP_DS [58].NOT_DS[26:26]	1
0xBB015024	CF_OP_DS [59].NOT_DS[27:27]	1
0xBB015024	CF_OP_DS [60].NOT_DS[28:28]	1
0xBB015024	CF_OP_DS [61].NOT_DS[29:29]	1
0xBB015024	CF_OP_DS [62].NOT_DS[30:30]	1
0xBB015024	CF_OP_DS [63].NOT_DS[31:31]	1
0xBB015028	CF_OP_DS [64].NOT_DS[0:0]	1
0xBB015028	CF_OP_DS [65].NOT_DS[1:1]	1
0xBB015028	CF_OP_DS [66].NOT_DS[2:2]	1
0xBB015028	CF_OP_DS [67].NOT_DS[3:3]	1
0xBB015028	CF_OP_DS [68].NOT_DS[4:4]	1
0xBB015028	CF_OP_DS [69].NOT_DS[5:5]	1
0xBB015028	CF_OP_DS [70].NOT_DS[6:6]	1
0xBB015028	CF_OP_DS [71].NOT_DS[7:7]	1
0xBB015028	CF_OP_DS [72].NOT_DS[8:8]	1
0xBB015028	CF_OP_DS [73].NOT_DS[9:9]	1
0xBB015028	CF_OP_DS [74].NOT_DS[10:10]	1
0xBB015028	CF_OP_DS [75].NOT_DS[11:11]	1
0xBB015028	CF_OP_DS [76].NOT_DS[12:12]	1
0xBB015028	CF_OP_DS [77].NOT_DS[13:13]	1
0xBB015028	CF_OP_DS [78].NOT_DS[14:14]	1
0xBB015028	CF_OP_DS [79].NOT_DS[15:15]	1
0xBB015028	CF_OP_DS [80].NOT_DS[16:16]	1
0xBB015028	CF_OP_DS [81].NOT_DS[17:17]	1
0xBB015028	CF_OP_DS [82].NOT_DS[18:18]	1
0xBB015028	CF_OP_DS [83].NOT_DS[19:19]	1
0xBB015028	CF_OP_DS [84].NOT_DS[20:20]	1
0xBB015028	CF_OP_DS [85].NOT_DS[21:21]	1
0xBB015028	CF_OP_DS [86].NOT_DS[22:22]	1
0xBB015028	CF_OP_DS [87].NOT_DS[23:23]	1
0xBB015028	CF_OP_DS [88].NOT_DS[24:24]	1
0xBB015028	CF_OP_DS [89].NOT_DS[25:25]	1
0xBB015028	CF_OP_DS [90].NOT_DS[26:26]	1
0xBB015028	CF_OP_DS [91].NOT_DS[27:27]	1
0xBB015028	CF_OP_DS [92].NOT_DS[28:28]	1
0xBB015028	CF_OP_DS [93].NOT_DS[29:29]	1
0xBB015028	CF_OP_DS [94].NOT_DS[30:30]	1
0xBB015028	CF_OP_DS [95].NOT_DS[31:31]	1
0xBB01502C	CF_OP_DS [96].NOT_DS[0:0]	1
0xBB01502C	CF_OP_DS [97].NOT_DS[1:1]	1
0xBB01502C	CF_OP_DS [98].NOT_DS[2:2]	1
0xBB01502C	CF_OP_DS [99].NOT_DS[3:3]	1
0xBB01502C	CF_OP_DS [100].NOT_DS[4:4]	1
0xBB01502C	CF_OP_DS [101].NOT_DS[5:5]	1
0xBB01502C	CF_OP_DS [102].NOT_DS[6:6]	1

Address	Register	Len
0xBB01502C	CF_OP_DS [103].NOT_DS[7:7]	1
0xBB01502C	CF_OP_DS [104].NOT_DS[8:8]	1
0xBB01502C	CF_OP_DS [105].NOT_DS[9:9]	1
0xBB01502C	CF_OP_DS [106].NOT_DS[10:10]	1
0xBB01502C	CF_OP_DS [107].NOT_DS[11:11]	1
0xBB01502C	CF_OP_DS [108].NOT_DS[12:12]	1
0xBB01502C	CF_OP_DS [109].NOT_DS[13:13]	1
0xBB01502C	CF_OP_DS [110].NOT_DS[14:14]	1
0xBB01502C	CF_OP_DS [111].NOT_DS[15:15]	1
0xBB01502C	CF_OP_DS [112].NOT_DS[16:16]	1
0xBB01502C	CF_OP_DS [113].NOT_DS[17:17]	1
0xBB01502C	CF_OP_DS [114].NOT_DS[18:18]	1
0xBB01502C	CF_OP_DS [115].NOT_DS[19:19]	1
0xBB01502C	CF_OP_DS [116].NOT_DS[20:20]	1
0xBB01502C	CF_OP_DS [117].NOT_DS[21:21]	1
0xBB01502C	CF_OP_DS [118].NOT_DS[22:22]	1
0xBB01502C	CF_OP_DS [119].NOT_DS[23:23]	1
0xBB01502C	CF_OP_DS [120].NOT_DS[24:24]	1
0xBB01502C	CF_OP_DS [121].NOT_DS[25:25]	1
0xBB01502C	CF_OP_DS [122].NOT_DS[26:26]	1
0xBB01502C	CF_OP_DS [123].NOT_DS[27:27]	1
0xBB01502C	CF_OP_DS [124].NOT_DS[28:28]	1
0xBB01502C	CF_OP_DS [125].NOT_DS[29:29]	1
0xBB01502C	CF_OP_DS [126].NOT_DS[30:30]	1
0xBB01502C	CF_OP_DS [127].NOT_DS[31:31]	1
0xBB015030	CF_OP_DS [128].NOT_DS[0:0]	1
0xBB015030	CF_OP_DS [129].NOT_DS[1:1]	1
0xBB015030	CF_OP_DS [130].NOT_DS[2:2]	1
0xBB015030	CF_OP_DS [131].NOT_DS[3:3]	1
0xBB015030	CF_OP_DS [132].NOT_DS[4:4]	1
0xBB015030	CF_OP_DS [133].NOT_DS[5:5]	1
0xBB015030	CF_OP_DS [134].NOT_DS[6:6]	1
0xBB015030	CF_OP_DS [135].NOT_DS[7:7]	1
0xBB015030	CF_OP_DS [136].NOT_DS[8:8]	1
0xBB015030	CF_OP_DS [137].NOT_DS[9:9]	1
0xBB015030	CF_OP_DS [138].NOT_DS[10:10]	1
0xBB015030	CF_OP_DS [139].NOT_DS[11:11]	1
0xBB015030	CF_OP_DS [140].NOT_DS[12:12]	1
0xBB015030	CF_OP_DS [141].NOT_DS[13:13]	1
0xBB015030	CF_OP_DS [142].NOT_DS[14:14]	1
0xBB015030	CF_OP_DS [143].NOT_DS[15:15]	1
0xBB015030	CF_OP_DS [144].NOT_DS[16:16]	1
0xBB015030	CF_OP_DS [145].NOT_DS[17:17]	1
0xBB015030	CF_OP_DS [146].NOT_DS[18:18]	1
0xBB015030	CF_OP_DS [147].NOT_DS[19:19]	1
0xBB015030	CF_OP_DS [148].NOT_DS[20:20]	1

Address	Register	Len
0xBB015030	CF_OP_DS [149].NOT_DS[21:21]	1
0xBB015030	CF_OP_DS [150].NOT_DS[22:22]	1
0xBB015030	CF_OP_DS [151].NOT_DS[23:23]	1
0xBB015030	CF_OP_DS [152].NOT_DS[24:24]	1
0xBB015030	CF_OP_DS [153].NOT_DS[25:25]	1
0xBB015030	CF_OP_DS [154].NOT_DS[26:26]	1
0xBB015030	CF_OP_DS [155].NOT_DS[27:27]	1
0xBB015030	CF_OP_DS [156].NOT_DS[28:28]	1
0xBB015030	CF_OP_DS [157].NOT_DS[29:29]	1
0xBB015030	CF_OP_DS [158].NOT_DS[30:30]	1
0xBB015030	CF_OP_DS [159].NOT_DS[31:31]	1
0xBB015034	CF_OP_DS [160].NOT_DS[0:0]	1
0xBB015034	CF_OP_DS [161].NOT_DS[1:1]	1
0xBB015034	CF_OP_DS [162].NOT_DS[2:2]	1
0xBB015034	CF_OP_DS [163].NOT_DS[3:3]	1
0xBB015034	CF_OP_DS [164].NOT_DS[4:4]	1
0xBB015034	CF_OP_DS [165].NOT_DS[5:5]	1
0xBB015034	CF_OP_DS [166].NOT_DS[6:6]	1
0xBB015034	CF_OP_DS [167].NOT_DS[7:7]	1
0xBB015034	CF_OP_DS [168].NOT_DS[8:8]	1
0xBB015034	CF_OP_DS [169].NOT_DS[9:9]	1
0xBB015034	CF_OP_DS [170].NOT_DS[10:10]	1
0xBB015034	CF_OP_DS [171].NOT_DS[11:11]	1
0xBB015034	CF_OP_DS [172].NOT_DS[12:12]	1
0xBB015034	CF_OP_DS [173].NOT_DS[13:13]	1
0xBB015034	CF_OP_DS [174].NOT_DS[14:14]	1
0xBB015034	CF_OP_DS [175].NOT_DS[15:15]	1
0xBB015034	CF_OP_DS [176].NOT_DS[16:16]	1
0xBB015034	CF_OP_DS [177].NOT_DS[17:17]	1
0xBB015034	CF_OP_DS [178].NOT_DS[18:18]	1
0xBB015034	CF_OP_DS [179].NOT_DS[19:19]	1
0xBB015034	CF_OP_DS [180].NOT_DS[20:20]	1
0xBB015034	CF_OP_DS [181].NOT_DS[21:21]	1
0xBB015034	CF_OP_DS [182].NOT_DS[22:22]	1
0xBB015034	CF_OP_DS [183].NOT_DS[23:23]	1
0xBB015034	CF_OP_DS [184].NOT_DS[24:24]	1
0xBB015034	CF_OP_DS [185].NOT_DS[25:25]	1
0xBB015034	CF_OP_DS [186].NOT_DS[26:26]	1
0xBB015034	CF_OP_DS [187].NOT_DS[27:27]	1
0xBB015034	CF_OP_DS [188].NOT_DS[28:28]	1
0xBB015034	CF_OP_DS [189].NOT_DS[29:29]	1
0xBB015034	CF_OP_DS [190].NOT_DS[30:30]	1
0xBB015034	CF_OP_DS [191].NOT_DS[31:31]	1
0xBB015038	CF_OP_DS [192].NOT_DS[0:0]	1
0xBB015038	CF_OP_DS [193].NOT_DS[1:1]	1
0xBB015038	CF_OP_DS [194].NOT_DS[2:2]	1

Address	Register	Len
0xBB015038	CF_OP_DS [195].NOT_DS[3:3]	1
0xBB015038	CF_OP_DS [196].NOT_DS[4:4]	1
0xBB015038	CF_OP_DS [197].NOT_DS[5:5]	1
0xBB015038	CF_OP_DS [198].NOT_DS[6:6]	1
0xBB015038	CF_OP_DS [199].NOT_DS[7:7]	1
0xBB015038	CF_OP_DS [200].NOT_DS[8:8]	1
0xBB015038	CF_OP_DS [201].NOT_DS[9:9]	1
0xBB015038	CF_OP_DS [202].NOT_DS[10:10]	1
0xBB015038	CF_OP_DS [203].NOT_DS[11:11]	1
0xBB015038	CF_OP_DS [204].NOT_DS[12:12]	1
0xBB015038	CF_OP_DS [205].NOT_DS[13:13]	1
0xBB015038	CF_OP_DS [206].NOT_DS[14:14]	1
0xBB015038	CF_OP_DS [207].NOT_DS[15:15]	1
0xBB015038	CF_OP_DS [208].NOT_DS[16:16]	1
0xBB015038	CF_OP_DS [209].NOT_DS[17:17]	1
0xBB015038	CF_OP_DS [210].NOT_DS[18:18]	1
0xBB015038	CF_OP_DS [211].NOT_DS[19:19]	1
0xBB015038	CF_OP_DS [212].NOT_DS[20:20]	1
0xBB015038	CF_OP_DS [213].NOT_DS[21:21]	1
0xBB015038	CF_OP_DS [214].NOT_DS[22:22]	1
0xBB015038	CF_OP_DS [215].NOT_DS[23:23]	1
0xBB015038	CF_OP_DS [216].NOT_DS[24:24]	1
0xBB015038	CF_OP_DS [217].NOT_DS[25:25]	1
0xBB015038	CF_OP_DS [218].NOT_DS[26:26]	1
0xBB015038	CF_OP_DS [219].NOT_DS[27:27]	1
0xBB015038	CF_OP_DS [220].NOT_DS[28:28]	1
0xBB015038	CF_OP_DS [221].NOT_DS[29:29]	1
0xBB015038	CF_OP_DS [222].NOT_DS[30:30]	1
0xBB015038	CF_OP_DS [223].NOT_DS[31:31]	1
0xBB01503C	CF_OP_DS [224].NOT_DS[0:0]	1
0xBB01503C	CF_OP_DS [225].NOT_DS[1:1]	1
0xBB01503C	CF_OP_DS [226].NOT_DS[2:2]	1
0xBB01503C	CF_OP_DS [227].NOT_DS[3:3]	1
0xBB01503C	CF_OP_DS [228].NOT_DS[4:4]	1
0xBB01503C	CF_OP_DS [229].NOT_DS[5:5]	1
0xBB01503C	CF_OP_DS [230].NOT_DS[6:6]	1
0xBB01503C	CF_OP_DS [231].NOT_DS[7:7]	1
0xBB01503C	CF_OP_DS [232].NOT_DS[8:8]	1
0xBB01503C	CF_OP_DS [233].NOT_DS[9:9]	1
0xBB01503C	CF_OP_DS [234].NOT_DS[10:10]	1
0xBB01503C	CF_OP_DS [235].NOT_DS[11:11]	1
0xBB01503C	CF_OP_DS [236].NOT_DS[12:12]	1
0xBB01503C	CF_OP_DS [237].NOT_DS[13:13]	1
0xBB01503C	CF_OP_DS [238].NOT_DS[14:14]	1
0xBB01503C	CF_OP_DS [239].NOT_DS[15:15]	1
0xBB01503C	CF_OP_DS [240].NOT_DS[16:16]	1

Address	Register	Len
0xBB01503C	CF_OP_DS [241].NOT_DS[17:17]	1
0xBB01503C	CF_OP_DS [242].NOT_DS[18:18]	1
0xBB01503C	CF_OP_DS [243].NOT_DS[19:19]	1
0xBB01503C	CF_OP_DS [244].NOT_DS[20:20]	1
0xBB01503C	CF_OP_DS [245].NOT_DS[21:21]	1
0xBB01503C	CF_OP_DS [246].NOT_DS[22:22]	1
0xBB01503C	CF_OP_DS [247].NOT_DS[23:23]	1
0xBB01503C	CF_OP_DS [248].NOT_DS[24:24]	1
0xBB01503C	CF_OP_DS [249].NOT_DS[25:25]	1
0xBB01503C	CF_OP_DS [250].NOT_DS[26:26]	1
0xBB01503C	CF_OP_DS [251].NOT_DS[27:27]	1
0xBB01503C	CF_OP_DS [252].NOT_DS[28:28]	1
0xBB01503C	CF_OP_DS [253].NOT_DS[29:29]	1
0xBB01503C	CF_OP_DS [254].NOT_DS[30:30]	1
0xBB01503C	CF_OP_DS [255].NOT_DS[31:31]	1
0xBB015040	CF_OP_DS [256].NOT_DS[0:0]	1
0xBB015040	CF_OP_DS [257].NOT_DS[1:1]	1
0xBB015040	CF_OP_DS [258].NOT_DS[2:2]	1
0xBB015040	CF_OP_DS [259].NOT_DS[3:3]	1
0xBB015040	CF_OP_DS [260].NOT_DS[4:4]	1
0xBB015040	CF_OP_DS [261].NOT_DS[5:5]	1
0xBB015040	CF_OP_DS [262].NOT_DS[6:6]	1
0xBB015040	CF_OP_DS [263].NOT_DS[7:7]	1
0xBB015040	CF_OP_DS [264].NOT_DS[8:8]	1
0xBB015040	CF_OP_DS [265].NOT_DS[9:9]	1
0xBB015040	CF_OP_DS [266].NOT_DS[10:10]	1
0xBB015040	CF_OP_DS [267].NOT_DS[11:11]	1
0xBB015040	CF_OP_DS [268].NOT_DS[12:12]	1
0xBB015040	CF_OP_DS [269].NOT_DS[13:13]	1
0xBB015040	CF_OP_DS [270].NOT_DS[14:14]	1
0xBB015040	CF_OP_DS [271].NOT_DS[15:15]	1
0xBB015040	CF_OP_DS [272].NOT_DS[16:16]	1
0xBB015040	CF_OP_DS [273].NOT_DS[17:17]	1
0xBB015040	CF_OP_DS [274].NOT_DS[18:18]	1
0xBB015040	CF_OP_DS [275].NOT_DS[19:19]	1
0xBB015040	CF_OP_DS [276].NOT_DS[20:20]	1
0xBB015040	CF_OP_DS [277].NOT_DS[21:21]	1
0xBB015040	CF_OP_DS [278].NOT_DS[22:22]	1
0xBB015040	CF_OP_DS [279].NOT_DS[23:23]	1
0xBB015040	CF_OP_DS [280].NOT_DS[24:24]	1
0xBB015040	CF_OP_DS [281].NOT_DS[25:25]	1
0xBB015040	CF_OP_DS [282].NOT_DS[26:26]	1
0xBB015040	CF_OP_DS [283].NOT_DS[27:27]	1
0xBB015040	CF_OP_DS [284].NOT_DS[28:28]	1
0xBB015040	CF_OP_DS [285].NOT_DS[29:29]	1
0xBB015040	CF_OP_DS [286].NOT_DS[30:30]	1



Address	Register	Len
0xBB015040	CF_OP_DS [287].NOT_DS[31:31]	1
0xBB015044	CF_OP_DS [288].NOT_DS[0:0]	1
0xBB015044	CF_OP_DS [289].NOT_DS[1:1]	1
0xBB015044	CF_OP_DS [290].NOT_DS[2:2]	1
0xBB015044	CF_OP_DS [291].NOT_DS[3:3]	1
0xBB015044	CF_OP_DS [292].NOT_DS[4:4]	1
0xBB015044	CF_OP_DS [293].NOT_DS[5:5]	1
0xBB015044	CF_OP_DS [294].NOT_DS[6:6]	1
0xBB015044	CF_OP_DS [295].NOT_DS[7:7]	1
0xBB015044	CF_OP_DS [296].NOT_DS[8:8]	1
0xBB015044	CF_OP_DS [297].NOT_DS[9:9]	1
0xBB015044	CF_OP_DS [298].NOT_DS[10:10]	1
0xBB015044	CF_OP_DS [299].NOT_DS[11:11]	1
0xBB015044	CF_OP_DS [300].NOT_DS[12:12]	1
0xBB015044	CF_OP_DS [301].NOT_DS[13:13]	1
0xBB015044	CF_OP_DS [302].NOT_DS[14:14]	1
0xBB015044	CF_OP_DS [303].NOT_DS[15:15]	1
0xBB015044	CF_OP_DS [304].NOT_DS[16:16]	1
0xBB015044	CF_OP_DS [305].NOT_DS[17:17]	1
0xBB015044	CF_OP_DS [306].NOT_DS[18:18]	1
0xBB015044	CF_OP_DS [307].NOT_DS[19:19]	1
0xBB015044	CF_OP_DS [308].NOT_DS[20:20]	1
0xBB015044	CF_OP_DS [309].NOT_DS[21:21]	1
0xBB015044	CF_OP_DS [310].NOT_DS[22:22]	1
0xBB015044	CF_OP_DS [311].NOT_DS[23:23]	1
0xBB015044	CF_OP_DS [312].NOT_DS[24:24]	1
0xBB015044	CF_OP_DS [313].NOT_DS[25:25]	1
0xBB015044	CF_OP_DS [314].NOT_DS[26:26]	1
0xBB015044	CF_OP_DS [315].NOT_DS[27:27]	1
0xBB015044	CF_OP_DS [316].NOT_DS[28:28]	1
0xBB015044	CF_OP_DS [317].NOT_DS[29:29]	1
0xBB015044	CF_OP_DS [318].NOT_DS[30:30]	1
0xBB015044	CF_OP_DS [319].NOT_DS[31:31]	1
0xBB015048	CF_OP_DS [320].NOT_DS[0:0]	1
0xBB015048	CF_OP_DS [321].NOT_DS[1:1]	1
0xBB015048	CF_OP_DS [322].NOT_DS[2:2]	1
0xBB015048	CF_OP_DS [323].NOT_DS[3:3]	1
0xBB015048	CF_OP_DS [324].NOT_DS[4:4]	1
0xBB015048	CF_OP_DS [325].NOT_DS[5:5]	1
0xBB015048	CF_OP_DS [326].NOT_DS[6:6]	1
0xBB015048	CF_OP_DS [327].NOT_DS[7:7]	1
0xBB015048	CF_OP_DS [328].NOT_DS[8:8]	1
0xBB015048	CF_OP_DS [329].NOT_DS[9:9]	1
0xBB015048	CF_OP_DS [330].NOT_DS[10:10]	1
0xBB015048	CF_OP_DS [331].NOT_DS[11:11]	1
0xBB015048	CF_OP_DS [332].NOT_DS[12:12]	1

Address	Register	Len
0xBB015048	CF_OP_DS [333].NOT_DS[13:13]	1
0xBB015048	CF_OP_DS [334].NOT_DS[14:14]	1
0xBB015048	CF_OP_DS [335].NOT_DS[15:15]	1
0xBB015048	CF_OP_DS [336].NOT_DS[16:16]	1
0xBB015048	CF_OP_DS [337].NOT_DS[17:17]	1
0xBB015048	CF_OP_DS [338].NOT_DS[18:18]	1
0xBB015048	CF_OP_DS [339].NOT_DS[19:19]	1
0xBB015048	CF_OP_DS [340].NOT_DS[20:20]	1
0xBB015048	CF_OP_DS [341].NOT_DS[21:21]	1
0xBB015048	CF_OP_DS [342].NOT_DS[22:22]	1
0xBB015048	CF_OP_DS [343].NOT_DS[23:23]	1
0xBB015048	CF_OP_DS [344].NOT_DS[24:24]	1
0xBB015048	CF_OP_DS [345].NOT_DS[25:25]	1
0xBB015048	CF_OP_DS [346].NOT_DS[26:26]	1
0xBB015048	CF_OP_DS [347].NOT_DS[27:27]	1
0xBB015048	CF_OP_DS [348].NOT_DS[28:28]	1
0xBB015048	CF_OP_DS [349].NOT_DS[29:29]	1
0xBB015048	CF_OP_DS [350].NOT_DS[30:30]	1
0xBB015048	CF_OP_DS [351].NOT_DS[31:31]	1
0xBB01504C	CF_OP_DS [352].NOT_DS[0:0]	1
0xBB01504C	CF_OP_DS [353].NOT_DS[1:1]	1
0xBB01504C	CF_OP_DS [354].NOT_DS[2:2]	1
0xBB01504C	CF_OP_DS [355].NOT_DS[3:3]	1
0xBB01504C	CF_OP_DS [356].NOT_DS[4:4]	1
0xBB01504C	CF_OP_DS [357].NOT_DS[5:5]	1
0xBB01504C	CF_OP_DS [358].NOT_DS[6:6]	1
0xBB01504C	CF_OP_DS [359].NOT_DS[7:7]	1
0xBB01504C	CF_OP_DS [360].NOT_DS[8:8]	1
0xBB01504C	CF_OP_DS [361].NOT_DS[9:9]	1
0xBB01504C	CF_OP_DS [362].NOT_DS[10:10]	1
0xBB01504C	CF_OP_DS [363].NOT_DS[11:11]	1
0xBB01504C	CF_OP_DS [364].NOT_DS[12:12]	1
0xBB01504C	CF_OP_DS [365].NOT_DS[13:13]	1
0xBB01504C	CF_OP_DS [366].NOT_DS[14:14]	1
0xBB01504C	CF_OP_DS [367].NOT_DS[15:15]	1
0xBB01504C	CF_OP_DS [368].NOT_DS[16:16]	1
0xBB01504C	CF_OP_DS [369].NOT_DS[17:17]	1
0xBB01504C	CF_OP_DS [370].NOT_DS[18:18]	1
0xBB01504C	CF_OP_DS [371].NOT_DS[19:19]	1
0xBB01504C	CF_OP_DS [372].NOT_DS[20:20]	1
0xBB01504C	CF_OP_DS [373].NOT_DS[21:21]	1
0xBB01504C	CF_OP_DS [374].NOT_DS[22:22]	1
0xBB01504C	CF_OP_DS [375].NOT_DS[23:23]	1
0xBB01504C	CF_OP_DS [376].NOT_DS[24:24]	1
0xBB01504C	CF_OP_DS [377].NOT_DS[25:25]	1
0xBB01504C	CF_OP_DS [378].NOT_DS[26:26]	1

Address	Register	Len
0xBB01504C	CF_OP_DS [379].NOT_DS[27:27]	1
0xBB01504C	CF_OP_DS [380].NOT_DS[28:28]	1
0xBB01504C	CF_OP_DS [381].NOT_DS[29:29]	1
0xBB01504C	CF_OP_DS [382].NOT_DS[30:30]	1
0xBB01504C	CF_OP_DS [383].NOT_DS[31:31]	1
0xBB015050	CF_OP_DS [384].NOT_DS[0:0]	1
0xBB015050	CF_OP_DS [385].NOT_DS[1:1]	1
0xBB015050	CF_OP_DS [386].NOT_DS[2:2]	1
0xBB015050	CF_OP_DS [387].NOT_DS[3:3]	1
0xBB015050	CF_OP_DS [388].NOT_DS[4:4]	1
0xBB015050	CF_OP_DS [389].NOT_DS[5:5]	1
0xBB015050	CF_OP_DS [390].NOT_DS[6:6]	1
0xBB015050	CF_OP_DS [391].NOT_DS[7:7]	1
0xBB015050	CF_OP_DS [392].NOT_DS[8:8]	1
0xBB015050	CF_OP_DS [393].NOT_DS[9:9]	1
0xBB015050	CF_OP_DS [394].NOT_DS[10:10]	1
0xBB015050	CF_OP_DS [395].NOT_DS[11:11]	1
0xBB015050	CF_OP_DS [396].NOT_DS[12:12]	1
0xBB015050	CF_OP_DS [397].NOT_DS[13:13]	1
0xBB015050	CF_OP_DS [398].NOT_DS[14:14]	1
0xBB015050	CF_OP_DS [399].NOT_DS[15:15]	1
0xBB015050	CF_OP_DS [400].NOT_DS[16:16]	1
0xBB015050	CF_OP_DS [401].NOT_DS[17:17]	1
0xBB015050	CF_OP_DS [402].NOT_DS[18:18]	1
0xBB015050	CF_OP_DS [403].NOT_DS[19:19]	1
0xBB015050	CF_OP_DS [404].NOT_DS[20:20]	1
0xBB015050	CF_OP_DS [405].NOT_DS[21:21]	1
0xBB015050	CF_OP_DS [406].NOT_DS[22:22]	1
0xBB015050	CF_OP_DS [407].NOT_DS[23:23]	1
0xBB015050	CF_OP_DS [408].NOT_DS[24:24]	1
0xBB015050	CF_OP_DS [409].NOT_DS[25:25]	1
0xBB015050	CF_OP_DS [410].NOT_DS[26:26]	1
0xBB015050	CF_OP_DS [411].NOT_DS[27:27]	1
0xBB015050	CF_OP_DS [412].NOT_DS[28:28]	1
0xBB015050	CF_OP_DS [413].NOT_DS[29:29]	1
0xBB015050	CF_OP_DS [414].NOT_DS[30:30]	1
0xBB015050	CF_OP_DS [415].NOT_DS[31:31]	1
0xBB015054	CF_OP_DS [416].NOT_DS[0:0]	1
0xBB015054	CF_OP_DS [417].NOT_DS[1:1]	1
0xBB015054	CF_OP_DS [418].NOT_DS[2:2]	1
0xBB015054	CF_OP_DS [419].NOT_DS[3:3]	1
0xBB015054	CF_OP_DS [420].NOT_DS[4:4]	1
0xBB015054	CF_OP_DS [421].NOT_DS[5:5]	1
0xBB015054	CF_OP_DS [422].NOT_DS[6:6]	1
0xBB015054	CF_OP_DS [423].NOT_DS[7:7]	1
0xBB015054	CF_OP_DS [424].NOT_DS[8:8]	1

Address	Register	Len
0xBB015054	CF_OP_DS [425].NOT_DS[9:9]	1
0xBB015054	CF_OP_DS [426].NOT_DS[10:10]	1
0xBB015054	CF_OP_DS [427].NOT_DS[11:11]	1
0xBB015054	CF_OP_DS [428].NOT_DS[12:12]	1
0xBB015054	CF_OP_DS [429].NOT_DS[13:13]	1
0xBB015054	CF_OP_DS [430].NOT_DS[14:14]	1
0xBB015054	CF_OP_DS [431].NOT_DS[15:15]	1
0xBB015054	CF_OP_DS [432].NOT_DS[16:16]	1
0xBB015054	CF_OP_DS [433].NOT_DS[17:17]	1
0xBB015054	CF_OP_DS [434].NOT_DS[18:18]	1
0xBB015054	CF_OP_DS [435].NOT_DS[19:19]	1
0xBB015054	CF_OP_DS [436].NOT_DS[20:20]	1
0xBB015054	CF_OP_DS [437].NOT_DS[21:21]	1
0xBB015054	CF_OP_DS [438].NOT_DS[22:22]	1
0xBB015054	CF_OP_DS [439].NOT_DS[23:23]	1
0xBB015054	CF_OP_DS [440].NOT_DS[24:24]	1
0xBB015054	CF_OP_DS [441].NOT_DS[25:25]	1
0xBB015054	CF_OP_DS [442].NOT_DS[26:26]	1
0xBB015054	CF_OP_DS [443].NOT_DS[27:27]	1
0xBB015054	CF_OP_DS [444].NOT_DS[28:28]	1
0xBB015054	CF_OP_DS [445].NOT_DS[29:29]	1
0xBB015054	CF_OP_DS [446].NOT_DS[30:30]	1
0xBB015054	CF_OP_DS [447].NOT_DS[31:31]	1
0xBB015058	CF_OP_DS [448].NOT_DS[0:0]	1
0xBB015058	CF_OP_DS [449].NOT_DS[1:1]	1
0xBB015058	CF_OP_DS [450].NOT_DS[2:2]	1
0xBB015058	CF_OP_DS [451].NOT_DS[3:3]	1
0xBB015058	CF_OP_DS [452].NOT_DS[4:4]	1
0xBB015058	CF_OP_DS [453].NOT_DS[5:5]	1
0xBB015058	CF_OP_DS [454].NOT_DS[6:6]	1
0xBB015058	CF_OP_DS [455].NOT_DS[7:7]	1
0xBB015058	CF_OP_DS [456].NOT_DS[8:8]	1
0xBB015058	CF_OP_DS [457].NOT_DS[9:9]	1
0xBB015058	CF_OP_DS [458].NOT_DS[10:10]	1
0xBB015058	CF_OP_DS [459].NOT_DS[11:11]	1
0xBB015058	CF_OP_DS [460].NOT_DS[12:12]	1
0xBB015058	CF_OP_DS [461].NOT_DS[13:13]	1
0xBB015058	CF_OP_DS [462].NOT_DS[14:14]	1
0xBB015058	CF_OP_DS [463].NOT_DS[15:15]	1
0xBB015058	CF_OP_DS [464].NOT_DS[16:16]	1
0xBB015058	CF_OP_DS [465].NOT_DS[17:17]	1
0xBB015058	CF_OP_DS [466].NOT_DS[18:18]	1
0xBB015058	CF_OP_DS [467].NOT_DS[19:19]	1
0xBB015058	CF_OP_DS [468].NOT_DS[20:20]	1
0xBB015058	CF_OP_DS [469].NOT_DS[21:21]	1
0xBB015058	CF_OP_DS [470].NOT_DS[22:22]	1

Address	Register	Len
0xBB015058	CF_OP_DS [471].NOT_DS[23:23]	1
0xBB015058	CF_OP_DS [472].NOT_DS[24:24]	1
0xBB015058	CF_OP_DS [473].NOT_DS[25:25]	1
0xBB015058	CF_OP_DS [474].NOT_DS[26:26]	1
0xBB015058	CF_OP_DS [475].NOT_DS[27:27]	1
0xBB015058	CF_OP_DS [476].NOT_DS[28:28]	1
0xBB015058	CF_OP_DS [477].NOT_DS[29:29]	1
0xBB015058	CF_OP_DS [478].NOT_DS[30:30]	1
0xBB015058	CF_OP_DS [479].NOT_DS[31:31]	1
0xBB01505C	CF_OP_DS [480].NOT_DS[0:0]	1
0xBB01505C	CF_OP_DS [481].NOT_DS[1:1]	1
0xBB01505C	CF_OP_DS [482].NOT_DS[2:2]	1
0xBB01505C	CF_OP_DS [483].NOT_DS[3:3]	1
0xBB01505C	CF_OP_DS [484].NOT_DS[4:4]	1
0xBB01505C	CF_OP_DS [485].NOT_DS[5:5]	1
0xBB01505C	CF_OP_DS [486].NOT_DS[6:6]	1
0xBB01505C	CF_OP_DS [487].NOT_DS[7:7]	1
0xBB01505C	CF_OP_DS [488].NOT_DS[8:8]	1
0xBB01505C	CF_OP_DS [489].NOT_DS[9:9]	1
0xBB01505C	CF_OP_DS [490].NOT_DS[10:10]	1
0xBB01505C	CF_OP_DS [491].NOT_DS[11:11]	1
0xBB01505C	CF_OP_DS [492].NOT_DS[12:12]	1
0xBB01505C	CF_OP_DS [493].NOT_DS[13:13]	1
0xBB01505C	CF_OP_DS [494].NOT_DS[14:14]	1
0xBB01505C	CF_OP_DS [495].NOT_DS[15:15]	1
0xBB01505C	CF_OP_DS [496].NOT_DS[16:16]	1
0xBB01505C	CF_OP_DS [497].NOT_DS[17:17]	1
0xBB01505C	CF_OP_DS [498].NOT_DS[18:18]	1
0xBB01505C	CF_OP_DS [499].NOT_DS[19:19]	1
0xBB01505C	CF_OP_DS [500].NOT_DS[20:20]	1
0xBB01505C	CF_OP_DS [501].NOT_DS[21:21]	1
0xBB01505C	CF_OP_DS [502].NOT_DS[22:22]	1
0xBB01505C	CF_OP_DS [503].NOT_DS[23:23]	1
0xBB01505C	CF_OP_DS [504].NOT_DS[24:24]	1
0xBB01505C	CF_OP_DS [505].NOT_DS[25:25]	1
0xBB01505C	CF_OP_DS [506].NOT_DS[26:26]	1
0xBB01505C	CF_OP_DS [507].NOT_DS[27:27]	1
0xBB01505C	CF_OP_DS [508].NOT_DS[28:28]	1
0xBB01505C	CF_OP_DS [509].NOT_DS[29:29]	1
0xBB01505C	CF_OP_DS [510].NOT_DS[30:30]	1
0xBB01505C	CF_OP_DS [511].NOT_DS[31:31]	1
0xBB015060	CF_OP_US [0].NOT_US[0:0]	1
0xBB015060	CF_OP_US [1].NOT_US[1:1]	1
0xBB015060	CF_OP_US [2].NOT_US[2:2]	1
0xBB015060	CF_OP_US [3].NOT_US[3:3]	1
0xBB015060	CF_OP_US [4].NOT_US[4:4]	1

Address	Register	Len
0xBB015060	CF_OP_US [5].NOT_US[5:5]	1
0xBB015060	CF_OP_US [6].NOT_US[6:6]	1
0xBB015060	CF_OP_US [7].NOT_US[7:7]	1
0xBB015060	CF_OP_US [8].NOT_US[8:8]	1
0xBB015060	CF_OP_US [9].NOT_US[9:9]	1
0xBB015060	CF_OP_US [10].NOT_US[10:10]	1
0xBB015060	CF_OP_US [11].NOT_US[11:11]	1
0xBB015060	CF_OP_US [12].NOT_US[12:12]	1
0xBB015060	CF_OP_US [13].NOT_US[13:13]	1
0xBB015060	CF_OP_US [14].NOT_US[14:14]	1
0xBB015060	CF_OP_US [15].NOT_US[15:15]	1
0xBB015060	CF_OP_US [16].NOT_US[16:16]	1
0xBB015060	CF_OP_US [17].NOT_US[17:17]	1
0xBB015060	CF_OP_US [18].NOT_US[18:18]	1
0xBB015060	CF_OP_US [19].NOT_US[19:19]	1
0xBB015060	CF_OP_US [20].NOT_US[20:20]	1
0xBB015060	CF_OP_US [21].NOT_US[21:21]	1
0xBB015060	CF_OP_US [22].NOT_US[22:22]	1
0xBB015060	CF_OP_US [23].NOT_US[23:23]	1
0xBB015060	CF_OP_US [24].NOT_US[24:24]	1
0xBB015060	CF_OP_US [25].NOT_US[25:25]	1
0xBB015060	CF_OP_US [26].NOT_US[26:26]	1
0xBB015060	CF_OP_US [27].NOT_US[27:27]	1
0xBB015060	CF_OP_US [28].NOT_US[28:28]	1
0xBB015060	CF_OP_US [29].NOT_US[29:29]	1
0xBB015060	CF_OP_US [30].NOT_US[30:30]	1
0xBB015060	CF_OP_US [31].NOT_US[31:31]	1
0xBB015064	CF_OP_US [32].NOT_US[0:0]	1
0xBB015064	CF_OP_US [33].NOT_US[1:1]	1
0xBB015064	CF_OP_US [34].NOT_US[2:2]	1
0xBB015064	CF_OP_US [35].NOT_US[3:3]	1
0xBB015064	CF_OP_US [36].NOT_US[4:4]	1
0xBB015064	CF_OP_US [37].NOT_US[5:5]	1
0xBB015064	CF_OP_US [38].NOT_US[6:6]	1
0xBB015064	CF_OP_US [39].NOT_US[7:7]	1
0xBB015064	CF_OP_US [40].NOT_US[8:8]	1
0xBB015064	CF_OP_US [41].NOT_US[9:9]	1
0xBB015064	CF_OP_US [42].NOT_US[10:10]	1
0xBB015064	CF_OP_US [43].NOT_US[11:11]	1
0xBB015064	CF_OP_US [44].NOT_US[12:12]	1
0xBB015064	CF_OP_US [45].NOT_US[13:13]	1
0xBB015064	CF_OP_US [46].NOT_US[14:14]	1
0xBB015064	CF_OP_US [47].NOT_US[15:15]	1
0xBB015064	CF_OP_US [48].NOT_US[16:16]	1
0xBB015064	CF_OP_US [49].NOT_US[17:17]	1
0xBB015064	CF_OP_US [50].NOT_US[18:18]	1

Address	Register	Len
0xBB015064	CF_OP_US [51].NOT_US[19:19]	1
0xBB015064	CF_OP_US [52].NOT_US[20:20]	1
0xBB015064	CF_OP_US [53].NOT_US[21:21]	1
0xBB015064	CF_OP_US [54].NOT_US[22:22]	1
0xBB015064	CF_OP_US [55].NOT_US[23:23]	1
0xBB015064	CF_OP_US [56].NOT_US[24:24]	1
0xBB015064	CF_OP_US [57].NOT_US[25:25]	1
0xBB015064	CF_OP_US [58].NOT_US[26:26]	1
0xBB015064	CF_OP_US [59].NOT_US[27:27]	1
0xBB015064	CF_OP_US [60].NOT_US[28:28]	1
0xBB015064	CF_OP_US [61].NOT_US[29:29]	1
0xBB015064	CF_OP_US [62].NOT_US[30:30]	1
0xBB015064	CF_OP_US [63].NOT_US[31:31]	1
0xBB015068	CF_OP_US [64].NOT_US[0:0]	1
0xBB015068	CF_OP_US [65].NOT_US[1:1]	1
0xBB015068	CF_OP_US [66].NOT_US[2:2]	1
0xBB015068	CF_OP_US [67].NOT_US[3:3]	1
0xBB015068	CF_OP_US [68].NOT_US[4:4]	1
0xBB015068	CF_OP_US [69].NOT_US[5:5]	1
0xBB015068	CF_OP_US [70].NOT_US[6:6]	1
0xBB015068	CF_OP_US [71].NOT_US[7:7]	1
0xBB015068	CF_OP_US [72].NOT_US[8:8]	1
0xBB015068	CF_OP_US [73].NOT_US[9:9]	1
0xBB015068	CF_OP_US [74].NOT_US[10:10]	1
0xBB015068	CF_OP_US [75].NOT_US[11:11]	1
0xBB015068	CF_OP_US [76].NOT_US[12:12]	1
0xBB015068	CF_OP_US [77].NOT_US[13:13]	1
0xBB015068	CF_OP_US [78].NOT_US[14:14]	1
0xBB015068	CF_OP_US [79].NOT_US[15:15]	1
0xBB015068	CF_OP_US [80].NOT_US[16:16]	1
0xBB015068	CF_OP_US [81].NOT_US[17:17]	1
0xBB015068	CF_OP_US [82].NOT_US[18:18]	1
0xBB015068	CF_OP_US [83].NOT_US[19:19]	1
0xBB015068	CF_OP_US [84].NOT_US[20:20]	1
0xBB015068	CF_OP_US [85].NOT_US[21:21]	1
0xBB015068	CF_OP_US [86].NOT_US[22:22]	1
0xBB015068	CF_OP_US [87].NOT_US[23:23]	1
0xBB015068	CF_OP_US [88].NOT_US[24:24]	1
0xBB015068	CF_OP_US [89].NOT_US[25:25]	1
0xBB015068	CF_OP_US [90].NOT_US[26:26]	1
0xBB015068	CF_OP_US [91].NOT_US[27:27]	1
0xBB015068	CF_OP_US [92].NOT_US[28:28]	1
0xBB015068	CF_OP_US [93].NOT_US[29:29]	1
0xBB015068	CF_OP_US [94].NOT_US[30:30]	1
0xBB015068	CF_OP_US [95].NOT_US[31:31]	1
0xBB01506C	CF_OP_US [96].NOT_US[0:0]	1

Address	Register	Len
0xBB01506C	CF_OP_US [97].NOT_US[1:1]	1
0xBB01506C	CF_OP_US [98].NOT_US[2:2]	1
0xBB01506C	CF_OP_US [99].NOT_US[3:3]	1
0xBB01506C	CF_OP_US [100].NOT_US[4:4]	1
0xBB01506C	CF_OP_US [101].NOT_US[5:5]	1
0xBB01506C	CF_OP_US [102].NOT_US[6:6]	1
0xBB01506C	CF_OP_US [103].NOT_US[7:7]	1
0xBB01506C	CF_OP_US [104].NOT_US[8:8]	1
0xBB01506C	CF_OP_US [105].NOT_US[9:9]	1
0xBB01506C	CF_OP_US [106].NOT_US[10:10]	1
0xBB01506C	CF_OP_US [107].NOT_US[11:11]	1
0xBB01506C	CF_OP_US [108].NOT_US[12:12]	1
0xBB01506C	CF_OP_US [109].NOT_US[13:13]	1
0xBB01506C	CF_OP_US [110].NOT_US[14:14]	1
0xBB01506C	CF_OP_US [111].NOT_US[15:15]	1
0xBB01506C	CF_OP_US [112].NOT_US[16:16]	1
0xBB01506C	CF_OP_US [113].NOT_US[17:17]	1
0xBB01506C	CF_OP_US [114].NOT_US[18:18]	1
0xBB01506C	CF_OP_US [115].NOT_US[19:19]	1
0xBB01506C	CF_OP_US [116].NOT_US[20:20]	1
0xBB01506C	CF_OP_US [117].NOT_US[21:21]	1
0xBB01506C	CF_OP_US [118].NOT_US[22:22]	1
0xBB01506C	CF_OP_US [119].NOT_US[23:23]	1
0xBB01506C	CF_OP_US [120].NOT_US[24:24]	1
0xBB01506C	CF_OP_US [121].NOT_US[25:25]	1
0xBB01506C	CF_OP_US [122].NOT_US[26:26]	1
0xBB01506C	CF_OP_US [123].NOT_US[27:27]	1
0xBB01506C	CF_OP_US [124].NOT_US[28:28]	1
0xBB01506C	CF_OP_US [125].NOT_US[29:29]	1
0xBB01506C	CF_OP_US [126].NOT_US[30:30]	1
0xBB01506C	CF_OP_US [127].NOT_US[31:31]	1
0xBB015070	CF_OP_US [128].NOT_US[0:0]	1
0xBB015070	CF_OP_US [129].NOT_US[1:1]	1
0xBB015070	CF_OP_US [130].NOT_US[2:2]	1
0xBB015070	CF_OP_US [131].NOT_US[3:3]	1
0xBB015070	CF_OP_US [132].NOT_US[4:4]	1
0xBB015070	CF_OP_US [133].NOT_US[5:5]	1
0xBB015070	CF_OP_US [134].NOT_US[6:6]	1
0xBB015070	CF_OP_US [135].NOT_US[7:7]	1
0xBB015070	CF_OP_US [136].NOT_US[8:8]	1
0xBB015070	CF_OP_US [137].NOT_US[9:9]	1
0xBB015070	CF_OP_US [138].NOT_US[10:10]	1
0xBB015070	CF_OP_US [139].NOT_US[11:11]	1
0xBB015070	CF_OP_US [140].NOT_US[12:12]	1
0xBB015070	CF_OP_US [141].NOT_US[13:13]	1
0xBB015070	CF_OP_US [142].NOT_US[14:14]	1



Address	Register	Len
0xBB015070	CF_OP_US [143].NOT_US[15:15]	1
0xBB015070	CF_OP_US [144].NOT_US[16:16]	1
0xBB015070	CF_OP_US [145].NOT_US[17:17]	1
0xBB015070	CF_OP_US [146].NOT_US[18:18]	1
0xBB015070	CF_OP_US [147].NOT_US[19:19]	1
0xBB015070	CF_OP_US [148].NOT_US[20:20]	1
0xBB015070	CF_OP_US [149].NOT_US[21:21]	1
0xBB015070	CF_OP_US [150].NOT_US[22:22]	1
0xBB015070	CF_OP_US [151].NOT_US[23:23]	1
0xBB015070	CF_OP_US [152].NOT_US[24:24]	1
0xBB015070	CF_OP_US [153].NOT_US[25:25]	1
0xBB015070	CF_OP_US [154].NOT_US[26:26]	1
0xBB015070	CF_OP_US [155].NOT_US[27:27]	1
0xBB015070	CF_OP_US [156].NOT_US[28:28]	1
0xBB015070	CF_OP_US [157].NOT_US[29:29]	1
0xBB015070	CF_OP_US [158].NOT_US[30:30]	1
0xBB015070	CF_OP_US [159].NOT_US[31:31]	1
0xBB015074	CF_OP_US [160].NOT_US[0:0]	1
0xBB015074	CF_OP_US [161].NOT_US[1:1]	1
0xBB015074	CF_OP_US [162].NOT_US[2:2]	1
0xBB015074	CF_OP_US [163].NOT_US[3:3]	1
0xBB015074	CF_OP_US [164].NOT_US[4:4]	1
0xBB015074	CF_OP_US [165].NOT_US[5:5]	1
0xBB015074	CF_OP_US [166].NOT_US[6:6]	1
0xBB015074	CF_OP_US [167].NOT_US[7:7]	1
0xBB015074	CF_OP_US [168].NOT_US[8:8]	1
0xBB015074	CF_OP_US [169].NOT_US[9:9]	1
0xBB015074	CF_OP_US [170].NOT_US[10:10]	1
0xBB015074	CF_OP_US [171].NOT_US[11:11]	1
0xBB015074	CF_OP_US [172].NOT_US[12:12]	1
0xBB015074	CF_OP_US [173].NOT_US[13:13]	1
0xBB015074	CF_OP_US [174].NOT_US[14:14]	1
0xBB015074	CF_OP_US [175].NOT_US[15:15]	1
0xBB015074	CF_OP_US [176].NOT_US[16:16]	1
0xBB015074	CF_OP_US [177].NOT_US[17:17]	1
0xBB015074	CF_OP_US [178].NOT_US[18:18]	1
0xBB015074	CF_OP_US [179].NOT_US[19:19]	1
0xBB015074	CF_OP_US [180].NOT_US[20:20]	1
0xBB015074	CF_OP_US [181].NOT_US[21:21]	1
0xBB015074	CF_OP_US [182].NOT_US[22:22]	1
0xBB015074	CF_OP_US [183].NOT_US[23:23]	1
0xBB015074	CF_OP_US [184].NOT_US[24:24]	1
0xBB015074	CF_OP_US [185].NOT_US[25:25]	1
0xBB015074	CF_OP_US [186].NOT_US[26:26]	1
0xBB015074	CF_OP_US [187].NOT_US[27:27]	1
0xBB015074	CF_OP_US [188].NOT_US[28:28]	1

Address	Register	Len
0xBB015074	CF_OP_US [189].NOT_US[29:29]	1
0xBB015074	CF_OP_US [190].NOT_US[30:30]	1
0xBB015074	CF_OP_US [191].NOT_US[31:31]	1
0xBB015078	CF_OP_US [192].NOT_US[0:0]	1
0xBB015078	CF_OP_US [193].NOT_US[1:1]	1
0xBB015078	CF_OP_US [194].NOT_US[2:2]	1
0xBB015078	CF_OP_US [195].NOT_US[3:3]	1
0xBB015078	CF_OP_US [196].NOT_US[4:4]	1
0xBB015078	CF_OP_US [197].NOT_US[5:5]	1
0xBB015078	CF_OP_US [198].NOT_US[6:6]	1
0xBB015078	CF_OP_US [199].NOT_US[7:7]	1
0xBB015078	CF_OP_US [200].NOT_US[8:8]	1
0xBB015078	CF_OP_US [201].NOT_US[9:9]	1
0xBB015078	CF_OP_US [202].NOT_US[10:10]	1
0xBB015078	CF_OP_US [203].NOT_US[11:11]	1
0xBB015078	CF_OP_US [204].NOT_US[12:12]	1
0xBB015078	CF_OP_US [205].NOT_US[13:13]	1
0xBB015078	CF_OP_US [206].NOT_US[14:14]	1
0xBB015078	CF_OP_US [207].NOT_US[15:15]	1
0xBB015078	CF_OP_US [208].NOT_US[16:16]	1
0xBB015078	CF_OP_US [209].NOT_US[17:17]	1
0xBB015078	CF_OP_US [210].NOT_US[18:18]	1
0xBB015078	CF_OP_US [211].NOT_US[19:19]	1
0xBB015078	CF_OP_US [212].NOT_US[20:20]	1
0xBB015078	CF_OP_US [213].NOT_US[21:21]	1
0xBB015078	CF_OP_US [214].NOT_US[22:22]	1
0xBB015078	CF_OP_US [215].NOT_US[23:23]	1
0xBB015078	CF_OP_US [216].NOT_US[24:24]	1
0xBB015078	CF_OP_US [217].NOT_US[25:25]	1
0xBB015078	CF_OP_US [218].NOT_US[26:26]	1
0xBB015078	CF_OP_US [219].NOT_US[27:27]	1
0xBB015078	CF_OP_US [220].NOT_US[28:28]	1
0xBB015078	CF_OP_US [221].NOT_US[29:29]	1
0xBB015078	CF_OP_US [222].NOT_US[30:30]	1
0xBB015078	CF_OP_US [223].NOT_US[31:31]	1
0xBB01507C	CF_OP_US [224].NOT_US[0:0]	1
0xBB01507C	CF_OP_US [225].NOT_US[1:1]	1
0xBB01507C	CF_OP_US [226].NOT_US[2:2]	1
0xBB01507C	CF_OP_US [227].NOT_US[3:3]	1
0xBB01507C	CF_OP_US [228].NOT_US[4:4]	1
0xBB01507C	CF_OP_US [229].NOT_US[5:5]	1
0xBB01507C	CF_OP_US [230].NOT_US[6:6]	1
0xBB01507C	CF_OP_US [231].NOT_US[7:7]	1
0xBB01507C	CF_OP_US [232].NOT_US[8:8]	1
0xBB01507C	CF_OP_US [233].NOT_US[9:9]	1
0xBB01507C	CF_OP_US [234].NOT_US[10:10]	1

Address	Register	Len
0xBB01507C	CF_OP_US [235].NOT_US[11:11]	1
0xBB01507C	CF_OP_US [236].NOT_US[12:12]	1
0xBB01507C	CF_OP_US [237].NOT_US[13:13]	1
0xBB01507C	CF_OP_US [238].NOT_US[14:14]	1
0xBB01507C	CF_OP_US [239].NOT_US[15:15]	1
0xBB01507C	CF_OP_US [240].NOT_US[16:16]	1
0xBB01507C	CF_OP_US [241].NOT_US[17:17]	1
0xBB01507C	CF_OP_US [242].NOT_US[18:18]	1
0xBB01507C	CF_OP_US [243].NOT_US[19:19]	1
0xBB01507C	CF_OP_US [244].NOT_US[20:20]	1
0xBB01507C	CF_OP_US [245].NOT_US[21:21]	1
0xBB01507C	CF_OP_US [246].NOT_US[22:22]	1
0xBB01507C	CF_OP_US [247].NOT_US[23:23]	1
0xBB01507C	CF_OP_US [248].NOT_US[24:24]	1
0xBB01507C	CF_OP_US [249].NOT_US[25:25]	1
0xBB01507C	CF_OP_US [250].NOT_US[26:26]	1
0xBB01507C	CF_OP_US [251].NOT_US[27:27]	1
0xBB01507C	CF_OP_US [252].NOT_US[28:28]	1
0xBB01507C	CF_OP_US [253].NOT_US[29:29]	1
0xBB01507C	CF_OP_US [254].NOT_US[30:30]	1
0xBB01507C	CF_OP_US [255].NOT_US[31:31]	1
0xBB015080	CF_OP_US [256].NOT_US[0:0]	1
0xBB015080	CF_OP_US [257].NOT_US[1:1]	1
0xBB015080	CF_OP_US [258].NOT_US[2:2]	1
0xBB015080	CF_OP_US [259].NOT_US[3:3]	1
0xBB015080	CF_OP_US [260].NOT_US[4:4]	1
0xBB015080	CF_OP_US [261].NOT_US[5:5]	1
0xBB015080	CF_OP_US [262].NOT_US[6:6]	1
0xBB015080	CF_OP_US [263].NOT_US[7:7]	1
0xBB015080	CF_OP_US [264].NOT_US[8:8]	1
0xBB015080	CF_OP_US [265].NOT_US[9:9]	1
0xBB015080	CF_OP_US [266].NOT_US[10:10]	1
0xBB015080	CF_OP_US [267].NOT_US[11:11]	1
0xBB015080	CF_OP_US [268].NOT_US[12:12]	1
0xBB015080	CF_OP_US [269].NOT_US[13:13]	1
0xBB015080	CF_OP_US [270].NOT_US[14:14]	1
0xBB015080	CF_OP_US [271].NOT_US[15:15]	1
0xBB015080	CF_OP_US [272].NOT_US[16:16]	1
0xBB015080	CF_OP_US [273].NOT_US[17:17]	1
0xBB015080	CF_OP_US [274].NOT_US[18:18]	1
0xBB015080	CF_OP_US [275].NOT_US[19:19]	1
0xBB015080	CF_OP_US [276].NOT_US[20:20]	1
0xBB015080	CF_OP_US [277].NOT_US[21:21]	1
0xBB015080	CF_OP_US [278].NOT_US[22:22]	1
0xBB015080	CF_OP_US [279].NOT_US[23:23]	1
0xBB015080	CF_OP_US [280].NOT_US[24:24]	1

Address	Register	Len
0xBB015080	CF_OP_US [281].NOT_US[25:25]	1
0xBB015080	CF_OP_US [282].NOT_US[26:26]	1
0xBB015080	CF_OP_US [283].NOT_US[27:27]	1
0xBB015080	CF_OP_US [284].NOT_US[28:28]	1
0xBB015080	CF_OP_US [285].NOT_US[29:29]	1
0xBB015080	CF_OP_US [286].NOT_US[30:30]	1
0xBB015080	CF_OP_US [287].NOT_US[31:31]	1
0xBB015084	CF_OP_US [288].NOT_US[0:0]	1
0xBB015084	CF_OP_US [289].NOT_US[1:1]	1
0xBB015084	CF_OP_US [290].NOT_US[2:2]	1
0xBB015084	CF_OP_US [291].NOT_US[3:3]	1
0xBB015084	CF_OP_US [292].NOT_US[4:4]	1
0xBB015084	CF_OP_US [293].NOT_US[5:5]	1
0xBB015084	CF_OP_US [294].NOT_US[6:6]	1
0xBB015084	CF_OP_US [295].NOT_US[7:7]	1
0xBB015084	CF_OP_US [296].NOT_US[8:8]	1
0xBB015084	CF_OP_US [297].NOT_US[9:9]	1
0xBB015084	CF_OP_US [298].NOT_US[10:10]	1
0xBB015084	CF_OP_US [299].NOT_US[11:11]	1
0xBB015084	CF_OP_US [300].NOT_US[12:12]	1
0xBB015084	CF_OP_US [301].NOT_US[13:13]	1
0xBB015084	CF_OP_US [302].NOT_US[14:14]	1
0xBB015084	CF_OP_US [303].NOT_US[15:15]	1
0xBB015084	CF_OP_US [304].NOT_US[16:16]	1
0xBB015084	CF_OP_US [305].NOT_US[17:17]	1
0xBB015084	CF_OP_US [306].NOT_US[18:18]	1
0xBB015084	CF_OP_US [307].NOT_US[19:19]	1
0xBB015084	CF_OP_US [308].NOT_US[20:20]	1
0xBB015084	CF_OP_US [309].NOT_US[21:21]	1
0xBB015084	CF_OP_US [310].NOT_US[22:22]	1
0xBB015084	CF_OP_US [311].NOT_US[23:23]	1
0xBB015084	CF_OP_US [312].NOT_US[24:24]	1
0xBB015084	CF_OP_US [313].NOT_US[25:25]	1
0xBB015084	CF_OP_US [314].NOT_US[26:26]	1
0xBB015084	CF_OP_US [315].NOT_US[27:27]	1
0xBB015084	CF_OP_US [316].NOT_US[28:28]	1
0xBB015084	CF_OP_US [317].NOT_US[29:29]	1
0xBB015084	CF_OP_US [318].NOT_US[30:30]	1
0xBB015084	CF_OP_US [319].NOT_US[31:31]	1
0xBB015088	CF_OP_US [320].NOT_US[0:0]	1
0xBB015088	CF_OP_US [321].NOT_US[1:1]	1
0xBB015088	CF_OP_US [322].NOT_US[2:2]	1
0xBB015088	CF_OP_US [323].NOT_US[3:3]	1
0xBB015088	CF_OP_US [324].NOT_US[4:4]	1
0xBB015088	CF_OP_US [325].NOT_US[5:5]	1
0xBB015088	CF_OP_US [326].NOT_US[6:6]	1

Address	Register	Len
0xBB015088	CF_OP_US [327].NOT_US[7:7]	1
0xBB015088	CF_OP_US [328].NOT_US[8:8]	1
0xBB015088	CF_OP_US [329].NOT_US[9:9]	1
0xBB015088	CF_OP_US [330].NOT_US[10:10]	1
0xBB015088	CF_OP_US [331].NOT_US[11:11]	1
0xBB015088	CF_OP_US [332].NOT_US[12:12]	1
0xBB015088	CF_OP_US [333].NOT_US[13:13]	1
0xBB015088	CF_OP_US [334].NOT_US[14:14]	1
0xBB015088	CF_OP_US [335].NOT_US[15:15]	1
0xBB015088	CF_OP_US [336].NOT_US[16:16]	1
0xBB015088	CF_OP_US [337].NOT_US[17:17]	1
0xBB015088	CF_OP_US [338].NOT_US[18:18]	1
0xBB015088	CF_OP_US [339].NOT_US[19:19]	1
0xBB015088	CF_OP_US [340].NOT_US[20:20]	1
0xBB015088	CF_OP_US [341].NOT_US[21:21]	1
0xBB015088	CF_OP_US [342].NOT_US[22:22]	1
0xBB015088	CF_OP_US [343].NOT_US[23:23]	1
0xBB015088	CF_OP_US [344].NOT_US[24:24]	1
0xBB015088	CF_OP_US [345].NOT_US[25:25]	1
0xBB015088	CF_OP_US [346].NOT_US[26:26]	1
0xBB015088	CF_OP_US [347].NOT_US[27:27]	1
0xBB015088	CF_OP_US [348].NOT_US[28:28]	1
0xBB015088	CF_OP_US [349].NOT_US[29:29]	1
0xBB015088	CF_OP_US [350].NOT_US[30:30]	1
0xBB015088	CF_OP_US [351].NOT_US[31:31]	1
0xBB01508C	CF_OP_US [352].NOT_US[0:0]	1
0xBB01508C	CF_OP_US [353].NOT_US[1:1]	1
0xBB01508C	CF_OP_US [354].NOT_US[2:2]	1
0xBB01508C	CF_OP_US [355].NOT_US[3:3]	1
0xBB01508C	CF_OP_US [356].NOT_US[4:4]	1
0xBB01508C	CF_OP_US [357].NOT_US[5:5]	1
0xBB01508C	CF_OP_US [358].NOT_US[6:6]	1
0xBB01508C	CF_OP_US [359].NOT_US[7:7]	1
0xBB01508C	CF_OP_US [360].NOT_US[8:8]	1
0xBB01508C	CF_OP_US [361].NOT_US[9:9]	1
0xBB01508C	CF_OP_US [362].NOT_US[10:10]	1
0xBB01508C	CF_OP_US [363].NOT_US[11:11]	1
0xBB01508C	CF_OP_US [364].NOT_US[12:12]	1
0xBB01508C	CF_OP_US [365].NOT_US[13:13]	1
0xBB01508C	CF_OP_US [366].NOT_US[14:14]	1
0xBB01508C	CF_OP_US [367].NOT_US[15:15]	1
0xBB01508C	CF_OP_US [368].NOT_US[16:16]	1
0xBB01508C	CF_OP_US [369].NOT_US[17:17]	1
0xBB01508C	CF_OP_US [370].NOT_US[18:18]	1
0xBB01508C	CF_OP_US [371].NOT_US[19:19]	1
0xBB01508C	CF_OP_US [372].NOT_US[20:20]	1

Address	Register	Len
0xBB01508C	CF_OP_US [373].NOT_US[21:21]	1
0xBB01508C	CF_OP_US [374].NOT_US[22:22]	1
0xBB01508C	CF_OP_US [375].NOT_US[23:23]	1
0xBB01508C	CF_OP_US [376].NOT_US[24:24]	1
0xBB01508C	CF_OP_US [377].NOT_US[25:25]	1
0xBB01508C	CF_OP_US [378].NOT_US[26:26]	1
0xBB01508C	CF_OP_US [379].NOT_US[27:27]	1
0xBB01508C	CF_OP_US [380].NOT_US[28:28]	1
0xBB01508C	CF_OP_US [381].NOT_US[29:29]	1
0xBB01508C	CF_OP_US [382].NOT_US[30:30]	1
0xBB01508C	CF_OP_US [383].NOT_US[31:31]	1
0xBB015090	CF_OP_US [384].NOT_US[0:0]	1
0xBB015090	CF_OP_US [385].NOT_US[1:1]	1
0xBB015090	CF_OP_US [386].NOT_US[2:2]	1
0xBB015090	CF_OP_US [387].NOT_US[3:3]	1
0xBB015090	CF_OP_US [388].NOT_US[4:4]	1
0xBB015090	CF_OP_US [389].NOT_US[5:5]	1
0xBB015090	CF_OP_US [390].NOT_US[6:6]	1
0xBB015090	CF_OP_US [391].NOT_US[7:7]	1
0xBB015090	CF_OP_US [392].NOT_US[8:8]	1
0xBB015090	CF_OP_US [393].NOT_US[9:9]	1
0xBB015090	CF_OP_US [394].NOT_US[10:10]	1
0xBB015090	CF_OP_US [395].NOT_US[11:11]	1
0xBB015090	CF_OP_US [396].NOT_US[12:12]	1
0xBB015090	CF_OP_US [397].NOT_US[13:13]	1
0xBB015090	CF_OP_US [398].NOT_US[14:14]	1
0xBB015090	CF_OP_US [399].NOT_US[15:15]	1
0xBB015090	CF_OP_US [400].NOT_US[16:16]	1
0xBB015090	CF_OP_US [401].NOT_US[17:17]	1
0xBB015090	CF_OP_US [402].NOT_US[18:18]	1
0xBB015090	CF_OP_US [403].NOT_US[19:19]	1
0xBB015090	CF_OP_US [404].NOT_US[20:20]	1
0xBB015090	CF_OP_US [405].NOT_US[21:21]	1
0xBB015090	CF_OP_US [406].NOT_US[22:22]	1
0xBB015090	CF_OP_US [407].NOT_US[23:23]	1
0xBB015090	CF_OP_US [408].NOT_US[24:24]	1
0xBB015090	CF_OP_US [409].NOT_US[25:25]	1
0xBB015090	CF_OP_US [410].NOT_US[26:26]	1
0xBB015090	CF_OP_US [411].NOT_US[27:27]	1
0xBB015090	CF_OP_US [412].NOT_US[28:28]	1
0xBB015090	CF_OP_US [413].NOT_US[29:29]	1
0xBB015090	CF_OP_US [414].NOT_US[30:30]	1
0xBB015090	CF_OP_US [415].NOT_US[31:31]	1
0xBB015094	CF_OP_US [416].NOT_US[0:0]	1
0xBB015094	CF_OP_US [417].NOT_US[1:1]	1
0xBB015094	CF_OP_US [418].NOT_US[2:2]	1

Address	Register	Len
0xBB015094	CF_OP_US [419].NOT_US[3:3]	1
0xBB015094	CF_OP_US [420].NOT_US[4:4]	1
0xBB015094	CF_OP_US [421].NOT_US[5:5]	1
0xBB015094	CF_OP_US [422].NOT_US[6:6]	1
0xBB015094	CF_OP_US [423].NOT_US[7:7]	1
0xBB015094	CF_OP_US [424].NOT_US[8:8]	1
0xBB015094	CF_OP_US [425].NOT_US[9:9]	1
0xBB015094	CF_OP_US [426].NOT_US[10:10]	1
0xBB015094	CF_OP_US [427].NOT_US[11:11]	1
0xBB015094	CF_OP_US [428].NOT_US[12:12]	1
0xBB015094	CF_OP_US [429].NOT_US[13:13]	1
0xBB015094	CF_OP_US [430].NOT_US[14:14]	1
0xBB015094	CF_OP_US [431].NOT_US[15:15]	1
0xBB015094	CF_OP_US [432].NOT_US[16:16]	1
0xBB015094	CF_OP_US [433].NOT_US[17:17]	1
0xBB015094	CF_OP_US [434].NOT_US[18:18]	1
0xBB015094	CF_OP_US [435].NOT_US[19:19]	1
0xBB015094	CF_OP_US [436].NOT_US[20:20]	1
0xBB015094	CF_OP_US [437].NOT_US[21:21]	1
0xBB015094	CF_OP_US [438].NOT_US[22:22]	1
0xBB015094	CF_OP_US [439].NOT_US[23:23]	1
0xBB015094	CF_OP_US [440].NOT_US[24:24]	1
0xBB015094	CF_OP_US [441].NOT_US[25:25]	1
0xBB015094	CF_OP_US [442].NOT_US[26:26]	1
0xBB015094	CF_OP_US [443].NOT_US[27:27]	1
0xBB015094	CF_OP_US [444].NOT_US[28:28]	1
0xBB015094	CF_OP_US [445].NOT_US[29:29]	1
0xBB015094	CF_OP_US [446].NOT_US[30:30]	1
0xBB015094	CF_OP_US [447].NOT_US[31:31]	1
0xBB015098	CF_OP_US [448].NOT_US[0:0]	1
0xBB015098	CF_OP_US [449].NOT_US[1:1]	1
0xBB015098	CF_OP_US [450].NOT_US[2:2]	1
0xBB015098	CF_OP_US [451].NOT_US[3:3]	1
0xBB015098	CF_OP_US [452].NOT_US[4:4]	1
0xBB015098	CF_OP_US [453].NOT_US[5:5]	1
0xBB015098	CF_OP_US [454].NOT_US[6:6]	1
0xBB015098	CF_OP_US [455].NOT_US[7:7]	1
0xBB015098	CF_OP_US [456].NOT_US[8:8]	1
0xBB015098	CF_OP_US [457].NOT_US[9:9]	1
0xBB015098	CF_OP_US [458].NOT_US[10:10]	1
0xBB015098	CF_OP_US [459].NOT_US[11:11]	1
0xBB015098	CF_OP_US [460].NOT_US[12:12]	1
0xBB015098	CF_OP_US [461].NOT_US[13:13]	1
0xBB015098	CF_OP_US [462].NOT_US[14:14]	1
0xBB015098	CF_OP_US [463].NOT_US[15:15]	1
0xBB015098	CF_OP_US [464].NOT_US[16:16]	1

Address	Register	Len
0xBB015098	CF_OP_US [465].NOT_US[17:17]	1
0xBB015098	CF_OP_US [466].NOT_US[18:18]	1
0xBB015098	CF_OP_US [467].NOT_US[19:19]	1
0xBB015098	CF_OP_US [468].NOT_US[20:20]	1
0xBB015098	CF_OP_US [469].NOT_US[21:21]	1
0xBB015098	CF_OP_US [470].NOT_US[22:22]	1
0xBB015098	CF_OP_US [471].NOT_US[23:23]	1
0xBB015098	CF_OP_US [472].NOT_US[24:24]	1
0xBB015098	CF_OP_US [473].NOT_US[25:25]	1
0xBB015098	CF_OP_US [474].NOT_US[26:26]	1
0xBB015098	CF_OP_US [475].NOT_US[27:27]	1
0xBB015098	CF_OP_US [476].NOT_US[28:28]	1
0xBB015098	CF_OP_US [477].NOT_US[29:29]	1
0xBB015098	CF_OP_US [478].NOT_US[30:30]	1
0xBB015098	CF_OP_US [479].NOT_US[31:31]	1
0xBB01509C	CF_OP_US [480].NOT_US[0:0]	1
0xBB01509C	CF_OP_US [481].NOT_US[1:1]	1
0xBB01509C	CF_OP_US [482].NOT_US[2:2]	1
0xBB01509C	CF_OP_US [483].NOT_US[3:3]	1
0xBB01509C	CF_OP_US [484].NOT_US[4:4]	1
0xBB01509C	CF_OP_US [485].NOT_US[5:5]	1
0xBB01509C	CF_OP_US [486].NOT_US[6:6]	1
0xBB01509C	CF_OP_US [487].NOT_US[7:7]	1
0xBB01509C	CF_OP_US [488].NOT_US[8:8]	1
0xBB01509C	CF_OP_US [489].NOT_US[9:9]	1
0xBB01509C	CF_OP_US [490].NOT_US[10:10]	1
0xBB01509C	CF_OP_US [491].NOT_US[11:11]	1
0xBB01509C	CF_OP_US [492].NOT_US[12:12]	1
0xBB01509C	CF_OP_US [493].NOT_US[13:13]	1
0xBB01509C	CF_OP_US [494].NOT_US[14:14]	1
0xBB01509C	CF_OP_US [495].NOT_US[15:15]	1
0xBB01509C	CF_OP_US [496].NOT_US[16:16]	1
0xBB01509C	CF_OP_US [497].NOT_US[17:17]	1
0xBB01509C	CF_OP_US [498].NOT_US[18:18]	1
0xBB01509C	CF_OP_US [499].NOT_US[19:19]	1
0xBB01509C	CF_OP_US [500].NOT_US[20:20]	1
0xBB01509C	CF_OP_US [501].NOT_US[21:21]	1
0xBB01509C	CF_OP_US [502].NOT_US[22:22]	1
0xBB01509C	CF_OP_US [503].NOT_US[23:23]	1
0xBB01509C	CF_OP_US [504].NOT_US[24:24]	1
0xBB01509C	CF_OP_US [505].NOT_US[25:25]	1
0xBB01509C	CF_OP_US [506].NOT_US[26:26]	1
0xBB01509C	CF_OP_US [507].NOT_US[27:27]	1
0xBB01509C	CF_OP_US [508].NOT_US[28:28]	1
0xBB01509C	CF_OP_US [509].NOT_US[29:29]	1
0xBB01509C	CF_OP_US [510].NOT_US[30:30]	1



Address	Register	Len
0xBB01509C	CF_OP_US [511].NOT_US[31:31]	1
0xBB0150A0	CF_VALID [0].VALID[0:0]	1
0xBB0150A0	CF_VALID [1].VALID[1:1]	1
0xBB0150A0	CF_VALID [2].VALID[2:2]	1
0xBB0150A0	CF_VALID [3].VALID[3:3]	1
0xBB0150A0	CF_VALID [4].VALID[4:4]	1
0xBB0150A0	CF_VALID [5].VALID[5:5]	1
0xBB0150A0	CF_VALID [6].VALID[6:6]	1
0xBB0150A0	CF_VALID [7].VALID[7:7]	1
0xBB0150A0	CF_VALID [8].VALID[8:8]	1
0xBB0150A0	CF_VALID [9].VALID[9:9]	1
0xBB0150A0	CF_VALID [10].VALID[10:10]	1
0xBB0150A0	CF_VALID [11].VALID[11:11]	1
0xBB0150A0	CF_VALID [12].VALID[12:12]	1
0xBB0150A0	CF_VALID [13].VALID[13:13]	1
0xBB0150A0	CF_VALID [14].VALID[14:14]	1
0xBB0150A0	CF_VALID [15].VALID[15:15]	1
0xBB0150A0	CF_VALID [16].VALID[16:16]	1
0xBB0150A0	CF_VALID [17].VALID[17:17]	1
0xBB0150A0	CF_VALID [18].VALID[18:18]	1
0xBB0150A0	CF_VALID [19].VALID[19:19]	1
0xBB0150A0	CF_VALID [20].VALID[20:20]	1
0xBB0150A0	CF_VALID [21].VALID[21:21]	1
0xBB0150A0	CF_VALID [22].VALID[22:22]	1
0xBB0150A0	CF_VALID [23].VALID[23:23]	1
0xBB0150A0	CF_VALID [24].VALID[24:24]	1
0xBB0150A0	CF_VALID [25].VALID[25:25]	1
0xBB0150A0	CF_VALID [26].VALID[26:26]	1
0xBB0150A0	CF_VALID [27].VALID[27:27]	1
0xBB0150A0	CF_VALID [28].VALID[28:28]	1
0xBB0150A0	CF_VALID [29].VALID[29:29]	1
0xBB0150A0	CF_VALID [30].VALID[30:30]	1
0xBB0150A0	CF_VALID [31].VALID[31:31]	1
0xBB0150A4	CF_VALID [32].VALID[0:0]	1
0xBB0150A4	CF_VALID [33].VALID[1:1]	1
0xBB0150A4	CF_VALID [34].VALID[2:2]	1
0xBB0150A4	CF_VALID [35].VALID[3:3]	1
0xBB0150A4	CF_VALID [36].VALID[4:4]	1
0xBB0150A4	CF_VALID [37].VALID[5:5]	1
0xBB0150A4	CF_VALID [38].VALID[6:6]	1
0xBB0150A4	CF_VALID [39].VALID[7:7]	1
0xBB0150A4	CF_VALID [40].VALID[8:8]	1
0xBB0150A4	CF_VALID [41].VALID[9:9]	1
0xBB0150A4	CF_VALID [42].VALID[10:10]	1
0xBB0150A4	CF_VALID [43].VALID[11:11]	1
0xBB0150A4	CF_VALID [44].VALID[12:12]	1

Address	Register	Len
0xBB0150A4	CF_VALID [45].VALID[13:13]	1
0xBB0150A4	CF_VALID [46].VALID[14:14]	1
0xBB0150A4	CF_VALID [47].VALID[15:15]	1
0xBB0150A4	CF_VALID [48].VALID[16:16]	1
0xBB0150A4	CF_VALID [49].VALID[17:17]	1
0xBB0150A4	CF_VALID [50].VALID[18:18]	1
0xBB0150A4	CF_VALID [51].VALID[19:19]	1
0xBB0150A4	CF_VALID [52].VALID[20:20]	1
0xBB0150A4	CF_VALID [53].VALID[21:21]	1
0xBB0150A4	CF_VALID [54].VALID[22:22]	1
0xBB0150A4	CF_VALID [55].VALID[23:23]	1
0xBB0150A4	CF_VALID [56].VALID[24:24]	1
0xBB0150A4	CF_VALID [57].VALID[25:25]	1
0xBB0150A4	CF_VALID [58].VALID[26:26]	1
0xBB0150A4	CF_VALID [59].VALID[27:27]	1
0xBB0150A4	CF_VALID [60].VALID[28:28]	1
0xBB0150A4	CF_VALID [61].VALID[29:29]	1
0xBB0150A4	CF_VALID [62].VALID[30:30]	1
0xBB0150A4	CF_VALID [63].VALID[31:31]	1
0xBB0150A8	CF_VALID [64].VALID[0:0]	1
0xBB0150A8	CF_VALID [65].VALID[1:1]	1
0xBB0150A8	CF_VALID [66].VALID[2:2]	1
0xBB0150A8	CF_VALID [67].VALID[3:3]	1
0xBB0150A8	CF_VALID [68].VALID[4:4]	1
0xBB0150A8	CF_VALID [69].VALID[5:5]	1
0xBB0150A8	CF_VALID [70].VALID[6:6]	1
0xBB0150A8	CF_VALID [71].VALID[7:7]	1
0xBB0150A8	CF_VALID [72].VALID[8:8]	1
0xBB0150A8	CF_VALID [73].VALID[9:9]	1
0xBB0150A8	CF_VALID [74].VALID[10:10]	1
0xBB0150A8	CF_VALID [75].VALID[11:11]	1
0xBB0150A8	CF_VALID [76].VALID[12:12]	1
0xBB0150A8	CF_VALID [77].VALID[13:13]	1
0xBB0150A8	CF_VALID [78].VALID[14:14]	1
0xBB0150A8	CF_VALID [79].VALID[15:15]	1
0xBB0150A8	CF_VALID [80].VALID[16:16]	1
0xBB0150A8	CF_VALID [81].VALID[17:17]	1
0xBB0150A8	CF_VALID [82].VALID[18:18]	1
0xBB0150A8	CF_VALID [83].VALID[19:19]	1
0xBB0150A8	CF_VALID [84].VALID[20:20]	1
0xBB0150A8	CF_VALID [85].VALID[21:21]	1
0xBB0150A8	CF_VALID [86].VALID[22:22]	1
0xBB0150A8	CF_VALID [87].VALID[23:23]	1
0xBB0150A8	CF_VALID [88].VALID[24:24]	1
0xBB0150A8	CF_VALID [89].VALID[25:25]	1
0xBB0150A8	CF_VALID [90].VALID[26:26]	1

Address	Register	Len
0xBB0150A8	CF_VALID [91].VALID[27:27]	1
0xBB0150A8	CF_VALID [92].VALID[28:28]	1
0xBB0150A8	CF_VALID [93].VALID[29:29]	1
0xBB0150A8	CF_VALID [94].VALID[30:30]	1
0xBB0150A8	CF_VALID [95].VALID[31:31]	1
0xBB0150AC	CF_VALID [96].VALID[0:0]	1
0xBB0150AC	CF_VALID [97].VALID[1:1]	1
0xBB0150AC	CF_VALID [98].VALID[2:2]	1
0xBB0150AC	CF_VALID [99].VALID[3:3]	1
0xBB0150AC	CF_VALID [100].VALID[4:4]	1
0xBB0150AC	CF_VALID [101].VALID[5:5]	1
0xBB0150AC	CF_VALID [102].VALID[6:6]	1
0xBB0150AC	CF_VALID [103].VALID[7:7]	1
0xBB0150AC	CF_VALID [104].VALID[8:8]	1
0xBB0150AC	CF_VALID [105].VALID[9:9]	1
0xBB0150AC	CF_VALID [106].VALID[10:10]	1
0xBB0150AC	CF_VALID [107].VALID[11:11]	1
0xBB0150AC	CF_VALID [108].VALID[12:12]	1
0xBB0150AC	CF_VALID [109].VALID[13:13]	1
0xBB0150AC	CF_VALID [110].VALID[14:14]	1
0xBB0150AC	CF_VALID [111].VALID[15:15]	1
0xBB0150AC	CF_VALID [112].VALID[16:16]	1
0xBB0150AC	CF_VALID [113].VALID[17:17]	1
0xBB0150AC	CF_VALID [114].VALID[18:18]	1
0xBB0150AC	CF_VALID [115].VALID[19:19]	1
0xBB0150AC	CF_VALID [116].VALID[20:20]	1
0xBB0150AC	CF_VALID [117].VALID[21:21]	1
0xBB0150AC	CF_VALID [118].VALID[22:22]	1
0xBB0150AC	CF_VALID [119].VALID[23:23]	1
0xBB0150AC	CF_VALID [120].VALID[24:24]	1
0xBB0150AC	CF_VALID [121].VALID[25:25]	1
0xBB0150AC	CF_VALID [122].VALID[26:26]	1
0xBB0150AC	CF_VALID [123].VALID[27:27]	1
0xBB0150AC	CF_VALID [124].VALID[28:28]	1
0xBB0150AC	CF_VALID [125].VALID[29:29]	1
0xBB0150AC	CF_VALID [126].VALID[30:30]	1
0xBB0150AC	CF_VALID [127].VALID[31:31]	1
0xBB0150B0	CF_VALID [128].VALID[0:0]	1
0xBB0150B0	CF_VALID [129].VALID[1:1]	1
0xBB0150B0	CF_VALID [130].VALID[2:2]	1
0xBB0150B0	CF_VALID [131].VALID[3:3]	1
0xBB0150B0	CF_VALID [132].VALID[4:4]	1
0xBB0150B0	CF_VALID [133].VALID[5:5]	1
0xBB0150B0	CF_VALID [134].VALID[6:6]	1
0xBB0150B0	CF_VALID [135].VALID[7:7]	1
0xBB0150B0	CF_VALID [136].VALID[8:8]	1

Address	Register	Len
0xBB0150B0	CF_VALID [137].VALID[9:9]	1
0xBB0150B0	CF_VALID [138].VALID[10:10]	1
0xBB0150B0	CF_VALID [139].VALID[11:11]	1
0xBB0150B0	CF_VALID [140].VALID[12:12]	1
0xBB0150B0	CF_VALID [141].VALID[13:13]	1
0xBB0150B0	CF_VALID [142].VALID[14:14]	1
0xBB0150B0	CF_VALID [143].VALID[15:15]	1
0xBB0150B0	CF_VALID [144].VALID[16:16]	1
0xBB0150B0	CF_VALID [145].VALID[17:17]	1
0xBB0150B0	CF_VALID [146].VALID[18:18]	1
0xBB0150B0	CF_VALID [147].VALID[19:19]	1
0xBB0150B0	CF_VALID [148].VALID[20:20]	1
0xBB0150B0	CF_VALID [149].VALID[21:21]	1
0xBB0150B0	CF_VALID [150].VALID[22:22]	1
0xBB0150B0	CF_VALID [151].VALID[23:23]	1
0xBB0150B0	CF_VALID [152].VALID[24:24]	1
0xBB0150B0	CF_VALID [153].VALID[25:25]	1
0xBB0150B0	CF_VALID [154].VALID[26:26]	1
0xBB0150B0	CF_VALID [155].VALID[27:27]	1
0xBB0150B0	CF_VALID [156].VALID[28:28]	1
0xBB0150B0	CF_VALID [157].VALID[29:29]	1
0xBB0150B0	CF_VALID [158].VALID[30:30]	1
0xBB0150B0	CF_VALID [159].VALID[31:31]	1
0xBB0150B4	CF_VALID [160].VALID[0:0]	1
0xBB0150B4	CF_VALID [161].VALID[1:1]	1
0xBB0150B4	CF_VALID [162].VALID[2:2]	1
0xBB0150B4	CF_VALID [163].VALID[3:3]	1
0xBB0150B4	CF_VALID [164].VALID[4:4]	1
0xBB0150B4	CF_VALID [165].VALID[5:5]	1
0xBB0150B4	CF_VALID [166].VALID[6:6]	1
0xBB0150B4	CF_VALID [167].VALID[7:7]	1
0xBB0150B4	CF_VALID [168].VALID[8:8]	1
0xBB0150B4	CF_VALID [169].VALID[9:9]	1
0xBB0150B4	CF_VALID [170].VALID[10:10]	1
0xBB0150B4	CF_VALID [171].VALID[11:11]	1
0xBB0150B4	CF_VALID [172].VALID[12:12]	1
0xBB0150B4	CF_VALID [173].VALID[13:13]	1
0xBB0150B4	CF_VALID [174].VALID[14:14]	1
0xBB0150B4	CF_VALID [175].VALID[15:15]	1
0xBB0150B4	CF_VALID [176].VALID[16:16]	1
0xBB0150B4	CF_VALID [177].VALID[17:17]	1
0xBB0150B4	CF_VALID [178].VALID[18:18]	1
0xBB0150B4	CF_VALID [179].VALID[19:19]	1
0xBB0150B4	CF_VALID [180].VALID[20:20]	1
0xBB0150B4	CF_VALID [181].VALID[21:21]	1
0xBB0150B4	CF_VALID [182].VALID[22:22]	1

Address	Register	Len
0xBB0150B4	CF_VALID [183].VALID[23:23]	1
0xBB0150B4	CF_VALID [184].VALID[24:24]	1
0xBB0150B4	CF_VALID [185].VALID[25:25]	1
0xBB0150B4	CF_VALID [186].VALID[26:26]	1
0xBB0150B4	CF_VALID [187].VALID[27:27]	1
0xBB0150B4	CF_VALID [188].VALID[28:28]	1
0xBB0150B4	CF_VALID [189].VALID[29:29]	1
0xBB0150B4	CF_VALID [190].VALID[30:30]	1
0xBB0150B4	CF_VALID [191].VALID[31:31]	1
0xBB0150B8	CF_VALID [192].VALID[0:0]	1
0xBB0150B8	CF_VALID [193].VALID[1:1]	1
0xBB0150B8	CF_VALID [194].VALID[2:2]	1
0xBB0150B8	CF_VALID [195].VALID[3:3]	1
0xBB0150B8	CF_VALID [196].VALID[4:4]	1
0xBB0150B8	CF_VALID [197].VALID[5:5]	1
0xBB0150B8	CF_VALID [198].VALID[6:6]	1
0xBB0150B8	CF_VALID [199].VALID[7:7]	1
0xBB0150B8	CF_VALID [200].VALID[8:8]	1
0xBB0150B8	CF_VALID [201].VALID[9:9]	1
0xBB0150B8	CF_VALID [202].VALID[10:10]	1
0xBB0150B8	CF_VALID [203].VALID[11:11]	1
0xBB0150B8	CF_VALID [204].VALID[12:12]	1
0xBB0150B8	CF_VALID [205].VALID[13:13]	1
0xBB0150B8	CF_VALID [206].VALID[14:14]	1
0xBB0150B8	CF_VALID [207].VALID[15:15]	1
0xBB0150B8	CF_VALID [208].VALID[16:16]	1
0xBB0150B8	CF_VALID [209].VALID[17:17]	1
0xBB0150B8	CF_VALID [210].VALID[18:18]	1
0xBB0150B8	CF_VALID [211].VALID[19:19]	1
0xBB0150B8	CF_VALID [212].VALID[20:20]	1
0xBB0150B8	CF_VALID [213].VALID[21:21]	1
0xBB0150B8	CF_VALID [214].VALID[22:22]	1
0xBB0150B8	CF_VALID [215].VALID[23:23]	1
0xBB0150B8	CF_VALID [216].VALID[24:24]	1
0xBB0150B8	CF_VALID [217].VALID[25:25]	1
0xBB0150B8	CF_VALID [218].VALID[26:26]	1
0xBB0150B8	CF_VALID [219].VALID[27:27]	1
0xBB0150B8	CF_VALID [220].VALID[28:28]	1
0xBB0150B8	CF_VALID [221].VALID[29:29]	1
0xBB0150B8	CF_VALID [222].VALID[30:30]	1
0xBB0150B8	CF_VALID [223].VALID[31:31]	1
0xBB0150BC	CF_VALID [224].VALID[0:0]	1
0xBB0150BC	CF_VALID [225].VALID[1:1]	1
0xBB0150BC	CF_VALID [226].VALID[2:2]	1
0xBB0150BC	CF_VALID [227].VALID[3:3]	1
0xBB0150BC	CF_VALID [228].VALID[4:4]	1

Address	Register	Len
0xBB0150BC	CF_VALID [229].VALID[5:5]	1
0xBB0150BC	CF_VALID [230].VALID[6:6]	1
0xBB0150BC	CF_VALID [231].VALID[7:7]	1
0xBB0150BC	CF_VALID [232].VALID[8:8]	1
0xBB0150BC	CF_VALID [233].VALID[9:9]	1
0xBB0150BC	CF_VALID [234].VALID[10:10]	1
0xBB0150BC	CF_VALID [235].VALID[11:11]	1
0xBB0150BC	CF_VALID [236].VALID[12:12]	1
0xBB0150BC	CF_VALID [237].VALID[13:13]	1
0xBB0150BC	CF_VALID [238].VALID[14:14]	1
0xBB0150BC	CF_VALID [239].VALID[15:15]	1
0xBB0150BC	CF_VALID [240].VALID[16:16]	1
0xBB0150BC	CF_VALID [241].VALID[17:17]	1
0xBB0150BC	CF_VALID [242].VALID[18:18]	1
0xBB0150BC	CF_VALID [243].VALID[19:19]	1
0xBB0150BC	CF_VALID [244].VALID[20:20]	1
0xBB0150BC	CF_VALID [245].VALID[21:21]	1
0xBB0150BC	CF_VALID [246].VALID[22:22]	1
0xBB0150BC	CF_VALID [247].VALID[23:23]	1
0xBB0150BC	CF_VALID [248].VALID[24:24]	1
0xBB0150BC	CF_VALID [249].VALID[25:25]	1
0xBB0150BC	CF_VALID [250].VALID[26:26]	1
0xBB0150BC	CF_VALID [251].VALID[27:27]	1
0xBB0150BC	CF_VALID [252].VALID[28:28]	1
0xBB0150BC	CF_VALID [253].VALID[29:29]	1
0xBB0150BC	CF_VALID [254].VALID[30:30]	1
0xBB0150BC	CF_VALID [255].VALID[31:31]	1
0xBB0150C0	CF_VALID [256].VALID[0:0]	1
0xBB0150C0	CF_VALID [257].VALID[1:1]	1
0xBB0150C0	CF_VALID [258].VALID[2:2]	1
0xBB0150C0	CF_VALID [259].VALID[3:3]	1
0xBB0150C0	CF_VALID [260].VALID[4:4]	1
0xBB0150C0	CF_VALID [261].VALID[5:5]	1
0xBB0150C0	CF_VALID [262].VALID[6:6]	1
0xBB0150C0	CF_VALID [263].VALID[7:7]	1
0xBB0150C0	CF_VALID [264].VALID[8:8]	1
0xBB0150C0	CF_VALID [265].VALID[9:9]	1
0xBB0150C0	CF_VALID [266].VALID[10:10]	1
0xBB0150C0	CF_VALID [267].VALID[11:11]	1
0xBB0150C0	CF_VALID [268].VALID[12:12]	1
0xBB0150C0	CF_VALID [269].VALID[13:13]	1
0xBB0150C0	CF_VALID [270].VALID[14:14]	1
0xBB0150C0	CF_VALID [271].VALID[15:15]	1
0xBB0150C0	CF_VALID [272].VALID[16:16]	1
0xBB0150C0	CF_VALID [273].VALID[17:17]	1
0xBB0150C0	CF_VALID [274].VALID[18:18]	1

Address	Register	Len
0xBB0150C0	CF_VALID [275].VALID[19:19]	1
0xBB0150C0	CF_VALID [276].VALID[20:20]	1
0xBB0150C0	CF_VALID [277].VALID[21:21]	1
0xBB0150C0	CF_VALID [278].VALID[22:22]	1
0xBB0150C0	CF_VALID [279].VALID[23:23]	1
0xBB0150C0	CF_VALID [280].VALID[24:24]	1
0xBB0150C0	CF_VALID [281].VALID[25:25]	1
0xBB0150C0	CF_VALID [282].VALID[26:26]	1
0xBB0150C0	CF_VALID [283].VALID[27:27]	1
0xBB0150C0	CF_VALID [284].VALID[28:28]	1
0xBB0150C0	CF_VALID [285].VALID[29:29]	1
0xBB0150C0	CF_VALID [286].VALID[30:30]	1
0xBB0150C0	CF_VALID [287].VALID[31:31]	1
0xBB0150C4	CF_VALID [288].VALID[0:0]	1
0xBB0150C4	CF_VALID [289].VALID[1:1]	1
0xBB0150C4	CF_VALID [290].VALID[2:2]	1
0xBB0150C4	CF_VALID [291].VALID[3:3]	1
0xBB0150C4	CF_VALID [292].VALID[4:4]	1
0xBB0150C4	CF_VALID [293].VALID[5:5]	1
0xBB0150C4	CF_VALID [294].VALID[6:6]	1
0xBB0150C4	CF_VALID [295].VALID[7:7]	1
0xBB0150C4	CF_VALID [296].VALID[8:8]	1
0xBB0150C4	CF_VALID [297].VALID[9:9]	1
0xBB0150C4	CF_VALID [298].VALID[10:10]	1
0xBB0150C4	CF_VALID [299].VALID[11:11]	1
0xBB0150C4	CF_VALID [300].VALID[12:12]	1
0xBB0150C4	CF_VALID [301].VALID[13:13]	1
0xBB0150C4	CF_VALID [302].VALID[14:14]	1
0xBB0150C4	CF_VALID [303].VALID[15:15]	1
0xBB0150C4	CF_VALID [304].VALID[16:16]	1
0xBB0150C4	CF_VALID [305].VALID[17:17]	1
0xBB0150C4	CF_VALID [306].VALID[18:18]	1
0xBB0150C4	CF_VALID [307].VALID[19:19]	1
0xBB0150C4	CF_VALID [308].VALID[20:20]	1
0xBB0150C4	CF_VALID [309].VALID[21:21]	1
0xBB0150C4	CF_VALID [310].VALID[22:22]	1
0xBB0150C4	CF_VALID [311].VALID[23:23]	1
0xBB0150C4	CF_VALID [312].VALID[24:24]	1
0xBB0150C4	CF_VALID [313].VALID[25:25]	1
0xBB0150C4	CF_VALID [314].VALID[26:26]	1
0xBB0150C4	CF_VALID [315].VALID[27:27]	1
0xBB0150C4	CF_VALID [316].VALID[28:28]	1
0xBB0150C4	CF_VALID [317].VALID[29:29]	1
0xBB0150C4	CF_VALID [318].VALID[30:30]	1
0xBB0150C4	CF_VALID [319].VALID[31:31]	1
0xBB0150C8	CF_VALID [320].VALID[0:0]	1

Address	Register	Len
0xBB0150C8	CF_VALID [321].VALID[1:1]	1
0xBB0150C8	CF_VALID [322].VALID[2:2]	1
0xBB0150C8	CF_VALID [323].VALID[3:3]	1
0xBB0150C8	CF_VALID [324].VALID[4:4]	1
0xBB0150C8	CF_VALID [325].VALID[5:5]	1
0xBB0150C8	CF_VALID [326].VALID[6:6]	1
0xBB0150C8	CF_VALID [327].VALID[7:7]	1
0xBB0150C8	CF_VALID [328].VALID[8:8]	1
0xBB0150C8	CF_VALID [329].VALID[9:9]	1
0xBB0150C8	CF_VALID [330].VALID[10:10]	1
0xBB0150C8	CF_VALID [331].VALID[11:11]	1
0xBB0150C8	CF_VALID [332].VALID[12:12]	1
0xBB0150C8	CF_VALID [333].VALID[13:13]	1
0xBB0150C8	CF_VALID [334].VALID[14:14]	1
0xBB0150C8	CF_VALID [335].VALID[15:15]	1
0xBB0150C8	CF_VALID [336].VALID[16:16]	1
0xBB0150C8	CF_VALID [337].VALID[17:17]	1
0xBB0150C8	CF_VALID [338].VALID[18:18]	1
0xBB0150C8	CF_VALID [339].VALID[19:19]	1
0xBB0150C8	CF_VALID [340].VALID[20:20]	1
0xBB0150C8	CF_VALID [341].VALID[21:21]	1
0xBB0150C8	CF_VALID [342].VALID[22:22]	1
0xBB0150C8	CF_VALID [343].VALID[23:23]	1
0xBB0150C8	CF_VALID [344].VALID[24:24]	1
0xBB0150C8	CF_VALID [345].VALID[25:25]	1
0xBB0150C8	CF_VALID [346].VALID[26:26]	1
0xBB0150C8	CF_VALID [347].VALID[27:27]	1
0xBB0150C8	CF_VALID [348].VALID[28:28]	1
0xBB0150C8	CF_VALID [349].VALID[29:29]	1
0xBB0150C8	CF_VALID [350].VALID[30:30]	1
0xBB0150C8	CF_VALID [351].VALID[31:31]	1
0xBB0150CC	CF_VALID [352].VALID[0:0]	1
0xBB0150CC	CF_VALID [353].VALID[1:1]	1
0xBB0150CC	CF_VALID [354].VALID[2:2]	1
0xBB0150CC	CF_VALID [355].VALID[3:3]	1
0xBB0150CC	CF_VALID [356].VALID[4:4]	1
0xBB0150CC	CF_VALID [357].VALID[5:5]	1
0xBB0150CC	CF_VALID [358].VALID[6:6]	1
0xBB0150CC	CF_VALID [359].VALID[7:7]	1
0xBB0150CC	CF_VALID [360].VALID[8:8]	1
0xBB0150CC	CF_VALID [361].VALID[9:9]	1
0xBB0150CC	CF_VALID [362].VALID[10:10]	1
0xBB0150CC	CF_VALID [363].VALID[11:11]	1
0xBB0150CC	CF_VALID [364].VALID[12:12]	1
0xBB0150CC	CF_VALID [365].VALID[13:13]	1
0xBB0150CC	CF_VALID [366].VALID[14:14]	1



Address	Register	Len
0xBB0150CC	CF_VALID [367].VALID[15:15]	1
0xBB0150CC	CF_VALID [368].VALID[16:16]	1
0xBB0150CC	CF_VALID [369].VALID[17:17]	1
0xBB0150CC	CF_VALID [370].VALID[18:18]	1
0xBB0150CC	CF_VALID [371].VALID[19:19]	1
0xBB0150CC	CF_VALID [372].VALID[20:20]	1
0xBB0150CC	CF_VALID [373].VALID[21:21]	1
0xBB0150CC	CF_VALID [374].VALID[22:22]	1
0xBB0150CC	CF_VALID [375].VALID[23:23]	1
0xBB0150CC	CF_VALID [376].VALID[24:24]	1
0xBB0150CC	CF_VALID [377].VALID[25:25]	1
0xBB0150CC	CF_VALID [378].VALID[26:26]	1
0xBB0150CC	CF_VALID [379].VALID[27:27]	1
0xBB0150CC	CF_VALID [380].VALID[28:28]	1
0xBB0150CC	CF_VALID [381].VALID[29:29]	1
0xBB0150CC	CF_VALID [382].VALID[30:30]	1
0xBB0150CC	CF_VALID [383].VALID[31:31]	1
0xBB0150D0	CF_VALID [384].VALID[0:0]	1
0xBB0150D0	CF_VALID [385].VALID[1:1]	1
0xBB0150D0	CF_VALID [386].VALID[2:2]	1
0xBB0150D0	CF_VALID [387].VALID[3:3]	1
0xBB0150D0	CF_VALID [388].VALID[4:4]	1
0xBB0150D0	CF_VALID [389].VALID[5:5]	1
0xBB0150D0	CF_VALID [390].VALID[6:6]	1
0xBB0150D0	CF_VALID [391].VALID[7:7]	1
0xBB0150D0	CF_VALID [392].VALID[8:8]	1
0xBB0150D0	CF_VALID [393].VALID[9:9]	1
0xBB0150D0	CF_VALID [394].VALID[10:10]	1
0xBB0150D0	CF_VALID [395].VALID[11:11]	1
0xBB0150D0	CF_VALID [396].VALID[12:12]	1
0xBB0150D0	CF_VALID [397].VALID[13:13]	1
0xBB0150D0	CF_VALID [398].VALID[14:14]	1
0xBB0150D0	CF_VALID [399].VALID[15:15]	1
0xBB0150D0	CF_VALID [400].VALID[16:16]	1
0xBB0150D0	CF_VALID [401].VALID[17:17]	1
0xBB0150D0	CF_VALID [402].VALID[18:18]	1
0xBB0150D0	CF_VALID [403].VALID[19:19]	1
0xBB0150D0	CF_VALID [404].VALID[20:20]	1
0xBB0150D0	CF_VALID [405].VALID[21:21]	1
0xBB0150D0	CF_VALID [406].VALID[22:22]	1
0xBB0150D0	CF_VALID [407].VALID[23:23]	1
0xBB0150D0	CF_VALID [408].VALID[24:24]	1
0xBB0150D0	CF_VALID [409].VALID[25:25]	1
0xBB0150D0	CF_VALID [410].VALID[26:26]	1
0xBB0150D0	CF_VALID [411].VALID[27:27]	1
0xBB0150D0	CF_VALID [412].VALID[28:28]	1

Address	Register	Len
0xBB0150D0	CF_VALID [413].VALID[29:29]	1
0xBB0150D0	CF_VALID [414].VALID[30:30]	1
0xBB0150D0	CF_VALID [415].VALID[31:31]	1
0xBB0150D4	CF_VALID [416].VALID[0:0]	1
0xBB0150D4	CF_VALID [417].VALID[1:1]	1
0xBB0150D4	CF_VALID [418].VALID[2:2]	1
0xBB0150D4	CF_VALID [419].VALID[3:3]	1
0xBB0150D4	CF_VALID [420].VALID[4:4]	1
0xBB0150D4	CF_VALID [421].VALID[5:5]	1
0xBB0150D4	CF_VALID [422].VALID[6:6]	1
0xBB0150D4	CF_VALID [423].VALID[7:7]	1
0xBB0150D4	CF_VALID [424].VALID[8:8]	1
0xBB0150D4	CF_VALID [425].VALID[9:9]	1
0xBB0150D4	CF_VALID [426].VALID[10:10]	1
0xBB0150D4	CF_VALID [427].VALID[11:11]	1
0xBB0150D4	CF_VALID [428].VALID[12:12]	1
0xBB0150D4	CF_VALID [429].VALID[13:13]	1
0xBB0150D4	CF_VALID [430].VALID[14:14]	1
0xBB0150D4	CF_VALID [431].VALID[15:15]	1
0xBB0150D4	CF_VALID [432].VALID[16:16]	1
0xBB0150D4	CF_VALID [433].VALID[17:17]	1
0xBB0150D4	CF_VALID [434].VALID[18:18]	1
0xBB0150D4	CF_VALID [435].VALID[19:19]	1
0xBB0150D4	CF_VALID [436].VALID[20:20]	1
0xBB0150D4	CF_VALID [437].VALID[21:21]	1
0xBB0150D4	CF_VALID [438].VALID[22:22]	1
0xBB0150D4	CF_VALID [439].VALID[23:23]	1
0xBB0150D4	CF_VALID [440].VALID[24:24]	1
0xBB0150D4	CF_VALID [441].VALID[25:25]	1
0xBB0150D4	CF_VALID [442].VALID[26:26]	1
0xBB0150D4	CF_VALID [443].VALID[27:27]	1
0xBB0150D4	CF_VALID [444].VALID[28:28]	1
0xBB0150D4	CF_VALID [445].VALID[29:29]	1
0xBB0150D4	CF_VALID [446].VALID[30:30]	1
0xBB0150D4	CF_VALID [447].VALID[31:31]	1
0xBB0150D8	CF_VALID [448].VALID[0:0]	1
0xBB0150D8	CF_VALID [449].VALID[1:1]	1
0xBB0150D8	CF_VALID [450].VALID[2:2]	1
0xBB0150D8	CF_VALID [451].VALID[3:3]	1
0xBB0150D8	CF_VALID [452].VALID[4:4]	1
0xBB0150D8	CF_VALID [453].VALID[5:5]	1
0xBB0150D8	CF_VALID [454].VALID[6:6]	1
0xBB0150D8	CF_VALID [455].VALID[7:7]	1
0xBB0150D8	CF_VALID [456].VALID[8:8]	1
0xBB0150D8	CF_VALID [457].VALID[9:9]	1
0xBB0150D8	CF_VALID [458].VALID[10:10]	1

Address	Register	Len
0xBB0150D8	CF_VALID [459].VALID[11:11]	1
0xBB0150D8	CF_VALID [460].VALID[12:12]	1
0xBB0150D8	CF_VALID [461].VALID[13:13]	1
0xBB0150D8	CF_VALID [462].VALID[14:14]	1
0xBB0150D8	CF_VALID [463].VALID[15:15]	1
0xBB0150D8	CF_VALID [464].VALID[16:16]	1
0xBB0150D8	CF_VALID [465].VALID[17:17]	1
0xBB0150D8	CF_VALID [466].VALID[18:18]	1
0xBB0150D8	CF_VALID [467].VALID[19:19]	1
0xBB0150D8	CF_VALID [468].VALID[20:20]	1
0xBB0150D8	CF_VALID [469].VALID[21:21]	1
0xBB0150D8	CF_VALID [470].VALID[22:22]	1
0xBB0150D8	CF_VALID [471].VALID[23:23]	1
0xBB0150D8	CF_VALID [472].VALID[24:24]	1
0xBB0150D8	CF_VALID [473].VALID[25:25]	1
0xBB0150D8	CF_VALID [474].VALID[26:26]	1
0xBB0150D8	CF_VALID [475].VALID[27:27]	1
0xBB0150D8	CF_VALID [476].VALID[28:28]	1
0xBB0150D8	CF_VALID [477].VALID[29:29]	1
0xBB0150D8	CF_VALID [478].VALID[30:30]	1
0xBB0150D8	CF_VALID [479].VALID[31:31]	1
0xBB0150DC	CF_VALID [480].VALID[0:0]	1
0xBB0150DC	CF_VALID [481].VALID[1:1]	1
0xBB0150DC	CF_VALID [482].VALID[2:2]	1
0xBB0150DC	CF_VALID [483].VALID[3:3]	1
0xBB0150DC	CF_VALID [484].VALID[4:4]	1
0xBB0150DC	CF_VALID [485].VALID[5:5]	1
0xBB0150DC	CF_VALID [486].VALID[6:6]	1
0xBB0150DC	CF_VALID [487].VALID[7:7]	1
0xBB0150DC	CF_VALID [488].VALID[8:8]	1
0xBB0150DC	CF_VALID [489].VALID[9:9]	1
0xBB0150DC	CF_VALID [490].VALID[10:10]	1
0xBB0150DC	CF_VALID [491].VALID[11:11]	1
0xBB0150DC	CF_VALID [492].VALID[12:12]	1
0xBB0150DC	CF_VALID [493].VALID[13:13]	1
0xBB0150DC	CF_VALID [494].VALID[14:14]	1
0xBB0150DC	CF_VALID [495].VALID[15:15]	1
0xBB0150DC	CF_VALID [496].VALID[16:16]	1
0xBB0150DC	CF_VALID [497].VALID[17:17]	1
0xBB0150DC	CF_VALID [498].VALID[18:18]	1
0xBB0150DC	CF_VALID [499].VALID[19:19]	1
0xBB0150DC	CF_VALID [500].VALID[20:20]	1
0xBB0150DC	CF_VALID [501].VALID[21:21]	1
0xBB0150DC	CF_VALID [502].VALID[22:22]	1
0xBB0150DC	CF_VALID [503].VALID[23:23]	1
0xBB0150DC	CF_VALID [504].VALID[24:24]	1

Address	Register	Len
0xBB0150DC	CF_VALID [505].VALID[25:25]	1
0xBB0150DC	CF_VALID [506].VALID[26:26]	1
0xBB0150DC	CF_VALID [507].VALID[27:27]	1
0xBB0150DC	CF_VALID [508].VALID[28:28]	1
0xBB0150DC	CF_VALID [509].VALID[29:29]	1
0xBB0150DC	CF_VALID [510].VALID[30:30]	1
0xBB0150DC	CF_VALID [511].VALID[31:31]	1
0xBB0150E0	CF_CFG.RESERVED[31:4]	28
0xBB0150E0	CF_CFG.CF_SEL_RGMII_EN[3:3]	1
0xBB0150E0	CF_CFG.CF_SEL_PON_EN[2:2]	1
0xBB0150E0	CF_CFG.CF_US_PERMIT[1:0]	2
0xBB0150E4	RMK_DSCP_CF_PRI_CTRL [0].RESERVED[31:6]	26
0xBB0150E4	RMK_DSCP_CF_PRI_CTRL [0].CFPRI_DSCP[5:0]	6
0xBB0150E8	RMK_DSCP_CF_PRI_CTRL [1].RESERVED[31:6]	26
0xBB0150E8	RMK_DSCP_CF_PRI_CTRL [1].CFPRI_DSCP[5:0]	6
0xBB0150EC	RMK_DSCP_CF_PRI_CTRL [2].RESERVED[31:6]	26
0xBB0150EC	RMK_DSCP_CF_PRI_CTRL [2].CFPRI_DSCP[5:0]	6
0xBB0150F0	RMK_DSCP_CF_PRI_CTRL [3].RESERVED[31:6]	26
0xBB0150F0	RMK_DSCP_CF_PRI_CTRL [3].CFPRI_DSCP[5:0]	6
0xBB0150F4	RMK_DSCP_CF_PRI_CTRL [4].RESERVED[31:6]	26
0xBB0150F4	RMK_DSCP_CF_PRI_CTRL [4].CFPRI_DSCP[5:0]	6
0xBB0150F8	RMK_DSCP_CF_PRI_CTRL [5].RESERVED[31:6]	26
0xBB0150F8	RMK_DSCP_CF_PRI_CTRL [5].CFPRI_DSCP[5:0]	6
0xBB0150FC	RMK_DSCP_CF_PRI_CTRL [6].RESERVED[31:6]	26
0xBB0150FC	RMK_DSCP_CF_PRI_CTRL [6].CFPRI_DSCP[5:0]	6
0xBB015100	RMK_DSCP_CF_PRI_CTRL [7].RESERVED[31:6]	26
0xBB015100	RMK_DSCP_CF_PRI_CTRL [7].CFPRI_DSCP[5:0]	6
0xBB015104	ACL_EN [0].EN[0:0]	1
0xBB015104	ACL_EN [1].EN[1:1]	1
0xBB015104	ACL_EN [2].EN[2:2]	1
0xBB015104	ACL_EN [3].EN[3:3]	1
0xBB015104	ACL_EN [4].EN[4:4]	1
0xBB015104	ACL_EN [5].EN[5:5]	1
0xBB015104	ACL_EN [6].EN[6:6]	1
0xBB015108	ACL_PERMIT [0].PERMIT[0:0]	1
0xBB015108	ACL_PERMIT [1].PERMIT[1:1]	1
0xBB015108	ACL_PERMIT [2].PERMIT[2:2]	1
0xBB015108	ACL_PERMIT [3].PERMIT[3:3]	1
0xBB015108	ACL_PERMIT [4].PERMIT[4:4]	1
0xBB015108	ACL_PERMIT [5].PERMIT[5:5]	1
0xBB015108	ACL_PERMIT [6].PERMIT[6:6]	1
0xBB01510C	ACL_ACTION [0].RESERVED[31:8]	24
0xBB01510C	ACL_ACTION [0].VALID[7:7]	1
0xBB01510C	ACL_ACTION [0].NOT[6:6]	1
0xBB01510C	ACL_ACTION [0].INT_CF[5:5]	1
0xBB01510C	ACL_ACTION [0].FWD[4:4]	1

Address	Register	Len
0xBB01510C	ACL_ACTION [0].POLICING[3:3]	1
0xBB01510C	ACL_ACTION [0].PRI[2:2]	1
0xBB01510C	ACL_ACTION [0].SVLAN[1:1]	1
0xBB01510C	ACL_ACTION [0].CVLAN[0:0]	1
0xBB015110	ACL_ACTION [1].RESERVED[31:8]	24
0xBB015110	ACL_ACTION [1].VALID[7:7]	1
0xBB015110	ACL_ACTION [1].NOT[6:6]	1
0xBB015110	ACL_ACTION [1].INT_CF[5:5]	1
0xBB015110	ACL_ACTION [1].FWD[4:4]	1
0xBB015110	ACL_ACTION [1].POLICING[3:3]	1
0xBB015110	ACL_ACTION [1].PRI[2:2]	1
0xBB015110	ACL_ACTION [1].SVLAN[1:1]	1
0xBB015110	ACL_ACTION [1].CVLAN[0:0]	1
0xBB015114	ACL_ACTION [2].RESERVED[31:8]	24
0xBB015114	ACL_ACTION [2].VALID[7:7]	1
0xBB015114	ACL_ACTION [2].NOT[6:6]	1
0xBB015114	ACL_ACTION [2].INT_CF[5:5]	1
0xBB015114	ACL_ACTION [2].FWD[4:4]	1
0xBB015114	ACL_ACTION [2].POLICING[3:3]	1
0xBB015114	ACL_ACTION [2].PRI[2:2]	1
0xBB015114	ACL_ACTION [2].SVLAN[1:1]	1
0xBB015114	ACL_ACTION [2].CVLAN[0:0]	1
0xBB015118	ACL_ACTION [3].RESERVED[31:8]	24
0xBB015118	ACL_ACTION [3].VALID[7:7]	1
0xBB015118	ACL_ACTION [3].NOT[6:6]	1
0xBB015118	ACL_ACTION [3].INT_CF[5:5]	1
0xBB015118	ACL_ACTION [3].FWD[4:4]	1
0xBB015118	ACL_ACTION [3].POLICING[3:3]	1
0xBB015118	ACL_ACTION [3].PRI[2:2]	1
0xBB015118	ACL_ACTION [3].SVLAN[1:1]	1
0xBB015118	ACL_ACTION [3].CVLAN[0:0]	1
0xBB01511C	ACL_ACTION [4].RESERVED[31:8]	24
0xBB01511C	ACL_ACTION [4].VALID[7:7]	1
0xBB01511C	ACL_ACTION [4].NOT[6:6]	1
0xBB01511C	ACL_ACTION [4].INT_CF[5:5]	1
0xBB01511C	ACL_ACTION [4].FWD[4:4]	1
0xBB01511C	ACL_ACTION [4].POLICING[3:3]	1
0xBB01511C	ACL_ACTION [4].PRI[2:2]	1
0xBB01511C	ACL_ACTION [4].SVLAN[1:1]	1
0xBB01511C	ACL_ACTION [4].CVLAN[0:0]	1
0xBB015120	ACL_ACTION [5].RESERVED[31:8]	24
0xBB015120	ACL_ACTION [5].VALID[7:7]	1
0xBB015120	ACL_ACTION [5].NOT[6:6]	1
0xBB015120	ACL_ACTION [5].INT_CF[5:5]	1
0xBB015120	ACL_ACTION [5].FWD[4:4]	1
0xBB015120	ACL_ACTION [5].POLICING[3:3]	1

Address	Register	Len
0xBB015120	ACL_ACTION [5].PRI[2:2]	1
0xBB015120	ACL_ACTION [5].SVLAN[1:1]	1
0xBB015120	ACL_ACTION [5].CVLAN[0:0]	1
0xBB015124	ACL_ACTION [6].RESERVED[31:8]	24
0xBB015124	ACL_ACTION [6].VALID[7:7]	1
0xBB015124	ACL_ACTION [6].NOT[6:6]	1
0xBB015124	ACL_ACTION [6].INT_CF[5:5]	1
0xBB015124	ACL_ACTION [6].FWD[4:4]	1
0xBB015124	ACL_ACTION [6].POLICING[3:3]	1
0xBB015124	ACL_ACTION [6].PRI[2:2]	1
0xBB015124	ACL_ACTION [6].SVLAN[1:1]	1
0xBB015124	ACL_ACTION [6].CVLAN[0:0]	1
0xBB015128	ACL_ACTION [7].RESERVED[31:8]	24
0xBB015128	ACL_ACTION [7].VALID[7:7]	1
0xBB015128	ACL_ACTION [7].NOT[6:6]	1
0xBB015128	ACL_ACTION [7].INT_CF[5:5]	1
0xBB015128	ACL_ACTION [7].FWD[4:4]	1
0xBB015128	ACL_ACTION [7].POLICING[3:3]	1
0xBB015128	ACL_ACTION [7].PRI[2:2]	1
0xBB015128	ACL_ACTION [7].SVLAN[1:1]	1
0xBB015128	ACL_ACTION [7].CVLAN[0:0]	1
0xBB01512C	ACL_ACTION [8].RESERVED[31:8]	24
0xBB01512C	ACL_ACTION [8].VALID[7:7]	1
0xBB01512C	ACL_ACTION [8].NOT[6:6]	1
0xBB01512C	ACL_ACTION [8].INT_CF[5:5]	1
0xBB01512C	ACL_ACTION [8].FWD[4:4]	1
0xBB01512C	ACL_ACTION [8].POLICING[3:3]	1
0xBB01512C	ACL_ACTION [8].PRI[2:2]	1
0xBB01512C	ACL_ACTION [8].SVLAN[1:1]	1
0xBB01512C	ACL_ACTION [8].CVLAN[0:0]	1
0xBB015130	ACL_ACTION [9].RESERVED[31:8]	24
0xBB015130	ACL_ACTION [9].VALID[7:7]	1
0xBB015130	ACL_ACTION [9].NOT[6:6]	1
0xBB015130	ACL_ACTION [9].INT_CF[5:5]	1
0xBB015130	ACL_ACTION [9].FWD[4:4]	1
0xBB015130	ACL_ACTION [9].POLICING[3:3]	1
0xBB015130	ACL_ACTION [9].PRI[2:2]	1
0xBB015130	ACL_ACTION [9].SVLAN[1:1]	1
0xBB015130	ACL_ACTION [9].CVLAN[0:0]	1
0xBB015134	ACL_ACTION [10].RESERVED[31:8]	24
0xBB015134	ACL_ACTION [10].VALID[7:7]	1
0xBB015134	ACL_ACTION [10].NOT[6:6]	1
0xBB015134	ACL_ACTION [10].INT_CF[5:5]	1
0xBB015134	ACL_ACTION [10].FWD[4:4]	1
0xBB015134	ACL_ACTION [10].POLICING[3:3]	1
0xBB015134	ACL_ACTION [10].PRI[2:2]	1

Address	Register	Len
0xBB015134	ACL_ACTION [10].SVLAN[1:1]	1
0xBB015134	ACL_ACTION [10].CVLAN[0:0]	1
0xBB015138	ACL_ACTION [11].RESERVED[31:8]	24
0xBB015138	ACL_ACTION [11].VALID[7:7]	1
0xBB015138	ACL_ACTION [11].NOT[6:6]	1
0xBB015138	ACL_ACTION [11].INT_CF[5:5]	1
0xBB015138	ACL_ACTION [11].FWD[4:4]	1
0xBB015138	ACL_ACTION [11].POLICING[3:3]	1
0xBB015138	ACL_ACTION [11].PRI[2:2]	1
0xBB015138	ACL_ACTION [11].SVLAN[1:1]	1
0xBB015138	ACL_ACTION [11].CVLAN[0:0]	1
0xBB01513C	ACL_ACTION [12].RESERVED[31:8]	24
0xBB01513C	ACL_ACTION [12].VALID[7:7]	1
0xBB01513C	ACL_ACTION [12].NOT[6:6]	1
0xBB01513C	ACL_ACTION [12].INT_CF[5:5]	1
0xBB01513C	ACL_ACTION [12].FWD[4:4]	1
0xBB01513C	ACL_ACTION [12].POLICING[3:3]	1
0xBB01513C	ACL_ACTION [12].PRI[2:2]	1
0xBB01513C	ACL_ACTION [12].SVLAN[1:1]	1
0xBB01513C	ACL_ACTION [12].CVLAN[0:0]	1
0xBB015140	ACL_ACTION [13].RESERVED[31:8]	24
0xBB015140	ACL_ACTION [13].VALID[7:7]	1
0xBB015140	ACL_ACTION [13].NOT[6:6]	1
0xBB015140	ACL_ACTION [13].INT_CF[5:5]	1
0xBB015140	ACL_ACTION [13].FWD[4:4]	1
0xBB015140	ACL_ACTION [13].POLICING[3:3]	1
0xBB015140	ACL_ACTION [13].PRI[2:2]	1
0xBB015140	ACL_ACTION [13].SVLAN[1:1]	1
0xBB015140	ACL_ACTION [13].CVLAN[0:0]	1
0xBB015144	ACL_ACTION [14].RESERVED[31:8]	24
0xBB015144	ACL_ACTION [14].VALID[7:7]	1
0xBB015144	ACL_ACTION [14].NOT[6:6]	1
0xBB015144	ACL_ACTION [14].INT_CF[5:5]	1
0xBB015144	ACL_ACTION [14].FWD[4:4]	1
0xBB015144	ACL_ACTION [14].POLICING[3:3]	1
0xBB015144	ACL_ACTION [14].PRI[2:2]	1
0xBB015144	ACL_ACTION [14].SVLAN[1:1]	1
0xBB015144	ACL_ACTION [14].CVLAN[0:0]	1
0xBB015148	ACL_ACTION [15].RESERVED[31:8]	24
0xBB015148	ACL_ACTION [15].VALID[7:7]	1
0xBB015148	ACL_ACTION [15].NOT[6:6]	1
0xBB015148	ACL_ACTION [15].INT_CF[5:5]	1
0xBB015148	ACL_ACTION [15].FWD[4:4]	1
0xBB015148	ACL_ACTION [15].POLICING[3:3]	1
0xBB015148	ACL_ACTION [15].PRI[2:2]	1
0xBB015148	ACL_ACTION [15].SVLAN[1:1]	1

Address	Register	Len
0xBB015148	ACL_ACTION [15].CVLAN[0:0]	1
0xBB01514C	ACL_ACTION [16].RESERVED[31:8]	24
0xBB01514C	ACL_ACTION [16].VALID[7:7]	1
0xBB01514C	ACL_ACTION [16].NOT[6:6]	1
0xBB01514C	ACL_ACTION [16].INT_CF[5:5]	1
0xBB01514C	ACL_ACTION [16].FWD[4:4]	1
0xBB01514C	ACL_ACTION [16].POLICING[3:3]	1
0xBB01514C	ACL_ACTION [16].PRI[2:2]	1
0xBB01514C	ACL_ACTION [16].SVLAN[1:1]	1
0xBB01514C	ACL_ACTION [16].CVLAN[0:0]	1
0xBB015150	ACL_ACTION [17].RESERVED[31:8]	24
0xBB015150	ACL_ACTION [17].VALID[7:7]	1
0xBB015150	ACL_ACTION [17].NOT[6:6]	1
0xBB015150	ACL_ACTION [17].INT_CF[5:5]	1
0xBB015150	ACL_ACTION [17].FWD[4:4]	1
0xBB015150	ACL_ACTION [17].POLICING[3:3]	1
0xBB015150	ACL_ACTION [17].PRI[2:2]	1
0xBB015150	ACL_ACTION [17].SVLAN[1:1]	1
0xBB015150	ACL_ACTION [17].CVLAN[0:0]	1
0xBB015154	ACL_ACTION [18].RESERVED[31:8]	24
0xBB015154	ACL_ACTION [18].VALID[7:7]	1
0xBB015154	ACL_ACTION [18].NOT[6:6]	1
0xBB015154	ACL_ACTION [18].INT_CF[5:5]	1
0xBB015154	ACL_ACTION [18].FWD[4:4]	1
0xBB015154	ACL_ACTION [18].POLICING[3:3]	1
0xBB015154	ACL_ACTION [18].PRI[2:2]	1
0xBB015154	ACL_ACTION [18].SVLAN[1:1]	1
0xBB015154	ACL_ACTION [18].CVLAN[0:0]	1
0xBB015158	ACL_ACTION [19].RESERVED[31:8]	24
0xBB015158	ACL_ACTION [19].VALID[7:7]	1
0xBB015158	ACL_ACTION [19].NOT[6:6]	1
0xBB015158	ACL_ACTION [19].INT_CF[5:5]	1
0xBB015158	ACL_ACTION [19].FWD[4:4]	1
0xBB015158	ACL_ACTION [19].POLICING[3:3]	1
0xBB015158	ACL_ACTION [19].PRI[2:2]	1
0xBB015158	ACL_ACTION [19].SVLAN[1:1]	1
0xBB015158	ACL_ACTION [19].CVLAN[0:0]	1
0xBB01515C	ACL_ACTION [20].RESERVED[31:8]	24
0xBB01515C	ACL_ACTION [20].VALID[7:7]	1
0xBB01515C	ACL_ACTION [20].NOT[6:6]	1
0xBB01515C	ACL_ACTION [20].INT_CF[5:5]	1
0xBB01515C	ACL_ACTION [20].FWD[4:4]	1
0xBB01515C	ACL_ACTION [20].POLICING[3:3]	1
0xBB01515C	ACL_ACTION [20].PRI[2:2]	1
0xBB01515C	ACL_ACTION [20].SVLAN[1:1]	1
0xBB01515C	ACL_ACTION [20].CVLAN[0:0]	1



Address	Register	Len
0xBB015160	ACL_ACTION [21].RESERVED[31:8]	24
0xBB015160	ACL_ACTION [21].VALID[7:7]	1
0xBB015160	ACL_ACTION [21].NOT[6:6]	1
0xBB015160	ACL_ACTION [21].INT_CF[5:5]	1
0xBB015160	ACL_ACTION [21].FWD[4:4]	1
0xBB015160	ACL_ACTION [21].POLICING[3:3]	1
0xBB015160	ACL_ACTION [21].PRI[2:2]	1
0xBB015160	ACL_ACTION [21].SVLAN[1:1]	1
0xBB015160	ACL_ACTION [21].CVLAN[0:0]	1
0xBB015164	ACL_ACTION [22].RESERVED[31:8]	24
0xBB015164	ACL_ACTION [22].VALID[7:7]	1
0xBB015164	ACL_ACTION [22].NOT[6:6]	1
0xBB015164	ACL_ACTION [22].INT_CF[5:5]	1
0xBB015164	ACL_ACTION [22].FWD[4:4]	1
0xBB015164	ACL_ACTION [22].POLICING[3:3]	1
0xBB015164	ACL_ACTION [22].PRI[2:2]	1
0xBB015164	ACL_ACTION [22].SVLAN[1:1]	1
0xBB015164	ACL_ACTION [22].CVLAN[0:0]	1
0xBB015168	ACL_ACTION [23].RESERVED[31:8]	24
0xBB015168	ACL_ACTION [23].VALID[7:7]	1
0xBB015168	ACL_ACTION [23].NOT[6:6]	1
0xBB015168	ACL_ACTION [23].INT_CF[5:5]	1
0xBB015168	ACL_ACTION [23].FWD[4:4]	1
0xBB015168	ACL_ACTION [23].POLICING[3:3]	1
0xBB015168	ACL_ACTION [23].PRI[2:2]	1
0xBB015168	ACL_ACTION [23].SVLAN[1:1]	1
0xBB015168	ACL_ACTION [23].CVLAN[0:0]	1
0xBB01516C	ACL_ACTION [24].RESERVED[31:8]	24
0xBB01516C	ACL_ACTION [24].VALID[7:7]	1
0xBB01516C	ACL_ACTION [24].NOT[6:6]	1
0xBB01516C	ACL_ACTION [24].INT_CF[5:5]	1
0xBB01516C	ACL_ACTION [24].FWD[4:4]	1
0xBB01516C	ACL_ACTION [24].POLICING[3:3]	1
0xBB01516C	ACL_ACTION [24].PRI[2:2]	1
0xBB01516C	ACL_ACTION [24].SVLAN[1:1]	1
0xBB01516C	ACL_ACTION [24].CVLAN[0:0]	1
0xBB015170	ACL_ACTION [25].RESERVED[31:8]	24
0xBB015170	ACL_ACTION [25].VALID[7:7]	1
0xBB015170	ACL_ACTION [25].NOT[6:6]	1
0xBB015170	ACL_ACTION [25].INT_CF[5:5]	1
0xBB015170	ACL_ACTION [25].FWD[4:4]	1
0xBB015170	ACL_ACTION [25].POLICING[3:3]	1
0xBB015170	ACL_ACTION [25].PRI[2:2]	1
0xBB015170	ACL_ACTION [25].SVLAN[1:1]	1
0xBB015170	ACL_ACTION [25].CVLAN[0:0]	1
0xBB015174	ACL_ACTION [26].RESERVED[31:8]	24

Address	Register	Len
0xBB015174	ACL_ACTION [26].VALID[7:7]	1
0xBB015174	ACL_ACTION [26].NOT[6:6]	1
0xBB015174	ACL_ACTION [26].INT_CF[5:5]	1
0xBB015174	ACL_ACTION [26].FWD[4:4]	1
0xBB015174	ACL_ACTION [26].POLICING[3:3]	1
0xBB015174	ACL_ACTION [26].PRI[2:2]	1
0xBB015174	ACL_ACTION [26].SVLAN[1:1]	1
0xBB015174	ACL_ACTION [26].CVLAN[0:0]	1
0xBB015178	ACL_ACTION [27].RESERVED[31:8]	24
0xBB015178	ACL_ACTION [27].VALID[7:7]	1
0xBB015178	ACL_ACTION [27].NOT[6:6]	1
0xBB015178	ACL_ACTION [27].INT_CF[5:5]	1
0xBB015178	ACL_ACTION [27].FWD[4:4]	1
0xBB015178	ACL_ACTION [27].POLICING[3:3]	1
0xBB015178	ACL_ACTION [27].PRI[2:2]	1
0xBB015178	ACL_ACTION [27].SVLAN[1:1]	1
0xBB015178	ACL_ACTION [27].CVLAN[0:0]	1
0xBB01517C	ACL_ACTION [28].RESERVED[31:8]	24
0xBB01517C	ACL_ACTION [28].VALID[7:7]	1
0xBB01517C	ACL_ACTION [28].NOT[6:6]	1
0xBB01517C	ACL_ACTION [28].INT_CF[5:5]	1
0xBB01517C	ACL_ACTION [28].FWD[4:4]	1
0xBB01517C	ACL_ACTION [28].POLICING[3:3]	1
0xBB01517C	ACL_ACTION [28].PRI[2:2]	1
0xBB01517C	ACL_ACTION [28].SVLAN[1:1]	1
0xBB01517C	ACL_ACTION [28].CVLAN[0:0]	1
0xBB015180	ACL_ACTION [29].RESERVED[31:8]	24
0xBB015180	ACL_ACTION [29].VALID[7:7]	1
0xBB015180	ACL_ACTION [29].NOT[6:6]	1
0xBB015180	ACL_ACTION [29].INT_CF[5:5]	1
0xBB015180	ACL_ACTION [29].FWD[4:4]	1
0xBB015180	ACL_ACTION [29].POLICING[3:3]	1
0xBB015180	ACL_ACTION [29].PRI[2:2]	1
0xBB015180	ACL_ACTION [29].SVLAN[1:1]	1
0xBB015180	ACL_ACTION [29].CVLAN[0:0]	1
0xBB015184	ACL_ACTION [30].RESERVED[31:8]	24
0xBB015184	ACL_ACTION [30].VALID[7:7]	1
0xBB015184	ACL_ACTION [30].NOT[6:6]	1
0xBB015184	ACL_ACTION [30].INT_CF[5:5]	1
0xBB015184	ACL_ACTION [30].FWD[4:4]	1
0xBB015184	ACL_ACTION [30].POLICING[3:3]	1
0xBB015184	ACL_ACTION [30].PRI[2:2]	1
0xBB015184	ACL_ACTION [30].SVLAN[1:1]	1
0xBB015184	ACL_ACTION [30].CVLAN[0:0]	1
0xBB015188	ACL_ACTION [31].RESERVED[31:8]	24
0xBB015188	ACL_ACTION [31].VALID[7:7]	1

Address	Register	Len
0xBB015188	ACL_ACTION [31].NOT[6:6]	1
0xBB015188	ACL_ACTION [31].INT_CF[5:5]	1
0xBB015188	ACL_ACTION [31].FWD[4:4]	1
0xBB015188	ACL_ACTION [31].POLICING[3:3]	1
0xBB015188	ACL_ACTION [31].PRI[2:2]	1
0xBB015188	ACL_ACTION [31].SVLAN[1:1]	1
0xBB015188	ACL_ACTION [31].CVLAN[0:0]	1
0xBB01518C	ACL_ACTION [32].RESERVED[31:8]	24
0xBB01518C	ACL_ACTION [32].VALID[7:7]	1
0xBB01518C	ACL_ACTION [32].NOT[6:6]	1
0xBB01518C	ACL_ACTION [32].INT_CF[5:5]	1
0xBB01518C	ACL_ACTION [32].FWD[4:4]	1
0xBB01518C	ACL_ACTION [32].POLICING[3:3]	1
0xBB01518C	ACL_ACTION [32].PRI[2:2]	1
0xBB01518C	ACL_ACTION [32].SVLAN[1:1]	1
0xBB01518C	ACL_ACTION [32].CVLAN[0:0]	1
0xBB015190	ACL_ACTION [33].RESERVED[31:8]	24
0xBB015190	ACL_ACTION [33].VALID[7:7]	1
0xBB015190	ACL_ACTION [33].NOT[6:6]	1
0xBB015190	ACL_ACTION [33].INT_CF[5:5]	1
0xBB015190	ACL_ACTION [33].FWD[4:4]	1
0xBB015190	ACL_ACTION [33].POLICING[3:3]	1
0xBB015190	ACL_ACTION [33].PRI[2:2]	1
0xBB015190	ACL_ACTION [33].SVLAN[1:1]	1
0xBB015190	ACL_ACTION [33].CVLAN[0:0]	1
0xBB015194	ACL_ACTION [34].RESERVED[31:8]	24
0xBB015194	ACL_ACTION [34].VALID[7:7]	1
0xBB015194	ACL_ACTION [34].NOT[6:6]	1
0xBB015194	ACL_ACTION [34].INT_CF[5:5]	1
0xBB015194	ACL_ACTION [34].FWD[4:4]	1
0xBB015194	ACL_ACTION [34].POLICING[3:3]	1
0xBB015194	ACL_ACTION [34].PRI[2:2]	1
0xBB015194	ACL_ACTION [34].SVLAN[1:1]	1
0xBB015194	ACL_ACTION [34].CVLAN[0:0]	1
0xBB015198	ACL_ACTION [35].RESERVED[31:8]	24
0xBB015198	ACL_ACTION [35].VALID[7:7]	1
0xBB015198	ACL_ACTION [35].NOT[6:6]	1
0xBB015198	ACL_ACTION [35].INT_CF[5:5]	1
0xBB015198	ACL_ACTION [35].FWD[4:4]	1
0xBB015198	ACL_ACTION [35].POLICING[3:3]	1
0xBB015198	ACL_ACTION [35].PRI[2:2]	1
0xBB015198	ACL_ACTION [35].SVLAN[1:1]	1
0xBB015198	ACL_ACTION [35].CVLAN[0:0]	1
0xBB01519C	ACL_ACTION [36].RESERVED[31:8]	24
0xBB01519C	ACL_ACTION [36].VALID[7:7]	1
0xBB01519C	ACL_ACTION [36].NOT[6:6]	1

Address	Register	Len
0xBB01519C	ACL_ACTION [36].INT_CF[5:5]	1
0xBB01519C	ACL_ACTION [36].FWD[4:4]	1
0xBB01519C	ACL_ACTION [36].POLICING[3:3]	1
0xBB01519C	ACL_ACTION [36].PRI[2:2]	1
0xBB01519C	ACL_ACTION [36].SVLAN[1:1]	1
0xBB01519C	ACL_ACTION [36].CVLAN[0:0]	1
0xBB0151A0	ACL_ACTION [37].RESERVED[31:8]	24
0xBB0151A0	ACL_ACTION [37].VALID[7:7]	1
0xBB0151A0	ACL_ACTION [37].NOT[6:6]	1
0xBB0151A0	ACL_ACTION [37].INT_CF[5:5]	1
0xBB0151A0	ACL_ACTION [37].FWD[4:4]	1
0xBB0151A0	ACL_ACTION [37].POLICING[3:3]	1
0xBB0151A0	ACL_ACTION [37].PRI[2:2]	1
0xBB0151A0	ACL_ACTION [37].SVLAN[1:1]	1
0xBB0151A0	ACL_ACTION [37].CVLAN[0:0]	1
0xBB0151A4	ACL_ACTION [38].RESERVED[31:8]	24
0xBB0151A4	ACL_ACTION [38].VALID[7:7]	1
0xBB0151A4	ACL_ACTION [38].NOT[6:6]	1
0xBB0151A4	ACL_ACTION [38].INT_CF[5:5]	1
0xBB0151A4	ACL_ACTION [38].FWD[4:4]	1
0xBB0151A4	ACL_ACTION [38].POLICING[3:3]	1
0xBB0151A4	ACL_ACTION [38].PRI[2:2]	1
0xBB0151A4	ACL_ACTION [38].SVLAN[1:1]	1
0xBB0151A4	ACL_ACTION [38].CVLAN[0:0]	1
0xBB0151A8	ACL_ACTION [39].RESERVED[31:8]	24
0xBB0151A8	ACL_ACTION [39].VALID[7:7]	1
0xBB0151A8	ACL_ACTION [39].NOT[6:6]	1
0xBB0151A8	ACL_ACTION [39].INT_CF[5:5]	1
0xBB0151A8	ACL_ACTION [39].FWD[4:4]	1
0xBB0151A8	ACL_ACTION [39].POLICING[3:3]	1
0xBB0151A8	ACL_ACTION [39].PRI[2:2]	1
0xBB0151A8	ACL_ACTION [39].SVLAN[1:1]	1
0xBB0151A8	ACL_ACTION [39].CVLAN[0:0]	1
0xBB0151AC	ACL_ACTION [40].RESERVED[31:8]	24
0xBB0151AC	ACL_ACTION [40].VALID[7:7]	1
0xBB0151AC	ACL_ACTION [40].NOT[6:6]	1
0xBB0151AC	ACL_ACTION [40].INT_CF[5:5]	1
0xBB0151AC	ACL_ACTION [40].FWD[4:4]	1
0xBB0151AC	ACL_ACTION [40].POLICING[3:3]	1
0xBB0151AC	ACL_ACTION [40].PRI[2:2]	1
0xBB0151AC	ACL_ACTION [40].SVLAN[1:1]	1
0xBB0151AC	ACL_ACTION [40].CVLAN[0:0]	1
0xBB0151B0	ACL_ACTION [41].RESERVED[31:8]	24
0xBB0151B0	ACL_ACTION [41].VALID[7:7]	1
0xBB0151B0	ACL_ACTION [41].NOT[6:6]	1
0xBB0151B0	ACL_ACTION [41].INT_CF[5:5]	1

Address	Register	Len
0xBB0151B0	ACL_ACTION [41].FWD[4:4]	1
0xBB0151B0	ACL_ACTION [41].POLICING[3:3]	1
0xBB0151B0	ACL_ACTION [41].PRI[2:2]	1
0xBB0151B0	ACL_ACTION [41].SVLAN[1:1]	1
0xBB0151B0	ACL_ACTION [41].CVLAN[0:0]	1
0xBB0151B4	ACL_ACTION [42].RESERVED[31:8]	24
0xBB0151B4	ACL_ACTION [42].VALID[7:7]	1
0xBB0151B4	ACL_ACTION [42].NOT[6:6]	1
0xBB0151B4	ACL_ACTION [42].INT_CF[5:5]	1
0xBB0151B4	ACL_ACTION [42].FWD[4:4]	1
0xBB0151B4	ACL_ACTION [42].POLICING[3:3]	1
0xBB0151B4	ACL_ACTION [42].PRI[2:2]	1
0xBB0151B4	ACL_ACTION [42].SVLAN[1:1]	1
0xBB0151B4	ACL_ACTION [42].CVLAN[0:0]	1
0xBB0151B8	ACL_ACTION [43].RESERVED[31:8]	24
0xBB0151B8	ACL_ACTION [43].VALID[7:7]	1
0xBB0151B8	ACL_ACTION [43].NOT[6:6]	1
0xBB0151B8	ACL_ACTION [43].INT_CF[5:5]	1
0xBB0151B8	ACL_ACTION [43].FWD[4:4]	1
0xBB0151B8	ACL_ACTION [43].POLICING[3:3]	1
0xBB0151B8	ACL_ACTION [43].PRI[2:2]	1
0xBB0151B8	ACL_ACTION [43].SVLAN[1:1]	1
0xBB0151B8	ACL_ACTION [43].CVLAN[0:0]	1
0xBB0151BC	ACL_ACTION [44].RESERVED[31:8]	24
0xBB0151BC	ACL_ACTION [44].VALID[7:7]	1
0xBB0151BC	ACL_ACTION [44].NOT[6:6]	1
0xBB0151BC	ACL_ACTION [44].INT_CF[5:5]	1
0xBB0151BC	ACL_ACTION [44].FWD[4:4]	1
0xBB0151BC	ACL_ACTION [44].POLICING[3:3]	1
0xBB0151BC	ACL_ACTION [44].PRI[2:2]	1
0xBB0151BC	ACL_ACTION [44].SVLAN[1:1]	1
0xBB0151BC	ACL_ACTION [44].CVLAN[0:0]	1
0xBB0151C0	ACL_ACTION [45].RESERVED[31:8]	24
0xBB0151C0	ACL_ACTION [45].VALID[7:7]	1
0xBB0151C0	ACL_ACTION [45].NOT[6:6]	1
0xBB0151C0	ACL_ACTION [45].INT_CF[5:5]	1
0xBB0151C0	ACL_ACTION [45].FWD[4:4]	1
0xBB0151C0	ACL_ACTION [45].POLICING[3:3]	1
0xBB0151C0	ACL_ACTION [45].PRI[2:2]	1
0xBB0151C0	ACL_ACTION [45].SVLAN[1:1]	1
0xBB0151C0	ACL_ACTION [45].CVLAN[0:0]	1
0xBB0151C4	ACL_ACTION [46].RESERVED[31:8]	24
0xBB0151C4	ACL_ACTION [46].VALID[7:7]	1
0xBB0151C4	ACL_ACTION [46].NOT[6:6]	1
0xBB0151C4	ACL_ACTION [46].INT_CF[5:5]	1
0xBB0151C4	ACL_ACTION [46].FWD[4:4]	1

Address	Register	Len
0xBB0151C4	ACL_ACTION [46].POLICING[3:3]	1
0xBB0151C4	ACL_ACTION [46].PRI[2:2]	1
0xBB0151C4	ACL_ACTION [46].SVLAN[1:1]	1
0xBB0151C4	ACL_ACTION [46].CVLAN[0:0]	1
0xBB0151C8	ACL_ACTION [47].RESERVED[31:8]	24
0xBB0151C8	ACL_ACTION [47].VALID[7:7]	1
0xBB0151C8	ACL_ACTION [47].NOT[6:6]	1
0xBB0151C8	ACL_ACTION [47].INT_CF[5:5]	1
0xBB0151C8	ACL_ACTION [47].FWD[4:4]	1
0xBB0151C8	ACL_ACTION [47].POLICING[3:3]	1
0xBB0151C8	ACL_ACTION [47].PRI[2:2]	1
0xBB0151C8	ACL_ACTION [47].SVLAN[1:1]	1
0xBB0151C8	ACL_ACTION [47].CVLAN[0:0]	1
0xBB0151CC	ACL_ACTION [48].RESERVED[31:8]	24
0xBB0151CC	ACL_ACTION [48].VALID[7:7]	1
0xBB0151CC	ACL_ACTION [48].NOT[6:6]	1
0xBB0151CC	ACL_ACTION [48].INT_CF[5:5]	1
0xBB0151CC	ACL_ACTION [48].FWD[4:4]	1
0xBB0151CC	ACL_ACTION [48].POLICING[3:3]	1
0xBB0151CC	ACL_ACTION [48].PRI[2:2]	1
0xBB0151CC	ACL_ACTION [48].SVLAN[1:1]	1
0xBB0151CC	ACL_ACTION [48].CVLAN[0:0]	1
0xBB0151D0	ACL_ACTION [49].RESERVED[31:8]	24
0xBB0151D0	ACL_ACTION [49].VALID[7:7]	1
0xBB0151D0	ACL_ACTION [49].NOT[6:6]	1
0xBB0151D0	ACL_ACTION [49].INT_CF[5:5]	1
0xBB0151D0	ACL_ACTION [49].FWD[4:4]	1
0xBB0151D0	ACL_ACTION [49].POLICING[3:3]	1
0xBB0151D0	ACL_ACTION [49].PRI[2:2]	1
0xBB0151D0	ACL_ACTION [49].SVLAN[1:1]	1
0xBB0151D0	ACL_ACTION [49].CVLAN[0:0]	1
0xBB0151D4	ACL_ACTION [50].RESERVED[31:8]	24
0xBB0151D4	ACL_ACTION [50].VALID[7:7]	1
0xBB0151D4	ACL_ACTION [50].NOT[6:6]	1
0xBB0151D4	ACL_ACTION [50].INT_CF[5:5]	1
0xBB0151D4	ACL_ACTION [50].FWD[4:4]	1
0xBB0151D4	ACL_ACTION [50].POLICING[3:3]	1
0xBB0151D4	ACL_ACTION [50].PRI[2:2]	1
0xBB0151D4	ACL_ACTION [50].SVLAN[1:1]	1
0xBB0151D4	ACL_ACTION [50].CVLAN[0:0]	1
0xBB0151D8	ACL_ACTION [51].RESERVED[31:8]	24
0xBB0151D8	ACL_ACTION [51].VALID[7:7]	1
0xBB0151D8	ACL_ACTION [51].NOT[6:6]	1
0xBB0151D8	ACL_ACTION [51].INT_CF[5:5]	1
0xBB0151D8	ACL_ACTION [51].FWD[4:4]	1
0xBB0151D8	ACL_ACTION [51].POLICING[3:3]	1

Address	Register	Len
0xBB0151D8	ACL_ACTION [51].PRI[2:2]	1
0xBB0151D8	ACL_ACTION [51].SVLAN[1:1]	1
0xBB0151D8	ACL_ACTION [51].CVLAN[0:0]	1
0xBB0151DC	ACL_ACTION [52].RESERVED[31:8]	24
0xBB0151DC	ACL_ACTION [52].VALID[7:7]	1
0xBB0151DC	ACL_ACTION [52].NOT[6:6]	1
0xBB0151DC	ACL_ACTION [52].INT_CF[5:5]	1
0xBB0151DC	ACL_ACTION [52].FWD[4:4]	1
0xBB0151DC	ACL_ACTION [52].POLICING[3:3]	1
0xBB0151DC	ACL_ACTION [52].PRI[2:2]	1
0xBB0151DC	ACL_ACTION [52].SVLAN[1:1]	1
0xBB0151DC	ACL_ACTION [52].CVLAN[0:0]	1
0xBB0151E0	ACL_ACTION [53].RESERVED[31:8]	24
0xBB0151E0	ACL_ACTION [53].VALID[7:7]	1
0xBB0151E0	ACL_ACTION [53].NOT[6:6]	1
0xBB0151E0	ACL_ACTION [53].INT_CF[5:5]	1
0xBB0151E0	ACL_ACTION [53].FWD[4:4]	1
0xBB0151E0	ACL_ACTION [53].POLICING[3:3]	1
0xBB0151E0	ACL_ACTION [53].PRI[2:2]	1
0xBB0151E0	ACL_ACTION [53].SVLAN[1:1]	1
0xBB0151E0	ACL_ACTION [53].CVLAN[0:0]	1
0xBB0151E4	ACL_ACTION [54].RESERVED[31:8]	24
0xBB0151E4	ACL_ACTION [54].VALID[7:7]	1
0xBB0151E4	ACL_ACTION [54].NOT[6:6]	1
0xBB0151E4	ACL_ACTION [54].INT_CF[5:5]	1
0xBB0151E4	ACL_ACTION [54].FWD[4:4]	1
0xBB0151E4	ACL_ACTION [54].POLICING[3:3]	1
0xBB0151E4	ACL_ACTION [54].PRI[2:2]	1
0xBB0151E4	ACL_ACTION [54].SVLAN[1:1]	1
0xBB0151E4	ACL_ACTION [54].CVLAN[0:0]	1
0xBB0151E8	ACL_ACTION [55].RESERVED[31:8]	24
0xBB0151E8	ACL_ACTION [55].VALID[7:7]	1
0xBB0151E8	ACL_ACTION [55].NOT[6:6]	1
0xBB0151E8	ACL_ACTION [55].INT_CF[5:5]	1
0xBB0151E8	ACL_ACTION [55].FWD[4:4]	1
0xBB0151E8	ACL_ACTION [55].POLICING[3:3]	1
0xBB0151E8	ACL_ACTION [55].PRI[2:2]	1
0xBB0151E8	ACL_ACTION [55].SVLAN[1:1]	1
0xBB0151E8	ACL_ACTION [55].CVLAN[0:0]	1
0xBB0151EC	ACL_ACTION [56].RESERVED[31:8]	24
0xBB0151EC	ACL_ACTION [56].VALID[7:7]	1
0xBB0151EC	ACL_ACTION [56].NOT[6:6]	1
0xBB0151EC	ACL_ACTION [56].INT_CF[5:5]	1
0xBB0151EC	ACL_ACTION [56].FWD[4:4]	1
0xBB0151EC	ACL_ACTION [56].POLICING[3:3]	1
0xBB0151EC	ACL_ACTION [56].PRI[2:2]	1

Address	Register	Len
0xBB0151EC	ACL_ACTION [56].SVLAN[1:1]	1
0xBB0151EC	ACL_ACTION [56].CVLAN[0:0]	1
0xBB0151F0	ACL_ACTION [57].RESERVED[31:8]	24
0xBB0151F0	ACL_ACTION [57].VALID[7:7]	1
0xBB0151F0	ACL_ACTION [57].NOT[6:6]	1
0xBB0151F0	ACL_ACTION [57].INT_CF[5:5]	1
0xBB0151F0	ACL_ACTION [57].FWD[4:4]	1
0xBB0151F0	ACL_ACTION [57].POLICING[3:3]	1
0xBB0151F0	ACL_ACTION [57].PRI[2:2]	1
0xBB0151F0	ACL_ACTION [57].SVLAN[1:1]	1
0xBB0151F0	ACL_ACTION [57].CVLAN[0:0]	1
0xBB0151F4	ACL_ACTION [58].RESERVED[31:8]	24
0xBB0151F4	ACL_ACTION [58].VALID[7:7]	1
0xBB0151F4	ACL_ACTION [58].NOT[6:6]	1
0xBB0151F4	ACL_ACTION [58].INT_CF[5:5]	1
0xBB0151F4	ACL_ACTION [58].FWD[4:4]	1
0xBB0151F4	ACL_ACTION [58].POLICING[3:3]	1
0xBB0151F4	ACL_ACTION [58].PRI[2:2]	1
0xBB0151F4	ACL_ACTION [58].SVLAN[1:1]	1
0xBB0151F4	ACL_ACTION [58].CVLAN[0:0]	1
0xBB0151F8	ACL_ACTION [59].RESERVED[31:8]	24
0xBB0151F8	ACL_ACTION [59].VALID[7:7]	1
0xBB0151F8	ACL_ACTION [59].NOT[6:6]	1
0xBB0151F8	ACL_ACTION [59].INT_CF[5:5]	1
0xBB0151F8	ACL_ACTION [59].FWD[4:4]	1
0xBB0151F8	ACL_ACTION [59].POLICING[3:3]	1
0xBB0151F8	ACL_ACTION [59].PRI[2:2]	1
0xBB0151F8	ACL_ACTION [59].SVLAN[1:1]	1
0xBB0151F8	ACL_ACTION [59].CVLAN[0:0]	1
0xBB0151FC	ACL_ACTION [60].RESERVED[31:8]	24
0xBB0151FC	ACL_ACTION [60].VALID[7:7]	1
0xBB0151FC	ACL_ACTION [60].NOT[6:6]	1
0xBB0151FC	ACL_ACTION [60].INT_CF[5:5]	1
0xBB0151FC	ACL_ACTION [60].FWD[4:4]	1
0xBB0151FC	ACL_ACTION [60].POLICING[3:3]	1
0xBB0151FC	ACL_ACTION [60].PRI[2:2]	1
0xBB0151FC	ACL_ACTION [60].SVLAN[1:1]	1
0xBB0151FC	ACL_ACTION [60].CVLAN[0:0]	1
0xBB015200	ACL_ACTION [61].RESERVED[31:8]	24
0xBB015200	ACL_ACTION [61].VALID[7:7]	1
0xBB015200	ACL_ACTION [61].NOT[6:6]	1
0xBB015200	ACL_ACTION [61].INT_CF[5:5]	1
0xBB015200	ACL_ACTION [61].FWD[4:4]	1
0xBB015200	ACL_ACTION [61].POLICING[3:3]	1
0xBB015200	ACL_ACTION [61].PRI[2:2]	1
0xBB015200	ACL_ACTION [61].SVLAN[1:1]	1



Address	Register	Len
0xBB015200	ACL_ACTION [61].CVLAN[0:0]	1
0xBB015204	ACL_ACTION [62].RESERVED[31:8]	24
0xBB015204	ACL_ACTION [62].VALID[7:7]	1
0xBB015204	ACL_ACTION [62].NOT[6:6]	1
0xBB015204	ACL_ACTION [62].INT_CF[5:5]	1
0xBB015204	ACL_ACTION [62].FWD[4:4]	1
0xBB015204	ACL_ACTION [62].POLICING[3:3]	1
0xBB015204	ACL_ACTION [62].PRI[2:2]	1
0xBB015204	ACL_ACTION [62].SVLAN[1:1]	1
0xBB015204	ACL_ACTION [62].CVLAN[0:0]	1
0xBB015208	ACL_ACTION [63].RESERVED[31:8]	24
0xBB015208	ACL_ACTION [63].VALID[7:7]	1
0xBB015208	ACL_ACTION [63].NOT[6:6]	1
0xBB015208	ACL_ACTION [63].INT_CF[5:5]	1
0xBB015208	ACL_ACTION [63].FWD[4:4]	1
0xBB015208	ACL_ACTION [63].POLICING[3:3]	1
0xBB015208	ACL_ACTION [63].PRI[2:2]	1
0xBB015208	ACL_ACTION [63].SVLAN[1:1]	1
0xBB015208	ACL_ACTION [63].CVLAN[0:0]	1
0xBB01520C	ACL_ACTION [64].RESERVED[31:8]	24
0xBB01520C	ACL_ACTION [64].VALID[7:7]	1
0xBB01520C	ACL_ACTION [64].NOT[6:6]	1
0xBB01520C	ACL_ACTION [64].INT_CF[5:5]	1
0xBB01520C	ACL_ACTION [64].FWD[4:4]	1
0xBB01520C	ACL_ACTION [64].POLICING[3:3]	1
0xBB01520C	ACL_ACTION [64].PRI[2:2]	1
0xBB01520C	ACL_ACTION [64].SVLAN[1:1]	1
0xBB01520C	ACL_ACTION [64].CVLAN[0:0]	1
0xBB015210	ACL_ACTION [65].RESERVED[31:8]	24
0xBB015210	ACL_ACTION [65].VALID[7:7]	1
0xBB015210	ACL_ACTION [65].NOT[6:6]	1
0xBB015210	ACL_ACTION [65].INT_CF[5:5]	1
0xBB015210	ACL_ACTION [65].FWD[4:4]	1
0xBB015210	ACL_ACTION [65].POLICING[3:3]	1
0xBB015210	ACL_ACTION [65].PRI[2:2]	1
0xBB015210	ACL_ACTION [65].SVLAN[1:1]	1
0xBB015210	ACL_ACTION [65].CVLAN[0:0]	1
0xBB015214	ACL_ACTION [66].RESERVED[31:8]	24
0xBB015214	ACL_ACTION [66].VALID[7:7]	1
0xBB015214	ACL_ACTION [66].NOT[6:6]	1
0xBB015214	ACL_ACTION [66].INT_CF[5:5]	1
0xBB015214	ACL_ACTION [66].FWD[4:4]	1
0xBB015214	ACL_ACTION [66].POLICING[3:3]	1
0xBB015214	ACL_ACTION [66].PRI[2:2]	1
0xBB015214	ACL_ACTION [66].SVLAN[1:1]	1
0xBB015214	ACL_ACTION [66].CVLAN[0:0]	1

Address	Register	Len
0xBB015218	ACL_ACTION [67].RESERVED[31:8]	24
0xBB015218	ACL_ACTION [67].VALID[7:7]	1
0xBB015218	ACL_ACTION [67].NOT[6:6]	1
0xBB015218	ACL_ACTION [67].INT_CF[5:5]	1
0xBB015218	ACL_ACTION [67].FWD[4:4]	1
0xBB015218	ACL_ACTION [67].POLICING[3:3]	1
0xBB015218	ACL_ACTION [67].PRI[2:2]	1
0xBB015218	ACL_ACTION [67].SVLAN[1:1]	1
0xBB015218	ACL_ACTION [67].CVLAN[0:0]	1
0xBB01521C	ACL_ACTION [68].RESERVED[31:8]	24
0xBB01521C	ACL_ACTION [68].VALID[7:7]	1
0xBB01521C	ACL_ACTION [68].NOT[6:6]	1
0xBB01521C	ACL_ACTION [68].INT_CF[5:5]	1
0xBB01521C	ACL_ACTION [68].FWD[4:4]	1
0xBB01521C	ACL_ACTION [68].POLICING[3:3]	1
0xBB01521C	ACL_ACTION [68].PRI[2:2]	1
0xBB01521C	ACL_ACTION [68].SVLAN[1:1]	1
0xBB01521C	ACL_ACTION [68].CVLAN[0:0]	1
0xBB015220	ACL_ACTION [69].RESERVED[31:8]	24
0xBB015220	ACL_ACTION [69].VALID[7:7]	1
0xBB015220	ACL_ACTION [69].NOT[6:6]	1
0xBB015220	ACL_ACTION [69].INT_CF[5:5]	1
0xBB015220	ACL_ACTION [69].FWD[4:4]	1
0xBB015220	ACL_ACTION [69].POLICING[3:3]	1
0xBB015220	ACL_ACTION [69].PRI[2:2]	1
0xBB015220	ACL_ACTION [69].SVLAN[1:1]	1
0xBB015220	ACL_ACTION [69].CVLAN[0:0]	1
0xBB015224	ACL_ACTION [70].RESERVED[31:8]	24
0xBB015224	ACL_ACTION [70].VALID[7:7]	1
0xBB015224	ACL_ACTION [70].NOT[6:6]	1
0xBB015224	ACL_ACTION [70].INT_CF[5:5]	1
0xBB015224	ACL_ACTION [70].FWD[4:4]	1
0xBB015224	ACL_ACTION [70].POLICING[3:3]	1
0xBB015224	ACL_ACTION [70].PRI[2:2]	1
0xBB015224	ACL_ACTION [70].SVLAN[1:1]	1
0xBB015224	ACL_ACTION [70].CVLAN[0:0]	1
0xBB015228	ACL_ACTION [71].RESERVED[31:8]	24
0xBB015228	ACL_ACTION [71].VALID[7:7]	1
0xBB015228	ACL_ACTION [71].NOT[6:6]	1
0xBB015228	ACL_ACTION [71].INT_CF[5:5]	1
0xBB015228	ACL_ACTION [71].FWD[4:4]	1
0xBB015228	ACL_ACTION [71].POLICING[3:3]	1
0xBB015228	ACL_ACTION [71].PRI[2:2]	1
0xBB015228	ACL_ACTION [71].SVLAN[1:1]	1
0xBB015228	ACL_ACTION [71].CVLAN[0:0]	1
0xBB01522C	ACL_ACTION [72].RESERVED[31:8]	24

Address	Register	Len
0xBB01522C	ACL_ACTION [72].VALID[7:7]	1
0xBB01522C	ACL_ACTION [72].NOT[6:6]	1
0xBB01522C	ACL_ACTION [72].INT_CF[5:5]	1
0xBB01522C	ACL_ACTION [72].FWD[4:4]	1
0xBB01522C	ACL_ACTION [72].POLICING[3:3]	1
0xBB01522C	ACL_ACTION [72].PRI[2:2]	1
0xBB01522C	ACL_ACTION [72].SVLAN[1:1]	1
0xBB01522C	ACL_ACTION [72].CVLAN[0:0]	1
0xBB015230	ACL_ACTION [73].RESERVED[31:8]	24
0xBB015230	ACL_ACTION [73].VALID[7:7]	1
0xBB015230	ACL_ACTION [73].NOT[6:6]	1
0xBB015230	ACL_ACTION [73].INT_CF[5:5]	1
0xBB015230	ACL_ACTION [73].FWD[4:4]	1
0xBB015230	ACL_ACTION [73].POLICING[3:3]	1
0xBB015230	ACL_ACTION [73].PRI[2:2]	1
0xBB015230	ACL_ACTION [73].SVLAN[1:1]	1
0xBB015230	ACL_ACTION [73].CVLAN[0:0]	1
0xBB015234	ACL_ACTION [74].RESERVED[31:8]	24
0xBB015234	ACL_ACTION [74].VALID[7:7]	1
0xBB015234	ACL_ACTION [74].NOT[6:6]	1
0xBB015234	ACL_ACTION [74].INT_CF[5:5]	1
0xBB015234	ACL_ACTION [74].FWD[4:4]	1
0xBB015234	ACL_ACTION [74].POLICING[3:3]	1
0xBB015234	ACL_ACTION [74].PRI[2:2]	1
0xBB015234	ACL_ACTION [74].SVLAN[1:1]	1
0xBB015234	ACL_ACTION [74].CVLAN[0:0]	1
0xBB015238	ACL_ACTION [75].RESERVED[31:8]	24
0xBB015238	ACL_ACTION [75].VALID[7:7]	1
0xBB015238	ACL_ACTION [75].NOT[6:6]	1
0xBB015238	ACL_ACTION [75].INT_CF[5:5]	1
0xBB015238	ACL_ACTION [75].FWD[4:4]	1
0xBB015238	ACL_ACTION [75].POLICING[3:3]	1
0xBB015238	ACL_ACTION [75].PRI[2:2]	1
0xBB015238	ACL_ACTION [75].SVLAN[1:1]	1
0xBB015238	ACL_ACTION [75].CVLAN[0:0]	1
0xBB01523C	ACL_ACTION [76].RESERVED[31:8]	24
0xBB01523C	ACL_ACTION [76].VALID[7:7]	1
0xBB01523C	ACL_ACTION [76].NOT[6:6]	1
0xBB01523C	ACL_ACTION [76].INT_CF[5:5]	1
0xBB01523C	ACL_ACTION [76].FWD[4:4]	1
0xBB01523C	ACL_ACTION [76].POLICING[3:3]	1
0xBB01523C	ACL_ACTION [76].PRI[2:2]	1
0xBB01523C	ACL_ACTION [76].SVLAN[1:1]	1
0xBB01523C	ACL_ACTION [76].CVLAN[0:0]	1
0xBB015240	ACL_ACTION [77].RESERVED[31:8]	24
0xBB015240	ACL_ACTION [77].VALID[7:7]	1

Address	Register	Len
0xBB015240	ACL_ACTION [77].NOT[6:6]	1
0xBB015240	ACL_ACTION [77].INT_CF[5:5]	1
0xBB015240	ACL_ACTION [77].FWD[4:4]	1
0xBB015240	ACL_ACTION [77].POLICING[3:3]	1
0xBB015240	ACL_ACTION [77].PRI[2:2]	1
0xBB015240	ACL_ACTION [77].SVLAN[1:1]	1
0xBB015240	ACL_ACTION [77].CVLAN[0:0]	1
0xBB015244	ACL_ACTION [78].RESERVED[31:8]	24
0xBB015244	ACL_ACTION [78].VALID[7:7]	1
0xBB015244	ACL_ACTION [78].NOT[6:6]	1
0xBB015244	ACL_ACTION [78].INT_CF[5:5]	1
0xBB015244	ACL_ACTION [78].FWD[4:4]	1
0xBB015244	ACL_ACTION [78].POLICING[3:3]	1
0xBB015244	ACL_ACTION [78].PRI[2:2]	1
0xBB015244	ACL_ACTION [78].SVLAN[1:1]	1
0xBB015244	ACL_ACTION [78].CVLAN[0:0]	1
0xBB015248	ACL_ACTION [79].RESERVED[31:8]	24
0xBB015248	ACL_ACTION [79].VALID[7:7]	1
0xBB015248	ACL_ACTION [79].NOT[6:6]	1
0xBB015248	ACL_ACTION [79].INT_CF[5:5]	1
0xBB015248	ACL_ACTION [79].FWD[4:4]	1
0xBB015248	ACL_ACTION [79].POLICING[3:3]	1
0xBB015248	ACL_ACTION [79].PRI[2:2]	1
0xBB015248	ACL_ACTION [79].SVLAN[1:1]	1
0xBB015248	ACL_ACTION [79].CVLAN[0:0]	1
0xBB01524C	ACL_ACTION [80].RESERVED[31:8]	24
0xBB01524C	ACL_ACTION [80].VALID[7:7]	1
0xBB01524C	ACL_ACTION [80].NOT[6:6]	1
0xBB01524C	ACL_ACTION [80].INT_CF[5:5]	1
0xBB01524C	ACL_ACTION [80].FWD[4:4]	1
0xBB01524C	ACL_ACTION [80].POLICING[3:3]	1
0xBB01524C	ACL_ACTION [80].PRI[2:2]	1
0xBB01524C	ACL_ACTION [80].SVLAN[1:1]	1
0xBB01524C	ACL_ACTION [80].CVLAN[0:0]	1
0xBB015250	ACL_ACTION [81].RESERVED[31:8]	24
0xBB015250	ACL_ACTION [81].VALID[7:7]	1
0xBB015250	ACL_ACTION [81].NOT[6:6]	1
0xBB015250	ACL_ACTION [81].INT_CF[5:5]	1
0xBB015250	ACL_ACTION [81].FWD[4:4]	1
0xBB015250	ACL_ACTION [81].POLICING[3:3]	1
0xBB015250	ACL_ACTION [81].PRI[2:2]	1
0xBB015250	ACL_ACTION [81].SVLAN[1:1]	1
0xBB015250	ACL_ACTION [81].CVLAN[0:0]	1
0xBB015254	ACL_ACTION [82].RESERVED[31:8]	24
0xBB015254	ACL_ACTION [82].VALID[7:7]	1
0xBB015254	ACL_ACTION [82].NOT[6:6]	1

Address	Register	Len
0xBB015254	ACL_ACTION [82].INT_CF[5:5]	1
0xBB015254	ACL_ACTION [82].FWD[4:4]	1
0xBB015254	ACL_ACTION [82].POLICING[3:3]	1
0xBB015254	ACL_ACTION [82].PRI[2:2]	1
0xBB015254	ACL_ACTION [82].SVLAN[1:1]	1
0xBB015254	ACL_ACTION [82].CVLAN[0:0]	1
0xBB015258	ACL_ACTION [83].RESERVED[31:8]	24
0xBB015258	ACL_ACTION [83].VALID[7:7]	1
0xBB015258	ACL_ACTION [83].NOT[6:6]	1
0xBB015258	ACL_ACTION [83].INT_CF[5:5]	1
0xBB015258	ACL_ACTION [83].FWD[4:4]	1
0xBB015258	ACL_ACTION [83].POLICING[3:3]	1
0xBB015258	ACL_ACTION [83].PRI[2:2]	1
0xBB015258	ACL_ACTION [83].SVLAN[1:1]	1
0xBB015258	ACL_ACTION [83].CVLAN[0:0]	1
0xBB01525C	ACL_ACTION [84].RESERVED[31:8]	24
0xBB01525C	ACL_ACTION [84].VALID[7:7]	1
0xBB01525C	ACL_ACTION [84].NOT[6:6]	1
0xBB01525C	ACL_ACTION [84].INT_CF[5:5]	1
0xBB01525C	ACL_ACTION [84].FWD[4:4]	1
0xBB01525C	ACL_ACTION [84].POLICING[3:3]	1
0xBB01525C	ACL_ACTION [84].PRI[2:2]	1
0xBB01525C	ACL_ACTION [84].SVLAN[1:1]	1
0xBB01525C	ACL_ACTION [84].CVLAN[0:0]	1
0xBB015260	ACL_ACTION [85].RESERVED[31:8]	24
0xBB015260	ACL_ACTION [85].VALID[7:7]	1
0xBB015260	ACL_ACTION [85].NOT[6:6]	1
0xBB015260	ACL_ACTION [85].INT_CF[5:5]	1
0xBB015260	ACL_ACTION [85].FWD[4:4]	1
0xBB015260	ACL_ACTION [85].POLICING[3:3]	1
0xBB015260	ACL_ACTION [85].PRI[2:2]	1
0xBB015260	ACL_ACTION [85].SVLAN[1:1]	1
0xBB015260	ACL_ACTION [85].CVLAN[0:0]	1
0xBB015264	ACL_ACTION [86].RESERVED[31:8]	24
0xBB015264	ACL_ACTION [86].VALID[7:7]	1
0xBB015264	ACL_ACTION [86].NOT[6:6]	1
0xBB015264	ACL_ACTION [86].INT_CF[5:5]	1
0xBB015264	ACL_ACTION [86].FWD[4:4]	1
0xBB015264	ACL_ACTION [86].POLICING[3:3]	1
0xBB015264	ACL_ACTION [86].PRI[2:2]	1
0xBB015264	ACL_ACTION [86].SVLAN[1:1]	1
0xBB015264	ACL_ACTION [86].CVLAN[0:0]	1
0xBB015268	ACL_ACTION [87].RESERVED[31:8]	24
0xBB015268	ACL_ACTION [87].VALID[7:7]	1
0xBB015268	ACL_ACTION [87].NOT[6:6]	1
0xBB015268	ACL_ACTION [87].INT_CF[5:5]	1

Address	Register	Len
0xBB015268	ACL_ACTION [87].FWD[4:4]	1
0xBB015268	ACL_ACTION [87].POLICING[3:3]	1
0xBB015268	ACL_ACTION [87].PRI[2:2]	1
0xBB015268	ACL_ACTION [87].SVLAN[1:1]	1
0xBB015268	ACL_ACTION [87].CVLAN[0:0]	1
0xBB01526C	ACL_ACTION [88].RESERVED[31:8]	24
0xBB01526C	ACL_ACTION [88].VALID[7:7]	1
0xBB01526C	ACL_ACTION [88].NOT[6:6]	1
0xBB01526C	ACL_ACTION [88].INT_CF[5:5]	1
0xBB01526C	ACL_ACTION [88].FWD[4:4]	1
0xBB01526C	ACL_ACTION [88].POLICING[3:3]	1
0xBB01526C	ACL_ACTION [88].PRI[2:2]	1
0xBB01526C	ACL_ACTION [88].SVLAN[1:1]	1
0xBB01526C	ACL_ACTION [88].CVLAN[0:0]	1
0xBB015270	ACL_ACTION [89].RESERVED[31:8]	24
0xBB015270	ACL_ACTION [89].VALID[7:7]	1
0xBB015270	ACL_ACTION [89].NOT[6:6]	1
0xBB015270	ACL_ACTION [89].INT_CF[5:5]	1
0xBB015270	ACL_ACTION [89].FWD[4:4]	1
0xBB015270	ACL_ACTION [89].POLICING[3:3]	1
0xBB015270	ACL_ACTION [89].PRI[2:2]	1
0xBB015270	ACL_ACTION [89].SVLAN[1:1]	1
0xBB015270	ACL_ACTION [89].CVLAN[0:0]	1
0xBB015274	ACL_ACTION [90].RESERVED[31:8]	24
0xBB015274	ACL_ACTION [90].VALID[7:7]	1
0xBB015274	ACL_ACTION [90].NOT[6:6]	1
0xBB015274	ACL_ACTION [90].INT_CF[5:5]	1
0xBB015274	ACL_ACTION [90].FWD[4:4]	1
0xBB015274	ACL_ACTION [90].POLICING[3:3]	1
0xBB015274	ACL_ACTION [90].PRI[2:2]	1
0xBB015274	ACL_ACTION [90].SVLAN[1:1]	1
0xBB015274	ACL_ACTION [90].CVLAN[0:0]	1
0xBB015278	ACL_ACTION [91].RESERVED[31:8]	24
0xBB015278	ACL_ACTION [91].VALID[7:7]	1
0xBB015278	ACL_ACTION [91].NOT[6:6]	1
0xBB015278	ACL_ACTION [91].INT_CF[5:5]	1
0xBB015278	ACL_ACTION [91].FWD[4:4]	1
0xBB015278	ACL_ACTION [91].POLICING[3:3]	1
0xBB015278	ACL_ACTION [91].PRI[2:2]	1
0xBB015278	ACL_ACTION [91].SVLAN[1:1]	1
0xBB015278	ACL_ACTION [91].CVLAN[0:0]	1
0xBB01527C	ACL_ACTION [92].RESERVED[31:8]	24
0xBB01527C	ACL_ACTION [92].VALID[7:7]	1
0xBB01527C	ACL_ACTION [92].NOT[6:6]	1
0xBB01527C	ACL_ACTION [92].INT_CF[5:5]	1
0xBB01527C	ACL_ACTION [92].FWD[4:4]	1

Address	Register	Len
0xBB01527C	ACL_ACTION [92].POLICING[3:3]	1
0xBB01527C	ACL_ACTION [92].PRI[2:2]	1
0xBB01527C	ACL_ACTION [92].SVLAN[1:1]	1
0xBB01527C	ACL_ACTION [92].CVLAN[0:0]	1
0xBB015280	ACL_ACTION [93].RESERVED[31:8]	24
0xBB015280	ACL_ACTION [93].VALID[7:7]	1
0xBB015280	ACL_ACTION [93].NOT[6:6]	1
0xBB015280	ACL_ACTION [93].INT_CF[5:5]	1
0xBB015280	ACL_ACTION [93].FWD[4:4]	1
0xBB015280	ACL_ACTION [93].POLICING[3:3]	1
0xBB015280	ACL_ACTION [93].PRI[2:2]	1
0xBB015280	ACL_ACTION [93].SVLAN[1:1]	1
0xBB015280	ACL_ACTION [93].CVLAN[0:0]	1
0xBB015284	ACL_ACTION [94].RESERVED[31:8]	24
0xBB015284	ACL_ACTION [94].VALID[7:7]	1
0xBB015284	ACL_ACTION [94].NOT[6:6]	1
0xBB015284	ACL_ACTION [94].INT_CF[5:5]	1
0xBB015284	ACL_ACTION [94].FWD[4:4]	1
0xBB015284	ACL_ACTION [94].POLICING[3:3]	1
0xBB015284	ACL_ACTION [94].PRI[2:2]	1
0xBB015284	ACL_ACTION [94].SVLAN[1:1]	1
0xBB015284	ACL_ACTION [94].CVLAN[0:0]	1
0xBB015288	ACL_ACTION [95].RESERVED[31:8]	24
0xBB015288	ACL_ACTION [95].VALID[7:7]	1
0xBB015288	ACL_ACTION [95].NOT[6:6]	1
0xBB015288	ACL_ACTION [95].INT_CF[5:5]	1
0xBB015288	ACL_ACTION [95].FWD[4:4]	1
0xBB015288	ACL_ACTION [95].POLICING[3:3]	1
0xBB015288	ACL_ACTION [95].PRI[2:2]	1
0xBB015288	ACL_ACTION [95].SVLAN[1:1]	1
0xBB015288	ACL_ACTION [95].CVLAN[0:0]	1
0xBB01528C	ACL_ACTION [96].RESERVED[31:8]	24
0xBB01528C	ACL_ACTION [96].VALID[7:7]	1
0xBB01528C	ACL_ACTION [96].NOT[6:6]	1
0xBB01528C	ACL_ACTION [96].INT_CF[5:5]	1
0xBB01528C	ACL_ACTION [96].FWD[4:4]	1
0xBB01528C	ACL_ACTION [96].POLICING[3:3]	1
0xBB01528C	ACL_ACTION [96].PRI[2:2]	1
0xBB01528C	ACL_ACTION [96].SVLAN[1:1]	1
0xBB01528C	ACL_ACTION [96].CVLAN[0:0]	1
0xBB015290	ACL_ACTION [97].RESERVED[31:8]	24
0xBB015290	ACL_ACTION [97].VALID[7:7]	1
0xBB015290	ACL_ACTION [97].NOT[6:6]	1
0xBB015290	ACL_ACTION [97].INT_CF[5:5]	1
0xBB015290	ACL_ACTION [97].FWD[4:4]	1
0xBB015290	ACL_ACTION [97].POLICING[3:3]	1

Address	Register	Len
0xBB015290	ACL_ACTION [97].PRI[2:2]	1
0xBB015290	ACL_ACTION [97].SVLAN[1:1]	1
0xBB015290	ACL_ACTION [97].CVLAN[0:0]	1
0xBB015294	ACL_ACTION [98].RESERVED[31:8]	24
0xBB015294	ACL_ACTION [98].VALID[7:7]	1
0xBB015294	ACL_ACTION [98].NOT[6:6]	1
0xBB015294	ACL_ACTION [98].INT_CF[5:5]	1
0xBB015294	ACL_ACTION [98].FWD[4:4]	1
0xBB015294	ACL_ACTION [98].POLICING[3:3]	1
0xBB015294	ACL_ACTION [98].PRI[2:2]	1
0xBB015294	ACL_ACTION [98].SVLAN[1:1]	1
0xBB015294	ACL_ACTION [98].CVLAN[0:0]	1
0xBB015298	ACL_ACTION [99].RESERVED[31:8]	24
0xBB015298	ACL_ACTION [99].VALID[7:7]	1
0xBB015298	ACL_ACTION [99].NOT[6:6]	1
0xBB015298	ACL_ACTION [99].INT_CF[5:5]	1
0xBB015298	ACL_ACTION [99].FWD[4:4]	1
0xBB015298	ACL_ACTION [99].POLICING[3:3]	1
0xBB015298	ACL_ACTION [99].PRI[2:2]	1
0xBB015298	ACL_ACTION [99].SVLAN[1:1]	1
0xBB015298	ACL_ACTION [99].CVLAN[0:0]	1
0xBB01529C	ACL_ACTION [100].RESERVED[31:8]	24
0xBB01529C	ACL_ACTION [100].VALID[7:7]	1
0xBB01529C	ACL_ACTION [100].NOT[6:6]	1
0xBB01529C	ACL_ACTION [100].INT_CF[5:5]	1
0xBB01529C	ACL_ACTION [100].FWD[4:4]	1
0xBB01529C	ACL_ACTION [100].POLICING[3:3]	1
0xBB01529C	ACL_ACTION [100].PRI[2:2]	1
0xBB01529C	ACL_ACTION [100].SVLAN[1:1]	1
0xBB01529C	ACL_ACTION [100].CVLAN[0:0]	1
0xBB0152A0	ACL_ACTION [101].RESERVED[31:8]	24
0xBB0152A0	ACL_ACTION [101].VALID[7:7]	1
0xBB0152A0	ACL_ACTION [101].NOT[6:6]	1
0xBB0152A0	ACL_ACTION [101].INT_CF[5:5]	1
0xBB0152A0	ACL_ACTION [101].FWD[4:4]	1
0xBB0152A0	ACL_ACTION [101].POLICING[3:3]	1
0xBB0152A0	ACL_ACTION [101].PRI[2:2]	1
0xBB0152A0	ACL_ACTION [101].SVLAN[1:1]	1
0xBB0152A0	ACL_ACTION [101].CVLAN[0:0]	1
0xBB0152A4	ACL_ACTION [102].RESERVED[31:8]	24
0xBB0152A4	ACL_ACTION [102].VALID[7:7]	1
0xBB0152A4	ACL_ACTION [102].NOT[6:6]	1
0xBB0152A4	ACL_ACTION [102].INT_CF[5:5]	1
0xBB0152A4	ACL_ACTION [102].FWD[4:4]	1
0xBB0152A4	ACL_ACTION [102].POLICING[3:3]	1
0xBB0152A4	ACL_ACTION [102].PRI[2:2]	1



Address	Register	Len
0xBB0152A4	ACL_ACTION [102].SVLAN[1:1]	1
0xBB0152A4	ACL_ACTION [102].CVLAN[0:0]	1
0xBB0152A8	ACL_ACTION [103].RESERVED[31:8]	24
0xBB0152A8	ACL_ACTION [103].VALID[7:7]	1
0xBB0152A8	ACL_ACTION [103].NOT[6:6]	1
0xBB0152A8	ACL_ACTION [103].INT_CF[5:5]	1
0xBB0152A8	ACL_ACTION [103].FWD[4:4]	1
0xBB0152A8	ACL_ACTION [103].POLICING[3:3]	1
0xBB0152A8	ACL_ACTION [103].PRI[2:2]	1
0xBB0152A8	ACL_ACTION [103].SVLAN[1:1]	1
0xBB0152A8	ACL_ACTION [103].CVLAN[0:0]	1
0xBB0152AC	ACL_ACTION [104].RESERVED[31:8]	24
0xBB0152AC	ACL_ACTION [104].VALID[7:7]	1
0xBB0152AC	ACL_ACTION [104].NOT[6:6]	1
0xBB0152AC	ACL_ACTION [104].INT_CF[5:5]	1
0xBB0152AC	ACL_ACTION [104].FWD[4:4]	1
0xBB0152AC	ACL_ACTION [104].POLICING[3:3]	1
0xBB0152AC	ACL_ACTION [104].PRI[2:2]	1
0xBB0152AC	ACL_ACTION [104].SVLAN[1:1]	1
0xBB0152AC	ACL_ACTION [104].CVLAN[0:0]	1
0xBB0152B0	ACL_ACTION [105].RESERVED[31:8]	24
0xBB0152B0	ACL_ACTION [105].VALID[7:7]	1
0xBB0152B0	ACL_ACTION [105].NOT[6:6]	1
0xBB0152B0	ACL_ACTION [105].INT_CF[5:5]	1
0xBB0152B0	ACL_ACTION [105].FWD[4:4]	1
0xBB0152B0	ACL_ACTION [105].POLICING[3:3]	1
0xBB0152B0	ACL_ACTION [105].PRI[2:2]	1
0xBB0152B0	ACL_ACTION [105].SVLAN[1:1]	1
0xBB0152B0	ACL_ACTION [105].CVLAN[0:0]	1
0xBB0152B4	ACL_ACTION [106].RESERVED[31:8]	24
0xBB0152B4	ACL_ACTION [106].VALID[7:7]	1
0xBB0152B4	ACL_ACTION [106].NOT[6:6]	1
0xBB0152B4	ACL_ACTION [106].INT_CF[5:5]	1
0xBB0152B4	ACL_ACTION [106].FWD[4:4]	1
0xBB0152B4	ACL_ACTION [106].POLICING[3:3]	1
0xBB0152B4	ACL_ACTION [106].PRI[2:2]	1
0xBB0152B4	ACL_ACTION [106].SVLAN[1:1]	1
0xBB0152B4	ACL_ACTION [106].CVLAN[0:0]	1
0xBB0152B8	ACL_ACTION [107].RESERVED[31:8]	24
0xBB0152B8	ACL_ACTION [107].VALID[7:7]	1
0xBB0152B8	ACL_ACTION [107].NOT[6:6]	1
0xBB0152B8	ACL_ACTION [107].INT_CF[5:5]	1
0xBB0152B8	ACL_ACTION [107].FWD[4:4]	1
0xBB0152B8	ACL_ACTION [107].POLICING[3:3]	1
0xBB0152B8	ACL_ACTION [107].PRI[2:2]	1
0xBB0152B8	ACL_ACTION [107].SVLAN[1:1]	1

Address	Register	Len
0xBB0152B8	ACL_ACTION [107].CVLAN[0:0]	1
0xBB0152BC	ACL_ACTION [108].RESERVED[31:8]	24
0xBB0152BC	ACL_ACTION [108].VALID[7:7]	1
0xBB0152BC	ACL_ACTION [108].NOT[6:6]	1
0xBB0152BC	ACL_ACTION [108].INT_CF[5:5]	1
0xBB0152BC	ACL_ACTION [108].FWD[4:4]	1
0xBB0152BC	ACL_ACTION [108].POLICING[3:3]	1
0xBB0152BC	ACL_ACTION [108].PRI[2:2]	1
0xBB0152BC	ACL_ACTION [108].SVLAN[1:1]	1
0xBB0152BC	ACL_ACTION [108].CVLAN[0:0]	1
0xBB0152C0	ACL_ACTION [109].RESERVED[31:8]	24
0xBB0152C0	ACL_ACTION [109].VALID[7:7]	1
0xBB0152C0	ACL_ACTION [109].NOT[6:6]	1
0xBB0152C0	ACL_ACTION [109].INT_CF[5:5]	1
0xBB0152C0	ACL_ACTION [109].FWD[4:4]	1
0xBB0152C0	ACL_ACTION [109].POLICING[3:3]	1
0xBB0152C0	ACL_ACTION [109].PRI[2:2]	1
0xBB0152C0	ACL_ACTION [109].SVLAN[1:1]	1
0xBB0152C0	ACL_ACTION [109].CVLAN[0:0]	1
0xBB0152C4	ACL_ACTION [110].RESERVED[31:8]	24
0xBB0152C4	ACL_ACTION [110].VALID[7:7]	1
0xBB0152C4	ACL_ACTION [110].NOT[6:6]	1
0xBB0152C4	ACL_ACTION [110].INT_CF[5:5]	1
0xBB0152C4	ACL_ACTION [110].FWD[4:4]	1
0xBB0152C4	ACL_ACTION [110].POLICING[3:3]	1
0xBB0152C4	ACL_ACTION [110].PRI[2:2]	1
0xBB0152C4	ACL_ACTION [110].SVLAN[1:1]	1
0xBB0152C4	ACL_ACTION [110].CVLAN[0:0]	1
0xBB0152C8	ACL_ACTION [111].RESERVED[31:8]	24
0xBB0152C8	ACL_ACTION [111].VALID[7:7]	1
0xBB0152C8	ACL_ACTION [111].NOT[6:6]	1
0xBB0152C8	ACL_ACTION [111].INT_CF[5:5]	1
0xBB0152C8	ACL_ACTION [111].FWD[4:4]	1
0xBB0152C8	ACL_ACTION [111].POLICING[3:3]	1
0xBB0152C8	ACL_ACTION [111].PRI[2:2]	1
0xBB0152C8	ACL_ACTION [111].SVLAN[1:1]	1
0xBB0152C8	ACL_ACTION [111].CVLAN[0:0]	1
0xBB0152CC	ACL_ACTION [112].RESERVED[31:8]	24
0xBB0152CC	ACL_ACTION [112].VALID[7:7]	1
0xBB0152CC	ACL_ACTION [112].NOT[6:6]	1
0xBB0152CC	ACL_ACTION [112].INT_CF[5:5]	1
0xBB0152CC	ACL_ACTION [112].FWD[4:4]	1
0xBB0152CC	ACL_ACTION [112].POLICING[3:3]	1
0xBB0152CC	ACL_ACTION [112].PRI[2:2]	1
0xBB0152CC	ACL_ACTION [112].SVLAN[1:1]	1
0xBB0152CC	ACL_ACTION [112].CVLAN[0:0]	1

Address	Register	Len
0xBB0152D0	ACL_ACTION [113].RESERVED[31:8]	24
0xBB0152D0	ACL_ACTION [113].VALID[7:7]	1
0xBB0152D0	ACL_ACTION [113].NOT[6:6]	1
0xBB0152D0	ACL_ACTION [113].INT_CF[5:5]	1
0xBB0152D0	ACL_ACTION [113].FWD[4:4]	1
0xBB0152D0	ACL_ACTION [113].POLICING[3:3]	1
0xBB0152D0	ACL_ACTION [113].PRI[2:2]	1
0xBB0152D0	ACL_ACTION [113].SVLAN[1:1]	1
0xBB0152D0	ACL_ACTION [113].CVLAN[0:0]	1
0xBB0152D4	ACL_ACTION [114].RESERVED[31:8]	24
0xBB0152D4	ACL_ACTION [114].VALID[7:7]	1
0xBB0152D4	ACL_ACTION [114].NOT[6:6]	1
0xBB0152D4	ACL_ACTION [114].INT_CF[5:5]	1
0xBB0152D4	ACL_ACTION [114].FWD[4:4]	1
0xBB0152D4	ACL_ACTION [114].POLICING[3:3]	1
0xBB0152D4	ACL_ACTION [114].PRI[2:2]	1
0xBB0152D4	ACL_ACTION [114].SVLAN[1:1]	1
0xBB0152D4	ACL_ACTION [114].CVLAN[0:0]	1
0xBB0152D8	ACL_ACTION [115].RESERVED[31:8]	24
0xBB0152D8	ACL_ACTION [115].VALID[7:7]	1
0xBB0152D8	ACL_ACTION [115].NOT[6:6]	1
0xBB0152D8	ACL_ACTION [115].INT_CF[5:5]	1
0xBB0152D8	ACL_ACTION [115].FWD[4:4]	1
0xBB0152D8	ACL_ACTION [115].POLICING[3:3]	1
0xBB0152D8	ACL_ACTION [115].PRI[2:2]	1
0xBB0152D8	ACL_ACTION [115].SVLAN[1:1]	1
0xBB0152D8	ACL_ACTION [115].CVLAN[0:0]	1
0xBB0152DC	ACL_ACTION [116].RESERVED[31:8]	24
0xBB0152DC	ACL_ACTION [116].VALID[7:7]	1
0xBB0152DC	ACL_ACTION [116].NOT[6:6]	1
0xBB0152DC	ACL_ACTION [116].INT_CF[5:5]	1
0xBB0152DC	ACL_ACTION [116].FWD[4:4]	1
0xBB0152DC	ACL_ACTION [116].POLICING[3:3]	1
0xBB0152DC	ACL_ACTION [116].PRI[2:2]	1
0xBB0152DC	ACL_ACTION [116].SVLAN[1:1]	1
0xBB0152DC	ACL_ACTION [116].CVLAN[0:0]	1
0xBB0152E0	ACL_ACTION [117].RESERVED[31:8]	24
0xBB0152E0	ACL_ACTION [117].VALID[7:7]	1
0xBB0152E0	ACL_ACTION [117].NOT[6:6]	1
0xBB0152E0	ACL_ACTION [117].INT_CF[5:5]	1
0xBB0152E0	ACL_ACTION [117].FWD[4:4]	1
0xBB0152E0	ACL_ACTION [117].POLICING[3:3]	1
0xBB0152E0	ACL_ACTION [117].PRI[2:2]	1
0xBB0152E0	ACL_ACTION [117].SVLAN[1:1]	1
0xBB0152E0	ACL_ACTION [117].CVLAN[0:0]	1
0xBB0152E4	ACL_ACTION [118].RESERVED[31:8]	24

Address	Register	Len
0xBB0152E4	ACL_ACTION [118].VALID[7:7]	1
0xBB0152E4	ACL_ACTION [118].NOT[6:6]	1
0xBB0152E4	ACL_ACTION [118].INT_CF[5:5]	1
0xBB0152E4	ACL_ACTION [118].FWD[4:4]	1
0xBB0152E4	ACL_ACTION [118].POLICING[3:3]	1
0xBB0152E4	ACL_ACTION [118].PRI[2:2]	1
0xBB0152E4	ACL_ACTION [118].SVLAN[1:1]	1
0xBB0152E4	ACL_ACTION [118].CVLAN[0:0]	1
0xBB0152E8	ACL_ACTION [119].RESERVED[31:8]	24
0xBB0152E8	ACL_ACTION [119].VALID[7:7]	1
0xBB0152E8	ACL_ACTION [119].NOT[6:6]	1
0xBB0152E8	ACL_ACTION [119].INT_CF[5:5]	1
0xBB0152E8	ACL_ACTION [119].FWD[4:4]	1
0xBB0152E8	ACL_ACTION [119].POLICING[3:3]	1
0xBB0152E8	ACL_ACTION [119].PRI[2:2]	1
0xBB0152E8	ACL_ACTION [119].SVLAN[1:1]	1
0xBB0152E8	ACL_ACTION [119].CVLAN[0:0]	1
0xBB0152EC	ACL_ACTION [120].RESERVED[31:8]	24
0xBB0152EC	ACL_ACTION [120].VALID[7:7]	1
0xBB0152EC	ACL_ACTION [120].NOT[6:6]	1
0xBB0152EC	ACL_ACTION [120].INT_CF[5:5]	1
0xBB0152EC	ACL_ACTION [120].FWD[4:4]	1
0xBB0152EC	ACL_ACTION [120].POLICING[3:3]	1
0xBB0152EC	ACL_ACTION [120].PRI[2:2]	1
0xBB0152EC	ACL_ACTION [120].SVLAN[1:1]	1
0xBB0152EC	ACL_ACTION [120].CVLAN[0:0]	1
0xBB0152F0	ACL_ACTION [121].RESERVED[31:8]	24
0xBB0152F0	ACL_ACTION [121].VALID[7:7]	1
0xBB0152F0	ACL_ACTION [121].NOT[6:6]	1
0xBB0152F0	ACL_ACTION [121].INT_CF[5:5]	1
0xBB0152F0	ACL_ACTION [121].FWD[4:4]	1
0xBB0152F0	ACL_ACTION [121].POLICING[3:3]	1
0xBB0152F0	ACL_ACTION [121].PRI[2:2]	1
0xBB0152F0	ACL_ACTION [121].SVLAN[1:1]	1
0xBB0152F0	ACL_ACTION [121].CVLAN[0:0]	1
0xBB0152F4	ACL_ACTION [122].RESERVED[31:8]	24
0xBB0152F4	ACL_ACTION [122].VALID[7:7]	1
0xBB0152F4	ACL_ACTION [122].NOT[6:6]	1
0xBB0152F4	ACL_ACTION [122].INT_CF[5:5]	1
0xBB0152F4	ACL_ACTION [122].FWD[4:4]	1
0xBB0152F4	ACL_ACTION [122].POLICING[3:3]	1
0xBB0152F4	ACL_ACTION [122].PRI[2:2]	1
0xBB0152F4	ACL_ACTION [122].SVLAN[1:1]	1
0xBB0152F4	ACL_ACTION [122].CVLAN[0:0]	1
0xBB0152F8	ACL_ACTION [123].RESERVED[31:8]	24
0xBB0152F8	ACL_ACTION [123].VALID[7:7]	1

Address	Register	Len
0xBB0152F8	ACL_ACTION [123].NOT[6:6]	1
0xBB0152F8	ACL_ACTION [123].INT_CF[5:5]	1
0xBB0152F8	ACL_ACTION [123].FWD[4:4]	1
0xBB0152F8	ACL_ACTION [123].POLICING[3:3]	1
0xBB0152F8	ACL_ACTION [123].PRI[2:2]	1
0xBB0152F8	ACL_ACTION [123].SVLAN[1:1]	1
0xBB0152F8	ACL_ACTION [123].CVLAN[0:0]	1
0xBB0152FC	ACL_ACTION [124].RESERVED[31:8]	24
0xBB0152FC	ACL_ACTION [124].VALID[7:7]	1
0xBB0152FC	ACL_ACTION [124].NOT[6:6]	1
0xBB0152FC	ACL_ACTION [124].INT_CF[5:5]	1
0xBB0152FC	ACL_ACTION [124].FWD[4:4]	1
0xBB0152FC	ACL_ACTION [124].POLICING[3:3]	1
0xBB0152FC	ACL_ACTION [124].PRI[2:2]	1
0xBB0152FC	ACL_ACTION [124].SVLAN[1:1]	1
0xBB0152FC	ACL_ACTION [124].CVLAN[0:0]	1
0xBB015300	ACL_ACTION [125].RESERVED[31:8]	24
0xBB015300	ACL_ACTION [125].VALID[7:7]	1
0xBB015300	ACL_ACTION [125].NOT[6:6]	1
0xBB015300	ACL_ACTION [125].INT_CF[5:5]	1
0xBB015300	ACL_ACTION [125].FWD[4:4]	1
0xBB015300	ACL_ACTION [125].POLICING[3:3]	1
0xBB015300	ACL_ACTION [125].PRI[2:2]	1
0xBB015300	ACL_ACTION [125].SVLAN[1:1]	1
0xBB015300	ACL_ACTION [125].CVLAN[0:0]	1
0xBB015304	ACL_ACTION [126].RESERVED[31:8]	24
0xBB015304	ACL_ACTION [126].VALID[7:7]	1
0xBB015304	ACL_ACTION [126].NOT[6:6]	1
0xBB015304	ACL_ACTION [126].INT_CF[5:5]	1
0xBB015304	ACL_ACTION [126].FWD[4:4]	1
0xBB015304	ACL_ACTION [126].POLICING[3:3]	1
0xBB015304	ACL_ACTION [126].PRI[2:2]	1
0xBB015304	ACL_ACTION [126].SVLAN[1:1]	1
0xBB015304	ACL_ACTION [126].CVLAN[0:0]	1
0xBB015308	ACL_ACTION [127].RESERVED[31:8]	24
0xBB015308	ACL_ACTION [127].VALID[7:7]	1
0xBB015308	ACL_ACTION [127].NOT[6:6]	1
0xBB015308	ACL_ACTION [127].INT_CF[5:5]	1
0xBB015308	ACL_ACTION [127].FWD[4:4]	1
0xBB015308	ACL_ACTION [127].POLICING[3:3]	1
0xBB015308	ACL_ACTION [127].PRI[2:2]	1
0xBB015308	ACL_ACTION [127].SVLAN[1:1]	1
0xBB015308	ACL_ACTION [127].CVLAN[0:0]	1
0xBB01530C	ACL_CFG.RESERVED[31:9]	23
0xBB01530C	ACL_CFG.CFHITLATCH[8:1]	8
0xBB01530C	ACL_CFG.MODE[0:0]	1

Address	Register	Len
0xBB015310	RNG_CHK_VID_RNG [0].RESERVED[31:26]	6
0xBB015310	RNG_CHK_VID_RNG [0].TYPE[25:24]	2
0xBB015310	RNG_CHK_VID_RNG [0].VID_UPPER[23:12]	12
0xBB015310	RNG_CHK_VID_RNG [0].VID_LOWER[11:0]	12
0xBB015314	RNG_CHK_VID_RNG [1].RESERVED[31:26]	6
0xBB015314	RNG_CHK_VID_RNG [1].TYPE[25:24]	2
0xBB015314	RNG_CHK_VID_RNG [1].VID_UPPER[23:12]	12
0xBB015314	RNG_CHK_VID_RNG [1].VID_LOWER[11:0]	12
0xBB015318	RNG_CHK_VID_RNG [2].RESERVED[31:26]	6
0xBB015318	RNG_CHK_VID_RNG [2].TYPE[25:24]	2
0xBB015318	RNG_CHK_VID_RNG [2].VID_UPPER[23:12]	12
0xBB015318	RNG_CHK_VID_RNG [2].VID_LOWER[11:0]	12
0xBB01531C	RNG_CHK_VID_RNG [3].RESERVED[31:26]	6
0xBB01531C	RNG_CHK_VID_RNG [3].TYPE[25:24]	2
0xBB01531C	RNG_CHK_VID_RNG [3].VID_UPPER[23:12]	12
0xBB01531C	RNG_CHK_VID_RNG [3].VID_LOWER[11:0]	12
0xBB015320	RNG_CHK_VID_RNG [4].RESERVED[31:26]	6
0xBB015320	RNG_CHK_VID_RNG [4].TYPE[25:24]	2
0xBB015320	RNG_CHK_VID_RNG [4].VID_UPPER[23:12]	12
0xBB015320	RNG_CHK_VID_RNG [4].VID_LOWER[11:0]	12
0xBB015324	RNG_CHK_VID_RNG [5].RESERVED[31:26]	6
0xBB015324	RNG_CHK_VID_RNG [5].TYPE[25:24]	2
0xBB015324	RNG_CHK_VID_RNG [5].VID_UPPER[23:12]	12
0xBB015324	RNG_CHK_VID_RNG [5].VID_LOWER[11:0]	12
0xBB015328	RNG_CHK_VID_RNG [6].RESERVED[31:26]	6
0xBB015328	RNG_CHK_VID_RNG [6].TYPE[25:24]	2
0xBB015328	RNG_CHK_VID_RNG [6].VID_UPPER[23:12]	12
0xBB015328	RNG_CHK_VID_RNG [6].VID_LOWER[11:0]	12
0xBB01532C	RNG_CHK_VID_RNG [7].RESERVED[31:26]	6
0xBB01532C	RNG_CHK_VID_RNG [7].TYPE[25:24]	2
0xBB01532C	RNG_CHK_VID_RNG [7].VID_UPPER[23:12]	12
0xBB01532C	RNG_CHK_VID_RNG [7].VID_LOWER[11:0]	12
0xBB015330	RNG_CHK_IP_RNG [0].RESERVED[31:3]	29
0xBB015330	RNG_CHK_IP_RNG [0].TYPE[2:0]	3
0xBB015334	RNG_CHK_IP_RNG [0].IP_UPPER[31:0]	32
0xBB015338	RNG_CHK_IP_RNG [0].IP_LOWER[31:0]	32
0xBB01533C	RNG_CHK_IP_RNG [1].RESERVED[31:3]	29
0xBB01533C	RNG_CHK_IP_RNG [1].TYPE[2:0]	3
0xBB015340	RNG_CHK_IP_RNG [1].IP_UPPER[31:0]	32
0xBB015344	RNG_CHK_IP_RNG [1].IP_LOWER[31:0]	32
0xBB015348	RNG_CHK_IP_RNG [2].RESERVED[31:3]	29
0xBB015348	RNG_CHK_IP_RNG [2].TYPE[2:0]	3
0xBB01534C	RNG_CHK_IP_RNG [2].IP_UPPER[31:0]	32
0xBB015350	RNG_CHK_IP_RNG [2].IP_LOWER[31:0]	32
0xBB015354	RNG_CHK_IP_RNG [3].RESERVED[31:3]	29
0xBB015354	RNG_CHK_IP_RNG [3].TYPE[2:0]	3

Address	Register	Len
0xBB015358	RNG_CHK_IP_RNG [3].IP_UPPER[31:0]	32
0xBB01535C	RNG_CHK_IP_RNG [3].IP_LOWER[31:0]	32
0xBB015360	RNG_CHK_IP_RNG [4].RESERVED[31:3]	29
0xBB015360	RNG_CHK_IP_RNG [4].TYPE[2:0]	3
0xBB015364	RNG_CHK_IP_RNG [4].IP_UPPER[31:0]	32
0xBB015368	RNG_CHK_IP_RNG [4].IP_LOWER[31:0]	32
0xBB01536C	RNG_CHK_IP_RNG [5].RESERVED[31:3]	29
0xBB01536C	RNG_CHK_IP_RNG [5].TYPE[2:0]	3
0xBB015370	RNG_CHK_IP_RNG [5].IP_UPPER[31:0]	32
0xBB015374	RNG_CHK_IP_RNG [5].IP_LOWER[31:0]	32
0xBB015378	RNG_CHK_IP_RNG [6].RESERVED[31:3]	29
0xBB015378	RNG_CHK_IP_RNG [6].TYPE[2:0]	3
0xBB01537C	RNG_CHK_IP_RNG [6].IP_UPPER[31:0]	32
0xBB015380	RNG_CHK_IP_RNG [6].IP_LOWER[31:0]	32
0xBB015384	RNG_CHK_IP_RNG [7].RESERVED[31:3]	29
0xBB015384	RNG_CHK_IP_RNG [7].TYPE[2:0]	3
0xBB015388	RNG_CHK_IP_RNG [7].IP_UPPER[31:0]	32
0xBB01538C	RNG_CHK_IP_RNG [7].IP_LOWER[31:0]	32
0xBB015390	RNG_CHK_L4PORT_RNG [0].RESERVED[31:2]	30
0xBB015390	RNG_CHK_L4PORT_RNG [0].TYPE[1:0]	2
0xBB015394	RNG_CHK_L4PORT_RNG [0].L4PORT_UPPER[31:16]	16
0xBB015394	RNG_CHK_L4PORT_RNG [0].L4PORT_LOWER[15:0]	16
0xBB015398	RNG_CHK_L4PORT_RNG [1].RESERVED[31:2]	30
0xBB015398	RNG_CHK_L4PORT_RNG [1].TYPE[1:0]	2
0xBB01539C	RNG_CHK_L4PORT_RNG [1].L4PORT_UPPER[31:16]	16
0xBB01539C	RNG_CHK_L4PORT_RNG [1].L4PORT_LOWER[15:0]	16
0xBB0153A0	RNG_CHK_L4PORT_RNG [2].RESERVED[31:2]	30
0xBB0153A0	RNG_CHK_L4PORT_RNG [2].TYPE[1:0]	2
0xBB0153A4	RNG_CHK_L4PORT_RNG [2].L4PORT_UPPER[31:16]	16
0xBB0153A4	RNG_CHK_L4PORT_RNG [2].L4PORT_LOWER[15:0]	16
0xBB0153A8	RNG_CHK_L4PORT_RNG [3].RESERVED[31:2]	30
0xBB0153A8	RNG_CHK_L4PORT_RNG [3].TYPE[1:0]	2
0xBB0153AC	RNG_CHK_L4PORT_RNG [3].L4PORT_UPPER[31:16]	16
0xBB0153AC	RNG_CHK_L4PORT_RNG [3].L4PORT_LOWER[15:0]	16
0xBB0153B0	RNG_CHK_L4PORT_RNG [4].RESERVED[31:2]	30
0xBB0153B0	RNG_CHK_L4PORT_RNG [4].TYPE[1:0]	2
0xBB0153B4	RNG_CHK_L4PORT_RNG [4].L4PORT_UPPER[31:16]	16
0xBB0153B4	RNG_CHK_L4PORT_RNG [4].L4PORT_LOWER[15:0]	16
0xBB0153B8	RNG_CHK_L4PORT_RNG [5].RESERVED[31:2]	30
0xBB0153B8	RNG_CHK_L4PORT_RNG [5].TYPE[1:0]	2
0xBB0153BC	RNG_CHK_L4PORT_RNG [5].L4PORT_UPPER[31:16]	16
0xBB0153BC	RNG_CHK_L4PORT_RNG [5].L4PORT_LOWER[15:0]	16
0xBB0153C0	RNG_CHK_L4PORT_RNG [6].RESERVED[31:2]	30
0xBB0153C0	RNG_CHK_L4PORT_RNG [6].TYPE[1:0]	2
0xBB0153C4	RNG_CHK_L4PORT_RNG [6].L4PORT_UPPER[31:16]	16
0xBB0153C4	RNG_CHK_L4PORT_RNG [6].L4PORT_LOWER[15:0]	16



Address	Register	Len
0xBB0153C8	RNG_CHK_L4PORT_RNG [7].RESERVED[31:2]	30
0xBB0153C8	RNG_CHK_L4PORT_RNG [7].TYPE[1:0]	2
0xBB0153CC	RNG_CHK_L4PORT_RNG [7].L4PORT_UPPER[31:16]	16
0xBB0153CC	RNG_CHK_L4PORT_RNG [7].L4PORT_LOWER[15:0]	16
0xBB0153D0	RNG_CHK_L4PORT_RNG [8].RESERVED[31:2]	30
0xBB0153D0	RNG_CHK_L4PORT_RNG [8].TYPE[1:0]	2
0xBB0153D4	RNG_CHK_L4PORT_RNG [8].L4PORT_UPPER[31:16]	16
0xBB0153D4	RNG_CHK_L4PORT_RNG [8].L4PORT_LOWER[15:0]	16
0xBB0153D8	RNG_CHK_L4PORT_RNG [9].RESERVED[31:2]	30
0xBB0153D8	RNG_CHK_L4PORT_RNG [9].TYPE[1:0]	2
0xBB0153DC	RNG_CHK_L4PORT_RNG [9].L4PORT_UPPER[31:16]	16
0xBB0153DC	RNG_CHK_L4PORT_RNG [9].L4PORT_LOWER[15:0]	16
0xBB0153E0	RNG_CHK_L4PORT_RNG [10].RESERVED[31:2]	30
0xBB0153E0	RNG_CHK_L4PORT_RNG [10].TYPE[1:0]	2
0xBB0153E4	RNG_CHK_L4PORT_RNG [10].L4PORT_UPPER[31:16]	16
0xBB0153E4	RNG_CHK_L4PORT_RNG [10].L4PORT_LOWER[15:0]	16
0xBB0153E8	RNG_CHK_L4PORT_RNG [11].RESERVED[31:2]	30
0xBB0153E8	RNG_CHK_L4PORT_RNG [11].TYPE[1:0]	2
0xBB0153EC	RNG_CHK_L4PORT_RNG [11].L4PORT_UPPER[31:16]	16
0xBB0153EC	RNG_CHK_L4PORT_RNG [11].L4PORT_LOWER[15:0]	16
0xBB0153F0	RNG_CHK_L4PORT_RNG [12].RESERVED[31:2]	30
0xBB0153F0	RNG_CHK_L4PORT_RNG [12].TYPE[1:0]	2
0xBB0153F4	RNG_CHK_L4PORT_RNG [12].L4PORT_UPPER[31:16]	16
0xBB0153F4	RNG_CHK_L4PORT_RNG [12].L4PORT_LOWER[15:0]	16
0xBB0153F8	RNG_CHK_L4PORT_RNG [13].RESERVED[31:2]	30
0xBB0153F8	RNG_CHK_L4PORT_RNG [13].TYPE[1:0]	2
0xBB0153FC	RNG_CHK_L4PORT_RNG [13].L4PORT_UPPER[31:16]	16
0xBB0153FC	RNG_CHK_L4PORT_RNG [13].L4PORT_LOWER[15:0]	16
0xBB015400	RNG_CHK_L4PORT_RNG [14].RESERVED[31:2]	30
0xBB015400	RNG_CHK_L4PORT_RNG [14].TYPE[1:0]	2
0xBB015404	RNG_CHK_L4PORT_RNG [14].L4PORT_UPPER[31:16]	16
0xBB015404	RNG_CHK_L4PORT_RNG [14].L4PORT_LOWER[15:0]	16
0xBB015408	RNG_CHK_L4PORT_RNG [15].RESERVED[31:2]	30
0xBB015408	RNG_CHK_L4PORT_RNG [15].TYPE[1:0]	2
0xBB01540C	RNG_CHK_L4PORT_RNG [15].L4PORT_UPPER[31:16]	16
0xBB01540C	RNG_CHK_L4PORT_RNG [15].L4PORT_LOWER[15:0]	16
0xBB015410	RNG_CHK_PKTLEN_RNG [0].RESERVED[31:29]	3
0xBB015410	RNG_CHK_PKTLEN_RNG [0].TYPE[28:28]	1
0xBB015410	RNG_CHK_PKTLEN_RNG [0].PKTLEN_UPPER[27:14]	14
0xBB015410	RNG_CHK_PKTLEN_RNG [0].PKTLEN_LOWER[13:0]	14
0xBB015414	RNG_CHK_PKTLEN_RNG [1].RESERVED[31:29]	3
0xBB015414	RNG_CHK_PKTLEN_RNG [1].TYPE[28:28]	1
0xBB015414	RNG_CHK_PKTLEN_RNG [1].PKTLEN_UPPER[27:14]	14
0xBB015414	RNG_CHK_PKTLEN_RNG [1].PKTLEN_LOWER[13:0]	14
0xBB015418	RNG_CHK_PKTLEN_RNG [2].RESERVED[31:29]	3
0xBB015418	RNG_CHK_PKTLEN_RNG [2].TYPE[28:28]	1



Address	Register	Len
0xBB015418	RNG_CHK_PKTLEN_RNG [2].PKTLEN_UPPER[27:14]	14
0xBB015418	RNG_CHK_PKTLEN_RNG [2].PKTLEN_LOWER[13:0]	14
0xBB01541C	RNG_CHK_PKTLEN_RNG [3].RESERVED[31:29]	3
0xBB01541C	RNG_CHK_PKTLEN_RNG [3].TYPE[28:28]	1
0xBB01541C	RNG_CHK_PKTLEN_RNG [3].PKTLEN_UPPER[27:14]	14
0xBB01541C	RNG_CHK_PKTLEN_RNG [3].PKTLEN_LOWER[13:0]	14
0xBB015420	RNG_CHK_PKTLEN_RNG [4].RESERVED[31:29]	3
0xBB015420	RNG_CHK_PKTLEN_RNG [4].TYPE[28:28]	1
0xBB015420	RNG_CHK_PKTLEN_RNG [4].PKTLEN_UPPER[27:14]	14
0xBB015420	RNG_CHK_PKTLEN_RNG [4].PKTLEN_LOWER[13:0]	14
0xBB015424	RNG_CHK_PKTLEN_RNG [5].RESERVED[31:29]	3
0xBB015424	RNG_CHK_PKTLEN_RNG [5].TYPE[28:28]	1
0xBB015424	RNG_CHK_PKTLEN_RNG [5].PKTLEN_UPPER[27:14]	14
0xBB015424	RNG_CHK_PKTLEN_RNG [5].PKTLEN_LOWER[13:0]	14
0xBB015428	RNG_CHK_PKTLEN_RNG [6].RESERVED[31:29]	3
0xBB015428	RNG_CHK_PKTLEN_RNG [6].TYPE[28:28]	1
0xBB015428	RNG_CHK_PKTLEN_RNG [6].PKTLEN_UPPER[27:14]	14
0xBB015428	RNG_CHK_PKTLEN_RNG [6].PKTLEN_LOWER[13:0]	14
0xBB01542C	RNG_CHK_PKTLEN_RNG [7].RESERVED[31:29]	3
0xBB01542C	RNG_CHK_PKTLEN_RNG [7].TYPE[28:28]	1
0xBB01542C	RNG_CHK_PKTLEN_RNG [7].PKTLEN_UPPER[27:14]	14
0xBB01542C	RNG_CHK_PKTLEN_RNG [7].PKTLEN_LOWER[13:0]	14
0xBB015430	RNG_CHK_IP_RNG_CF [0].RESERVED[31:1]	31
0xBB015430	RNG_CHK_IP_RNG_CF [0].TYPE[0:0]	1
0xBB015434	RNG_CHK_IP_RNG_CF [0].IP_UPPER[31:0]	32
0xBB015438	RNG_CHK_IP_RNG_CF [0].IP_LOWER[31:0]	32
0xBB01543C	RNG_CHK_IP_RNG_CF [1].RESERVED[31:1]	31
0xBB01543C	RNG_CHK_IP_RNG_CF [1].TYPE[0:0]	1
0xBB015440	RNG_CHK_IP_RNG_CF [1].IP_UPPER[31:0]	32
0xBB015444	RNG_CHK_IP_RNG_CF [1].IP_LOWER[31:0]	32
0xBB015448	RNG_CHK_IP_RNG_CF [2].RESERVED[31:1]	31
0xBB015448	RNG_CHK_IP_RNG_CF [2].TYPE[0:0]	1
0xBB01544C	RNG_CHK_IP_RNG_CF [2].IP_UPPER[31:0]	32
0xBB015450	RNG_CHK_IP_RNG_CF [2].IP_LOWER[31:0]	32
0xBB015454	RNG_CHK_IP_RNG_CF [3].RESERVED[31:1]	31
0xBB015454	RNG_CHK_IP_RNG_CF [3].TYPE[0:0]	1
0xBB015458	RNG_CHK_IP_RNG_CF [3].IP_UPPER[31:0]	32
0xBB01545C	RNG_CHK_IP_RNG_CF [3].IP_LOWER[31:0]	32
0xBB015460	RNG_CHK_IP_RNG_CF [4].RESERVED[31:1]	31
0xBB015460	RNG_CHK_IP_RNG_CF [4].TYPE[0:0]	1
0xBB015464	RNG_CHK_IP_RNG_CF [4].IP_UPPER[31:0]	32
0xBB015468	RNG_CHK_IP_RNG_CF [4].IP_LOWER[31:0]	32
0xBB01546C	RNG_CHK_IP_RNG_CF [5].RESERVED[31:1]	31
0xBB01546C	RNG_CHK_IP_RNG_CF [5].TYPE[0:0]	1
0xBB015470	RNG_CHK_IP_RNG_CF [5].IP_UPPER[31:0]	32
0xBB015474	RNG_CHK_IP_RNG_CF [5].IP_LOWER[31:0]	32

Address	Register	Len
0xBB015478	RNG_CHK_IP_RNG_CF [6].RESERVED[31:1]	31
0xBB015478	RNG_CHK_IP_RNG_CF [6].TYPE[0:0]	1
0xBB01547C	RNG_CHK_IP_RNG_CF [6].IP_UPPER[31:0]	32
0xBB015480	RNG_CHK_IP_RNG_CF [6].IP_LOWER[31:0]	32
0xBB015484	RNG_CHK_IP_RNG_CF [7].RESERVED[31:1]	31
0xBB015484	RNG_CHK_IP_RNG_CF [7].TYPE[0:0]	1
0xBB015488	RNG_CHK_IP_RNG_CF [7].IP_UPPER[31:0]	32
0xBB01548C	RNG_CHK_IP_RNG_CF [7].IP_LOWER[31:0]	32
0xBB015490	RNG_CHK_L4PORT_RNG_CF [0].RESERVED[31:1]	31
0xBB015490	RNG_CHK_L4PORT_RNG_CF [0].TYPE[0:0]	1
0xBB015494	RNG_CHK_L4PORT_RNG_CF [0].L4PORT_UPPER[31:16]	16
0xBB015494	RNG_CHK_L4PORT_RNG_CF [0].L4PORT_LOWER[15:0]	16
0xBB015498	RNG_CHK_L4PORT_RNG_CF [1].RESERVED[31:1]	31
0xBB015498	RNG_CHK_L4PORT_RNG_CF [1].TYPE[0:0]	1
0xBB01549C	RNG_CHK_L4PORT_RNG_CF [1].L4PORT_UPPER[31:16]	16
0xBB01549C	RNG_CHK_L4PORT_RNG_CF [1].L4PORT_LOWER[15:0]	16
0xBB0154A0	RNG_CHK_L4PORT_RNG_CF [2].RESERVED[31:1]	31
0xBB0154A0	RNG_CHK_L4PORT_RNG_CF [2].TYPE[0:0]	1
0xBB0154A4	RNG_CHK_L4PORT_RNG_CF [2].L4PORT_UPPER[31:16]	16
0xBB0154A4	RNG_CHK_L4PORT_RNG_CF [2].L4PORT_LOWER[15:0]	16
0xBB0154A8	RNG_CHK_L4PORT_RNG_CF [3].RESERVED[31:1]	31
0xBB0154A8	RNG_CHK_L4PORT_RNG_CF [3].TYPE[0:0]	1
0xBB0154AC	RNG_CHK_L4PORT_RNG_CF [3].L4PORT_UPPER[31:16]	16
0xBB0154AC	RNG_CHK_L4PORT_RNG_CF [3].L4PORT_LOWER[15:0]	16
0xBB0154B0	RNG_CHK_L4PORT_RNG_CF [4].RESERVED[31:1]	31
0xBB0154B0	RNG_CHK_L4PORT_RNG_CF [4].TYPE[0:0]	1
0xBB0154B4	RNG_CHK_L4PORT_RNG_CF [4].L4PORT_UPPER[31:16]	16
0xBB0154B4	RNG_CHK_L4PORT_RNG_CF [4].L4PORT_LOWER[15:0]	16
0xBB0154B8	RNG_CHK_L4PORT_RNG_CF [5].RESERVED[31:1]	31
0xBB0154B8	RNG_CHK_L4PORT_RNG_CF [5].TYPE[0:0]	1
0xBB0154BC	RNG_CHK_L4PORT_RNG_CF [5].L4PORT_UPPER[31:16]	16
0xBB0154BC	RNG_CHK_L4PORT_RNG_CF [5].L4PORT_LOWER[15:0]	16
0xBB0154C0	RNG_CHK_L4PORT_RNG_CF [6].RESERVED[31:1]	31
0xBB0154C0	RNG_CHK_L4PORT_RNG_CF [6].TYPE[0:0]	1
0xBB0154C4	RNG_CHK_L4PORT_RNG_CF [6].L4PORT_UPPER[31:16]	16
0xBB0154C4	RNG_CHK_L4PORT_RNG_CF [6].L4PORT_LOWER[15:0]	16
0xBB0154C8	RNG_CHK_L4PORT_RNG_CF [7].RESERVED[31:1]	31
0xBB0154C8	RNG_CHK_L4PORT_RNG_CF [7].TYPE[0:0]	1
0xBB0154CC	RNG_CHK_L4PORT_RNG_CF [7].L4PORT_UPPER[31:16]	16
0xBB0154CC	RNG_CHK_L4PORT_RNG_CF [7].L4PORT_LOWER[15:0]	16
0xBB0154D0	RGF_VER_ALE_ACL.REGFILE_VER[31:0]	32
0xBB0154D4	RSVD_ALE_ACL [0].RSVD_MEM[31:0]	32
0xBB0154D8	RSVD_ALE_ACL [1].RSVD_MEM[31:0]	32
0xBB0154DC	RSVD_ALE_ACL [2].RSVD_MEM[31:0]	32
0xBB0154E0	RSVD_ALE_ACL [3].RSVD_MEM[31:0]	32
0xBB0154E4	RSVD_ALE_ACL [4].RSVD_MEM[31:0]	32

Address	Register	Len
0xBB0154E8	RSVD_ALE_ACL [5].RSVD_MEM[31:0]	32
0xBB0154EC	RSVD_ALE_ACL [6].RSVD_MEM[31:0]	32
0xBB0154F0	RSVD_ALE_ACL [7].RSVD_MEM[31:0]	32
0xBB0154F4	RSVD_ALE_ACL [8].RSVD_MEM[31:0]	32
0xBB0154F8	RSVD_ALE_ACL [9].RSVD_MEM[31:0]	32
0xBB0154FC	RSVD_ALE_ACL [10].RSVD_MEM[31:0]	32
0xBB015500	RSVD_ALE_ACL [11].RSVD_MEM[31:0]	32
0xBB015504	RSVD_ALE_ACL [12].RSVD_MEM[31:0]	32
0xBB015508	RSVD_ALE_ACL [13].RSVD_MEM[31:0]	32
0xBB01550C	RSVD_ALE_ACL [14].RSVD_MEM[31:0]	32
0xBB015510	RSVD_ALE_ACL [15].RSVD_MEM[31:0]	32
0xBB017000	LUT_CFG.RESERVED[31:26]	6
0xBB017000	LUT_CFG.LUT_IPMC_LOOKUP_OP[25:25]	1
0xBB017000	LUT_CFG.LUT_IPMC_HASH[24:23]	2
0xBB017000	LUT_CFG.LINKDOWN_AGEOUT[22:22]	1
0xBB017000	LUT_CFG.BCAM_DIS[21:21]	1
0xBB017000	LUT_CFG.AGE_SPD[20:0]	21
0xBB017004	LUT_AGEOUT_CTRL [0].AGEOUT_OUT[0:0]	1
0xBB017004	LUT_AGEOUT_CTRL [1].AGEOUT_OUT[1:1]	1
0xBB017004	LUT_AGEOUT_CTRL [2].AGEOUT_OUT[2:2]	1
0xBB017004	LUT_AGEOUT_CTRL [3].AGEOUT_OUT[3:3]	1
0xBB017004	LUT_AGEOUT_CTRL [4].AGEOUT_OUT[4:4]	1
0xBB017004	LUT_AGEOUT_CTRL [5].AGEOUT_OUT[5:5]	1
0xBB017004	LUT_AGEOUT_CTRL [6].AGEOUT_OUT[6:6]	1
0xBB017008	LUT_LRN_LIMITNO [0].NUM[11:0]	12
0xBB017008	LUT_LRN_LIMITNO [1].NUM[23:12]	12
0xBB01700C	LUT_LRN_LIMITNO [2].NUM[11:0]	12
0xBB01700C	LUT_LRN_LIMITNO [3].NUM[23:12]	12
0xBB017010	LUT_LRN_LIMITNO [4].NUM[11:0]	12
0xBB017010	LUT_LRN_LIMITNO [5].NUM[23:12]	12
0xBB017014	LUT_LRN_LIMITNO [6].NUM[11:0]	12
0xBB017018	L2_LRN_CNT [0].L2_LRN_CNT[11:0]	12
0xBB017018	L2_LRN_CNT [1].L2_LRN_CNT[23:12]	12
0xBB01701C	L2_LRN_CNT [2].L2_LRN_CNT[11:0]	12
0xBB01701C	L2_LRN_CNT [3].L2_LRN_CNT[23:12]	12
0xBB017020	L2_LRN_CNT [4].L2_LRN_CNT[11:0]	12
0xBB017020	L2_LRN_CNT [5].L2_LRN_CNT[23:12]	12
0xBB017024	L2_LRN_CNT [6].L2_LRN_CNT[11:0]	12
0xBB017028	LUT_SYS_LRN_LIMITNO.RESERVED[31:12]	20
0xBB017028	LUT_SYS_LRN_LIMITNO.SYS_LRN_LIMITNO[11:0]	12
0xBB01702C	L2_SYS_LRN_CNT.RESERVED[31:12]	20
0xBB01702C	L2_SYS_LRN_CNT.SYS_L2_LRN_CNT[11:0]	12
0xBB017030	L2_EFID [0].EFID[2:0]	3
0xBB017030	L2_EFID [1].EFID[5:3]	3
0xBB017030	L2_EFID [2].EFID[8:6]	3
0xBB017030	L2_EFID [3].EFID[11:9]	3

Address	Register	Len
0xBB017030	L2_EFID [4].EFID[14:12]	3
0xBB017030	L2_EFID [5].EFID[17:15]	3
0xBB017030	L2_EFID [6].EFID[20:18]	3
0xBB017034	LUT_SYS_LRN_OVER_CTRL.RESERVED[31:2]	30
0xBB017034	LUT_SYS_LRN_OVER_CTRL.ACT[1:0]	2
0xBB017038	L2_TBL_FLUSH_CTRL.RESERVED[31:21]	11
0xBB017038	L2_TBL_FLUSH_CTRL.LUT_FLUSH_FID[20:17]	4
0xBB017038	L2_TBL_FLUSH_CTRL.LUT_FLUSH_VID[16:5]	12
0xBB017038	L2_TBL_FLUSH_CTRL.LUT_FLUSH_DYNAMIC[4:4]	1
0xBB017038	L2_TBL_FLUSH_CTRL.LUT_FLUSH_STATIC[3:3]	1
0xBB017038	L2_TBL_FLUSH_CTRL.LUT_FLUSH_MODE[2:1]	2
0xBB017038	L2_TBL_FLUSH_CTRL.FLUSH_STATUS[0:0]	1
0xBB01703C	L2_TBL_FLUSH_EN [0].EN[0:0]	1
0xBB01703C	L2_TBL_FLUSH_EN [1].EN[1:1]	1
0xBB01703C	L2_TBL_FLUSH_EN [2].EN[2:2]	1
0xBB01703C	L2_TBL_FLUSH_EN [3].EN[3:3]	1
0xBB01703C	L2_TBL_FLUSH_EN [4].EN[4:4]	1
0xBB01703C	L2_TBL_FLUSH_EN [5].EN[5:5]	1
0xBB01703C	L2_TBL_FLUSH_EN [6].EN[6:6]	1
0xBB017040	MSTI_CTRL [0][0].STATE[1:0]	2
0xBB017040	MSTI_CTRL [0][1].STATE[3:2]	2
0xBB017040	MSTI_CTRL [0][2].STATE[5:4]	2
0xBB017040	MSTI_CTRL [0][3].STATE[7:6]	2
0xBB017040	MSTI_CTRL [0][4].STATE[9:8]	2
0xBB017040	MSTI_CTRL [0][5].STATE[11:10]	2
0xBB017040	MSTI_CTRL [0][6].STATE[13:12]	2
0xBB017040	MSTI_CTRL [0][7].STATE[15:14]	2
0xBB017040	MSTI_CTRL [0][8].STATE[17:16]	2
0xBB017040	MSTI_CTRL [0][9].STATE[19:18]	2
0xBB017040	MSTI_CTRL [0][10].STATE[21:20]	2
0xBB017040	MSTI_CTRL [0][11].STATE[23:22]	2
0xBB017040	MSTI_CTRL [0][12].STATE[25:24]	2
0xBB017040	MSTI_CTRL [0][13].STATE[27:26]	2
0xBB017040	MSTI_CTRL [0][14].STATE[29:28]	2
0xBB017040	MSTI_CTRL [0][15].STATE[31:30]	2
0xBB017044	MSTI_CTRL [1][0].STATE[1:0]	2
0xBB017044	MSTI_CTRL [1][1].STATE[3:2]	2
0xBB017044	MSTI_CTRL [1][2].STATE[5:4]	2
0xBB017044	MSTI_CTRL [1][3].STATE[7:6]	2
0xBB017044	MSTI_CTRL [1][4].STATE[9:8]	2
0xBB017044	MSTI_CTRL [1][5].STATE[11:10]	2
0xBB017044	MSTI_CTRL [1][6].STATE[13:12]	2
0xBB017044	MSTI_CTRL [1][7].STATE[15:14]	2
0xBB017044	MSTI_CTRL [1][8].STATE[17:16]	2
0xBB017044	MSTI_CTRL [1][9].STATE[19:18]	2
0xBB017044	MSTI_CTRL [1][10].STATE[21:20]	2

Address	Register	Len
0xBB017044	MSTI_CTRL [1][11].STATE[23:22]	2
0xBB017044	MSTI_CTRL [1][12].STATE[25:24]	2
0xBB017044	MSTI_CTRL [1][13].STATE[27:26]	2
0xBB017044	MSTI_CTRL [1][14].STATE[29:28]	2
0xBB017044	MSTI_CTRL [1][15].STATE[31:30]	2
0xBB017048	MSTI_CTRL [2][0].STATE[1:0]	2
0xBB017048	MSTI_CTRL [2][1].STATE[3:2]	2
0xBB017048	MSTI_CTRL [2][2].STATE[5:4]	2
0xBB017048	MSTI_CTRL [2][3].STATE[7:6]	2
0xBB017048	MSTI_CTRL [2][4].STATE[9:8]	2
0xBB017048	MSTI_CTRL [2][5].STATE[11:10]	2
0xBB017048	MSTI_CTRL [2][6].STATE[13:12]	2
0xBB017048	MSTI_CTRL [2][7].STATE[15:14]	2
0xBB017048	MSTI_CTRL [2][8].STATE[17:16]	2
0xBB017048	MSTI_CTRL [2][9].STATE[19:18]	2
0xBB017048	MSTI_CTRL [2][10].STATE[21:20]	2
0xBB017048	MSTI_CTRL [2][11].STATE[23:22]	2
0xBB017048	MSTI_CTRL [2][12].STATE[25:24]	2
0xBB017048	MSTI_CTRL [2][13].STATE[27:26]	2
0xBB017048	MSTI_CTRL [2][14].STATE[29:28]	2
0xBB017048	MSTI_CTRL [2][15].STATE[31:30]	2
0xBB01704C	MSTI_CTRL [3][0].STATE[1:0]	2
0xBB01704C	MSTI_CTRL [3][1].STATE[3:2]	2
0xBB01704C	MSTI_CTRL [3][2].STATE[5:4]	2
0xBB01704C	MSTI_CTRL [3][3].STATE[7:6]	2
0xBB01704C	MSTI_CTRL [3][4].STATE[9:8]	2
0xBB01704C	MSTI_CTRL [3][5].STATE[11:10]	2
0xBB01704C	MSTI_CTRL [3][6].STATE[13:12]	2
0xBB01704C	MSTI_CTRL [3][7].STATE[15:14]	2
0xBB01704C	MSTI_CTRL [3][8].STATE[17:16]	2
0xBB01704C	MSTI_CTRL [3][9].STATE[19:18]	2
0xBB01704C	MSTI_CTRL [3][10].STATE[21:20]	2
0xBB01704C	MSTI_CTRL [3][11].STATE[23:22]	2
0xBB01704C	MSTI_CTRL [3][12].STATE[25:24]	2
0xBB01704C	MSTI_CTRL [3][13].STATE[27:26]	2
0xBB01704C	MSTI_CTRL [3][14].STATE[29:28]	2
0xBB01704C	MSTI_CTRL [3][15].STATE[31:30]	2
0xBB017050	MSTI_CTRL [4][0].STATE[1:0]	2
0xBB017050	MSTI_CTRL [4][1].STATE[3:2]	2
0xBB017050	MSTI_CTRL [4][2].STATE[5:4]	2
0xBB017050	MSTI_CTRL [4][3].STATE[7:6]	2
0xBB017050	MSTI_CTRL [4][4].STATE[9:8]	2
0xBB017050	MSTI_CTRL [4][5].STATE[11:10]	2
0xBB017050	MSTI_CTRL [4][6].STATE[13:12]	2
0xBB017050	MSTI_CTRL [4][7].STATE[15:14]	2
0xBB017050	MSTI_CTRL [4][8].STATE[17:16]	2

Address	Register	Len
0xBB017050	MSTI_CTRL [4][9].STATE[19:18]	2
0xBB017050	MSTI_CTRL [4][10].STATE[21:20]	2
0xBB017050	MSTI_CTRL [4][11].STATE[23:22]	2
0xBB017050	MSTI_CTRL [4][12].STATE[25:24]	2
0xBB017050	MSTI_CTRL [4][13].STATE[27:26]	2
0xBB017050	MSTI_CTRL [4][14].STATE[29:28]	2
0xBB017050	MSTI_CTRL [4][15].STATE[31:30]	2
0xBB017054	MSTI_CTRL [5][0].STATE[1:0]	2
0xBB017054	MSTI_CTRL [5][1].STATE[3:2]	2
0xBB017054	MSTI_CTRL [5][2].STATE[5:4]	2
0xBB017054	MSTI_CTRL [5][3].STATE[7:6]	2
0xBB017054	MSTI_CTRL [5][4].STATE[9:8]	2
0xBB017054	MSTI_CTRL [5][5].STATE[11:10]	2
0xBB017054	MSTI_CTRL [5][6].STATE[13:12]	2
0xBB017054	MSTI_CTRL [5][7].STATE[15:14]	2
0xBB017054	MSTI_CTRL [5][8].STATE[17:16]	2
0xBB017054	MSTI_CTRL [5][9].STATE[19:18]	2
0xBB017054	MSTI_CTRL [5][10].STATE[21:20]	2
0xBB017054	MSTI_CTRL [5][11].STATE[23:22]	2
0xBB017054	MSTI_CTRL [5][12].STATE[25:24]	2
0xBB017054	MSTI_CTRL [5][13].STATE[27:26]	2
0xBB017054	MSTI_CTRL [5][14].STATE[29:28]	2
0xBB017054	MSTI_CTRL [5][15].STATE[31:30]	2
0xBB017058	MSTI_CTRL [6][0].STATE[1:0]	2
0xBB017058	MSTI_CTRL [6][1].STATE[3:2]	2
0xBB017058	MSTI_CTRL [6][2].STATE[5:4]	2
0xBB017058	MSTI_CTRL [6][3].STATE[7:6]	2
0xBB017058	MSTI_CTRL [6][4].STATE[9:8]	2
0xBB017058	MSTI_CTRL [6][5].STATE[11:10]	2
0xBB017058	MSTI_CTRL [6][6].STATE[13:12]	2
0xBB017058	MSTI_CTRL [6][7].STATE[15:14]	2
0xBB017058	MSTI_CTRL [6][8].STATE[17:16]	2
0xBB017058	MSTI_CTRL [6][9].STATE[19:18]	2
0xBB017058	MSTI_CTRL [6][10].STATE[21:20]	2
0xBB017058	MSTI_CTRL [6][11].STATE[23:22]	2
0xBB017058	MSTI_CTRL [6][12].STATE[25:24]	2
0xBB017058	MSTI_CTRL [6][13].STATE[27:26]	2
0xBB017058	MSTI_CTRL [6][14].STATE[29:28]	2
0xBB017058	MSTI_CTRL [6][15].STATE[31:30]	2
0xBB01705C	STORM_CTRL_UM_CTRL [0].EN[0:0]	1
0xBB01705C	STORM_CTRL_UM_CTRL [1].EN[1:1]	1
0xBB01705C	STORM_CTRL_UM_CTRL [2].EN[2:2]	1
0xBB01705C	STORM_CTRL_UM_CTRL [3].EN[3:3]	1
0xBB01705C	STORM_CTRL_UM_CTRL [4].EN[4:4]	1
0xBB01705C	STORM_CTRL_UM_CTRL [5].EN[5:5]	1
0xBB01705C	STORM_CTRL_UM_CTRL [6].EN[6:6]	1

Address	Register	Len
0xBB017060	STORM_CTRL_UC_CTRL [0].EN[0:0]	1
0xBB017060	STORM_CTRL_UC_CTRL [1].EN[1:1]	1
0xBB017060	STORM_CTRL_UC_CTRL [2].EN[2:2]	1
0xBB017060	STORM_CTRL_UC_CTRL [3].EN[3:3]	1
0xBB017060	STORM_CTRL_UC_CTRL [4].EN[4:4]	1
0xBB017060	STORM_CTRL_UC_CTRL [5].EN[5:5]	1
0xBB017060	STORM_CTRL_UC_CTRL [6].EN[6:6]	1
0xBB017064	STORM_CTRL_MC_CTRL [0].EN[0:0]	1
0xBB017064	STORM_CTRL_MC_CTRL [1].EN[1:1]	1
0xBB017064	STORM_CTRL_MC_CTRL [2].EN[2:2]	1
0xBB017064	STORM_CTRL_MC_CTRL [3].EN[3:3]	1
0xBB017064	STORM_CTRL_MC_CTRL [4].EN[4:4]	1
0xBB017064	STORM_CTRL_MC_CTRL [5].EN[5:5]	1
0xBB017064	STORM_CTRL_MC_CTRL [6].EN[6:6]	1
0xBB017068	STORM_CTRL_BC_CTRL [0].EN[0:0]	1
0xBB017068	STORM_CTRL_BC_CTRL [1].EN[1:1]	1
0xBB017068	STORM_CTRL_BC_CTRL [2].EN[2:2]	1
0xBB017068	STORM_CTRL_BC_CTRL [3].EN[3:3]	1
0xBB017068	STORM_CTRL_BC_CTRL [4].EN[4:4]	1
0xBB017068	STORM_CTRL_BC_CTRL [5].EN[5:5]	1
0xBB017068	STORM_CTRL_BC_CTRL [6].EN[6:6]	1
0xBB01706C	STORM_CTRL_UM_METER_IDX [0].IDX[4:0]	5
0xBB01706C	STORM_CTRL_UM_METER_IDX [1].IDX[9:5]	5
0xBB01706C	STORM_CTRL_UM_METER_IDX [2].IDX[14:10]	5
0xBB01706C	STORM_CTRL_UM_METER_IDX [3].IDX[19:15]	5
0xBB01706C	STORM_CTRL_UM_METER_IDX [4].IDX[24:20]	5
0xBB01706C	STORM_CTRL_UM_METER_IDX [5].IDX[29:25]	5
0xBB017070	STORM_CTRL_UM_METER_IDX [6].IDX[4:0]	5
0xBB017074	STORM_CTRL_UC_METER_IDX [0].IDX[4:0]	5
0xBB017074	STORM_CTRL_UC_METER_IDX [1].IDX[9:5]	5
0xBB017074	STORM_CTRL_UC_METER_IDX [2].IDX[14:10]	5
0xBB017074	STORM_CTRL_UC_METER_IDX [3].IDX[19:15]	5
0xBB017074	STORM_CTRL_UC_METER_IDX [4].IDX[24:20]	5
0xBB017074	STORM_CTRL_UC_METER_IDX [5].IDX[29:25]	5
0xBB017078	STORM_CTRL_UC_METER_IDX [6].IDX[4:0]	5
0xBB01707C	STORM_CTRL_MC_METER_IDX [0].IDX[4:0]	5
0xBB01707C	STORM_CTRL_MC_METER_IDX [1].IDX[9:5]	5
0xBB01707C	STORM_CTRL_MC_METER_IDX [2].IDX[14:10]	5
0xBB01707C	STORM_CTRL_MC_METER_IDX [3].IDX[19:15]	5
0xBB01707C	STORM_CTRL_MC_METER_IDX [4].IDX[24:20]	5
0xBB01707C	STORM_CTRL_MC_METER_IDX [5].IDX[29:25]	5
0xBB017080	STORM_CTRL_MC_METER_IDX [6].IDX[4:0]	5
0xBB017084	STORM_CTRL_BC_METER_IDX [0].IDX[4:0]	5
0xBB017084	STORM_CTRL_BC_METER_IDX [1].IDX[9:5]	5
0xBB017084	STORM_CTRL_BC_METER_IDX [2].IDX[14:10]	5
0xBB017084	STORM_CTRL_BC_METER_IDX [3].IDX[19:15]	5

Address	Register	Len
0xBB017084	STORM_CTRL_BC_METER_IDX [4].IDX[24:20]	5
0xBB017084	STORM_CTRL_BC_METER_IDX [5].IDX[29:25]	5
0xBB017088	STORM_CTRL_BC_METER_IDX [6].IDX[4:0]	5
0xBB01708C	STORM_CTRL_ALT_TYPE_SEL.RESERVED[31:8]	24
0xBB01708C	STORM_CTRL_ALT_TYPE_SEL.UNMC_TYPE[7:6]	2
0xBB01708C	STORM_CTRL_ALT_TYPE_SEL.UNDA_TYPE[5:4]	2
0xBB01708C	STORM_CTRL_ALT_TYPE_SEL.MC_TYPE[3:2]	2
0xBB01708C	STORM_CTRL_ALT_TYPE_SEL.BC_TYPE[1:0]	2
0xBB017090	DOT1X_CFG_1.RESERVED[31:7]	25
0xBB017090	DOT1X_CFG_1.DOT1X_GVOPDIR[6:6]	1
0xBB017090	DOT1X_CFG_1.DOT1X_MAC_OPDIR[5:5]	1
0xBB017090	DOT1X_CFG_1.DOT1X_GVIDX[4:0]	5
0xBB017094	DOT1X_P_CTRL [0].RESERVED[31:6]	26
0xBB017094	DOT1X_P_CTRL [0].PB_EN[5:5]	1
0xBB017094	DOT1X_P_CTRL [0].MAC_EN[4:4]	1
0xBB017094	DOT1X_P_CTRL [0].PB_AUTH[3:3]	1
0xBB017094	DOT1X_P_CTRL [0].PB_DIR[2:2]	1
0xBB017094	DOT1X_P_CTRL [0].UNAUTH_ACT[1:0]	2
0xBB017098	DOT1X_P_CTRL [1].RESERVED[31:6]	26
0xBB017098	DOT1X_P_CTRL [1].PB_EN[5:5]	1
0xBB017098	DOT1X_P_CTRL [1].MAC_EN[4:4]	1
0xBB017098	DOT1X_P_CTRL [1].PB_AUTH[3:3]	1
0xBB017098	DOT1X_P_CTRL [1].PB_DIR[2:2]	1
0xBB017098	DOT1X_P_CTRL [1].UNAUTH_ACT[1:0]	2
0xBB01709C	DOT1X_P_CTRL [2].RESERVED[31:6]	26
0xBB01709C	DOT1X_P_CTRL [2].PB_EN[5:5]	1
0xBB01709C	DOT1X_P_CTRL [2].MAC_EN[4:4]	1
0xBB01709C	DOT1X_P_CTRL [2].PB_AUTH[3:3]	1
0xBB01709C	DOT1X_P_CTRL [2].PB_DIR[2:2]	1
0xBB01709C	DOT1X_P_CTRL [2].UNAUTH_ACT[1:0]	2
0xBB0170A0	DOT1X_P_CTRL [3].RESERVED[31:6]	26
0xBB0170A0	DOT1X_P_CTRL [3].PB_EN[5:5]	1
0xBB0170A0	DOT1X_P_CTRL [3].MAC_EN[4:4]	1
0xBB0170A0	DOT1X_P_CTRL [3].PB_AUTH[3:3]	1
0xBB0170A0	DOT1X_P_CTRL [3].PB_DIR[2:2]	1
0xBB0170A0	DOT1X_P_CTRL [3].UNAUTH_ACT[1:0]	2
0xBB0170A4	DOT1X_P_CTRL [4].RESERVED[31:6]	26
0xBB0170A4	DOT1X_P_CTRL [4].PB_EN[5:5]	1
0xBB0170A4	DOT1X_P_CTRL [4].MAC_EN[4:4]	1
0xBB0170A4	DOT1X_P_CTRL [4].PB_AUTH[3:3]	1
0xBB0170A4	DOT1X_P_CTRL [4].PB_DIR[2:2]	1
0xBB0170A4	DOT1X_P_CTRL [4].UNAUTH_ACT[1:0]	2
0xBB0170A8	DOT1X_P_CTRL [5].RESERVED[31:6]	26
0xBB0170A8	DOT1X_P_CTRL [5].PB_EN[5:5]	1
0xBB0170A8	DOT1X_P_CTRL [5].MAC_EN[4:4]	1
0xBB0170A8	DOT1X_P_CTRL [5].PB_AUTH[3:3]	1



Address	Register	Len
0xBB0170A8	DOT1X_P_CTRL [5].PB_DIR[2:2]	1
0xBB0170A8	DOT1X_P_CTRL [5].UNAUTH_ACT[1:0]	2
0xBB0170AC	DOT1X_P_CTRL [6].RESERVED[31:6]	26
0xBB0170AC	DOT1X_P_CTRL [6].PB_EN[5:5]	1
0xBB0170AC	DOT1X_P_CTRL [6].MAC_EN[4:4]	1
0xBB0170AC	DOT1X_P_CTRL [6].PB_AUTH[3:3]	1
0xBB0170AC	DOT1X_P_CTRL [6].PB_DIR[2:2]	1
0xBB0170AC	DOT1X_P_CTRL [6].UNAUTH_ACT[1:0]	2
0xBB0170B0	OAM_P_CTRL_0 [0].OAM_PARSER[1:0]	2
0xBB0170B0	OAM_P_CTRL_0 [1].OAM_PARSER[3:2]	2
0xBB0170B0	OAM_P_CTRL_0 [2].OAM_PARSER[5:4]	2
0xBB0170B0	OAM_P_CTRL_0 [3].OAM_PARSER[7:6]	2
0xBB0170B0	OAM_P_CTRL_0 [4].OAM_PARSER[9:8]	2
0xBB0170B0	OAM_P_CTRL_0 [5].OAM_PARSER[11:10]	2
0xBB0170B0	OAM_P_CTRL_0 [6].OAM_PARSER[13:12]	2
0xBB0170B4	OAM_P_CTRL_1 [0].OAM_MULTIPLEXER[1:0]	2
0xBB0170B4	OAM_P_CTRL_1 [1].OAM_MULTIPLEXER[3:2]	2
0xBB0170B4	OAM_P_CTRL_1 [2].OAM_MULTIPLEXER[5:4]	2
0xBB0170B4	OAM_P_CTRL_1 [3].OAM_MULTIPLEXER[7:6]	2
0xBB0170B4	OAM_P_CTRL_1 [4].OAM_MULTIPLEXER[9:8]	2
0xBB0170B4	OAM_P_CTRL_1 [5].OAM_MULTIPLEXER[11:10]	2
0xBB0170B4	OAM_P_CTRL_1 [6].OAM_MULTIPLEXER[13:12]	2
0xBB0170B8	OAM_CTRL_1.RESERVED[31:1]	31
0xBB0170B8	OAM_CTRL_1.OAM_ENABLE[0:0]	1
0xBB0170BC	RGF_VER_ALE_L2.REGFILE_VER[31:0]	32
0xBB0170C0	RSVD_ALE_L2 [0].RSVD_MEM[31:0]	32
0xBB0170C4	RSVD_ALE_L2 [1].RSVD_MEM[31:0]	32
0xBB0170C8	RSVD_ALE_L2 [2].RSVD_MEM[31:0]	32
0xBB0170CC	RSVD_ALE_L2 [3].RSVD_MEM[31:0]	32
0xBB0170D0	RSVD_ALE_L2 [4].RSVD_MEM[31:0]	32
0xBB0170D4	RSVD_ALE_L2 [5].RSVD_MEM[31:0]	32
0xBB0170D8	RSVD_ALE_L2 [6].RSVD_MEM[31:0]	32
0xBB0170DC	RSVD_ALE_L2 [7].RSVD_MEM[31:0]	32
0xBB0170E0	RSVD_ALE_L2 [8].RSVD_MEM[31:0]	32
0xBB0170E4	RSVD_ALE_L2 [9].RSVD_MEM[31:0]	32
0xBB0170E8	RSVD_ALE_L2 [10].RSVD_MEM[31:0]	32
0xBB0170EC	RSVD_ALE_L2 [11].RSVD_MEM[31:0]	32
0xBB0170F0	RSVD_ALE_L2 [12].RSVD_MEM[31:0]	32
0xBB0170F4	RSVD_ALE_L2 [13].RSVD_MEM[31:0]	32
0xBB0170F8	RSVD_ALE_L2 [14].RSVD_MEM[31:0]	32
0xBB0170FC	RSVD_ALE_L2 [15].RSVD_MEM[31:0]	32
0xBB018000	SVLAN_MC2S [0].RESERVED[31:8]	24
0xBB018000	SVLAN_MC2S [0].SVIDX[7:2]	6
0xBB018000	SVLAN_MC2S [0].FORMAT[1:1]	1
0xBB018000	SVLAN_MC2S [0].VALID[0:0]	1
0xBB018004	SVLAN_MC2S [0].DATA[31:0]	32

Address	Register	Len
0xBB018008	SVLAN_MC2S [0].MASK[31:0]	32
0xBB01800C	SVLAN_MC2S [1].RESERVED[31:8]	24
0xBB01800C	SVLAN_MC2S [1].SVIDX[7:2]	6
0xBB01800C	SVLAN_MC2S [1].FORMAT[1:1]	1
0xBB01800C	SVLAN_MC2S [1].VALID[0:0]	1
0xBB018010	SVLAN_MC2S [1].DATA[31:0]	32
0xBB018014	SVLAN_MC2S [1].MASK[31:0]	32
0xBB018018	SVLAN_MC2S [2].RESERVED[31:8]	24
0xBB018018	SVLAN_MC2S [2].SVIDX[7:2]	6
0xBB018018	SVLAN_MC2S [2].FORMAT[1:1]	1
0xBB018018	SVLAN_MC2S [2].VALID[0:0]	1
0xBB01801C	SVLAN_MC2S [2].DATA[31:0]	32
0xBB018020	SVLAN_MC2S [2].MASK[31:0]	32
0xBB018024	SVLAN_MC2S [3].RESERVED[31:8]	24
0xBB018024	SVLAN_MC2S [3].SVIDX[7:2]	6
0xBB018024	SVLAN_MC2S [3].FORMAT[1:1]	1
0xBB018024	SVLAN_MC2S [3].VALID[0:0]	1
0xBB018028	SVLAN_MC2S [3].DATA[31:0]	32
0xBB01802C	SVLAN_MC2S [3].MASK[31:0]	32
0xBB018030	SVLAN_MC2S [4].RESERVED[31:8]	24
0xBB018030	SVLAN_MC2S [4].SVIDX[7:2]	6
0xBB018030	SVLAN_MC2S [4].FORMAT[1:1]	1
0xBB018030	SVLAN_MC2S [4].VALID[0:0]	1
0xBB018034	SVLAN_MC2S [4].DATA[31:0]	32
0xBB018038	SVLAN_MC2S [4].MASK[31:0]	32
0xBB01803C	SVLAN_MC2S [5].RESERVED[31:8]	24
0xBB01803C	SVLAN_MC2S [5].SVIDX[7:2]	6
0xBB01803C	SVLAN_MC2S [5].FORMAT[1:1]	1
0xBB01803C	SVLAN_MC2S [5].VALID[0:0]	1
0xBB018040	SVLAN_MC2S [5].DATA[31:0]	32
0xBB018044	SVLAN_MC2S [5].MASK[31:0]	32
0xBB018048	SVLAN_MC2S [6].RESERVED[31:8]	24
0xBB018048	SVLAN_MC2S [6].SVIDX[7:2]	6
0xBB018048	SVLAN_MC2S [6].FORMAT[1:1]	1
0xBB018048	SVLAN_MC2S [6].VALID[0:0]	1
0xBB01804C	SVLAN_MC2S [6].DATA[31:0]	32
0xBB018050	SVLAN_MC2S [6].MASK[31:0]	32
0xBB018054	SVLAN_MC2S [7].RESERVED[31:8]	24
0xBB018054	SVLAN_MC2S [7].SVIDX[7:2]	6
0xBB018054	SVLAN_MC2S [7].FORMAT[1:1]	1
0xBB018054	SVLAN_MC2S [7].VALID[0:0]	1
0xBB018058	SVLAN_MC2S [7].DATA[31:0]	32
0xBB01805C	SVLAN_MC2S [7].MASK[31:0]	32
0xBB018060	RGF_VER_ALE_MLTVLAN.REGFILE_VER[31:0]	32
0xBB018064	RSVD_ALE_MLTVLAN [0].RSVD_MEM[31:0]	32
0xBB018068	RSVD_ALE_MLTVLAN [1].RSVD_MEM[31:0]	32

Address	Register	Len
0xBB01806C	RSVD_ALE_MLTVLAN [2].RSVD_MEM[31:0]	32
0xBB018070	RSVD_ALE_MLTVLAN [3].RSVD_MEM[31:0]	32
0xBB018074	RSVD_ALE_MLTVLAN [4].RSVD_MEM[31:0]	32
0xBB018078	RSVD_ALE_MLTVLAN [5].RSVD_MEM[31:0]	32
0xBB01807C	RSVD_ALE_MLTVLAN [6].RSVD_MEM[31:0]	32
0xBB018080	RSVD_ALE_MLTVLAN [7].RSVD_MEM[31:0]	32
0xBB018084	RSVD_ALE_MLTVLAN [8].RSVD_MEM[31:0]	32
0xBB018088	RSVD_ALE_MLTVLAN [9].RSVD_MEM[31:0]	32
0xBB01808C	RSVD_ALE_MLTVLAN [10].RSVD_MEM[31:0]	32
0xBB018090	RSVD_ALE_MLTVLAN [11].RSVD_MEM[31:0]	32
0xBB018094	RSVD_ALE_MLTVLAN [12].RSVD_MEM[31:0]	32
0xBB018098	RSVD_ALE_MLTVLAN [13].RSVD_MEM[31:0]	32
0xBB01809C	RSVD_ALE_MLTVLAN [14].RSVD_MEM[31:0]	32
0xBB0180A0	RSVD_ALE_MLTVLAN [15].RSVD_MEM[31:0]	32
0xBB019000	RGF_VER_ALE_EEE_LLDP.REGFILE_VER[31:0]	32
0xBB019004	RSVD_ALE_EEE_LLDP [0].RSVD_MEM[31:0]	32
0xBB019008	RSVD_ALE_EEE_LLDP [1].RSVD_MEM[31:0]	32
0xBB01900C	RSVD_ALE_EEE_LLDP [2].RSVD_MEM[31:0]	32
0xBB019010	RSVD_ALE_EEE_LLDP [3].RSVD_MEM[31:0]	32
0xBB019014	RSVD_ALE_EEE_LLDP [4].RSVD_MEM[31:0]	32
0xBB019018	RSVD_ALE_EEE_LLDP [5].RSVD_MEM[31:0]	32
0xBB01901C	RSVD_ALE_EEE_LLDP [6].RSVD_MEM[31:0]	32
0xBB019020	RSVD_ALE_EEE_LLDP [7].RSVD_MEM[31:0]	32
0xBB019024	RSVD_ALE_EEE_LLDP [8].RSVD_MEM[31:0]	32
0xBB019028	RSVD_ALE_EEE_LLDP [9].RSVD_MEM[31:0]	32
0xBB01902C	RSVD_ALE_EEE_LLDP [10].RSVD_MEM[31:0]	32
0xBB019030	RSVD_ALE_EEE_LLDP [11].RSVD_MEM[31:0]	32
0xBB019034	RSVD_ALE_EEE_LLDP [12].RSVD_MEM[31:0]	32
0xBB019038	RSVD_ALE_EEE_LLDP [13].RSVD_MEM[31:0]	32
0xBB01903C	RSVD_ALE_EEE_LLDP [14].RSVD_MEM[31:0]	32
0xBB019040	RSVD_ALE_EEE_LLDP [15].RSVD_MEM[31:0]	32
0xBB01A000	RLDP_CTRL_1.RESERVED[31:6]	26
0xBB01A000	RLDP_CTRL_1.TRIG_MODE[5:5]	1
0xBB01A000	RLDP_CTRL_1.RESERVED[4:4]	1
0xBB01A000	RLDP_CTRL_1.GEN_RNDM[3:3]	1
0xBB01A000	RLDP_CTRL_1.CMP_TYPE[2:2]	1
0xBB01A000	RLDP_CTRL_1.CPU_HANDLE[1:1]	1
0xBB01A000	RLDP_CTRL_1.EN[0:0]	1
0xBB01A004	RLDP_CHK_STS_CTRL.RESERVED[31:24]	8
0xBB01A004	RLDP_CHK_STS_CTRL.PERIOD[23:8]	16
0xBB01A004	RLDP_CHK_STS_CTRL.CNT[7:0]	8
0xBB01A008	RLDP_LP_STS_CTRL.RESERVED[31:24]	8
0xBB01A008	RLDP_LP_STS_CTRL.PERIOD[23:8]	16
0xBB01A008	RLDP_LP_STS_CTRL.CNT[7:0]	8
0xBB01A00C	RLDP_RNDM_NUM.RESERVED[31:16]	16
0xBB01A00C	RLDP_RNDM_NUM.NUM_47_32[15:0]	16

Address	Register	Len
0xBB01A010	RLDP_RNDM_NUM.NUM_31_0[31:0]	32
0xBB01A014	RLDP_MAGIC_NUM.RESERVED[31:16]	16
0xBB01A014	RLDP_MAGIC_NUM.NUM_47_32[15:0]	16
0xBB01A018	RLDP_MAGIC_NUM.NUM_31_0[31:0]	32
0xBB01A01C	RLDP_PORT_TX_EN [0].EN[0:0]	1
0xBB01A01C	RLDP_PORT_TX_EN [1].EN[1:1]	1
0xBB01A01C	RLDP_PORT_TX_EN [2].EN[2:2]	1
0xBB01A01C	RLDP_PORT_TX_EN [3].EN[3:3]	1
0xBB01A01C	RLDP_PORT_TX_EN [4].EN[4:4]	1
0xBB01A01C	RLDP_PORT_TX_EN [5].EN[5:5]	1
0xBB01A020	RLDP_PORT_LP_ENTER_STS [0].STS[0:0]	1
0xBB01A020	RLDP_PORT_LP_ENTER_STS [1].STS[1:1]	1
0xBB01A020	RLDP_PORT_LP_ENTER_STS [2].STS[2:2]	1
0xBB01A020	RLDP_PORT_LP_ENTER_STS [3].STS[3:3]	1
0xBB01A020	RLDP_PORT_LP_ENTER_STS [4].STS[4:4]	1
0xBB01A020	RLDP_PORT_LP_ENTER_STS [5].STS[5:5]	1
0xBB01A024	RLDP_PORT_LP_LEAVE_STS [0].STS[0:0]	1
0xBB01A024	RLDP_PORT_LP_LEAVE_STS [1].STS[1:1]	1
0xBB01A024	RLDP_PORT_LP_LEAVE_STS [2].STS[2:2]	1
0xBB01A024	RLDP_PORT_LP_LEAVE_STS [3].STS[3:3]	1
0xBB01A024	RLDP_PORT_LP_LEAVE_STS [4].STS[4:4]	1
0xBB01A024	RLDP_PORT_LP_LEAVE_STS [5].STS[5:5]	1
0xBB01A028	RLDP_PORT_LP_STS [0].STS[0:0]	1
0xBB01A028	RLDP_PORT_LP_STS [1].STS[1:1]	1
0xBB01A028	RLDP_PORT_LP_STS [2].STS[2:2]	1
0xBB01A028	RLDP_PORT_LP_STS [3].STS[3:3]	1
0xBB01A028	RLDP_PORT_LP_STS [4].STS[4:4]	1
0xBB01A028	RLDP_PORT_LP_STS [5].STS[5:5]	1
0xBB01A02C	RLDP_PORT_CPU_LP_STS [0].STS[0:0]	1
0xBB01A02C	RLDP_PORT_CPU_LP_STS [1].STS[1:1]	1
0xBB01A02C	RLDP_PORT_CPU_LP_STS [2].STS[2:2]	1
0xBB01A02C	RLDP_PORT_CPU_LP_STS [3].STS[3:3]	1
0xBB01A02C	RLDP_PORT_CPU_LP_STS [4].STS[4:4]	1
0xBB01A02C	RLDP_PORT_CPU_LP_STS [5].STS[5:5]	1
0xBB01A030	RLDP_PORT_LP_PNUM [0].P_NUM[2:0]	3
0xBB01A030	RLDP_PORT_LP_PNUM [1].P_NUM[5:3]	3
0xBB01A030	RLDP_PORT_LP_PNUM [2].P_NUM[8:6]	3
0xBB01A030	RLDP_PORT_LP_PNUM [3].P_NUM[11:9]	3
0xBB01A030	RLDP_PORT_LP_PNUM [4].P_NUM[14:12]	3
0xBB01A030	RLDP_PORT_LP_PNUM [5].P_NUM[17:15]	3
0xBB01A034	RLPP_CTRL.RESERVED[31:1]	31
0xBB01A034	RLPP_CTRL.TRAP_EN[0:0]	1
0xBB01A038	RGF_VER_ALE_RLDP.REGFILE_VER[31:0]	32
0xBB01A03C	RSVD_ALE_RLDP [0].RSVD_MEM[31:0]	32
0xBB01A040	RSVD_ALE_RLDP [1].RSVD_MEM[31:0]	32
0xBB01A044	RSVD_ALE_RLDP [2].RSVD_MEM[31:0]	32

Address	Register	Len
0xBB01A048	RSVD_ALE_RLDP [3].RSVD_MEM[31:0]	32
0xBB01A04C	RSVD_ALE_RLDP [4].RSVD_MEM[31:0]	32
0xBB01A050	RSVD_ALE_RLDP [5].RSVD_MEM[31:0]	32
0xBB01A054	RSVD_ALE_RLDP [6].RSVD_MEM[31:0]	32
0xBB01A058	RSVD_ALE_RLDP [7].RSVD_MEM[31:0]	32
0xBB01A05C	RSVD_ALE_RLDP [8].RSVD_MEM[31:0]	32
0xBB01A060	RSVD_ALE_RLDP [9].RSVD_MEM[31:0]	32
0xBB01A064	RSVD_ALE_RLDP [10].RSVD_MEM[31:0]	32
0xBB01A068	RSVD_ALE_RLDP [11].RSVD_MEM[31:0]	32
0xBB01A06C	RSVD_ALE_RLDP [12].RSVD_MEM[31:0]	32
0xBB01A070	RSVD_ALE_RLDP [13].RSVD_MEM[31:0]	32
0xBB01A074	RSVD_ALE_RLDP [14].RSVD_MEM[31:0]	32
0xBB01A078	RSVD_ALE_RLDP [15].RSVD_MEM[31:0]	32
0xBB01B000	FB_CTRL.RESERVED[31:17]	15
0xBB01B000	FB_CTRL.STOP_TMR[16:16]	1
0xBB01B000	FB_CTRL.ERR_TH[15:13]	3
0xBB01B000	FB_CTRL.MAX_TH[12:10]	3
0xBB01B000	FB_CTRL.TO_IGNORE[9:9]	1
0xBB01B000	FB_CTRL.TO_TH[8:1]	8
0xBB01B000	FB_CTRL.PL_DEC_EN[0:0]	1
0xBB01B004	FB_PORT_CFG [0].RESERVED[31:4]	28
0xBB01B004	FB_PORT_CFG [0].CPL[3:3]	1
0xBB01B004	FB_PORT_CFG [0].VALID_FLOW[2:2]	1
0xBB01B004	FB_PORT_CFG [0].RST_PL[1:1]	1
0xBB01B004	FB_PORT_CFG [0].EN[0:0]	1
0xBB01B008	FB_PORT_CFG [1].RESERVED[31:4]	28
0xBB01B008	FB_PORT_CFG [1].CPL[3:3]	1
0xBB01B008	FB_PORT_CFG [1].VALID_FLOW[2:2]	1
0xBB01B008	FB_PORT_CFG [1].RST_PL[1:1]	1
0xBB01B008	FB_PORT_CFG [1].EN[0:0]	1
0xBB01B00C	FB_PORT_CFG [2].RESERVED[31:4]	28
0xBB01B00C	FB_PORT_CFG [2].CPL[3:3]	1
0xBB01B00C	FB_PORT_CFG [2].VALID_FLOW[2:2]	1
0xBB01B00C	FB_PORT_CFG [2].RST_PL[1:1]	1
0xBB01B00C	FB_PORT_CFG [2].EN[0:0]	1
0xBB01B010	FB_PORT_CFG [3].RESERVED[31:4]	28
0xBB01B010	FB_PORT_CFG [3].CPL[3:3]	1
0xBB01B010	FB_PORT_CFG [3].VALID_FLOW[2:2]	1
0xBB01B010	FB_PORT_CFG [3].RST_PL[1:1]	1
0xBB01B010	FB_PORT_CFG [3].EN[0:0]	1
0xBB01B014	FB_PORT_CFG [4].RESERVED[31:4]	28
0xBB01B014	FB_PORT_CFG [4].CPL[3:3]	1
0xBB01B014	FB_PORT_CFG [4].VALID_FLOW[2:2]	1
0xBB01B014	FB_PORT_CFG [4].RST_PL[1:1]	1
0xBB01B014	FB_PORT_CFG [4].EN[0:0]	1
0xBB01B018	FB_PORT_ERR_CNT [0].CNT[7:0]	8

Address	Register	Len
0xBB01B018	FB_PORT_ERR_CNT [1].CNT[15:8]	8
0xBB01B018	FB_PORT_ERR_CNT [2].CNT[23:16]	8
0xBB01B018	FB_PORT_ERR_CNT [3].CNT[31:24]	8
0xBB01B01C	FB_PORT_ERR_CNT [4].CNT[7:0]	8
0xBB01B020	FB_PORT_MONITOR_CNT [0].CNT[27:0]	28
0xBB01B024	FB_PORT_MONITOR_CNT [1].CNT[27:0]	28
0xBB01B028	FB_PORT_MONITOR_CNT [2].CNT[27:0]	28
0xBB01B02C	FB_PORT_MONITOR_CNT [3].CNT[27:0]	28
0xBB01B030	FB_PORT_MONITOR_CNT [4].CNT[27:0]	28
0xBB01B034	PTP_TIME_SEC.RESERVED[31:16]	16
0xBB01B034	PTP_TIME_SEC.SEC_47_32[15:0]	16
0xBB01B038	PTP_TIME_SEC.SEC_31_0[31:0]	32
0xBB01B03C	PTP_TIME_NSEC.NSEC_UNIT[31:3]	29
0xBB01B03C	PTP_TIME_NSEC.RESERVED[2:0]	3
0xBB01B040	PTP_TIME_OFFSET_SEC.RESERVED[31:16]	16
0xBB01B040	PTP_TIME_OFFSET_SEC.SEC_47_32[15:0]	16
0xBB01B044	PTP_TIME_OFFSET_SEC.SEC_31_0[31:0]	32
0xBB01B048	PTP_TIME_OFFSET_8NSEC.NSEC_UNIT[31:3]	29
0xBB01B048	PTP_TIME_OFFSET_8NSEC.RESERVED[2:0]	3
0xBB01B04C	PTP_TIME_FREQ.RESERVED[31:27]	5
0xBB01B04C	PTP_TIME_FREQ.FREQ[26:0]	27
0xBB01B050	PTP_TIME_CTRL.RESERVED[31:2]	30
0xBB01B050	PTP_TIME_CTRL.PTP_TIME_LATCH[1:1]	1
0xBB01B050	PTP_TIME_CTRL.CMD[0:0]	1
0xBB01B054	PTP_MEANPATH_DEALY.RESERVED[31:31]	1
0xBB01B054	PTP_MEANPATH_DEALY.DELAY[30:0]	31
0xBB01B058	RGF_VER_ALE_EAV_AFBK.REGFILE_VER[31:0]	32
0xBB01B05C	RSVD_ALE_EAV_AFBK [0].RSVD_MEM[31:0]	32
0xBB01B060	RSVD_ALE_EAV_AFBK [1].RSVD_MEM[31:0]	32
0xBB01B064	RSVD_ALE_EAV_AFBK [2].RSVD_MEM[31:0]	32
0xBB01B068	RSVD_ALE_EAV_AFBK [3].RSVD_MEM[31:0]	32
0xBB01B06C	RSVD_ALE_EAV_AFBK [4].RSVD_MEM[31:0]	32
0xBB01B070	RSVD_ALE_EAV_AFBK [5].RSVD_MEM[31:0]	32
0xBB01B074	RSVD_ALE_EAV_AFBK [6].RSVD_MEM[31:0]	32
0xBB01B078	RSVD_ALE_EAV_AFBK [7].RSVD_MEM[31:0]	32
0xBB01B07C	RSVD_ALE_EAV_AFBK [8].RSVD_MEM[31:0]	32
0xBB01B080	RSVD_ALE_EAV_AFBK [9].RSVD_MEM[31:0]	32
0xBB01B084	RSVD_ALE_EAV_AFBK [10].RSVD_MEM[31:0]	32
0xBB01B088	RSVD_ALE_EAV_AFBK [11].RSVD_MEM[31:0]	32
0xBB01B08C	RSVD_ALE_EAV_AFBK [12].RSVD_MEM[31:0]	32
0xBB01B090	RSVD_ALE_EAV_AFBK [13].RSVD_MEM[31:0]	32
0xBB01B094	RSVD_ALE_EAV_AFBK [14].RSVD_MEM[31:0]	32
0xBB01B098	RSVD_ALE_EAV_AFBK [15].RSVD_MEM[31:0]	32
0xBB01B09C	FB_GPHY_ADDR_CTRL.RESERVED[31:21]	11
0xBB01B09C	FB_GPHY_ADDR_CTRL.GPHY_REG_ADDR[20:16]	5
0xBB01B09C	FB_GPHY_ADDR_CTRL.GPHY_REG_PAGE[15:0]	16

Address	Register	Len
0xBB01C000	LUT_UNMATCHED_SA_CTRL [0].ACT[1:0]	2
0xBB01C000	LUT_UNMATCHED_SA_CTRL [1].ACT[3:2]	2
0xBB01C000	LUT_UNMATCHED_SA_CTRL [2].ACT[5:4]	2
0xBB01C000	LUT_UNMATCHED_SA_CTRL [3].ACT[7:6]	2
0xBB01C000	LUT_UNMATCHED_SA_CTRL [4].ACT[9:8]	2
0xBB01C000	LUT_UNMATCHED_SA_CTRL [5].ACT[11:10]	2
0xBB01C000	LUT_UNMATCHED_SA_CTRL [6].ACT[13:12]	2
0xBB01C004	LUT_UNKN_SA_CTRL [0].ACT[1:0]	2
0xBB01C004	LUT_UNKN_SA_CTRL [1].ACT[3:2]	2
0xBB01C004	LUT_UNKN_SA_CTRL [2].ACT[5:4]	2
0xBB01C004	LUT_UNKN_SA_CTRL [3].ACT[7:6]	2
0xBB01C004	LUT_UNKN_SA_CTRL [4].ACT[9:8]	2
0xBB01C004	LUT_UNKN_SA_CTRL [5].ACT[11:10]	2
0xBB01C004	LUT_UNKN_SA_CTRL [6].ACT[13:12]	2
0xBB01C008	LUT_UNKN_UC_DA_CTRL [0].ACT[1:0]	2
0xBB01C008	LUT_UNKN_UC_DA_CTRL [1].ACT[3:2]	2
0xBB01C008	LUT_UNKN_UC_DA_CTRL [2].ACT[5:4]	2
0xBB01C008	LUT_UNKN_UC_DA_CTRL [3].ACT[7:6]	2
0xBB01C008	LUT_UNKN_UC_DA_CTRL [4].ACT[9:8]	2
0xBB01C008	LUT_UNKN_UC_DA_CTRL [5].ACT[11:10]	2
0xBB01C008	LUT_UNKN_UC_DA_CTRL [6].ACT[13:12]	2
0xBB01C00C	LUT_LEARN_OVER_CTRL [0].ACT[1:0]	2
0xBB01C00C	LUT_LEARN_OVER_CTRL [1].ACT[3:2]	2
0xBB01C00C	LUT_LEARN_OVER_CTRL [2].ACT[5:4]	2
0xBB01C00C	LUT_LEARN_OVER_CTRL [3].ACT[7:6]	2
0xBB01C00C	LUT_LEARN_OVER_CTRL [4].ACT[9:8]	2
0xBB01C00C	LUT_LEARN_OVER_CTRL [5].ACT[11:10]	2
0xBB01C00C	LUT_LEARN_OVER_CTRL [6].ACT[13:12]	2
0xBB01C010	UNKN_L2_MC [0].ACT[1:0]	2
0xBB01C010	UNKN_L2_MC [1].ACT[3:2]	2
0xBB01C010	UNKN_L2_MC [2].ACT[5:4]	2
0xBB01C010	UNKN_L2_MC [3].ACT[7:6]	2
0xBB01C010	UNKN_L2_MC [4].ACT[9:8]	2
0xBB01C010	UNKN_L2_MC [5].ACT[11:10]	2
0xBB01C010	UNKN_L2_MC [6].ACT[13:12]	2
0xBB01C014	UNKN_IP4_MC [0].ACT[1:0]	2
0xBB01C014	UNKN_IP4_MC [1].ACT[3:2]	2
0xBB01C014	UNKN_IP4_MC [2].ACT[5:4]	2
0xBB01C014	UNKN_IP4_MC [3].ACT[7:6]	2
0xBB01C014	UNKN_IP4_MC [4].ACT[9:8]	2
0xBB01C014	UNKN_IP4_MC [5].ACT[11:10]	2
0xBB01C014	UNKN_IP4_MC [6].ACT[13:12]	2
0xBB01C018	UNKN_IP6_MC [0].ACT[1:0]	2
0xBB01C018	UNKN_IP6_MC [1].ACT[3:2]	2
0xBB01C018	UNKN_IP6_MC [2].ACT[5:4]	2
0xBB01C018	UNKN_IP6_MC [3].ACT[7:6]	2

Address	Register	Len
0xBB01C018	UNKN_IP6_MC [4].ACT[9:8]	2
0xBB01C018	UNKN_IP6_MC [5].ACT[11:10]	2
0xBB01C018	UNKN_IP6_MC [6].ACT[13:12]	2
0xBB01C01C	UNKN_MC_PRI.RESERVED[31:3]	29
0xBB01C01C	UNKN_MC_PRI.UNKN_MC_PRI[2:0]	3
0xBB01C020	LUT_BC_FLOOD [0].EN[0:0]	1
0xBB01C020	LUT_BC_FLOOD [1].EN[1:1]	1
0xBB01C020	LUT_BC_FLOOD [2].EN[2:2]	1
0xBB01C020	LUT_BC_FLOOD [3].EN[3:3]	1
0xBB01C020	LUT_BC_FLOOD [4].EN[4:4]	1
0xBB01C020	LUT_BC_FLOOD [5].EN[5:5]	1
0xBB01C020	LUT_BC_FLOOD [6].EN[6:6]	1
0xBB01C024	LUT_UNKN_MC_FLOOD [0].EN[0:0]	1
0xBB01C024	LUT_UNKN_MC_FLOOD [1].EN[1:1]	1
0xBB01C024	LUT_UNKN_MC_FLOOD [2].EN[2:2]	1
0xBB01C024	LUT_UNKN_MC_FLOOD [3].EN[3:3]	1
0xBB01C024	LUT_UNKN_MC_FLOOD [4].EN[4:4]	1
0xBB01C024	LUT_UNKN_MC_FLOOD [5].EN[5:5]	1
0xBB01C024	LUT_UNKN_MC_FLOOD [6].EN[6:6]	1
0xBB01C028	LUT_UNKN_UC_FLOOD [0].EN[0:0]	1
0xBB01C028	LUT_UNKN_UC_FLOOD [1].EN[1:1]	1
0xBB01C028	LUT_UNKN_UC_FLOOD [2].EN[2:2]	1
0xBB01C028	LUT_UNKN_UC_FLOOD [3].EN[3:3]	1
0xBB01C028	LUT_UNKN_UC_FLOOD [4].EN[4:4]	1
0xBB01C028	LUT_UNKN_UC_FLOOD [5].EN[5:5]	1
0xBB01C028	LUT_UNKN_UC_FLOOD [6].EN[6:6]	1
0xBB01C02C	L2_IPMC_VLAN_LEAKY [0].EN[0:0]	1
0xBB01C02C	L2_IPMC_VLAN_LEAKY [1].EN[1:1]	1
0xBB01C02C	L2_IPMC_VLAN_LEAKY [2].EN[2:2]	1
0xBB01C02C	L2_IPMC_VLAN_LEAKY [3].EN[3:3]	1
0xBB01C02C	L2_IPMC_VLAN_LEAKY [4].EN[4:4]	1
0xBB01C02C	L2_IPMC_VLAN_LEAKY [5].EN[5:5]	1
0xBB01C02C	L2_IPMC_VLAN_LEAKY [6].EN[6:6]	1
0xBB01C030	L2_IPMC_ISO_LEAKY [0].EN[0:0]	1
0xBB01C030	L2_IPMC_ISO_LEAKY [1].EN[1:1]	1
0xBB01C030	L2_IPMC_ISO_LEAKY [2].EN[2:2]	1
0xBB01C030	L2_IPMC_ISO_LEAKY [3].EN[3:3]	1
0xBB01C030	L2_IPMC_ISO_LEAKY [4].EN[4:4]	1
0xBB01C030	L2_IPMC_ISO_LEAKY [5].EN[5:5]	1
0xBB01C030	L2_IPMC_ISO_LEAKY [6].EN[6:6]	1
0xBB01C034	VLAN_PB_PRI [0].PB_PRI[2:0]	3
0xBB01C034	VLAN_PB_PRI [1].PB_PRI[5:3]	3
0xBB01C034	VLAN_PB_PRI [2].PB_PRI[8:6]	3
0xBB01C034	VLAN_PB_PRI [3].PB_PRI[11:9]	3
0xBB01C034	VLAN_PB_PRI [4].PB_PRI[14:12]	3
0xBB01C034	VLAN_PB_PRI [5].PB_PRI[17:15]	3



Address	Register	Len
0xBB01C034	VLAN_PB_PRI [6].PB_PRI[20:18]	3
0xBB01C038	VLAN_EGRESS_KEEP [0].MBR[6:0]	7
0xBB01C038	VLAN_EGRESS_KEEP [1].MBR[13:7]	7
0xBB01C038	VLAN_EGRESS_KEEP [2].MBR[20:14]	7
0xBB01C038	VLAN_EGRESS_KEEP [3].MBR[27:21]	7
0xBB01C03C	VLAN_EGRESS_KEEP [4].MBR[6:0]	7
0xBB01C03C	VLAN_EGRESS_KEEP [5].MBR[13:7]	7
0xBB01C03C	VLAN_EGRESS_KEEP [6].MBR[20:14]	7
0xBB01C040	PORT_TRUNK_GROUP_EN [0].RESERVED[31:1]	31
0xBB01C040	PORT_TRUNK_GROUP_EN [0].EN[0:0]	1
0xBB01C044	PORT_TRUNK_GROUP_EN [1].RESERVED[31:1]	31
0xBB01C044	PORT_TRUNK_GROUP_EN [1].EN[0:0]	1
0xBB01C048	PORT_TRUNK_GROUP_EN [2].RESERVED[31:1]	31
0xBB01C048	PORT_TRUNK_GROUP_EN [2].EN[0:0]	1
0xBB01C04C	PORT_TRUNK_GROUP_EN [3].RESERVED[31:1]	31
0xBB01C04C	PORT_TRUNK_GROUP_EN [3].EN[0:0]	1
0xBB01C050	PORT_TRUNK_CTRL.RESERVED[31:10]	22
0xBB01C050	PORT_TRUNK_CTRL.EN_FLOWCTRL_TG0[9:9]	1
0xBB01C050	PORT_TRUNK_CTRL.PORT_TRUNK_DUMB[8:8]	1
0xBB01C050	PORT_TRUNK_CTRL.PORT_TRUNK_FLOOD[7:7]	1
0xBB01C050	PORT_TRUNK_CTRL.DPORT_HASH[6:6]	1
0xBB01C050	PORT_TRUNK_CTRL.SPORT_HASH[5:5]	1
0xBB01C050	PORT_TRUNK_CTRL.DIP_HASH[4:4]	1
0xBB01C050	PORT_TRUNK_CTRL.SIP_HASH[3:3]	1
0xBB01C050	PORT_TRUNK_CTRL.DMAC_HASH[2:2]	1
0xBB01C050	PORT_TRUNK_CTRL.SMAC_HASH[1:1]	1
0xBB01C050	PORT_TRUNK_CTRL.SPA_HASH[0:0]	1
0xBB01C054	PORT_TRUNK_HASH_MAPPING [0].HASH[1:0]	2
0xBB01C054	PORT_TRUNK_HASH_MAPPING [1].HASH[3:2]	2
0xBB01C054	PORT_TRUNK_HASH_MAPPING [2].HASH[5:4]	2
0xBB01C054	PORT_TRUNK_HASH_MAPPING [3].HASH[7:6]	2
0xBB01C054	PORT_TRUNK_HASH_MAPPING [4].HASH[9:8]	2
0xBB01C054	PORT_TRUNK_HASH_MAPPING [5].HASH[11:10]	2
0xBB01C054	PORT_TRUNK_HASH_MAPPING [6].HASH[13:12]	2
0xBB01C054	PORT_TRUNK_HASH_MAPPING [7].HASH[15:14]	2
0xBB01C054	PORT_TRUNK_HASH_MAPPING [8].HASH[17:16]	2
0xBB01C054	PORT_TRUNK_HASH_MAPPING [9].HASH[19:18]	2
0xBB01C054	PORT_TRUNK_HASH_MAPPING [10].HASH[21:20]	2
0xBB01C054	PORT_TRUNK_HASH_MAPPING [11].HASH[23:22]	2
0xBB01C054	PORT_TRUNK_HASH_MAPPING [12].HASH[25:24]	2
0xBB01C054	PORT_TRUNK_HASH_MAPPING [13].HASH[27:26]	2
0xBB01C054	PORT_TRUNK_HASH_MAPPING [14].HASH[29:28]	2
0xBB01C054	PORT_TRUNK_HASH_MAPPING [15].HASH[31:30]	2
0xBB01C058	RMA_CTRL00.RESERVED[31:6]	26
0xBB01C058	RMA_CTRL00.OPERATION[5:4]	2
0xBB01C058	RMA_CTRL00.DISCARD_STORM_FILTER[3:3]	1

Address	Register	Len
0xBB01C058	RMA_CTRL00.KEEP_FORMAT[2:2]	1
0xBB01C058	RMA_CTRL00.VLAN_LEAKY[1:1]	1
0xBB01C058	RMA_CTRL00.PORTISO_LEAKY[0:0]	1
0xBB01C05C	RMA_CTRL01.RESERVED[31:6]	26
0xBB01C05C	RMA_CTRL01.OPERATION[5:4]	2
0xBB01C05C	RMA_CTRL01.DISCARD_STORM_FILTER[3:3]	1
0xBB01C05C	RMA_CTRL01.KEEP_FORMAT[2:2]	1
0xBB01C05C	RMA_CTRL01.VLAN_LEAKY[1:1]	1
0xBB01C05C	RMA_CTRL01.PORTISO_LEAKY[0:0]	1
0xBB01C060	RMA_CTRL02.RESERVED[31:6]	26
0xBB01C060	RMA_CTRL02.OPERATION[5:4]	2
0xBB01C060	RMA_CTRL02.DISCARD_STORM_FILTER[3:3]	1
0xBB01C060	RMA_CTRL02.KEEP_FORMAT[2:2]	1
0xBB01C060	RMA_CTRL02.VLAN_LEAKY[1:1]	1
0xBB01C060	RMA_CTRL02.PORTISO_LEAKY[0:0]	1
0xBB01C064	RMA_CTRL03.RESERVED[31:6]	26
0xBB01C064	RMA_CTRL03.OPERATION[5:4]	2
0xBB01C064	RMA_CTRL03.DISCARD_STORM_FILTER[3:3]	1
0xBB01C064	RMA_CTRL03.KEEP_FORMAT[2:2]	1
0xBB01C064	RMA_CTRL03.VLAN_LEAKY[1:1]	1
0xBB01C064	RMA_CTRL03.PORTISO_LEAKY[0:0]	1
0xBB01C068	RMA_CTRL04.RESERVED[31:6]	26
0xBB01C068	RMA_CTRL04.OPERATION[5:4]	2
0xBB01C068	RMA_CTRL04.DISCARD_STORM_FILTER[3:3]	1
0xBB01C068	RMA_CTRL04.KEEP_FORMAT[2:2]	1
0xBB01C068	RMA_CTRL04.VLAN_LEAKY[1:1]	1
0xBB01C068	RMA_CTRL04.PORTISO_LEAKY[0:0]	1
0xBB01C06C	RMA_CTRL08.RESERVED[31:6]	26
0xBB01C06C	RMA_CTRL08.OPERATION[5:4]	2
0xBB01C06C	RMA_CTRL08.DISCARD_STORM_FILTER[3:3]	1
0xBB01C06C	RMA_CTRL08.KEEP_FORMAT[2:2]	1
0xBB01C06C	RMA_CTRL08.VLAN_LEAKY[1:1]	1
0xBB01C06C	RMA_CTRL08.PORTISO_LEAKY[0:0]	1
0xBB01C070	RMA_CTRL0D.RESERVED[31:6]	26
0xBB01C070	RMA_CTRL0D.OPERATION[5:4]	2
0xBB01C070	RMA_CTRL0D.DISCARD_STORM_FILTER[3:3]	1
0xBB01C070	RMA_CTRL0D.KEEP_FORMAT[2:2]	1
0xBB01C070	RMA_CTRL0D.VLAN_LEAKY[1:1]	1
0xBB01C070	RMA_CTRL0D.PORTISO_LEAKY[0:0]	1
0xBB01C074	RMA_CTRL0E.RESERVED[31:6]	26
0xBB01C074	RMA_CTRL0E.OPERATION[5:4]	2
0xBB01C074	RMA_CTRL0E.DISCARD_STORM_FILTER[3:3]	1
0xBB01C074	RMA_CTRL0E.KEEP_FORMAT[2:2]	1
0xBB01C074	RMA_CTRL0E.VLAN_LEAKY[1:1]	1
0xBB01C074	RMA_CTRL0E.PORTISO_LEAKY[0:0]	1
0xBB01C078	RMA_CTRL10.RESERVED[31:6]	26

Address	Register	Len
0xBB01C078	RMA_CTRL10.OPERATION[5:4]	2
0xBB01C078	RMA_CTRL10.DISCARD_STORM_FILTER[3:3]	1
0xBB01C078	RMA_CTRL10.KEEP_FORMAT[2:2]	1
0xBB01C078	RMA_CTRL10.VLAN_LEAKY[1:1]	1
0xBB01C078	RMA_CTRL10.PORTISO_LEAKY[0:0]	1
0xBB01C07C	RMA_CTRL11.RESERVED[31:6]	26
0xBB01C07C	RMA_CTRL11.OPERATION[5:4]	2
0xBB01C07C	RMA_CTRL11.DISCARD_STORM_FILTER[3:3]	1
0xBB01C07C	RMA_CTRL11.KEEP_FORMAT[2:2]	1
0xBB01C07C	RMA_CTRL11.VLAN_LEAKY[1:1]	1
0xBB01C07C	RMA_CTRL11.PORTISO_LEAKY[0:0]	1
0xBB01C080	RMA_CTRL12.RESERVED[31:6]	26
0xBB01C080	RMA_CTRL12.OPERATION[5:4]	2
0xBB01C080	RMA_CTRL12.DISCARD_STORM_FILTER[3:3]	1
0xBB01C080	RMA_CTRL12.KEEP_FORMAT[2:2]	1
0xBB01C080	RMA_CTRL12.VLAN_LEAKY[1:1]	1
0xBB01C080	RMA_CTRL12.PORTISO_LEAKY[0:0]	1
0xBB01C084	RMA_CTRL13.RESERVED[31:6]	26
0xBB01C084	RMA_CTRL13.OPERATION[5:4]	2
0xBB01C084	RMA_CTRL13.DISCARD_STORM_FILTER[3:3]	1
0xBB01C084	RMA_CTRL13.KEEP_FORMAT[2:2]	1
0xBB01C084	RMA_CTRL13.VLAN_LEAKY[1:1]	1
0xBB01C084	RMA_CTRL13.PORTISO_LEAKY[0:0]	1
0xBB01C088	RMA_CTRL18.RESERVED[31:6]	26
0xBB01C088	RMA_CTRL18.OPERATION[5:4]	2
0xBB01C088	RMA_CTRL18.DISCARD_STORM_FILTER[3:3]	1
0xBB01C088	RMA_CTRL18.KEEP_FORMAT[2:2]	1
0xBB01C088	RMA_CTRL18.VLAN_LEAKY[1:1]	1
0xBB01C088	RMA_CTRL18.PORTISO_LEAKY[0:0]	1
0xBB01C08C	RMA_CTRL1A.RESERVED[31:6]	26
0xBB01C08C	RMA_CTRL1A.OPERATION[5:4]	2
0xBB01C08C	RMA_CTRL1A.DISCARD_STORM_FILTER[3:3]	1
0xBB01C08C	RMA_CTRL1A.KEEP_FORMAT[2:2]	1
0xBB01C08C	RMA_CTRL1A.VLAN_LEAKY[1:1]	1
0xBB01C08C	RMA_CTRL1A.PORTISO_LEAKY[0:0]	1
0xBB01C090	RMA_CTRL20.RESERVED[31:6]	26
0xBB01C090	RMA_CTRL20.OPERATION[5:4]	2
0xBB01C090	RMA_CTRL20.DISCARD_STORM_FILTER[3:3]	1
0xBB01C090	RMA_CTRL20.KEEP_FORMAT[2:2]	1
0xBB01C090	RMA_CTRL20.VLAN_LEAKY[1:1]	1
0xBB01C090	RMA_CTRL20.PORTISO_LEAKY[0:0]	1
0xBB01C094	RMA_CTRL21.RESERVED[31:6]	26
0xBB01C094	RMA_CTRL21.OPERATION[5:4]	2
0xBB01C094	RMA_CTRL21.DISCARD_STORM_FILTER[3:3]	1
0xBB01C094	RMA_CTRL21.KEEP_FORMAT[2:2]	1
0xBB01C094	RMA_CTRL21.VLAN_LEAKY[1:1]	1

Address	Register	Len
0xBB01C094	RMA_CTRL21.PORTISO_LEAKY[0:0]	1
0xBB01C098	RMA_CTRL22.RESERVED[31:6]	26
0xBB01C098	RMA_CTRL22.OPERATION[5:4]	2
0xBB01C098	RMA_CTRL22.DISCARD_STORM_FILTER[3:3]	1
0xBB01C098	RMA_CTRL22.KEEP_FORMAT[2:2]	1
0xBB01C098	RMA_CTRL22.VLAN_LEAKY[1:1]	1
0xBB01C098	RMA_CTRL22.PORTISO_LEAKY[0:0]	1
0xBB01C09C	RMA_CTRL_CDP.RESERVED[31:6]	26
0xBB01C09C	RMA_CTRL_CDP.OPERATION[5:4]	2
0xBB01C09C	RMA_CTRL_CDP.DISCARD_STORM_FILTER[3:3]	1
0xBB01C09C	RMA_CTRL_CDP.KEEP_FORMAT[2:2]	1
0xBB01C09C	RMA_CTRL_CDP.VLAN_LEAKY[1:1]	1
0xBB01C09C	RMA_CTRL_CDP.PORTISO_LEAKY[0:0]	1
0xBB01C0A0	RMA_CTRL_SSTP.RESERVED[31:6]	26
0xBB01C0A0	RMA_CTRL_SSTP.OPERATION[5:4]	2
0xBB01C0A0	RMA_CTRL_SSTP.DISCARD_STORM_FILTER[3:3]	1
0xBB01C0A0	RMA_CTRL_SSTP.KEEP_FORMAT[2:2]	1
0xBB01C0A0	RMA_CTRL_SSTP.VLAN_LEAKY[1:1]	1
0xBB01C0A0	RMA_CTRL_SSTP.PORTISO_LEAKY[0:0]	1
0xBB01C0A4	RMA_CFG.RESERVED[31:3]	29
0xBB01C0A4	RMA_CFG.RMA_TRAP_PRIORITY[2:0]	3
0xBB01C0A8	EEELDP_CTRL_0.RESERVED[31:10]	22
0xBB01C0A8	EEELDP_CTRL_0.EN[9:9]	1
0xBB01C0A8	EEELDP_CTRL_0.TRAP_EN[8:8]	1
0xBB01C0A8	EEELDP_CTRL_0.SUBTYPE[7:0]	8
0xBB01C0AC	EEELDP_CTRL_1.RESERVED[31:3]	29
0xBB01C0AC	EEELDP_CTRL_1.TRAP_PRI[2:0]	3
0xBB01C0B0	L2_SRC_PORT_PERMIT [0].EN[0:0]	1
0xBB01C0B0	L2_SRC_PORT_PERMIT [1].EN[1:1]	1
0xBB01C0B0	L2_SRC_PORT_PERMIT [2].EN[2:2]	1
0xBB01C0B0	L2_SRC_PORT_PERMIT [3].EN[3:3]	1
0xBB01C0B0	L2_SRC_PORT_PERMIT [4].EN[4:4]	1
0xBB01C0B0	L2_SRC_PORT_PERMIT [5].EN[5:5]	1
0xBB01C0B0	L2_SRC_PORT_PERMIT [6].EN[6:6]	1
0xBB01C0B4	L2_SRC_EXT_PERMIT [0].EN[0:0]	1
0xBB01C0B4	L2_SRC_EXT_PERMIT [1].EN[1:1]	1
0xBB01C0B4	L2_SRC_EXT_PERMIT [2].EN[2:2]	1
0xBB01C0B4	L2_SRC_EXT_PERMIT [3].EN[3:3]	1
0xBB01C0B4	L2_SRC_EXT_PERMIT [4].EN[4:4]	1
0xBB01C0B8	IGR_BWCTRL_GLB_CTRL.RESERVED[31:1]	31
0xBB01C0B8	IGR_BWCTRL_GLB_CTRL.BYPASS_EN[0:0]	1
0xBB01C0BC	DOT1X_CFG_0.RESERVED[31:3]	29
0xBB01C0BC	DOT1X_CFG_0.DOT1X_PRIORITY[2:0]	3
0xBB01C0C0	STAT_PRIVATE_REASON [0].PKT_INFO[9:0]	10
0xBB01C0C0	STAT_PRIVATE_REASON [1].PKT_INFO[19:10]	10
0xBB01C0C0	STAT_PRIVATE_REASON [2].PKT_INFO[29:20]	10

Address	Register	Len
0xBB01C0C4	STAT_PRIVATE_REASON [3].PKT_INFO[9:0]	10
0xBB01C0C4	STAT_PRIVATE_REASON [4].PKT_INFO[19:10]	10
0xBB01C0C4	STAT_PRIVATE_REASON [5].PKT_INFO[29:20]	10
0xBB01C0C8	STAT_PRIVATE_REASON [6].PKT_INFO[9:0]	10
0xBB01C0CC	STAT_ACL_REASON [0].ACL_HIT_INFO[7:0]	8
0xBB01C0CC	STAT_ACL_REASON [1].ACL_HIT_INFO[15:8]	8
0xBB01C0CC	STAT_ACL_REASON [2].ACL_HIT_INFO[23:16]	8
0xBB01C0CC	STAT_ACL_REASON [3].ACL_HIT_INFO[31:24]	8
0xBB01C0D0	STAT_ACL_REASON [4].ACL_HIT_INFO[7:0]	8
0xBB01C0D0	STAT_ACL_REASON [5].ACL_HIT_INFO[15:8]	8
0xBB01C0D4	STAT_CF_REASON [0].CF_HIT_INFO[9:0]	10
0xBB01C0D4	STAT_CF_REASON [1].CF_HIT_INFO[19:10]	10
0xBB01C0D8	FC_P_Q_EGR_DROP_EN [0][0].TH[0:0]	1
0xBB01C0D8	FC_P_Q_EGR_DROP_EN [0][1].TH[1:1]	1
0xBB01C0D8	FC_P_Q_EGR_DROP_EN [0][2].TH[2:2]	1
0xBB01C0D8	FC_P_Q_EGR_DROP_EN [0][3].TH[3:3]	1
0xBB01C0D8	FC_P_Q_EGR_DROP_EN [0][4].TH[4:4]	1
0xBB01C0D8	FC_P_Q_EGR_DROP_EN [0][5].TH[5:5]	1
0xBB01C0D8	FC_P_Q_EGR_DROP_EN [0][6].TH[6:6]	1
0xBB01C0D8	FC_P_Q_EGR_DROP_EN [0][7].TH[7:7]	1
0xBB01C0DC	FC_P_Q_EGR_DROP_EN [1][0].TH[0:0]	1
0xBB01C0DC	FC_P_Q_EGR_DROP_EN [1][1].TH[1:1]	1
0xBB01C0DC	FC_P_Q_EGR_DROP_EN [1][2].TH[2:2]	1
0xBB01C0DC	FC_P_Q_EGR_DROP_EN [1][3].TH[3:3]	1
0xBB01C0DC	FC_P_Q_EGR_DROP_EN [1][4].TH[4:4]	1
0xBB01C0DC	FC_P_Q_EGR_DROP_EN [1][5].TH[5:5]	1
0xBB01C0DC	FC_P_Q_EGR_DROP_EN [1][6].TH[6:6]	1
0xBB01C0DC	FC_P_Q_EGR_DROP_EN [1][7].TH[7:7]	1
0xBB01C0E0	FC_P_Q_EGR_DROP_EN [2][0].TH[0:0]	1
0xBB01C0E0	FC_P_Q_EGR_DROP_EN [2][1].TH[1:1]	1
0xBB01C0E0	FC_P_Q_EGR_DROP_EN [2][2].TH[2:2]	1
0xBB01C0E0	FC_P_Q_EGR_DROP_EN [2][3].TH[3:3]	1
0xBB01C0E0	FC_P_Q_EGR_DROP_EN [2][4].TH[4:4]	1
0xBB01C0E0	FC_P_Q_EGR_DROP_EN [2][5].TH[5:5]	1
0xBB01C0E0	FC_P_Q_EGR_DROP_EN [2][6].TH[6:6]	1
0xBB01C0E0	FC_P_Q_EGR_DROP_EN [2][7].TH[7:7]	1
0xBB01C0E4	FC_P_Q_EGR_DROP_EN [3][0].TH[0:0]	1
0xBB01C0E4	FC_P_Q_EGR_DROP_EN [3][1].TH[1:1]	1
0xBB01C0E4	FC_P_Q_EGR_DROP_EN [3][2].TH[2:2]	1
0xBB01C0E4	FC_P_Q_EGR_DROP_EN [3][3].TH[3:3]	1
0xBB01C0E4	FC_P_Q_EGR_DROP_EN [3][4].TH[4:4]	1
0xBB01C0E4	FC_P_Q_EGR_DROP_EN [3][5].TH[5:5]	1
0xBB01C0E4	FC_P_Q_EGR_DROP_EN [3][6].TH[6:6]	1
0xBB01C0E4	FC_P_Q_EGR_DROP_EN [3][7].TH[7:7]	1
0xBB01C0E8	FC_P_Q_EGR_DROP_EN [4][0].TH[0:0]	1
0xBB01C0E8	FC_P_Q_EGR_DROP_EN [4][1].TH[1:1]	1

Address	Register	Len
0xBB01C0E8	FC_P_Q_EGR_DROP_EN [4][2].TH[2:2]	1
0xBB01C0E8	FC_P_Q_EGR_DROP_EN [4][3].TH[3:3]	1
0xBB01C0E8	FC_P_Q_EGR_DROP_EN [4][4].TH[4:4]	1
0xBB01C0E8	FC_P_Q_EGR_DROP_EN [4][5].TH[5:5]	1
0xBB01C0E8	FC_P_Q_EGR_DROP_EN [4][6].TH[6:6]	1
0xBB01C0E8	FC_P_Q_EGR_DROP_EN [4][7].TH[7:7]	1
0xBB01C0EC	FC_P_Q_EGR_DROP_EN [5][0].TH[0:0]	1
0xBB01C0EC	FC_P_Q_EGR_DROP_EN [5][1].TH[1:1]	1
0xBB01C0EC	FC_P_Q_EGR_DROP_EN [5][2].TH[2:2]	1
0xBB01C0EC	FC_P_Q_EGR_DROP_EN [5][3].TH[3:3]	1
0xBB01C0EC	FC_P_Q_EGR_DROP_EN [5][4].TH[4:4]	1
0xBB01C0EC	FC_P_Q_EGR_DROP_EN [5][5].TH[5:5]	1
0xBB01C0EC	FC_P_Q_EGR_DROP_EN [5][6].TH[6:6]	1
0xBB01C0EC	FC_P_Q_EGR_DROP_EN [5][7].TH[7:7]	1
0xBB01C0F0	FC_P_Q_EGR_DROP_EN [6][0].TH[0:0]	1
0xBB01C0F0	FC_P_Q_EGR_DROP_EN [6][1].TH[1:1]	1
0xBB01C0F0	FC_P_Q_EGR_DROP_EN [6][2].TH[2:2]	1
0xBB01C0F0	FC_P_Q_EGR_DROP_EN [6][3].TH[3:3]	1
0xBB01C0F0	FC_P_Q_EGR_DROP_EN [6][4].TH[4:4]	1
0xBB01C0F0	FC_P_Q_EGR_DROP_EN [6][5].TH[5:5]	1
0xBB01C0F0	FC_P_Q_EGR_DROP_EN [6][6].TH[6:6]	1
0xBB01C0F0	FC_P_Q_EGR_DROP_EN [6][7].TH[7:7]	1
0xBB01C0F4	QOS_INTPRI_TO_QID [0][0].PRI_TO_QID[2:0]	3
0xBB01C0F4	QOS_INTPRI_TO_QID [0][1].PRI_TO_QID[5:3]	3
0xBB01C0F4	QOS_INTPRI_TO_QID [0][2].PRI_TO_QID[8:6]	3
0xBB01C0F4	QOS_INTPRI_TO_QID [0][3].PRI_TO_QID[11:9]	3
0xBB01C0F4	QOS_INTPRI_TO_QID [0][4].PRI_TO_QID[14:12]	3
0xBB01C0F4	QOS_INTPRI_TO_QID [0][5].PRI_TO_QID[17:15]	3
0xBB01C0F4	QOS_INTPRI_TO_QID [0][6].PRI_TO_QID[20:18]	3
0xBB01C0F4	QOS_INTPRI_TO_QID [0][7].PRI_TO_QID[23:21]	3
0xBB01C0F8	QOS_INTPRI_TO_QID [1][0].PRI_TO_QID[2:0]	3
0xBB01C0F8	QOS_INTPRI_TO_QID [1][1].PRI_TO_QID[5:3]	3
0xBB01C0F8	QOS_INTPRI_TO_QID [1][2].PRI_TO_QID[8:6]	3
0xBB01C0F8	QOS_INTPRI_TO_QID [1][3].PRI_TO_QID[11:9]	3
0xBB01C0F8	QOS_INTPRI_TO_QID [1][4].PRI_TO_QID[14:12]	3
0xBB01C0F8	QOS_INTPRI_TO_QID [1][5].PRI_TO_QID[17:15]	3
0xBB01C0F8	QOS_INTPRI_TO_QID [1][6].PRI_TO_QID[20:18]	3
0xBB01C0F8	QOS_INTPRI_TO_QID [1][7].PRI_TO_QID[23:21]	3
0xBB01C0FC	QOS_INTPRI_TO_QID [2][0].PRI_TO_QID[2:0]	3
0xBB01C0FC	QOS_INTPRI_TO_QID [2][1].PRI_TO_QID[5:3]	3
0xBB01C0FC	QOS_INTPRI_TO_QID [2][2].PRI_TO_QID[8:6]	3
0xBB01C0FC	QOS_INTPRI_TO_QID [2][3].PRI_TO_QID[11:9]	3
0xBB01C0FC	QOS_INTPRI_TO_QID [2][4].PRI_TO_QID[14:12]	3
0xBB01C0FC	QOS_INTPRI_TO_QID [2][5].PRI_TO_QID[17:15]	3
0xBB01C0FC	QOS_INTPRI_TO_QID [2][6].PRI_TO_QID[20:18]	3
0xBB01C0FC	QOS_INTPRI_TO_QID [2][7].PRI_TO_QID[23:21]	3

Address	Register	Len
0xBB01C100	QOS_INTPRI_TO_QID [3][0].PRI_TO_QID[2:0]	3
0xBB01C100	QOS_INTPRI_TO_QID [3][1].PRI_TO_QID[5:3]	3
0xBB01C100	QOS_INTPRI_TO_QID [3][2].PRI_TO_QID[8:6]	3
0xBB01C100	QOS_INTPRI_TO_QID [3][3].PRI_TO_QID[11:9]	3
0xBB01C100	QOS_INTPRI_TO_QID [3][4].PRI_TO_QID[14:12]	3
0xBB01C100	QOS_INTPRI_TO_QID [3][5].PRI_TO_QID[17:15]	3
0xBB01C100	QOS_INTPRI_TO_QID [3][6].PRI_TO_QID[20:18]	3
0xBB01C100	QOS_INTPRI_TO_QID [3][7].PRI_TO_QID[23:21]	3
0xBB01C104	QOS_PORT_QMAP_CTRL [0].IDX[1:0]	2
0xBB01C104	QOS_PORT_QMAP_CTRL [1].IDX[3:2]	2
0xBB01C104	QOS_PORT_QMAP_CTRL [2].IDX[5:4]	2
0xBB01C104	QOS_PORT_QMAP_CTRL [3].IDX[7:6]	2
0xBB01C104	QOS_PORT_QMAP_CTRL [4].IDX[9:8]	2
0xBB01C104	QOS_PORT_QMAP_CTRL [5].IDX[11:10]	2
0xBB01C104	QOS_PORT_QMAP_CTRL [6].IDX[13:12]	2
0xBB01C108	QOS_PRI_REMAP_IN_CPU [0].PRI[2:0]	3
0xBB01C108	QOS_PRI_REMAP_IN_CPU [1].PRI[5:3]	3
0xBB01C108	QOS_PRI_REMAP_IN_CPU [2].PRI[8:6]	3
0xBB01C108	QOS_PRI_REMAP_IN_CPU [3].PRI[11:9]	3
0xBB01C108	QOS_PRI_REMAP_IN_CPU [4].PRI[14:12]	3
0xBB01C108	QOS_PRI_REMAP_IN_CPU [5].PRI[17:15]	3
0xBB01C108	QOS_PRI_REMAP_IN_CPU [6].PRI[20:18]	3
0xBB01C108	QOS_PRI_REMAP_IN_CPU [7].PRI[23:21]	3
0xBB01C10C	QOS_1Q_PRI_REMAP [0].INTPRI_1Q[2:0]	3
0xBB01C10C	QOS_1Q_PRI_REMAP [1].INTPRI_1Q[5:3]	3
0xBB01C10C	QOS_1Q_PRI_REMAP [2].INTPRI_1Q[8:6]	3
0xBB01C10C	QOS_1Q_PRI_REMAP [3].INTPRI_1Q[11:9]	3
0xBB01C10C	QOS_1Q_PRI_REMAP [4].INTPRI_1Q[14:12]	3
0xBB01C10C	QOS_1Q_PRI_REMAP [5].INTPRI_1Q[17:15]	3
0xBB01C10C	QOS_1Q_PRI_REMAP [6].INTPRI_1Q[20:18]	3
0xBB01C10C	QOS_1Q_PRI_REMAP [7].INTPRI_1Q[23:21]	3
0xBB01C110	QOS_DSCP_REMAP [0].INTPRI_DSCP[2:0]	3
0xBB01C110	QOS_DSCP_REMAP [1].INTPRI_DSCP[5:3]	3
0xBB01C110	QOS_DSCP_REMAP [2].INTPRI_DSCP[8:6]	3
0xBB01C110	QOS_DSCP_REMAP [3].INTPRI_DSCP[11:9]	3
0xBB01C110	QOS_DSCP_REMAP [4].INTPRI_DSCP[14:12]	3
0xBB01C110	QOS_DSCP_REMAP [5].INTPRI_DSCP[17:15]	3
0xBB01C110	QOS_DSCP_REMAP [6].INTPRI_DSCP[20:18]	3
0xBB01C110	QOS_DSCP_REMAP [7].INTPRI_DSCP[23:21]	3
0xBB01C110	QOS_DSCP_REMAP [8].INTPRI_DSCP[26:24]	3
0xBB01C110	QOS_DSCP_REMAP [9].INTPRI_DSCP[29:27]	3
0xBB01C114	QOS_DSCP_REMAP [10].INTPRI_DSCP[2:0]	3
0xBB01C114	QOS_DSCP_REMAP [11].INTPRI_DSCP[5:3]	3
0xBB01C114	QOS_DSCP_REMAP [12].INTPRI_DSCP[8:6]	3
0xBB01C114	QOS_DSCP_REMAP [13].INTPRI_DSCP[11:9]	3
0xBB01C114	QOS_DSCP_REMAP [14].INTPRI_DSCP[14:12]	3



Address	Register	Len
0xBB01C114	QOS_DSCP_REMAP [15].INTPRI_DSCP[17:15]	3
0xBB01C114	QOS_DSCP_REMAP [16].INTPRI_DSCP[20:18]	3
0xBB01C114	QOS_DSCP_REMAP [17].INTPRI_DSCP[23:21]	3
0xBB01C114	QOS_DSCP_REMAP [18].INTPRI_DSCP[26:24]	3
0xBB01C114	QOS_DSCP_REMAP [19].INTPRI_DSCP[29:27]	3
0xBB01C118	QOS_DSCP_REMAP [20].INTPRI_DSCP[2:0]	3
0xBB01C118	QOS_DSCP_REMAP [21].INTPRI_DSCP[5:3]	3
0xBB01C118	QOS_DSCP_REMAP [22].INTPRI_DSCP[8:6]	3
0xBB01C118	QOS_DSCP_REMAP [23].INTPRI_DSCP[11:9]	3
0xBB01C118	QOS_DSCP_REMAP [24].INTPRI_DSCP[14:12]	3
0xBB01C118	QOS_DSCP_REMAP [25].INTPRI_DSCP[17:15]	3
0xBB01C118	QOS_DSCP_REMAP [26].INTPRI_DSCP[20:18]	3
0xBB01C118	QOS_DSCP_REMAP [27].INTPRI_DSCP[23:21]	3
0xBB01C118	QOS_DSCP_REMAP [28].INTPRI_DSCP[26:24]	3
0xBB01C118	QOS_DSCP_REMAP [29].INTPRI_DSCP[29:27]	3
0xBB01C11C	QOS_DSCP_REMAP [30].INTPRI_DSCP[2:0]	3
0xBB01C11C	QOS_DSCP_REMAP [31].INTPRI_DSCP[5:3]	3
0xBB01C11C	QOS_DSCP_REMAP [32].INTPRI_DSCP[8:6]	3
0xBB01C11C	QOS_DSCP_REMAP [33].INTPRI_DSCP[11:9]	3
0xBB01C11C	QOS_DSCP_REMAP [34].INTPRI_DSCP[14:12]	3
0xBB01C11C	QOS_DSCP_REMAP [35].INTPRI_DSCP[17:15]	3
0xBB01C11C	QOS_DSCP_REMAP [36].INTPRI_DSCP[20:18]	3
0xBB01C11C	QOS_DSCP_REMAP [37].INTPRI_DSCP[23:21]	3
0xBB01C11C	QOS_DSCP_REMAP [38].INTPRI_DSCP[26:24]	3
0xBB01C11C	QOS_DSCP_REMAP [39].INTPRI_DSCP[29:27]	3
0xBB01C120	QOS_DSCP_REMAP [40].INTPRI_DSCP[2:0]	3
0xBB01C120	QOS_DSCP_REMAP [41].INTPRI_DSCP[5:3]	3
0xBB01C120	QOS_DSCP_REMAP [42].INTPRI_DSCP[8:6]	3
0xBB01C120	QOS_DSCP_REMAP [43].INTPRI_DSCP[11:9]	3
0xBB01C120	QOS_DSCP_REMAP [44].INTPRI_DSCP[14:12]	3
0xBB01C120	QOS_DSCP_REMAP [45].INTPRI_DSCP[17:15]	3
0xBB01C120	QOS_DSCP_REMAP [46].INTPRI_DSCP[20:18]	3
0xBB01C120	QOS_DSCP_REMAP [47].INTPRI_DSCP[23:21]	3
0xBB01C120	QOS_DSCP_REMAP [48].INTPRI_DSCP[26:24]	3
0xBB01C120	QOS_DSCP_REMAP [49].INTPRI_DSCP[29:27]	3
0xBB01C124	QOS_DSCP_REMAP [50].INTPRI_DSCP[2:0]	3
0xBB01C124	QOS_DSCP_REMAP [51].INTPRI_DSCP[5:3]	3
0xBB01C124	QOS_DSCP_REMAP [52].INTPRI_DSCP[8:6]	3
0xBB01C124	QOS_DSCP_REMAP [53].INTPRI_DSCP[11:9]	3
0xBB01C124	QOS_DSCP_REMAP [54].INTPRI_DSCP[14:12]	3
0xBB01C124	QOS_DSCP_REMAP [55].INTPRI_DSCP[17:15]	3
0xBB01C124	QOS_DSCP_REMAP [56].INTPRI_DSCP[20:18]	3
0xBB01C124	QOS_DSCP_REMAP [57].INTPRI_DSCP[23:21]	3
0xBB01C124	QOS_DSCP_REMAP [58].INTPRI_DSCP[26:24]	3
0xBB01C124	QOS_DSCP_REMAP [59].INTPRI_DSCP[29:27]	3
0xBB01C128	QOS_DSCP_REMAP [60].INTPRI_DSCP[2:0]	3



Address	Register	Len
0xBB01C128	QOS_DSCP_REMAP [61].INTPRI_DSCP[5:3]	3
0xBB01C128	QOS_DSCP_REMAP [62].INTPRI_DSCP[8:6]	3
0xBB01C128	QOS_DSCP_REMAP [63].INTPRI_DSCP[11:9]	3
0xBB01C12C	QOS_PB_PRI [0].INTPRI_PB[2:0]	3
0xBB01C12C	QOS_PB_PRI [1].INTPRI_PB[5:3]	3
0xBB01C12C	QOS_PB_PRI [2].INTPRI_PB[8:6]	3
0xBB01C12C	QOS_PB_PRI [3].INTPRI_PB[11:9]	3
0xBB01C12C	QOS_PB_PRI [4].INTPRI_PB[14:12]	3
0xBB01C12C	QOS_PB_PRI [5].INTPRI_PB[17:15]	3
0xBB01C12C	QOS_PB_PRI [6].INTPRI_PB[20:18]	3
0xBB01C130	PRI_SEL_TBL_CTRL.SVLAN_WEIGHT[31:28]	4
0xBB01C130	PRI_SEL_TBL_CTRL.SA_WEIGHT[27:24]	4
0xBB01C130	PRI_SEL_TBL_CTRL.LUTFWD_WEIGHT[23:20]	4
0xBB01C130	PRI_SEL_TBL_CTRL.CVLAN_WEIGHT[19:16]	4
0xBB01C130	PRI_SEL_TBL_CTRL.ACL_WEIGHT[15:12]	4
0xBB01C130	PRI_SEL_TBL_CTRL.DSCP_WEIGHT[11:8]	4
0xBB01C130	PRI_SEL_TBL_CTRL.DOT1Q_WEIGHT[7:4]	4
0xBB01C130	PRI_SEL_TBL_CTRL.PORT_WEIGHT[3:0]	4
0xBB01C134	PRI_SEL_TBL_CTRL2.RESERVED[31:4]	28
0xBB01C134	PRI_SEL_TBL_CTRL2.L4_WEIGHT[3:0]	4
0xBB01C138	OAM_CTRL_0.RESERVED[31:3]	29
0xBB01C138	OAM_CTRL_0.OAM_PRIORITY[2:0]	3
0xBB01C13C	IGMP_MC_GROUP [0].RESERVED[31:13]	19
0xBB01C13C	IGMP_MC_GROUP [0].EXT_PMSK[12:7]	6
0xBB01C13C	IGMP_MC_GROUP [0].PMSK[6:0]	7
0xBB01C140	IGMP_MC_GROUP [0].RESERVED[31:28]	4
0xBB01C140	IGMP_MC_GROUP [0].GIP[27:0]	28
0xBB01C144	IGMP_MC_GROUP [1].RESERVED[31:13]	19
0xBB01C144	IGMP_MC_GROUP [1].EXT_PMSK[12:7]	6
0xBB01C144	IGMP_MC_GROUP [1].PMSK[6:0]	7
0xBB01C148	IGMP_MC_GROUP [1].RESERVED[31:28]	4
0xBB01C148	IGMP_MC_GROUP [1].GIP[27:0]	28
0xBB01C14C	IGMP_MC_GROUP [2].RESERVED[31:13]	19
0xBB01C14C	IGMP_MC_GROUP [2].EXT_PMSK[12:7]	6
0xBB01C14C	IGMP_MC_GROUP [2].PMSK[6:0]	7
0xBB01C150	IGMP_MC_GROUP [2].RESERVED[31:28]	4
0xBB01C150	IGMP_MC_GROUP [2].GIP[27:0]	28
0xBB01C154	IGMP_MC_GROUP [3].RESERVED[31:13]	19
0xBB01C154	IGMP_MC_GROUP [3].EXT_PMSK[12:7]	6
0xBB01C154	IGMP_MC_GROUP [3].PMSK[6:0]	7
0xBB01C158	IGMP_MC_GROUP [3].RESERVED[31:28]	4
0xBB01C158	IGMP_MC_GROUP [3].GIP[27:0]	28
0xBB01C15C	IGMP_MC_GROUP [4].RESERVED[31:13]	19
0xBB01C15C	IGMP_MC_GROUP [4].EXT_PMSK[12:7]	6
0xBB01C15C	IGMP_MC_GROUP [4].PMSK[6:0]	7
0xBB01C160	IGMP_MC_GROUP [4].RESERVED[31:28]	4

Address	Register	Len
0xBB01C160	IGMP_MC_GROUP [4].GIP[27:0]	28
0xBB01C164	IGMP_MC_GROUP [5].RESERVED[31:13]	19
0xBB01C164	IGMP_MC_GROUP [5].EXT_PMSK[12:7]	6
0xBB01C164	IGMP_MC_GROUP [5].PMSK[6:0]	7
0xBB01C168	IGMP_MC_GROUP [5].RESERVED[31:28]	4
0xBB01C168	IGMP_MC_GROUP [5].GIP[27:0]	28
0xBB01C16C	IGMP_MC_GROUP [6].RESERVED[31:13]	19
0xBB01C16C	IGMP_MC_GROUP [6].EXT_PMSK[12:7]	6
0xBB01C16C	IGMP_MC_GROUP [6].PMSK[6:0]	7
0xBB01C170	IGMP_MC_GROUP [6].RESERVED[31:28]	4
0xBB01C170	IGMP_MC_GROUP [6].GIP[27:0]	28
0xBB01C174	IGMP_MC_GROUP [7].RESERVED[31:13]	19
0xBB01C174	IGMP_MC_GROUP [7].EXT_PMSK[12:7]	6
0xBB01C174	IGMP_MC_GROUP [7].PMSK[6:0]	7
0xBB01C178	IGMP_MC_GROUP [7].RESERVED[31:28]	4
0xBB01C178	IGMP_MC_GROUP [7].GIP[27:0]	28
0xBB01C17C	IGMP_MC_GROUP [8].RESERVED[31:13]	19
0xBB01C17C	IGMP_MC_GROUP [8].EXT_PMSK[12:7]	6
0xBB01C17C	IGMP_MC_GROUP [8].PMSK[6:0]	7
0xBB01C180	IGMP_MC_GROUP [8].RESERVED[31:28]	4
0xBB01C180	IGMP_MC_GROUP [8].GIP[27:0]	28
0xBB01C184	IGMP_MC_GROUP [9].RESERVED[31:13]	19
0xBB01C184	IGMP_MC_GROUP [9].EXT_PMSK[12:7]	6
0xBB01C184	IGMP_MC_GROUP [9].PMSK[6:0]	7
0xBB01C188	IGMP_MC_GROUP [9].RESERVED[31:28]	4
0xBB01C188	IGMP_MC_GROUP [9].GIP[27:0]	28
0xBB01C18C	IGMP_MC_GROUP [10].RESERVED[31:13]	19
0xBB01C18C	IGMP_MC_GROUP [10].EXT_PMSK[12:7]	6
0xBB01C18C	IGMP_MC_GROUP [10].PMSK[6:0]	7
0xBB01C190	IGMP_MC_GROUP [10].RESERVED[31:28]	4
0xBB01C190	IGMP_MC_GROUP [10].GIP[27:0]	28
0xBB01C194	IGMP_MC_GROUP [11].RESERVED[31:13]	19
0xBB01C194	IGMP_MC_GROUP [11].EXT_PMSK[12:7]	6
0xBB01C194	IGMP_MC_GROUP [11].PMSK[6:0]	7
0xBB01C198	IGMP_MC_GROUP [11].RESERVED[31:28]	4
0xBB01C198	IGMP_MC_GROUP [11].GIP[27:0]	28
0xBB01C19C	IGMP_MC_GROUP [12].RESERVED[31:13]	19
0xBB01C19C	IGMP_MC_GROUP [12].EXT_PMSK[12:7]	6
0xBB01C19C	IGMP_MC_GROUP [12].PMSK[6:0]	7
0xBB01C1A0	IGMP_MC_GROUP [12].RESERVED[31:28]	4
0xBB01C1A0	IGMP_MC_GROUP [12].GIP[27:0]	28
0xBB01C1A4	IGMP_MC_GROUP [13].RESERVED[31:13]	19
0xBB01C1A4	IGMP_MC_GROUP [13].EXT_PMSK[12:7]	6
0xBB01C1A4	IGMP_MC_GROUP [13].PMSK[6:0]	7
0xBB01C1A8	IGMP_MC_GROUP [13].RESERVED[31:28]	4
0xBB01C1A8	IGMP_MC_GROUP [13].GIP[27:0]	28

Address	Register	Len
0xBB01C1AC	IGMP_MC_GROUP [14].RESERVED[31:13]	19
0xBB01C1AC	IGMP_MC_GROUP [14].EXT_PMSK[12:7]	6
0xBB01C1AC	IGMP_MC_GROUP [14].PMSK[6:0]	7
0xBB01C1B0	IGMP_MC_GROUP [14].RESERVED[31:28]	4
0xBB01C1B0	IGMP_MC_GROUP [14].GIP[27:0]	28
0xBB01C1B4	IGMP_MC_GROUP [15].RESERVED[31:13]	19
0xBB01C1B4	IGMP_MC_GROUP [15].EXT_PMSK[12:7]	6
0xBB01C1B4	IGMP_MC_GROUP [15].PMSK[6:0]	7
0xBB01C1B8	IGMP_MC_GROUP [15].RESERVED[31:28]	4
0xBB01C1B8	IGMP_MC_GROUP [15].GIP[27:0]	28
0xBB01C1BC	IGMP_MC_GROUP [16].RESERVED[31:13]	19
0xBB01C1BC	IGMP_MC_GROUP [16].EXT_PMSK[12:7]	6
0xBB01C1BC	IGMP_MC_GROUP [16].PMSK[6:0]	7
0xBB01C1C0	IGMP_MC_GROUP [16].RESERVED[31:28]	4
0xBB01C1C0	IGMP_MC_GROUP [16].GIP[27:0]	28
0xBB01C1C4	IGMP_MC_GROUP [17].RESERVED[31:13]	19
0xBB01C1C4	IGMP_MC_GROUP [17].EXT_PMSK[12:7]	6
0xBB01C1C4	IGMP_MC_GROUP [17].PMSK[6:0]	7
0xBB01C1C8	IGMP_MC_GROUP [17].RESERVED[31:28]	4
0xBB01C1C8	IGMP_MC_GROUP [17].GIP[27:0]	28
0xBB01C1CC	IGMP_MC_GROUP [18].RESERVED[31:13]	19
0xBB01C1CC	IGMP_MC_GROUP [18].EXT_PMSK[12:7]	6
0xBB01C1CC	IGMP_MC_GROUP [18].PMSK[6:0]	7
0xBB01C1D0	IGMP_MC_GROUP [18].RESERVED[31:28]	4
0xBB01C1D0	IGMP_MC_GROUP [18].GIP[27:0]	28
0xBB01C1D4	IGMP_MC_GROUP [19].RESERVED[31:13]	19
0xBB01C1D4	IGMP_MC_GROUP [19].EXT_PMSK[12:7]	6
0xBB01C1D4	IGMP_MC_GROUP [19].PMSK[6:0]	7
0xBB01C1D8	IGMP_MC_GROUP [19].RESERVED[31:28]	4
0xBB01C1D8	IGMP_MC_GROUP [19].GIP[27:0]	28
0xBB01C1DC	IGMP_MC_GROUP [20].RESERVED[31:13]	19
0xBB01C1DC	IGMP_MC_GROUP [20].EXT_PMSK[12:7]	6
0xBB01C1DC	IGMP_MC_GROUP [20].PMSK[6:0]	7
0xBB01C1E0	IGMP_MC_GROUP [20].RESERVED[31:28]	4
0xBB01C1E0	IGMP_MC_GROUP [20].GIP[27:0]	28
0xBB01C1E4	IGMP_MC_GROUP [21].RESERVED[31:13]	19
0xBB01C1E4	IGMP_MC_GROUP [21].EXT_PMSK[12:7]	6
0xBB01C1E4	IGMP_MC_GROUP [21].PMSK[6:0]	7
0xBB01C1E8	IGMP_MC_GROUP [21].RESERVED[31:28]	4
0xBB01C1E8	IGMP_MC_GROUP [21].GIP[27:0]	28
0xBB01C1EC	IGMP_MC_GROUP [22].RESERVED[31:13]	19
0xBB01C1EC	IGMP_MC_GROUP [22].EXT_PMSK[12:7]	6
0xBB01C1EC	IGMP_MC_GROUP [22].PMSK[6:0]	7
0xBB01C1F0	IGMP_MC_GROUP [22].RESERVED[31:28]	4
0xBB01C1F0	IGMP_MC_GROUP [22].GIP[27:0]	28
0xBB01C1F4	IGMP_MC_GROUP [23].RESERVED[31:13]	19

Address	Register	Len
0xBB01C1F4	IGMP_MC_GROUP [23].EXT_PMSK[12:7]	6
0xBB01C1F4	IGMP_MC_GROUP [23].PMSK[6:0]	7
0xBB01C1F8	IGMP_MC_GROUP [23].RESERVED[31:28]	4
0xBB01C1F8	IGMP_MC_GROUP [23].GIP[27:0]	28
0xBB01C1FC	IGMP_MC_GROUP [24].RESERVED[31:13]	19
0xBB01C1FC	IGMP_MC_GROUP [24].EXT_PMSK[12:7]	6
0xBB01C1FC	IGMP_MC_GROUP [24].PMSK[6:0]	7
0xBB01C200	IGMP_MC_GROUP [24].RESERVED[31:28]	4
0xBB01C200	IGMP_MC_GROUP [24].GIP[27:0]	28
0xBB01C204	IGMP_MC_GROUP [25].RESERVED[31:13]	19
0xBB01C204	IGMP_MC_GROUP [25].EXT_PMSK[12:7]	6
0xBB01C204	IGMP_MC_GROUP [25].PMSK[6:0]	7
0xBB01C208	IGMP_MC_GROUP [25].RESERVED[31:28]	4
0xBB01C208	IGMP_MC_GROUP [25].GIP[27:0]	28
0xBB01C20C	IGMP_MC_GROUP [26].RESERVED[31:13]	19
0xBB01C20C	IGMP_MC_GROUP [26].EXT_PMSK[12:7]	6
0xBB01C20C	IGMP_MC_GROUP [26].PMSK[6:0]	7
0xBB01C210	IGMP_MC_GROUP [26].RESERVED[31:28]	4
0xBB01C210	IGMP_MC_GROUP [26].GIP[27:0]	28
0xBB01C214	IGMP_MC_GROUP [27].RESERVED[31:13]	19
0xBB01C214	IGMP_MC_GROUP [27].EXT_PMSK[12:7]	6
0xBB01C214	IGMP_MC_GROUP [27].PMSK[6:0]	7
0xBB01C218	IGMP_MC_GROUP [27].RESERVED[31:28]	4
0xBB01C218	IGMP_MC_GROUP [27].GIP[27:0]	28
0xBB01C21C	IGMP_MC_GROUP [28].RESERVED[31:13]	19
0xBB01C21C	IGMP_MC_GROUP [28].EXT_PMSK[12:7]	6
0xBB01C21C	IGMP_MC_GROUP [28].PMSK[6:0]	7
0xBB01C220	IGMP_MC_GROUP [28].RESERVED[31:28]	4
0xBB01C220	IGMP_MC_GROUP [28].GIP[27:0]	28
0xBB01C224	IGMP_MC_GROUP [29].RESERVED[31:13]	19
0xBB01C224	IGMP_MC_GROUP [29].EXT_PMSK[12:7]	6
0xBB01C224	IGMP_MC_GROUP [29].PMSK[6:0]	7
0xBB01C228	IGMP_MC_GROUP [29].RESERVED[31:28]	4
0xBB01C228	IGMP_MC_GROUP [29].GIP[27:0]	28
0xBB01C22C	IGMP_MC_GROUP [30].RESERVED[31:13]	19
0xBB01C22C	IGMP_MC_GROUP [30].EXT_PMSK[12:7]	6
0xBB01C22C	IGMP_MC_GROUP [30].PMSK[6:0]	7
0xBB01C230	IGMP_MC_GROUP [30].RESERVED[31:28]	4
0xBB01C230	IGMP_MC_GROUP [30].GIP[27:0]	28
0xBB01C234	IGMP_MC_GROUP [31].RESERVED[31:13]	19
0xBB01C234	IGMP_MC_GROUP [31].EXT_PMSK[12:7]	6
0xBB01C234	IGMP_MC_GROUP [31].PMSK[6:0]	7
0xBB01C238	IGMP_MC_GROUP [31].RESERVED[31:28]	4
0xBB01C238	IGMP_MC_GROUP [31].GIP[27:0]	28
0xBB01C23C	IGMP_MC_GROUP [32].RESERVED[31:13]	19
0xBB01C23C	IGMP_MC_GROUP [32].EXT_PMSK[12:7]	6

Address	Register	Len
0xBB01C23C	IGMP_MC_GROUP [32].PMSK[6:0]	7
0xBB01C240	IGMP_MC_GROUP [32].RESERVED[31:28]	4
0xBB01C240	IGMP_MC_GROUP [32].GIP[27:0]	28
0xBB01C244	IGMP_MC_GROUP [33].RESERVED[31:13]	19
0xBB01C244	IGMP_MC_GROUP [33].EXT_PMSK[12:7]	6
0xBB01C244	IGMP_MC_GROUP [33].PMSK[6:0]	7
0xBB01C248	IGMP_MC_GROUP [33].RESERVED[31:28]	4
0xBB01C248	IGMP_MC_GROUP [33].GIP[27:0]	28
0xBB01C24C	IGMP_MC_GROUP [34].RESERVED[31:13]	19
0xBB01C24C	IGMP_MC_GROUP [34].EXT_PMSK[12:7]	6
0xBB01C24C	IGMP_MC_GROUP [34].PMSK[6:0]	7
0xBB01C250	IGMP_MC_GROUP [34].RESERVED[31:28]	4
0xBB01C250	IGMP_MC_GROUP [34].GIP[27:0]	28
0xBB01C254	IGMP_MC_GROUP [35].RESERVED[31:13]	19
0xBB01C254	IGMP_MC_GROUP [35].EXT_PMSK[12:7]	6
0xBB01C254	IGMP_MC_GROUP [35].PMSK[6:0]	7
0xBB01C258	IGMP_MC_GROUP [35].RESERVED[31:28]	4
0xBB01C258	IGMP_MC_GROUP [35].GIP[27:0]	28
0xBB01C25C	IGMP_MC_GROUP [36].RESERVED[31:13]	19
0xBB01C25C	IGMP_MC_GROUP [36].EXT_PMSK[12:7]	6
0xBB01C25C	IGMP_MC_GROUP [36].PMSK[6:0]	7
0xBB01C260	IGMP_MC_GROUP [36].RESERVED[31:28]	4
0xBB01C260	IGMP_MC_GROUP [36].GIP[27:0]	28
0xBB01C264	IGMP_MC_GROUP [37].RESERVED[31:13]	19
0xBB01C264	IGMP_MC_GROUP [37].EXT_PMSK[12:7]	6
0xBB01C264	IGMP_MC_GROUP [37].PMSK[6:0]	7
0xBB01C268	IGMP_MC_GROUP [37].RESERVED[31:28]	4
0xBB01C268	IGMP_MC_GROUP [37].GIP[27:0]	28
0xBB01C26C	IGMP_MC_GROUP [38].RESERVED[31:13]	19
0xBB01C26C	IGMP_MC_GROUP [38].EXT_PMSK[12:7]	6
0xBB01C26C	IGMP_MC_GROUP [38].PMSK[6:0]	7
0xBB01C270	IGMP_MC_GROUP [38].RESERVED[31:28]	4
0xBB01C270	IGMP_MC_GROUP [38].GIP[27:0]	28
0xBB01C274	IGMP_MC_GROUP [39].RESERVED[31:13]	19
0xBB01C274	IGMP_MC_GROUP [39].EXT_PMSK[12:7]	6
0xBB01C274	IGMP_MC_GROUP [39].PMSK[6:0]	7
0xBB01C278	IGMP_MC_GROUP [39].RESERVED[31:28]	4
0xBB01C278	IGMP_MC_GROUP [39].GIP[27:0]	28
0xBB01C27C	IGMP_MC_GROUP [40].RESERVED[31:13]	19
0xBB01C27C	IGMP_MC_GROUP [40].EXT_PMSK[12:7]	6
0xBB01C27C	IGMP_MC_GROUP [40].PMSK[6:0]	7
0xBB01C280	IGMP_MC_GROUP [40].RESERVED[31:28]	4
0xBB01C280	IGMP_MC_GROUP [40].GIP[27:0]	28
0xBB01C284	IGMP_MC_GROUP [41].RESERVED[31:13]	19
0xBB01C284	IGMP_MC_GROUP [41].EXT_PMSK[12:7]	6
0xBB01C284	IGMP_MC_GROUP [41].PMSK[6:0]	7

Address	Register	Len
0xBB01C288	IGMP_MC_GROUP [41].RESERVED[31:28]	4
0xBB01C288	IGMP_MC_GROUP [41].GIP[27:0]	28
0xBB01C28C	IGMP_MC_GROUP [42].RESERVED[31:13]	19
0xBB01C28C	IGMP_MC_GROUP [42].EXT_PMSK[12:7]	6
0xBB01C28C	IGMP_MC_GROUP [42].PMSK[6:0]	7
0xBB01C290	IGMP_MC_GROUP [42].RESERVED[31:28]	4
0xBB01C290	IGMP_MC_GROUP [42].GIP[27:0]	28
0xBB01C294	IGMP_MC_GROUP [43].RESERVED[31:13]	19
0xBB01C294	IGMP_MC_GROUP [43].EXT_PMSK[12:7]	6
0xBB01C294	IGMP_MC_GROUP [43].PMSK[6:0]	7
0xBB01C298	IGMP_MC_GROUP [43].RESERVED[31:28]	4
0xBB01C298	IGMP_MC_GROUP [43].GIP[27:0]	28
0xBB01C29C	IGMP_MC_GROUP [44].RESERVED[31:13]	19
0xBB01C29C	IGMP_MC_GROUP [44].EXT_PMSK[12:7]	6
0xBB01C29C	IGMP_MC_GROUP [44].PMSK[6:0]	7
0xBB01C2A0	IGMP_MC_GROUP [44].RESERVED[31:28]	4
0xBB01C2A0	IGMP_MC_GROUP [44].GIP[27:0]	28
0xBB01C2A4	IGMP_MC_GROUP [45].RESERVED[31:13]	19
0xBB01C2A4	IGMP_MC_GROUP [45].EXT_PMSK[12:7]	6
0xBB01C2A4	IGMP_MC_GROUP [45].PMSK[6:0]	7
0xBB01C2A8	IGMP_MC_GROUP [45].RESERVED[31:28]	4
0xBB01C2A8	IGMP_MC_GROUP [45].GIP[27:0]	28
0xBB01C2AC	IGMP_MC_GROUP [46].RESERVED[31:13]	19
0xBB01C2AC	IGMP_MC_GROUP [46].EXT_PMSK[12:7]	6
0xBB01C2AC	IGMP_MC_GROUP [46].PMSK[6:0]	7
0xBB01C2B0	IGMP_MC_GROUP [46].RESERVED[31:28]	4
0xBB01C2B0	IGMP_MC_GROUP [46].GIP[27:0]	28
0xBB01C2B4	IGMP_MC_GROUP [47].RESERVED[31:13]	19
0xBB01C2B4	IGMP_MC_GROUP [47].EXT_PMSK[12:7]	6
0xBB01C2B4	IGMP_MC_GROUP [47].PMSK[6:0]	7
0xBB01C2B8	IGMP_MC_GROUP [47].RESERVED[31:28]	4
0xBB01C2B8	IGMP_MC_GROUP [47].GIP[27:0]	28
0xBB01C2BC	IGMP_MC_GROUP [48].RESERVED[31:13]	19
0xBB01C2BC	IGMP_MC_GROUP [48].EXT_PMSK[12:7]	6
0xBB01C2BC	IGMP_MC_GROUP [48].PMSK[6:0]	7
0xBB01C2C0	IGMP_MC_GROUP [48].RESERVED[31:28]	4
0xBB01C2C0	IGMP_MC_GROUP [48].GIP[27:0]	28
0xBB01C2C4	IGMP_MC_GROUP [49].RESERVED[31:13]	19
0xBB01C2C4	IGMP_MC_GROUP [49].EXT_PMSK[12:7]	6
0xBB01C2C4	IGMP_MC_GROUP [49].PMSK[6:0]	7
0xBB01C2C8	IGMP_MC_GROUP [49].RESERVED[31:28]	4
0xBB01C2C8	IGMP_MC_GROUP [49].GIP[27:0]	28
0xBB01C2CC	IGMP_MC_GROUP [50].RESERVED[31:13]	19
0xBB01C2CC	IGMP_MC_GROUP [50].EXT_PMSK[12:7]	6
0xBB01C2CC	IGMP_MC_GROUP [50].PMSK[6:0]	7
0xBB01C2D0	IGMP_MC_GROUP [50].RESERVED[31:28]	4

Address	Register	Len
0xBB01C2D0	IGMP_MC_GROUP [50].GIP[27:0]	28
0xBB01C2D4	IGMP_MC_GROUP [51].RESERVED[31:13]	19
0xBB01C2D4	IGMP_MC_GROUP [51].EXT_PMSK[12:7]	6
0xBB01C2D4	IGMP_MC_GROUP [51].PMSK[6:0]	7
0xBB01C2D8	IGMP_MC_GROUP [51].RESERVED[31:28]	4
0xBB01C2D8	IGMP_MC_GROUP [51].GIP[27:0]	28
0xBB01C2DC	IGMP_MC_GROUP [52].RESERVED[31:13]	19
0xBB01C2DC	IGMP_MC_GROUP [52].EXT_PMSK[12:7]	6
0xBB01C2DC	IGMP_MC_GROUP [52].PMSK[6:0]	7
0xBB01C2E0	IGMP_MC_GROUP [52].RESERVED[31:28]	4
0xBB01C2E0	IGMP_MC_GROUP [52].GIP[27:0]	28
0xBB01C2E4	IGMP_MC_GROUP [53].RESERVED[31:13]	19
0xBB01C2E4	IGMP_MC_GROUP [53].EXT_PMSK[12:7]	6
0xBB01C2E4	IGMP_MC_GROUP [53].PMSK[6:0]	7
0xBB01C2E8	IGMP_MC_GROUP [53].RESERVED[31:28]	4
0xBB01C2E8	IGMP_MC_GROUP [53].GIP[27:0]	28
0xBB01C2EC	IGMP_MC_GROUP [54].RESERVED[31:13]	19
0xBB01C2EC	IGMP_MC_GROUP [54].EXT_PMSK[12:7]	6
0xBB01C2EC	IGMP_MC_GROUP [54].PMSK[6:0]	7
0xBB01C2F0	IGMP_MC_GROUP [54].RESERVED[31:28]	4
0xBB01C2F0	IGMP_MC_GROUP [54].GIP[27:0]	28
0xBB01C2F4	IGMP_MC_GROUP [55].RESERVED[31:13]	19
0xBB01C2F4	IGMP_MC_GROUP [55].EXT_PMSK[12:7]	6
0xBB01C2F4	IGMP_MC_GROUP [55].PMSK[6:0]	7
0xBB01C2F8	IGMP_MC_GROUP [55].RESERVED[31:28]	4
0xBB01C2F8	IGMP_MC_GROUP [55].GIP[27:0]	28
0xBB01C2FC	IGMP_MC_GROUP [56].RESERVED[31:13]	19
0xBB01C2FC	IGMP_MC_GROUP [56].EXT_PMSK[12:7]	6
0xBB01C2FC	IGMP_MC_GROUP [56].PMSK[6:0]	7
0xBB01C300	IGMP_MC_GROUP [56].RESERVED[31:28]	4
0xBB01C300	IGMP_MC_GROUP [56].GIP[27:0]	28
0xBB01C304	IGMP_MC_GROUP [57].RESERVED[31:13]	19
0xBB01C304	IGMP_MC_GROUP [57].EXT_PMSK[12:7]	6
0xBB01C304	IGMP_MC_GROUP [57].PMSK[6:0]	7
0xBB01C308	IGMP_MC_GROUP [57].RESERVED[31:28]	4
0xBB01C308	IGMP_MC_GROUP [57].GIP[27:0]	28
0xBB01C30C	IGMP_MC_GROUP [58].RESERVED[31:13]	19
0xBB01C30C	IGMP_MC_GROUP [58].EXT_PMSK[12:7]	6
0xBB01C30C	IGMP_MC_GROUP [58].PMSK[6:0]	7
0xBB01C310	IGMP_MC_GROUP [58].RESERVED[31:28]	4
0xBB01C310	IGMP_MC_GROUP [58].GIP[27:0]	28
0xBB01C314	IGMP_MC_GROUP [59].RESERVED[31:13]	19
0xBB01C314	IGMP_MC_GROUP [59].EXT_PMSK[12:7]	6
0xBB01C314	IGMP_MC_GROUP [59].PMSK[6:0]	7
0xBB01C318	IGMP_MC_GROUP [59].RESERVED[31:28]	4
0xBB01C318	IGMP_MC_GROUP [59].GIP[27:0]	28



Address	Register	Len
0xBB01C31C	IGMP_MC_GROUP [60].RESERVED[31:13]	19
0xBB01C31C	IGMP_MC_GROUP [60].EXT_PMSK[12:7]	6
0xBB01C31C	IGMP_MC_GROUP [60].PMSK[6:0]	7
0xBB01C320	IGMP_MC_GROUP [60].RESERVED[31:28]	4
0xBB01C320	IGMP_MC_GROUP [60].GIP[27:0]	28
0xBB01C324	IGMP_MC_GROUP [61].RESERVED[31:13]	19
0xBB01C324	IGMP_MC_GROUP [61].EXT_PMSK[12:7]	6
0xBB01C324	IGMP_MC_GROUP [61].PMSK[6:0]	7
0xBB01C328	IGMP_MC_GROUP [61].RESERVED[31:28]	4
0xBB01C328	IGMP_MC_GROUP [61].GIP[27:0]	28
0xBB01C32C	IGMP_MC_GROUP [62].RESERVED[31:13]	19
0xBB01C32C	IGMP_MC_GROUP [62].EXT_PMSK[12:7]	6
0xBB01C32C	IGMP_MC_GROUP [62].PMSK[6:0]	7
0xBB01C330	IGMP_MC_GROUP [62].RESERVED[31:28]	4
0xBB01C330	IGMP_MC_GROUP [62].GIP[27:0]	28
0xBB01C334	IGMP_MC_GROUP [63].RESERVED[31:13]	19
0xBB01C334	IGMP_MC_GROUP [63].EXT_PMSK[12:7]	6
0xBB01C334	IGMP_MC_GROUP [63].PMSK[6:0]	7
0xBB01C338	IGMP_MC_GROUP [63].RESERVED[31:28]	4
0xBB01C338	IGMP_MC_GROUP [63].GIP[27:0]	28
0xBB01C33C	PON_SID_TO_QID [0].QID[6:0]	7
0xBB01C33C	PON_SID_TO_QID [1].QID[13:7]	7
0xBB01C33C	PON_SID_TO_QID [2].QID[20:14]	7
0xBB01C33C	PON_SID_TO_QID [3].QID[27:21]	7
0xBB01C340	PON_SID_TO_QID [4].QID[6:0]	7
0xBB01C340	PON_SID_TO_QID [5].QID[13:7]	7
0xBB01C340	PON_SID_TO_QID [6].QID[20:14]	7
0xBB01C340	PON_SID_TO_QID [7].QID[27:21]	7
0xBB01C344	PON_SID_TO_QID [8].QID[6:0]	7
0xBB01C344	PON_SID_TO_QID [9].QID[13:7]	7
0xBB01C344	PON_SID_TO_QID [10].QID[20:14]	7
0xBB01C344	PON_SID_TO_QID [11].QID[27:21]	7
0xBB01C348	PON_SID_TO_QID [12].QID[6:0]	7
0xBB01C348	PON_SID_TO_QID [13].QID[13:7]	7
0xBB01C348	PON_SID_TO_QID [14].QID[20:14]	7
0xBB01C348	PON_SID_TO_QID [15].QID[27:21]	7
0xBB01C34C	PON_SID_TO_QID [16].QID[6:0]	7
0xBB01C34C	PON_SID_TO_QID [17].QID[13:7]	7
0xBB01C34C	PON_SID_TO_QID [18].QID[20:14]	7
0xBB01C34C	PON_SID_TO_QID [19].QID[27:21]	7
0xBB01C350	PON_SID_TO_QID [20].QID[6:0]	7
0xBB01C350	PON_SID_TO_QID [21].QID[13:7]	7
0xBB01C350	PON_SID_TO_QID [22].QID[20:14]	7
0xBB01C350	PON_SID_TO_QID [23].QID[27:21]	7
0xBB01C354	PON_SID_TO_QID [24].QID[6:0]	7
0xBB01C354	PON_SID_TO_QID [25].QID[13:7]	7



Address	Register	Len
0xBB01C354	PON_SID_TO_QID [26].QID[20:14]	7
0xBB01C354	PON_SID_TO_QID [27].QID[27:21]	7
0xBB01C358	PON_SID_TO_QID [28].QID[6:0]	7
0xBB01C358	PON_SID_TO_QID [29].QID[13:7]	7
0xBB01C358	PON_SID_TO_QID [30].QID[20:14]	7
0xBB01C358	PON_SID_TO_QID [31].QID[27:21]	7
0xBB01C35C	PON_SID_TO_QID [32].QID[6:0]	7
0xBB01C35C	PON_SID_TO_QID [33].QID[13:7]	7
0xBB01C35C	PON_SID_TO_QID [34].QID[20:14]	7
0xBB01C35C	PON_SID_TO_QID [35].QID[27:21]	7
0xBB01C360	PON_SID_TO_QID [36].QID[6:0]	7
0xBB01C360	PON_SID_TO_QID [37].QID[13:7]	7
0xBB01C360	PON_SID_TO_QID [38].QID[20:14]	7
0xBB01C360	PON_SID_TO_QID [39].QID[27:21]	7
0xBB01C364	PON_SID_TO_QID [40].QID[6:0]	7
0xBB01C364	PON_SID_TO_QID [41].QID[13:7]	7
0xBB01C364	PON_SID_TO_QID [42].QID[20:14]	7
0xBB01C364	PON_SID_TO_QID [43].QID[27:21]	7
0xBB01C368	PON_SID_TO_QID [44].QID[6:0]	7
0xBB01C368	PON_SID_TO_QID [45].QID[13:7]	7
0xBB01C368	PON_SID_TO_QID [46].QID[20:14]	7
0xBB01C368	PON_SID_TO_QID [47].QID[27:21]	7
0xBB01C36C	PON_SID_TO_QID [48].QID[6:0]	7
0xBB01C36C	PON_SID_TO_QID [49].QID[13:7]	7
0xBB01C36C	PON_SID_TO_QID [50].QID[20:14]	7
0xBB01C36C	PON_SID_TO_QID [51].QID[27:21]	7
0xBB01C370	PON_SID_TO_QID [52].QID[6:0]	7
0xBB01C370	PON_SID_TO_QID [53].QID[13:7]	7
0xBB01C370	PON_SID_TO_QID [54].QID[20:14]	7
0xBB01C370	PON_SID_TO_QID [55].QID[27:21]	7
0xBB01C374	PON_SID_TO_QID [56].QID[6:0]	7
0xBB01C374	PON_SID_TO_QID [57].QID[13:7]	7
0xBB01C374	PON_SID_TO_QID [58].QID[20:14]	7
0xBB01C374	PON_SID_TO_QID [59].QID[27:21]	7
0xBB01C378	PON_SID_TO_QID [60].QID[6:0]	7
0xBB01C378	PON_SID_TO_QID [61].QID[13:7]	7
0xBB01C378	PON_SID_TO_QID [62].QID[20:14]	7
0xBB01C378	PON_SID_TO_QID [63].QID[27:21]	7
0xBB01C37C	PON_SID_TO_QID [64].QID[6:0]	7
0xBB01C37C	PON_SID_TO_QID [65].QID[13:7]	7
0xBB01C37C	PON_SID_TO_QID [66].QID[20:14]	7
0xBB01C37C	PON_SID_TO_QID [67].QID[27:21]	7
0xBB01C380	PON_SID_TO_QID [68].QID[6:0]	7
0xBB01C380	PON_SID_TO_QID [69].QID[13:7]	7
0xBB01C380	PON_SID_TO_QID [70].QID[20:14]	7
0xBB01C380	PON_SID_TO_QID [71].QID[27:21]	7

Address	Register	Len
0xBB01C384	PON_SID_TO_QID [72].QID[6:0]	7
0xBB01C384	PON_SID_TO_QID [73].QID[13:7]	7
0xBB01C384	PON_SID_TO_QID [74].QID[20:14]	7
0xBB01C384	PON_SID_TO_QID [75].QID[27:21]	7
0xBB01C388	PON_SID_TO_QID [76].QID[6:0]	7
0xBB01C388	PON_SID_TO_QID [77].QID[13:7]	7
0xBB01C388	PON_SID_TO_QID [78].QID[20:14]	7
0xBB01C388	PON_SID_TO_QID [79].QID[27:21]	7
0xBB01C38C	PON_SID_TO_QID [80].QID[6:0]	7
0xBB01C38C	PON_SID_TO_QID [81].QID[13:7]	7
0xBB01C38C	PON_SID_TO_QID [82].QID[20:14]	7
0xBB01C38C	PON_SID_TO_QID [83].QID[27:21]	7
0xBB01C390	PON_SID_TO_QID [84].QID[6:0]	7
0xBB01C390	PON_SID_TO_QID [85].QID[13:7]	7
0xBB01C390	PON_SID_TO_QID [86].QID[20:14]	7
0xBB01C390	PON_SID_TO_QID [87].QID[27:21]	7
0xBB01C394	PON_SID_TO_QID [88].QID[6:0]	7
0xBB01C394	PON_SID_TO_QID [89].QID[13:7]	7
0xBB01C394	PON_SID_TO_QID [90].QID[20:14]	7
0xBB01C394	PON_SID_TO_QID [91].QID[27:21]	7
0xBB01C398	PON_SID_TO_QID [92].QID[6:0]	7
0xBB01C398	PON_SID_TO_QID [93].QID[13:7]	7
0xBB01C398	PON_SID_TO_QID [94].QID[20:14]	7
0xBB01C398	PON_SID_TO_QID [95].QID[27:21]	7
0xBB01C39C	PON_SID_TO_QID [96].QID[6:0]	7
0xBB01C39C	PON_SID_TO_QID [97].QID[13:7]	7
0xBB01C39C	PON_SID_TO_QID [98].QID[20:14]	7
0xBB01C39C	PON_SID_TO_QID [99].QID[27:21]	7
0xBB01C3A0	PON_SID_TO_QID [100].QID[6:0]	7
0xBB01C3A0	PON_SID_TO_QID [101].QID[13:7]	7
0xBB01C3A0	PON_SID_TO_QID [102].QID[20:14]	7
0xBB01C3A0	PON_SID_TO_QID [103].QID[27:21]	7
0xBB01C3A4	PON_SID_TO_QID [104].QID[6:0]	7
0xBB01C3A4	PON_SID_TO_QID [105].QID[13:7]	7
0xBB01C3A4	PON_SID_TO_QID [106].QID[20:14]	7
0xBB01C3A4	PON_SID_TO_QID [107].QID[27:21]	7
0xBB01C3A8	PON_SID_TO_QID [108].QID[6:0]	7
0xBB01C3A8	PON_SID_TO_QID [109].QID[13:7]	7
0xBB01C3A8	PON_SID_TO_QID [110].QID[20:14]	7
0xBB01C3A8	PON_SID_TO_QID [111].QID[27:21]	7
0xBB01C3AC	PON_SID_TO_QID [112].QID[6:0]	7
0xBB01C3AC	PON_SID_TO_QID [113].QID[13:7]	7
0xBB01C3AC	PON_SID_TO_QID [114].QID[20:14]	7
0xBB01C3AC	PON_SID_TO_QID [115].QID[27:21]	7
0xBB01C3B0	PON_SID_TO_QID [116].QID[6:0]	7
0xBB01C3B0	PON_SID_TO_QID [117].QID[13:7]	7

Address	Register	Len
0xBB01C3B0	PON_SID_TO_QID [118].QID[20:14]	7
0xBB01C3B0	PON_SID_TO_QID [119].QID[27:21]	7
0xBB01C3B4	PON_SID_TO_QID [120].QID[6:0]	7
0xBB01C3B4	PON_SID_TO_QID [121].QID[13:7]	7
0xBB01C3B4	PON_SID_TO_QID [122].QID[20:14]	7
0xBB01C3B4	PON_SID_TO_QID [123].QID[27:21]	7
0xBB01C3B8	PON_SID_TO_QID [124].QID[6:0]	7
0xBB01C3B8	PON_SID_TO_QID [125].QID[13:7]	7
0xBB01C3B8	PON_SID_TO_QID [126].QID[20:14]	7
0xBB01C3B8	PON_SID_TO_QID [127].QID[27:21]	7
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [0].TH[0:0]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [1].TH[1:1]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [2].TH[2:2]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [3].TH[3:3]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [4].TH[4:4]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [5].TH[5:5]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [6].TH[6:6]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [7].TH[7:7]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [8].TH[8:8]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [9].TH[9:9]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [10].TH[10:10]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [11].TH[11:11]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [12].TH[12:12]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [13].TH[13:13]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [14].TH[14:14]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [15].TH[15:15]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [16].TH[16:16]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [17].TH[17:17]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [18].TH[18:18]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [19].TH[19:19]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [20].TH[20:20]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [21].TH[21:21]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [22].TH[22:22]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [23].TH[23:23]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [24].TH[24:24]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [25].TH[25:25]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [26].TH[26:26]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [27].TH[27:27]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [28].TH[28:28]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [29].TH[29:29]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [30].TH[30:30]	1
0xBB01C3BC	FC_PON_Q_EGR_DROP_EN [31].TH[31:31]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [32].TH[0:0]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [33].TH[1:1]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [34].TH[2:2]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [35].TH[3:3]	1

Address	Register	Len
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [36].TH[4:4]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [37].TH[5:5]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [38].TH[6:6]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [39].TH[7:7]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [40].TH[8:8]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [41].TH[9:9]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [42].TH[10:10]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [43].TH[11:11]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [44].TH[12:12]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [45].TH[13:13]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [46].TH[14:14]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [47].TH[15:15]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [48].TH[16:16]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [49].TH[17:17]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [50].TH[18:18]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [51].TH[19:19]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [52].TH[20:20]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [53].TH[21:21]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [54].TH[22:22]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [55].TH[23:23]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [56].TH[24:24]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [57].TH[25:25]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [58].TH[26:26]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [59].TH[27:27]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [60].TH[28:28]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [61].TH[29:29]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [62].TH[30:30]	1
0xBB01C3C0	FC_PON_Q_EGR_DROP_EN [63].TH[31:31]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [64].TH[0:0]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [65].TH[1:1]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [66].TH[2:2]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [67].TH[3:3]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [68].TH[4:4]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [69].TH[5:5]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [70].TH[6:6]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [71].TH[7:7]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [72].TH[8:8]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [73].TH[9:9]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [74].TH[10:10]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [75].TH[11:11]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [76].TH[12:12]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [77].TH[13:13]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [78].TH[14:14]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [79].TH[15:15]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [80].TH[16:16]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [81].TH[17:17]	1

Address	Register	Len
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [82].TH[18:18]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [83].TH[19:19]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [84].TH[20:20]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [85].TH[21:21]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [86].TH[22:22]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [87].TH[23:23]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [88].TH[24:24]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [89].TH[25:25]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [90].TH[26:26]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [91].TH[27:27]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [92].TH[28:28]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [93].TH[29:29]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [94].TH[30:30]	1
0xBB01C3C4	FC_PON_Q_EGR_DROP_EN [95].TH[31:31]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [96].TH[0:0]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [97].TH[1:1]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [98].TH[2:2]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [99].TH[3:3]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [100].TH[4:4]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [101].TH[5:5]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [102].TH[6:6]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [103].TH[7:7]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [104].TH[8:8]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [105].TH[9:9]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [106].TH[10:10]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [107].TH[11:11]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [108].TH[12:12]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [109].TH[13:13]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [110].TH[14:14]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [111].TH[15:15]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [112].TH[16:16]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [113].TH[17:17]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [114].TH[18:18]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [115].TH[19:19]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [116].TH[20:20]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [117].TH[21:21]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [118].TH[22:22]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [119].TH[23:23]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [120].TH[24:24]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [121].TH[25:25]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [122].TH[26:26]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [123].TH[27:27]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [124].TH[28:28]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [125].TH[29:29]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [126].TH[30:30]	1
0xBB01C3C8	FC_PON_Q_EGR_DROP_EN [127].TH[31:31]	1

Address	Register	Len
0xBB01C3CC	RGF_VER_ALE_DPM.REGFILE_VER[31:0]	32
0xBB01C3D0	RSVD_ALE_DPM [0].RSVD_MEM[31:0]	32
0xBB01C3D4	RSVD_ALE_DPM [1].RSVD_MEM[31:0]	32
0xBB01C3D8	RSVD_ALE_DPM [2].RSVD_MEM[31:0]	32
0xBB01C3DC	RSVD_ALE_DPM [3].RSVD_MEM[31:0]	32
0xBB01C3E0	RSVD_ALE_DPM [4].RSVD_MEM[31:0]	32
0xBB01C3E4	RSVD_ALE_DPM [5].RSVD_MEM[31:0]	32
0xBB01C3E8	RSVD_ALE_DPM [6].RSVD_MEM[31:0]	32
0xBB01C3EC	RSVD_ALE_DPM [7].RSVD_MEM[31:0]	32
0xBB01C3F0	RSVD_ALE_DPM [8].RSVD_MEM[31:0]	32
0xBB01C3F4	RSVD_ALE_DPM [9].RSVD_MEM[31:0]	32
0xBB01C3F8	RSVD_ALE_DPM [10].RSVD_MEM[31:0]	32
0xBB01C3FC	RSVD_ALE_DPM [11].RSVD_MEM[31:0]	32
0xBB01C400	RSVD_ALE_DPM [12].RSVD_MEM[31:0]	32
0xBB01C404	RSVD_ALE_DPM [13].RSVD_MEM[31:0]	32
0xBB01C408	RSVD_ALE_DPM [14].RSVD_MEM[31:0]	32
0xBB01C40C	RSVD_ALE_DPM [15].RSVD_MEM[31:0]	32
0xBB01D000	INTR_CTRL.RESERVED[31:1]	31
0xBB01D000	INTR_CTRL.INTR_POLARITY[0:0]	1
0xBB01D004	INTR_IMR.RESERVED[31:16]	16
0xBB01D004	INTR_IMR.IMR_ADC_ALARM[15:15]	1
0xBB01D004	INTR_IMR.IMR_THERMAL_ALARM[14:14]	1
0xBB01D004	INTR_IMR.IMR_DYING_GASP[13:13]	1
0xBB01D004	INTR_IMR.IMR_PTP[12:12]	1
0xBB01D004	INTR_IMR.IMR_EPON[11:11]	1
0xBB01D004	INTR_IMR.IMR_GPON[10:10]	1
0xBB01D004	INTR_IMR.IMR_SERDES[9:9]	1
0xBB01D004	INTR_IMR.IMR_GPHY[8:8]	1
0xBB01D004	INTR_IMR.IMR_ACL[7:7]	1
0xBB01D004	INTR_IMR.IMR_RTCT[6:6]	1
0xBB01D004	INTR_IMR.IMR_LOOP[5:5]	1
0xBB01D004	INTR_IMR.IMR_SPE_CONGEST[4:4]	1
0xBB01D004	INTR_IMR.IMR_SPE_CHG[3:3]	1
0xBB01D004	INTR_IMR.IMR_L2_LRN_OVER[2:2]	1
0xBB01D004	INTR_IMR.IMR_METER_EXCEED[1:1]	1
0xBB01D004	INTR_IMR.IMR_LINK_CHG[0:0]	1
0xBB01D008	INTR_IMS.RESERVED[31:16]	16
0xBB01D008	INTR_IMS.IMS_ADC_ALARM[15:15]	1
0xBB01D008	INTR_IMS.IMS_THERMAL_ALARM[14:14]	1
0xBB01D008	INTR_IMS.IMS_DYING_GASP[13:13]	1
0xBB01D008	INTR_IMS.IMS_PTP[12:12]	1
0xBB01D008	INTR_IMS.IMS_EPON[11:11]	1
0xBB01D008	INTR_IMS.IMS_GPON[10:10]	1
0xBB01D008	INTR_IMS.IMS_SERDES[9:9]	1
0xBB01D008	INTR_IMS.IMS_GPHY[8:8]	1
0xBB01D008	INTR_IMS.IMS_ACL[7:7]	1

Address	Register	Len
0xBB01D008	INTR_IMS.IMS_RTCT[6:6]	1
0xBB01D008	INTR_IMS.IMS_LOOP[5:5]	1
0xBB01D008	INTR_IMS.IMS_SPE_CONGEST[4:4]	1
0xBB01D008	INTR_IMS.IMS_SPE_CHG[3:3]	1
0xBB01D008	INTR_IMS.IMS_L2_LRN_OVER[2:2]	1
0xBB01D008	INTR_IMS.IMS_METER_EXCEED[1:1]	1
0xBB01D008	INTR_IMS.IMS_LINK_CHG[0:0]	1
0xBB01D00C	INTR_STAT.RESERVED[31:28]	4
0xBB01D00C	INTR_STAT.INTR_STAT_GPHY[27:23]	5
0xBB01D00C	INTR_STAT.INTR_STAT_PORT_LINKDOWN[22:16]	7
0xBB01D00C	INTR_STAT.RESERVED[15:15]	1
0xBB01D00C	INTR_STAT.INTR_STAT_PORT_LINKUP[14:8]	7
0xBB01D00C	INTR_STAT.RESERVED[7:7]	1
0xBB01D00C	INTR_STAT.INTR_STAT_PORT_CHANGE[6:0]	7
0xBB01D010	L2_LRN_OVER_STS [0].LRN_OVER_IND[0:0]	1
0xBB01D010	L2_LRN_OVER_STS [1].LRN_OVER_IND[1:1]	1
0xBB01D010	L2_LRN_OVER_STS [2].LRN_OVER_IND[2:2]	1
0xBB01D010	L2_LRN_OVER_STS [3].LRN_OVER_IND[3:3]	1
0xBB01D010	L2_LRN_OVER_STS [4].LRN_OVER_IND[4:4]	1
0xBB01D010	L2_LRN_OVER_STS [5].LRN_OVER_IND[5:5]	1
0xBB01D010	L2_LRN_OVER_STS [6].LRN_OVER_IND[6:6]	1
0xBB01D014	L2_SYS_LRN_OVER_STS.RESERVED[31:1]	31
0xBB01D014	L2_SYS_LRN_OVER_STS.LRN_OVER_IND[0:0]	1
0xBB01D018	SC_P_CTRL_1.RESERVED[31:7]	25
0xBB01D018	SC_P_CTRL_1.CGST_IND[6:0]	7
0xBB01D01C	RGF_VER_INTR.REGFILE_VER[31:0]	32
0xBB01D020	RSVD_INTR [0].RSVD_MEM[31:0]	32
0xBB01D024	RSVD_INTR [1].RSVD_MEM[31:0]	32
0xBB01D028	RSVD_INTR [2].RSVD_MEM[31:0]	32
0xBB01D02C	RSVD_INTR [3].RSVD_MEM[31:0]	32
0xBB01D030	RSVD_INTR [4].RSVD_MEM[31:0]	32
0xBB01D034	RSVD_INTR [5].RSVD_MEM[31:0]	32
0xBB01D038	RSVD_INTR [6].RSVD_MEM[31:0]	32
0xBB01D03C	RSVD_INTR [7].RSVD_MEM[31:0]	32
0xBB01D040	RSVD_INTR [8].RSVD_MEM[31:0]	32
0xBB01D044	RSVD_INTR [9].RSVD_MEM[31:0]	32
0xBB01D048	RSVD_INTR [10].RSVD_MEM[31:0]	32
0xBB01D04C	RSVD_INTR [11].RSVD_MEM[31:0]	32
0xBB01D050	RSVD_INTR [12].RSVD_MEM[31:0]	32
0xBB01D054	RSVD_INTR [13].RSVD_MEM[31:0]	32
0xBB01D058	RSVD_INTR [14].RSVD_MEM[31:0]	32
0xBB01D05C	RSVD_INTR [15].RSVD_MEM[31:0]	32
0xBB01E000	LED_LED.RESERVED[31:1]	31
0xBB01E000	LED_LED.LED_SEL[0:0]	1
0xBB01E004	DATA_LED_CFG [0].RESERVED[31:21]	11
0xBB01E004	DATA_LED_CFG [0].LED_CFG[20:16]	5



Address	Register	Len
0xBB01E004	DATA_LED_CFG [0].RESERVED[15:13]	3
0xBB01E004	DATA_LED_CFG [0].CPU_FORCE_MOD[12:12]	1
0xBB01E004	DATA_LED_CFG [0].UTP_SPD1000[11:11]	1
0xBB01E004	DATA_LED_CFG [0].UTP_SPD500[10:10]	1
0xBB01E004	DATA_LED_CFG [0].UTP_SPD100[9:9]	1
0xBB01E004	DATA_LED_CFG [0].UTP_SPD10[8:8]	1
0xBB01E004	DATA_LED_CFG [0].UTP_DUP[7:7]	1
0xBB01E004	DATA_LED_CFG [0].UTP_SPD1000_ACT[6:6]	1
0xBB01E004	DATA_LED_CFG [0].UTP_SPD500_ACT[5:5]	1
0xBB01E004	DATA_LED_CFG [0].UTP_SPD100_ACT[4:4]	1
0xBB01E004	DATA_LED_CFG [0].UTP_SPD10_ACT[3:3]	1
0xBB01E004	DATA_LED_CFG [0].UTP_RX_ACT[2:2]	1
0xBB01E004	DATA_LED_CFG [0].UTP_TX_ACT[1:1]	1
0xBB01E004	DATA_LED_CFG [0].UTP_COL[0:0]	1
0xBB01E008	DATA_LED_CFG [1].RESERVED[31:21]	11
0xBB01E008	DATA_LED_CFG [1].LED_CFG[20:16]	5
0xBB01E008	DATA_LED_CFG [1].RESERVED[15:13]	3
0xBB01E008	DATA_LED_CFG [1].CPU_FORCE_MOD[12:12]	1
0xBB01E008	DATA_LED_CFG [1].UTP_SPD1000[11:11]	1
0xBB01E008	DATA_LED_CFG [1].UTP_SPD500[10:10]	1
0xBB01E008	DATA_LED_CFG [1].UTP_SPD100[9:9]	1
0xBB01E008	DATA_LED_CFG [1].UTP_SPD10[8:8]	1
0xBB01E008	DATA_LED_CFG [1].UTP_DUP[7:7]	1
0xBB01E008	DATA_LED_CFG [1].UTP_SPD1000_ACT[6:6]	1
0xBB01E008	DATA_LED_CFG [1].UTP_SPD500_ACT[5:5]	1
0xBB01E008	DATA_LED_CFG [1].UTP_SPD100_ACT[4:4]	1
0xBB01E008	DATA_LED_CFG [1].UTP_SPD10_ACT[3:3]	1
0xBB01E008	DATA_LED_CFG [1].UTP_RX_ACT[2:2]	1
0xBB01E008	DATA_LED_CFG [1].UTP_TX_ACT[1:1]	1
0xBB01E008	DATA_LED_CFG [1].UTP_COL[0:0]	1
0xBB01E00C	DATA_LED_CFG [2].RESERVED[31:21]	11
0xBB01E00C	DATA_LED_CFG [2].LED_CFG[20:16]	5
0xBB01E00C	DATA_LED_CFG [2].RESERVED[15:13]	3
0xBB01E00C	DATA_LED_CFG [2].CPU_FORCE_MOD[12:12]	1
0xBB01E00C	DATA_LED_CFG [2].UTP_SPD1000[11:11]	1
0xBB01E00C	DATA_LED_CFG [2].UTP_SPD500[10:10]	1
0xBB01E00C	DATA_LED_CFG [2].UTP_SPD100[9:9]	1
0xBB01E00C	DATA_LED_CFG [2].UTP_SPD10[8:8]	1
0xBB01E00C	DATA_LED_CFG [2].UTP_DUP[7:7]	1
0xBB01E00C	DATA_LED_CFG [2].UTP_SPD1000_ACT[6:6]	1
0xBB01E00C	DATA_LED_CFG [2].UTP_SPD500_ACT[5:5]	1
0xBB01E00C	DATA_LED_CFG [2].UTP_SPD100_ACT[4:4]	1
0xBB01E00C	DATA_LED_CFG [2].UTP_SPD10_ACT[3:3]	1
0xBB01E00C	DATA_LED_CFG [2].UTP_RX_ACT[2:2]	1
0xBB01E00C	DATA_LED_CFG [2].UTP_TX_ACT[1:1]	1
0xBB01E00C	DATA_LED_CFG [2].UTP_COL[0:0]	1



Address	Register	Len
0xBB01E010	DATA_LED_CFG [3].RESERVED[31:21]	11
0xBB01E010	DATA_LED_CFG [3].LED_CFG[20:16]	5
0xBB01E010	DATA_LED_CFG [3].RESERVED[15:13]	3
0xBB01E010	DATA_LED_CFG [3].CPU_FORCE_MOD[12:12]	1
0xBB01E010	DATA_LED_CFG [3].UTP_SPD1000[11:11]	1
0xBB01E010	DATA_LED_CFG [3].UTP_SPD500[10:10]	1
0xBB01E010	DATA_LED_CFG [3].UTP_SPD100[9:9]	1
0xBB01E010	DATA_LED_CFG [3].UTP_SPD10[8:8]	1
0xBB01E010	DATA_LED_CFG [3].UTP_DUP[7:7]	1
0xBB01E010	DATA_LED_CFG [3].UTP_SPD1000_ACT[6:6]	1
0xBB01E010	DATA_LED_CFG [3].UTP_SPD500_ACT[5:5]	1
0xBB01E010	DATA_LED_CFG [3].UTP_SPD100_ACT[4:4]	1
0xBB01E010	DATA_LED_CFG [3].UTP_SPD10_ACT[3:3]	1
0xBB01E010	DATA_LED_CFG [3].UTP_RX_ACT[2:2]	1
0xBB01E010	DATA_LED_CFG [3].UTP_TX_ACT[1:1]	1
0xBB01E010	DATA_LED_CFG [3].UTP_COL[0:0]	1
0xBB01E014	DATA_LED_CFG [4].RESERVED[31:21]	11
0xBB01E014	DATA_LED_CFG [4].LED_CFG[20:16]	5
0xBB01E014	DATA_LED_CFG [4].RESERVED[15:13]	3
0xBB01E014	DATA_LED_CFG [4].CPU_FORCE_MOD[12:12]	1
0xBB01E014	DATA_LED_CFG [4].UTP_SPD1000[11:11]	1
0xBB01E014	DATA_LED_CFG [4].UTP_SPD500[10:10]	1
0xBB01E014	DATA_LED_CFG [4].UTP_SPD100[9:9]	1
0xBB01E014	DATA_LED_CFG [4].UTP_SPD10[8:8]	1
0xBB01E014	DATA_LED_CFG [4].UTP_DUP[7:7]	1
0xBB01E014	DATA_LED_CFG [4].UTP_SPD1000_ACT[6:6]	1
0xBB01E014	DATA_LED_CFG [4].UTP_SPD500_ACT[5:5]	1
0xBB01E014	DATA_LED_CFG [4].UTP_SPD100_ACT[4:4]	1
0xBB01E014	DATA_LED_CFG [4].UTP_SPD10_ACT[3:3]	1
0xBB01E014	DATA_LED_CFG [4].UTP_RX_ACT[2:2]	1
0xBB01E014	DATA_LED_CFG [4].UTP_TX_ACT[1:1]	1
0xBB01E014	DATA_LED_CFG [4].UTP_COL[0:0]	1
0xBB01E018	DATA_LED_CFG [5].RESERVED[31:21]	11
0xBB01E018	DATA_LED_CFG [5].LED_CFG[20:16]	5
0xBB01E018	DATA_LED_CFG [5].RESERVED[15:13]	3
0xBB01E018	DATA_LED_CFG [5].CPU_FORCE_MOD[12:12]	1
0xBB01E018	DATA_LED_CFG [5].UTP_SPD1000[11:11]	1
0xBB01E018	DATA_LED_CFG [5].UTP_SPD500[10:10]	1
0xBB01E018	DATA_LED_CFG [5].UTP_SPD100[9:9]	1
0xBB01E018	DATA_LED_CFG [5].UTP_SPD10[8:8]	1
0xBB01E018	DATA_LED_CFG [5].UTP_DUP[7:7]	1
0xBB01E018	DATA_LED_CFG [5].UTP_SPD1000_ACT[6:6]	1
0xBB01E018	DATA_LED_CFG [5].UTP_SPD500_ACT[5:5]	1
0xBB01E018	DATA_LED_CFG [5].UTP_SPD100_ACT[4:4]	1
0xBB01E018	DATA_LED_CFG [5].UTP_SPD10_ACT[3:3]	1
0xBB01E018	DATA_LED_CFG [5].UTP_RX_ACT[2:2]	1

Address	Register	Len
0xBB01E018	DATA_LED_CFG [5].UTP_TX_ACT[1:1]	1
0xBB01E018	DATA_LED_CFG [5].UTP_COL[0:0]	1
0xBB01E01C	DATA_LED_CFG [6].RESERVED[31:21]	11
0xBB01E01C	DATA_LED_CFG [6].LED_CFG[20:16]	5
0xBB01E01C	DATA_LED_CFG [6].RESERVED[15:13]	3
0xBB01E01C	DATA_LED_CFG [6].CPU_FORCE_MOD[12:12]	1
0xBB01E01C	DATA_LED_CFG [6].UTP_SPD1000[11:11]	1
0xBB01E01C	DATA_LED_CFG [6].UTP_SPD500[10:10]	1
0xBB01E01C	DATA_LED_CFG [6].UTP_SPD100[9:9]	1
0xBB01E01C	DATA_LED_CFG [6].UTP_SPD10[8:8]	1
0xBB01E01C	DATA_LED_CFG [6].UTP_DUP[7:7]	1
0xBB01E01C	DATA_LED_CFG [6].UTP_SPD1000_ACT[6:6]	1
0xBB01E01C	DATA_LED_CFG [6].UTP_SPD500_ACT[5:5]	1
0xBB01E01C	DATA_LED_CFG [6].UTP_SPD100_ACT[4:4]	1
0xBB01E01C	DATA_LED_CFG [6].UTP_SPD10_ACT[3:3]	1
0xBB01E01C	DATA_LED_CFG [6].UTP_RX_ACT[2:2]	1
0xBB01E01C	DATA_LED_CFG [6].UTP_TX_ACT[1:1]	1
0xBB01E01C	DATA_LED_CFG [6].UTP_COL[0:0]	1
0xBB01E020	DATA_LED_CFG [7].RESERVED[31:21]	11
0xBB01E020	DATA_LED_CFG [7].LED_CFG[20:16]	5
0xBB01E020	DATA_LED_CFG [7].RESERVED[15:13]	3
0xBB01E020	DATA_LED_CFG [7].CPU_FORCE_MOD[12:12]	1
0xBB01E020	DATA_LED_CFG [7].UTP_SPD1000[11:11]	1
0xBB01E020	DATA_LED_CFG [7].UTP_SPD500[10:10]	1
0xBB01E020	DATA_LED_CFG [7].UTP_SPD100[9:9]	1
0xBB01E020	DATA_LED_CFG [7].UTP_SPD10[8:8]	1
0xBB01E020	DATA_LED_CFG [7].UTP_DUP[7:7]	1
0xBB01E020	DATA_LED_CFG [7].UTP_SPD1000_ACT[6:6]	1
0xBB01E020	DATA_LED_CFG [7].UTP_SPD500_ACT[5:5]	1
0xBB01E020	DATA_LED_CFG [7].UTP_SPD100_ACT[4:4]	1
0xBB01E020	DATA_LED_CFG [7].UTP_SPD10_ACT[3:3]	1
0xBB01E020	DATA_LED_CFG [7].UTP_RX_ACT[2:2]	1
0xBB01E020	DATA_LED_CFG [7].UTP_TX_ACT[1:1]	1
0xBB01E020	DATA_LED_CFG [7].UTP_COL[0:0]	1
0xBB01E024	DATA_LED_CFG [8].RESERVED[31:21]	11
0xBB01E024	DATA_LED_CFG [8].LED_CFG[20:16]	5
0xBB01E024	DATA_LED_CFG [8].RESERVED[15:13]	3
0xBB01E024	DATA_LED_CFG [8].CPU_FORCE_MOD[12:12]	1
0xBB01E024	DATA_LED_CFG [8].UTP_SPD1000[11:11]	1
0xBB01E024	DATA_LED_CFG [8].UTP_SPD500[10:10]	1
0xBB01E024	DATA_LED_CFG [8].UTP_SPD100[9:9]	1
0xBB01E024	DATA_LED_CFG [8].UTP_SPD10[8:8]	1
0xBB01E024	DATA_LED_CFG [8].UTP_DUP[7:7]	1
0xBB01E024	DATA_LED_CFG [8].UTP_SPD1000_ACT[6:6]	1
0xBB01E024	DATA_LED_CFG [8].UTP_SPD500_ACT[5:5]	1
0xBB01E024	DATA_LED_CFG [8].UTP_SPD100_ACT[4:4]	1

Address	Register	Len
0xBB01E024	DATA_LED_CFG [8].UTP_SPD10_ACT[3:3]	1
0xBB01E024	DATA_LED_CFG [8].UTP_RX_ACT[2:2]	1
0xBB01E024	DATA_LED_CFG [8].UTP_TX_ACT[1:1]	1
0xBB01E024	DATA_LED_CFG [8].UTP_COL[0:0]	1
0xBB01E028	DATA_LED_CFG [9].RESERVED[31:21]	11
0xBB01E028	DATA_LED_CFG [9].LED_CFG[20:16]	5
0xBB01E028	DATA_LED_CFG [9].RESERVED[15:13]	3
0xBB01E028	DATA_LED_CFG [9].CPU_FORCE_MOD[12:12]	1
0xBB01E028	DATA_LED_CFG [9].UTP_SPD1000[11:11]	1
0xBB01E028	DATA_LED_CFG [9].UTP_SPD500[10:10]	1
0xBB01E028	DATA_LED_CFG [9].UTP_SPD100[9:9]	1
0xBB01E028	DATA_LED_CFG [9].UTP_SPD10[8:8]	1
0xBB01E028	DATA_LED_CFG [9].UTP_DUP[7:7]	1
0xBB01E028	DATA_LED_CFG [9].UTP_SPD1000_ACT[6:6]	1
0xBB01E028	DATA_LED_CFG [9].UTP_SPD500_ACT[5:5]	1
0xBB01E028	DATA_LED_CFG [9].UTP_SPD100_ACT[4:4]	1
0xBB01E028	DATA_LED_CFG [9].UTP_SPD10_ACT[3:3]	1
0xBB01E028	DATA_LED_CFG [9].UTP_RX_ACT[2:2]	1
0xBB01E028	DATA_LED_CFG [9].UTP_TX_ACT[1:1]	1
0xBB01E028	DATA_LED_CFG [9].UTP_COL[0:0]	1
0xBB01E02C	DATA_LED_CFG [10].RESERVED[31:21]	11
0xBB01E02C	DATA_LED_CFG [10].LED_CFG[20:16]	5
0xBB01E02C	DATA_LED_CFG [10].RESERVED[15:13]	3
0xBB01E02C	DATA_LED_CFG [10].CPU_FORCE_MOD[12:12]	1
0xBB01E02C	DATA_LED_CFG [10].UTP_SPD1000[11:11]	1
0xBB01E02C	DATA_LED_CFG [10].UTP_SPD500[10:10]	1
0xBB01E02C	DATA_LED_CFG [10].UTP_SPD100[9:9]	1
0xBB01E02C	DATA_LED_CFG [10].UTP_SPD10[8:8]	1
0xBB01E02C	DATA_LED_CFG [10].UTP_DUP[7:7]	1
0xBB01E02C	DATA_LED_CFG [10].UTP_SPD1000_ACT[6:6]	1
0xBB01E02C	DATA_LED_CFG [10].UTP_SPD500_ACT[5:5]	1
0xBB01E02C	DATA_LED_CFG [10].UTP_SPD100_ACT[4:4]	1
0xBB01E02C	DATA_LED_CFG [10].UTP_SPD10_ACT[3:3]	1
0xBB01E02C	DATA_LED_CFG [10].UTP_RX_ACT[2:2]	1
0xBB01E02C	DATA_LED_CFG [10].UTP_TX_ACT[1:1]	1
0xBB01E02C	DATA_LED_CFG [10].UTP_COL[0:0]	1
0xBB01E030	DATA_LED_CFG [11].RESERVED[31:21]	11
0xBB01E030	DATA_LED_CFG [11].LED_CFG[20:16]	5
0xBB01E030	DATA_LED_CFG [11].RESERVED[15:13]	3
0xBB01E030	DATA_LED_CFG [11].CPU_FORCE_MOD[12:12]	1
0xBB01E030	DATA_LED_CFG [11].UTP_SPD1000[11:11]	1
0xBB01E030	DATA_LED_CFG [11].UTP_SPD500[10:10]	1
0xBB01E030	DATA_LED_CFG [11].UTP_SPD100[9:9]	1
0xBB01E030	DATA_LED_CFG [11].UTP_SPD10[8:8]	1
0xBB01E030	DATA_LED_CFG [11].UTP_DUP[7:7]	1
0xBB01E030	DATA_LED_CFG [11].UTP_SPD1000_ACT[6:6]	1

Address	Register	Len
0xBB01E030	DATA_LED_CFG [11].UTP_SPD500_ACT[5:5]	1
0xBB01E030	DATA_LED_CFG [11].UTP_SPD100_ACT[4:4]	1
0xBB01E030	DATA_LED_CFG [11].UTP_SPD10_ACT[3:3]	1
0xBB01E030	DATA_LED_CFG [11].UTP_RX_ACT[2:2]	1
0xBB01E030	DATA_LED_CFG [11].UTP_TX_ACT[1:1]	1
0xBB01E030	DATA_LED_CFG [11].UTP_COL[0:0]	1
0xBB01E034	DATA_LED_CFG [12].RESERVED[31:21]	11
0xBB01E034	DATA_LED_CFG [12].LED_CFG[20:16]	5
0xBB01E034	DATA_LED_CFG [12].RESERVED[15:13]	3
0xBB01E034	DATA_LED_CFG [12].CPU_FORCE_MOD[12:12]	1
0xBB01E034	DATA_LED_CFG [12].UTP_SPD1000[11:11]	1
0xBB01E034	DATA_LED_CFG [12].UTP_SPD500[10:10]	1
0xBB01E034	DATA_LED_CFG [12].UTP_SPD100[9:9]	1
0xBB01E034	DATA_LED_CFG [12].UTP_SPD10[8:8]	1
0xBB01E034	DATA_LED_CFG [12].UTP_DUP[7:7]	1
0xBB01E034	DATA_LED_CFG [12].UTP_SPD1000_ACT[6:6]	1
0xBB01E034	DATA_LED_CFG [12].UTP_SPD500_ACT[5:5]	1
0xBB01E034	DATA_LED_CFG [12].UTP_SPD100_ACT[4:4]	1
0xBB01E034	DATA_LED_CFG [12].UTP_SPD10_ACT[3:3]	1
0xBB01E034	DATA_LED_CFG [12].UTP_RX_ACT[2:2]	1
0xBB01E034	DATA_LED_CFG [12].UTP_TX_ACT[1:1]	1
0xBB01E034	DATA_LED_CFG [12].UTP_COL[0:0]	1
0xBB01E038	DATA_LED_CFG [13].RESERVED[31:21]	11
0xBB01E038	DATA_LED_CFG [13].LED_CFG[20:16]	5
0xBB01E038	DATA_LED_CFG [13].RESERVED[15:13]	3
0xBB01E038	DATA_LED_CFG [13].CPU_FORCE_MOD[12:12]	1
0xBB01E038	DATA_LED_CFG [13].UTP_SPD1000[11:11]	1
0xBB01E038	DATA_LED_CFG [13].UTP_SPD500[10:10]	1
0xBB01E038	DATA_LED_CFG [13].UTP_SPD100[9:9]	1
0xBB01E038	DATA_LED_CFG [13].UTP_SPD10[8:8]	1
0xBB01E038	DATA_LED_CFG [13].UTP_DUP[7:7]	1
0xBB01E038	DATA_LED_CFG [13].UTP_SPD1000_ACT[6:6]	1
0xBB01E038	DATA_LED_CFG [13].UTP_SPD500_ACT[5:5]	1
0xBB01E038	DATA_LED_CFG [13].UTP_SPD100_ACT[4:4]	1
0xBB01E038	DATA_LED_CFG [13].UTP_SPD10_ACT[3:3]	1
0xBB01E038	DATA_LED_CFG [13].UTP_RX_ACT[2:2]	1
0xBB01E038	DATA_LED_CFG [13].UTP_TX_ACT[1:1]	1
0xBB01E038	DATA_LED_CFG [13].UTP_COL[0:0]	1
0xBB01E03C	DATA_LED_CFG [14].RESERVED[31:21]	11
0xBB01E03C	DATA_LED_CFG [14].LED_CFG[20:16]	5
0xBB01E03C	DATA_LED_CFG [14].RESERVED[15:13]	3
0xBB01E03C	DATA_LED_CFG [14].CPU_FORCE_MOD[12:12]	1
0xBB01E03C	DATA_LED_CFG [14].UTP_SPD1000[11:11]	1
0xBB01E03C	DATA_LED_CFG [14].UTP_SPD500[10:10]	1
0xBB01E03C	DATA_LED_CFG [14].UTP_SPD100[9:9]	1
0xBB01E03C	DATA_LED_CFG [14].UTP_SPD10[8:8]	1

Address	Register	Len
0xBB01E03C	DATA_LED_CFG [14].UTP_DUP[7:7]	1
0xBB01E03C	DATA_LED_CFG [14].UTP_SPD1000_ACT[6:6]	1
0xBB01E03C	DATA_LED_CFG [14].UTP_SPD500_ACT[5:5]	1
0xBB01E03C	DATA_LED_CFG [14].UTP_SPD100_ACT[4:4]	1
0xBB01E03C	DATA_LED_CFG [14].UTP_SPD10_ACT[3:3]	1
0xBB01E03C	DATA_LED_CFG [14].UTP_RX_ACT[2:2]	1
0xBB01E03C	DATA_LED_CFG [14].UTP_TX_ACT[1:1]	1
0xBB01E03C	DATA_LED_CFG [14].UTP_COL[0:0]	1
0xBB01E040	DATA_LED_CFG [15].RESERVED[31:21]	11
0xBB01E040	DATA_LED_CFG [15].LED_CFG[20:16]	5
0xBB01E040	DATA_LED_CFG [15].RESERVED[15:13]	3
0xBB01E040	DATA_LED_CFG [15].CPU_FORCE_MOD[12:12]	1
0xBB01E040	DATA_LED_CFG [15].UTP_SPD1000[11:11]	1
0xBB01E040	DATA_LED_CFG [15].UTP_SPD500[10:10]	1
0xBB01E040	DATA_LED_CFG [15].UTP_SPD100[9:9]	1
0xBB01E040	DATA_LED_CFG [15].UTP_SPD10[8:8]	1
0xBB01E040	DATA_LED_CFG [15].UTP_DUP[7:7]	1
0xBB01E040	DATA_LED_CFG [15].UTP_SPD1000_ACT[6:6]	1
0xBB01E040	DATA_LED_CFG [15].UTP_SPD500_ACT[5:5]	1
0xBB01E040	DATA_LED_CFG [15].UTP_SPD100_ACT[4:4]	1
0xBB01E040	DATA_LED_CFG [15].UTP_SPD10_ACT[3:3]	1
0xBB01E040	DATA_LED_CFG [15].UTP_RX_ACT[2:2]	1
0xBB01E040	DATA_LED_CFG [15].UTP_TX_ACT[1:1]	1
0xBB01E040	DATA_LED_CFG [15].UTP_COL[0:0]	1
0xBB01E044	DATA_LED_CFG [16].RESERVED[31:21]	11
0xBB01E044	DATA_LED_CFG [16].LED_CFG[20:16]	5
0xBB01E044	DATA_LED_CFG [16].RESERVED[15:13]	3
0xBB01E044	DATA_LED_CFG [16].CPU_FORCE_MOD[12:12]	1
0xBB01E044	DATA_LED_CFG [16].UTP_SPD1000[11:11]	1
0xBB01E044	DATA_LED_CFG [16].UTP_SPD500[10:10]	1
0xBB01E044	DATA_LED_CFG [16].UTP_SPD100[9:9]	1
0xBB01E044	DATA_LED_CFG [16].UTP_SPD10[8:8]	1
0xBB01E044	DATA_LED_CFG [16].UTP_DUP[7:7]	1
0xBB01E044	DATA_LED_CFG [16].UTP_SPD1000_ACT[6:6]	1
0xBB01E044	DATA_LED_CFG [16].UTP_SPD500_ACT[5:5]	1
0xBB01E044	DATA_LED_CFG [16].UTP_SPD100_ACT[4:4]	1
0xBB01E044	DATA_LED_CFG [16].UTP_SPD10_ACT[3:3]	1
0xBB01E044	DATA_LED_CFG [16].UTP_RX_ACT[2:2]	1
0xBB01E044	DATA_LED_CFG [16].UTP_TX_ACT[1:1]	1
0xBB01E044	DATA_LED_CFG [16].UTP_COL[0:0]	1
0xBB01E048	DATA_LED_CFG [17].RESERVED[31:21]	11
0xBB01E048	DATA_LED_CFG [17].LED_CFG[20:16]	5
0xBB01E048	DATA_LED_CFG [17].RESERVED[15:13]	3
0xBB01E048	DATA_LED_CFG [17].CPU_FORCE_MOD[12:12]	1
0xBB01E048	DATA_LED_CFG [17].UTP_SPD1000[11:11]	1
0xBB01E048	DATA_LED_CFG [17].UTP_SPD500[10:10]	1

Address	Register	Len
0xBB01E048	DATA_LED_CFG [17].UTP_SPD100[9:9]	1
0xBB01E048	DATA_LED_CFG [17].UTP_SPD10[8:8]	1
0xBB01E048	DATA_LED_CFG [17].UTP_DUP[7:7]	1
0xBB01E048	DATA_LED_CFG [17].UTP_SPD1000_ACT[6:6]	1
0xBB01E048	DATA_LED_CFG [17].UTP_SPD500_ACT[5:5]	1
0xBB01E048	DATA_LED_CFG [17].UTP_SPD100_ACT[4:4]	1
0xBB01E048	DATA_LED_CFG [17].UTP_SPD10_ACT[3:3]	1
0xBB01E048	DATA_LED_CFG [17].UTP_RX_ACT[2:2]	1
0xBB01E048	DATA_LED_CFG [17].UTP_TX_ACT[1:1]	1
0xBB01E048	DATA_LED_CFG [17].UTP_COL[0:0]	1
0xBB01E04C	DATA_LED_CFG [18].RESERVED[31:21]	11
0xBB01E04C	DATA_LED_CFG [18].LED_CFG[20:16]	5
0xBB01E04C	DATA_LED_CFG [18].RESERVED[15:13]	3
0xBB01E04C	DATA_LED_CFG [18].CPU_FORCE_MOD[12:12]	1
0xBB01E04C	DATA_LED_CFG [18].UTP_SPD1000[11:11]	1
0xBB01E04C	DATA_LED_CFG [18].UTP_SPD500[10:10]	1
0xBB01E04C	DATA_LED_CFG [18].UTP_SPD100[9:9]	1
0xBB01E04C	DATA_LED_CFG [18].UTP_SPD10[8:8]	1
0xBB01E04C	DATA_LED_CFG [18].UTP_DUP[7:7]	1
0xBB01E04C	DATA_LED_CFG [18].UTP_SPD1000_ACT[6:6]	1
0xBB01E04C	DATA_LED_CFG [18].UTP_SPD500_ACT[5:5]	1
0xBB01E04C	DATA_LED_CFG [18].UTP_SPD100_ACT[4:4]	1
0xBB01E04C	DATA_LED_CFG [18].UTP_SPD10_ACT[3:3]	1
0xBB01E04C	DATA_LED_CFG [18].UTP_RX_ACT[2:2]	1
0xBB01E04C	DATA_LED_CFG [18].UTP_TX_ACT[1:1]	1
0xBB01E04C	DATA_LED_CFG [18].UTP_COL[0:0]	1
0xBB01E050	DATA_LED_CFG [19].RESERVED[31:21]	11
0xBB01E050	DATA_LED_CFG [19].LED_CFG[20:16]	5
0xBB01E050	DATA_LED_CFG [19].RESERVED[15:13]	3
0xBB01E050	DATA_LED_CFG [19].CPU_FORCE_MOD[12:12]	1
0xBB01E050	DATA_LED_CFG [19].UTP_SPD1000[11:11]	1
0xBB01E050	DATA_LED_CFG [19].UTP_SPD500[10:10]	1
0xBB01E050	DATA_LED_CFG [19].UTP_SPD100[9:9]	1
0xBB01E050	DATA_LED_CFG [19].UTP_SPD10[8:8]	1
0xBB01E050	DATA_LED_CFG [19].UTP_DUP[7:7]	1
0xBB01E050	DATA_LED_CFG [19].UTP_SPD1000_ACT[6:6]	1
0xBB01E050	DATA_LED_CFG [19].UTP_SPD500_ACT[5:5]	1
0xBB01E050	DATA_LED_CFG [19].UTP_SPD100_ACT[4:4]	1
0xBB01E050	DATA_LED_CFG [19].UTP_SPD10_ACT[3:3]	1
0xBB01E050	DATA_LED_CFG [19].UTP_RX_ACT[2:2]	1
0xBB01E050	DATA_LED_CFG [19].UTP_TX_ACT[1:1]	1
0xBB01E050	DATA_LED_CFG [19].UTP_COL[0:0]	1
0xBB01E054	DATA_LED_CFG [20].RESERVED[31:21]	11
0xBB01E054	DATA_LED_CFG [20].LED_CFG[20:16]	5
0xBB01E054	DATA_LED_CFG [20].RESERVED[15:13]	3
0xBB01E054	DATA_LED_CFG [20].CPU_FORCE_MOD[12:12]	1

Address	Register	Len
0xBB01E054	DATA_LED_CFG [20].UTP_SPD1000[11:11]	1
0xBB01E054	DATA_LED_CFG [20].UTP_SPD500[10:10]	1
0xBB01E054	DATA_LED_CFG [20].UTP_SPD100[9:9]	1
0xBB01E054	DATA_LED_CFG [20].UTP_SPD10[8:8]	1
0xBB01E054	DATA_LED_CFG [20].UTP_DUP[7:7]	1
0xBB01E054	DATA_LED_CFG [20].UTP_SPD1000_ACT[6:6]	1
0xBB01E054	DATA_LED_CFG [20].UTP_SPD500_ACT[5:5]	1
0xBB01E054	DATA_LED_CFG [20].UTP_SPD100_ACT[4:4]	1
0xBB01E054	DATA_LED_CFG [20].UTP_SPD10_ACT[3:3]	1
0xBB01E054	DATA_LED_CFG [20].UTP_RX_ACT[2:2]	1
0xBB01E054	DATA_LED_CFG [20].UTP_TX_ACT[1:1]	1
0xBB01E054	DATA_LED_CFG [20].UTP_COL[0:0]	1
0xBB01E058	DATA_LED_CFG [21].RESERVED[31:21]	11
0xBB01E058	DATA_LED_CFG [21].LED_CFG[20:16]	5
0xBB01E058	DATA_LED_CFG [21].RESERVED[15:13]	3
0xBB01E058	DATA_LED_CFG [21].CPU_FORCE_MOD[12:12]	1
0xBB01E058	DATA_LED_CFG [21].UTP_SPD1000[11:11]	1
0xBB01E058	DATA_LED_CFG [21].UTP_SPD500[10:10]	1
0xBB01E058	DATA_LED_CFG [21].UTP_SPD100[9:9]	1
0xBB01E058	DATA_LED_CFG [21].UTP_SPD10[8:8]	1
0xBB01E058	DATA_LED_CFG [21].UTP_DUP[7:7]	1
0xBB01E058	DATA_LED_CFG [21].UTP_SPD1000_ACT[6:6]	1
0xBB01E058	DATA_LED_CFG [21].UTP_SPD500_ACT[5:5]	1
0xBB01E058	DATA_LED_CFG [21].UTP_SPD100_ACT[4:4]	1
0xBB01E058	DATA_LED_CFG [21].UTP_SPD10_ACT[3:3]	1
0xBB01E058	DATA_LED_CFG [21].UTP_RX_ACT[2:2]	1
0xBB01E058	DATA_LED_CFG [21].UTP_TX_ACT[1:1]	1
0xBB01E058	DATA_LED_CFG [21].UTP_COL[0:0]	1
0xBB01E05C	DATA_LED_CFG [22].RESERVED[31:21]	11
0xBB01E05C	DATA_LED_CFG [22].LED_CFG[20:16]	5
0xBB01E05C	DATA_LED_CFG [22].RESERVED[15:13]	3
0xBB01E05C	DATA_LED_CFG [22].CPU_FORCE_MOD[12:12]	1
0xBB01E05C	DATA_LED_CFG [22].UTP_SPD1000[11:11]	1
0xBB01E05C	DATA_LED_CFG [22].UTP_SPD500[10:10]	1
0xBB01E05C	DATA_LED_CFG [22].UTP_SPD100[9:9]	1
0xBB01E05C	DATA_LED_CFG [22].UTP_SPD10[8:8]	1
0xBB01E05C	DATA_LED_CFG [22].UTP_DUP[7:7]	1
0xBB01E05C	DATA_LED_CFG [22].UTP_SPD1000_ACT[6:6]	1
0xBB01E05C	DATA_LED_CFG [22].UTP_SPD500_ACT[5:5]	1
0xBB01E05C	DATA_LED_CFG [22].UTP_SPD100_ACT[4:4]	1
0xBB01E05C	DATA_LED_CFG [22].UTP_SPD10_ACT[3:3]	1
0xBB01E05C	DATA_LED_CFG [22].UTP_RX_ACT[2:2]	1
0xBB01E05C	DATA_LED_CFG [22].UTP_TX_ACT[1:1]	1
0xBB01E05C	DATA_LED_CFG [22].UTP_COL[0:0]	1
0xBB01E060	DATA_LED_CFG [23].RESERVED[31:21]	11
0xBB01E060	DATA_LED_CFG [23].LED_CFG[20:16]	5



Address	Register	Len
0xBB01E060	DATA_LED_CFG [23].RESERVED[15:13]	3
0xBB01E060	DATA_LED_CFG [23].CPU_FORCE_MOD[12:12]	1
0xBB01E060	DATA_LED_CFG [23].UTP_SPD1000[11:11]	1
0xBB01E060	DATA_LED_CFG [23].UTP_SPD500[10:10]	1
0xBB01E060	DATA_LED_CFG [23].UTP_SPD100[9:9]	1
0xBB01E060	DATA_LED_CFG [23].UTP_SPD10[8:8]	1
0xBB01E060	DATA_LED_CFG [23].UTP_DUP[7:7]	1
0xBB01E060	DATA_LED_CFG [23].UTP_SPD1000_ACT[6:6]	1
0xBB01E060	DATA_LED_CFG [23].UTP_SPD500_ACT[5:5]	1
0xBB01E060	DATA_LED_CFG [23].UTP_SPD100_ACT[4:4]	1
0xBB01E060	DATA_LED_CFG [23].UTP_SPD10_ACT[3:3]	1
0xBB01E060	DATA_LED_CFG [23].UTP_RX_ACT[2:2]	1
0xBB01E060	DATA_LED_CFG [23].UTP_TX_ACT[1:1]	1
0xBB01E060	DATA_LED_CFG [23].UTP_COL[0:0]	1
0xBB01E064	DATA_LED_CFG [24].RESERVED[31:21]	11
0xBB01E064	DATA_LED_CFG [24].LED_CFG[20:16]	5
0xBB01E064	DATA_LED_CFG [24].RESERVED[15:13]	3
0xBB01E064	DATA_LED_CFG [24].CPU_FORCE_MOD[12:12]	1
0xBB01E064	DATA_LED_CFG [24].UTP_SPD1000[11:11]	1
0xBB01E064	DATA_LED_CFG [24].UTP_SPD500[10:10]	1
0xBB01E064	DATA_LED_CFG [24].UTP_SPD100[9:9]	1
0xBB01E064	DATA_LED_CFG [24].UTP_SPD10[8:8]	1
0xBB01E064	DATA_LED_CFG [24].UTP_DUP[7:7]	1
0xBB01E064	DATA_LED_CFG [24].UTP_SPD1000_ACT[6:6]	1
0xBB01E064	DATA_LED_CFG [24].UTP_SPD500_ACT[5:5]	1
0xBB01E064	DATA_LED_CFG [24].UTP_SPD100_ACT[4:4]	1
0xBB01E064	DATA_LED_CFG [24].UTP_SPD10_ACT[3:3]	1
0xBB01E064	DATA_LED_CFG [24].UTP_RX_ACT[2:2]	1
0xBB01E064	DATA_LED_CFG [24].UTP_TX_ACT[1:1]	1
0xBB01E064	DATA_LED_CFG [24].UTP_COL[0:0]	1
0xBB01E068	DATA_LED_CFG [25].RESERVED[31:21]	11
0xBB01E068	DATA_LED_CFG [25].LED_CFG[20:16]	5
0xBB01E068	DATA_LED_CFG [25].RESERVED[15:13]	3
0xBB01E068	DATA_LED_CFG [25].CPU_FORCE_MOD[12:12]	1
0xBB01E068	DATA_LED_CFG [25].UTP_SPD1000[11:11]	1
0xBB01E068	DATA_LED_CFG [25].UTP_SPD500[10:10]	1
0xBB01E068	DATA_LED_CFG [25].UTP_SPD100[9:9]	1
0xBB01E068	DATA_LED_CFG [25].UTP_SPD10[8:8]	1
0xBB01E068	DATA_LED_CFG [25].UTP_DUP[7:7]	1
0xBB01E068	DATA_LED_CFG [25].UTP_SPD1000_ACT[6:6]	1
0xBB01E068	DATA_LED_CFG [25].UTP_SPD500_ACT[5:5]	1
0xBB01E068	DATA_LED_CFG [25].UTP_SPD100_ACT[4:4]	1
0xBB01E068	DATA_LED_CFG [25].UTP_SPD10_ACT[3:3]	1
0xBB01E068	DATA_LED_CFG [25].UTP_RX_ACT[2:2]	1
0xBB01E068	DATA_LED_CFG [25].UTP_TX_ACT[1:1]	1
0xBB01E068	DATA_LED_CFG [25].UTP_COL[0:0]	1



Address	Register	Len
0xBB01E06C	DATA_LED_CFG [26].RESERVED[31:21]	11
0xBB01E06C	DATA_LED_CFG [26].LED_CFG[20:16]	5
0xBB01E06C	DATA_LED_CFG [26].RESERVED[15:13]	3
0xBB01E06C	DATA_LED_CFG [26].CPU_FORCE_MOD[12:12]	1
0xBB01E06C	DATA_LED_CFG [26].UTP_SPD1000[11:11]	1
0xBB01E06C	DATA_LED_CFG [26].UTP_SPD500[10:10]	1
0xBB01E06C	DATA_LED_CFG [26].UTP_SPD100[9:9]	1
0xBB01E06C	DATA_LED_CFG [26].UTP_SPD10[8:8]	1
0xBB01E06C	DATA_LED_CFG [26].UTP_DUP[7:7]	1
0xBB01E06C	DATA_LED_CFG [26].UTP_SPD1000_ACT[6:6]	1
0xBB01E06C	DATA_LED_CFG [26].UTP_SPD500_ACT[5:5]	1
0xBB01E06C	DATA_LED_CFG [26].UTP_SPD100_ACT[4:4]	1
0xBB01E06C	DATA_LED_CFG [26].UTP_SPD10_ACT[3:3]	1
0xBB01E06C	DATA_LED_CFG [26].UTP_RX_ACT[2:2]	1
0xBB01E06C	DATA_LED_CFG [26].UTP_TX_ACT[1:1]	1
0xBB01E06C	DATA_LED_CFG [26].UTP_COL[0:0]	1
0xBB01E070	DATA_LED_CFG [27].RESERVED[31:21]	11
0xBB01E070	DATA_LED_CFG [27].LED_CFG[20:16]	5
0xBB01E070	DATA_LED_CFG [27].RESERVED[15:13]	3
0xBB01E070	DATA_LED_CFG [27].CPU_FORCE_MOD[12:12]	1
0xBB01E070	DATA_LED_CFG [27].UTP_SPD1000[11:11]	1
0xBB01E070	DATA_LED_CFG [27].UTP_SPD500[10:10]	1
0xBB01E070	DATA_LED_CFG [27].UTP_SPD100[9:9]	1
0xBB01E070	DATA_LED_CFG [27].UTP_SPD10[8:8]	1
0xBB01E070	DATA_LED_CFG [27].UTP_DUP[7:7]	1
0xBB01E070	DATA_LED_CFG [27].UTP_SPD1000_ACT[6:6]	1
0xBB01E070	DATA_LED_CFG [27].UTP_SPD500_ACT[5:5]	1
0xBB01E070	DATA_LED_CFG [27].UTP_SPD100_ACT[4:4]	1
0xBB01E070	DATA_LED_CFG [27].UTP_SPD10_ACT[3:3]	1
0xBB01E070	DATA_LED_CFG [27].UTP_RX_ACT[2:2]	1
0xBB01E070	DATA_LED_CFG [27].UTP_TX_ACT[1:1]	1
0xBB01E070	DATA_LED_CFG [27].UTP_COL[0:0]	1
0xBB01E074	DATA_LED_CFG [28].RESERVED[31:21]	11
0xBB01E074	DATA_LED_CFG [28].LED_CFG[20:16]	5
0xBB01E074	DATA_LED_CFG [28].RESERVED[15:13]	3
0xBB01E074	DATA_LED_CFG [28].CPU_FORCE_MOD[12:12]	1
0xBB01E074	DATA_LED_CFG [28].UTP_SPD1000[11:11]	1
0xBB01E074	DATA_LED_CFG [28].UTP_SPD500[10:10]	1
0xBB01E074	DATA_LED_CFG [28].UTP_SPD100[9:9]	1
0xBB01E074	DATA_LED_CFG [28].UTP_SPD10[8:8]	1
0xBB01E074	DATA_LED_CFG [28].UTP_DUP[7:7]	1
0xBB01E074	DATA_LED_CFG [28].UTP_SPD1000_ACT[6:6]	1
0xBB01E074	DATA_LED_CFG [28].UTP_SPD500_ACT[5:5]	1
0xBB01E074	DATA_LED_CFG [28].UTP_SPD100_ACT[4:4]	1
0xBB01E074	DATA_LED_CFG [28].UTP_SPD10_ACT[3:3]	1
0xBB01E074	DATA_LED_CFG [28].UTP_RX_ACT[2:2]	1

Address	Register	Len
0xBB01E074	DATA_LED_CFG [28].UTP_TX_ACT[1:1]	1
0xBB01E074	DATA_LED_CFG [28].UTP_COL[0:0]	1
0xBB01E078	DATA_LED_CFG [29].RESERVED[31:21]	11
0xBB01E078	DATA_LED_CFG [29].LED_CFG[20:16]	5
0xBB01E078	DATA_LED_CFG [29].RESERVED[15:13]	3
0xBB01E078	DATA_LED_CFG [29].CPU_FORCE_MOD[12:12]	1
0xBB01E078	DATA_LED_CFG [29].UTP_SPD1000[11:11]	1
0xBB01E078	DATA_LED_CFG [29].UTP_SPD500[10:10]	1
0xBB01E078	DATA_LED_CFG [29].UTP_SPD100[9:9]	1
0xBB01E078	DATA_LED_CFG [29].UTP_SPD10[8:8]	1
0xBB01E078	DATA_LED_CFG [29].UTP_DUP[7:7]	1
0xBB01E078	DATA_LED_CFG [29].UTP_SPD1000_ACT[6:6]	1
0xBB01E078	DATA_LED_CFG [29].UTP_SPD500_ACT[5:5]	1
0xBB01E078	DATA_LED_CFG [29].UTP_SPD100_ACT[4:4]	1
0xBB01E078	DATA_LED_CFG [29].UTP_SPD10_ACT[3:3]	1
0xBB01E078	DATA_LED_CFG [29].UTP_RX_ACT[2:2]	1
0xBB01E078	DATA_LED_CFG [29].UTP_TX_ACT[1:1]	1
0xBB01E078	DATA_LED_CFG [29].UTP_COL[0:0]	1
0xBB01E07C	DATA_LED_CFG [30].RESERVED[31:21]	11
0xBB01E07C	DATA_LED_CFG [30].LED_CFG[20:16]	5
0xBB01E07C	DATA_LED_CFG [30].RESERVED[15:13]	3
0xBB01E07C	DATA_LED_CFG [30].CPU_FORCE_MOD[12:12]	1
0xBB01E07C	DATA_LED_CFG [30].UTP_SPD1000[11:11]	1
0xBB01E07C	DATA_LED_CFG [30].UTP_SPD500[10:10]	1
0xBB01E07C	DATA_LED_CFG [30].UTP_SPD100[9:9]	1
0xBB01E07C	DATA_LED_CFG [30].UTP_SPD10[8:8]	1
0xBB01E07C	DATA_LED_CFG [30].UTP_DUP[7:7]	1
0xBB01E07C	DATA_LED_CFG [30].UTP_SPD1000_ACT[6:6]	1
0xBB01E07C	DATA_LED_CFG [30].UTP_SPD500_ACT[5:5]	1
0xBB01E07C	DATA_LED_CFG [30].UTP_SPD100_ACT[4:4]	1
0xBB01E07C	DATA_LED_CFG [30].UTP_SPD10_ACT[3:3]	1
0xBB01E07C	DATA_LED_CFG [30].UTP_RX_ACT[2:2]	1
0xBB01E07C	DATA_LED_CFG [30].UTP_TX_ACT[1:1]	1
0xBB01E07C	DATA_LED_CFG [30].UTP_COL[0:0]	1
0xBB01E080	DATA_LED_CFG [31].RESERVED[31:21]	11
0xBB01E080	DATA_LED_CFG [31].LED_CFG[20:16]	5
0xBB01E080	DATA_LED_CFG [31].RESERVED[15:13]	3
0xBB01E080	DATA_LED_CFG [31].CPU_FORCE_MOD[12:12]	1
0xBB01E080	DATA_LED_CFG [31].UTP_SPD1000[11:11]	1
0xBB01E080	DATA_LED_CFG [31].UTP_SPD500[10:10]	1
0xBB01E080	DATA_LED_CFG [31].UTP_SPD100[9:9]	1
0xBB01E080	DATA_LED_CFG [31].UTP_SPD10[8:8]	1
0xBB01E080	DATA_LED_CFG [31].UTP_DUP[7:7]	1
0xBB01E080	DATA_LED_CFG [31].UTP_SPD1000_ACT[6:6]	1
0xBB01E080	DATA_LED_CFG [31].UTP_SPD500_ACT[5:5]	1
0xBB01E080	DATA_LED_CFG [31].UTP_SPD100_ACT[4:4]	1

Address	Register	Len
0xBB01E080	DATA_LED_CFG [31].UTP_SPD10_ACT[3:3]	1
0xBB01E080	DATA_LED_CFG [31].UTP_RX_ACT[2:2]	1
0xBB01E080	DATA_LED_CFG [31].UTP_TX_ACT[1:1]	1
0xBB01E080	DATA_LED_CFG [31].UTP_COL[0:0]	1
0xBB01E084	LED_ACTIVE_LOW_CFG [0].LED_ACTIVE_LOW[0:0]	1
0xBB01E084	LED_ACTIVE_LOW_CFG [1].LED_ACTIVE_LOW[1:1]	1
0xBB01E084	LED_ACTIVE_LOW_CFG [2].LED_ACTIVE_LOW[2:2]	1
0xBB01E084	LED_ACTIVE_LOW_CFG [3].LED_ACTIVE_LOW[3:3]	1
0xBB01E084	LED_ACTIVE_LOW_CFG [4].LED_ACTIVE_LOW[4:4]	1
0xBB01E084	LED_ACTIVE_LOW_CFG [5].LED_ACTIVE_LOW[5:5]	1
0xBB01E084	LED_ACTIVE_LOW_CFG [6].LED_ACTIVE_LOW[6:6]	1
0xBB01E084	LED_ACTIVE_LOW_CFG [7].LED_ACTIVE_LOW[7:7]	1
0xBB01E084	LED_ACTIVE_LOW_CFG [8].LED_ACTIVE_LOW[8:8]	1
0xBB01E084	LED_ACTIVE_LOW_CFG [9].LED_ACTIVE_LOW[9:9]	1
0xBB01E084	LED_ACTIVE_LOW_CFG [10].LED_ACTIVE_LOW[10:10]	1
0xBB01E084	LED_ACTIVE_LOW_CFG [11].LED_ACTIVE_LOW[11:11]	1
0xBB01E084	LED_ACTIVE_LOW_CFG [12].LED_ACTIVE_LOW[12:12]	1
0xBB01E084	LED_ACTIVE_LOW_CFG [13].LED_ACTIVE_LOW[13:13]	1
0xBB01E084	LED_ACTIVE_LOW_CFG [14].LED_ACTIVE_LOW[14:14]	1
0xBB01E084	LED_ACTIVE_LOW_CFG [15].LED_ACTIVE_LOW[15:15]	1
0xBB01E084	LED_ACTIVE_LOW_CFG [16].LED_ACTIVE_LOW[16:16]	1
0xBB01E088	SERI_LED_ACTIVE_LOW_CFG.RESERVED[31:1]	31
0xBB01E088	SERI_LED_ACTIVE_LOW_CFG.SERI_LED_ACTIVE_LOW[0:0]	1
0xBB01E08C	LED_FORCE_VALUE_CFG [0].SEL_LED_FORCE_VALUE[1:0]	2
0xBB01E08C	LED_FORCE_VALUE_CFG [1].SEL_LED_FORCE_VALUE[3:2]	2
0xBB01E08C	LED_FORCE_VALUE_CFG [2].SEL_LED_FORCE_VALUE[5:4]	2
0xBB01E08C	LED_FORCE_VALUE_CFG [3].SEL_LED_FORCE_VALUE[7:6]	2
0xBB01E08C	LED_FORCE_VALUE_CFG [4].SEL_LED_FORCE_VALUE[9:8]	2
0xBB01E08C	LED_FORCE_VALUE_CFG [5].SEL_LED_FORCE_VALUE[11:10]	2
0xBB01E08C	LED_FORCE_VALUE_CFG [6].SEL_LED_FORCE_VALUE[13:12]	2
0xBB01E08C	LED_FORCE_VALUE_CFG [7].SEL_LED_FORCE_VALUE[15:14]	2
0xBB01E08C	LED_FORCE_VALUE_CFG [8].SEL_LED_FORCE_VALUE[17:16]	2
0xBB01E08C	LED_FORCE_VALUE_CFG [9].SEL_LED_FORCE_VALUE[19:18]	2
0xBB01E08C	LED_FORCE_VALUE_CFG [10].SEL_LED_FORCE_VALUE[21:20]	2
0xBB01E08C	LED_FORCE_VALUE_CFG [11].SEL_LED_FORCE_VALUE[23:22]	2
0xBB01E08C	LED_FORCE_VALUE_CFG [12].SEL_LED_FORCE_VALUE[25:24]	2
0xBB01E08C	LED_FORCE_VALUE_CFG [13].SEL_LED_FORCE_VALUE[27:26]	2
0xBB01E08C	LED_FORCE_VALUE_CFG [14].SEL_LED_FORCE_VALUE[29:28]	2
0xBB01E08C	LED_FORCE_VALUE_CFG [15].SEL_LED_FORCE_VALUE[31:30]	2
0xBB01E090	LED_FORCE_VALUE_CFG [16].SEL_LED_FORCE_VALUE[1:0]	2
0xBB01E090	LED_FORCE_VALUE_CFG [17].SEL_LED_FORCE_VALUE[3:2]	2
0xBB01E090	LED_FORCE_VALUE_CFG [18].SEL_LED_FORCE_VALUE[5:4]	2
0xBB01E090	LED_FORCE_VALUE_CFG [19].SEL_LED_FORCE_VALUE[7:6]	2
0xBB01E090	LED_FORCE_VALUE_CFG [20].SEL_LED_FORCE_VALUE[9:8]	2
0xBB01E090	LED_FORCE_VALUE_CFG [21].SEL_LED_FORCE_VALUE[11:10]	2
0xBB01E090	LED_FORCE_VALUE_CFG [22].SEL_LED_FORCE_VALUE[13:12]	2

Address	Register	Len
0xBB01E090	LED_FORCE_VALUE_CFG [23].SEL_LED_FORCE_VALUE[15:14]	2
0xBB01E090	LED_FORCE_VALUE_CFG [24].SEL_LED_FORCE_VALUE[17:16]	2
0xBB01E090	LED_FORCE_VALUE_CFG [25].SEL_LED_FORCE_VALUE[19:18]	2
0xBB01E090	LED_FORCE_VALUE_CFG [26].SEL_LED_FORCE_VALUE[21:20]	2
0xBB01E090	LED_FORCE_VALUE_CFG [27].SEL_LED_FORCE_VALUE[23:22]	2
0xBB01E090	LED_FORCE_VALUE_CFG [28].SEL_LED_FORCE_VALUE[25:24]	2
0xBB01E090	LED_FORCE_VALUE_CFG [29].SEL_LED_FORCE_VALUE[27:26]	2
0xBB01E090	LED_FORCE_VALUE_CFG [30].SEL_LED_FORCE_VALUE[29:28]	2
0xBB01E090	LED_FORCE_VALUE_CFG [31].SEL_LED_FORCE_VALUE[31:30]	2
0xBB01E094	LED_BLINK_RATE_CFG.RESERVED[31:15]	17
0xBB01E094	LED_BLINK_RATE_CFG.SEL_LED_FORCE_RATE[14:12]	3
0xBB01E094	LED_BLINK_RATE_CFG.SEL_MAC_LED_RATE[11:9]	3
0xBB01E094	LED_BLINK_RATE_CFG.SEL_USB_LED_RATE[8:6]	3
0xBB01E094	LED_BLINK_RATE_CFG.SEL_SATA_LED_RATE[5:3]	3
0xBB01E094	LED_BLINK_RATE_CFG.SEL_PCIE_LED_RATE[2:0]	3
0xBB01E098	LOW_RATE_BLINK_CFG.RESERVED[31:1]	31
0xBB01E098	LOW_RATE_BLINK_CFG.SEL_LOW_RATE_BLINK[0:0]	1
0xBB01E0A0	LED_EN.CFG_LPI_TAG3[31:28]	4
0xBB01E0A0	LED_EN.CFG_LPI_TAG2[27:24]	4
0xBB01E0A0	LED_EN.CFG_LPI_TAG1[23:20]	4
0xBB01E0A0	LED_EN.LED_SERI_DATA_EN[19:19]	1
0xBB01E0A0	LED_EN.LED_SERI_CLK_EN[18:18]	1
0xBB01E0A0	LED_EN.LED_PARA_P04_EN[17:1]	17
0xBB01E0A0	LED_EN.RESERVED[0:0]	1
0xBB01E0A4	SERI_LED_CLK_PER.RESERVED[31:2]	30
0xBB01E0A4	SERI_LED_CLK_PER.CFG_SERI_LED_CLK_PER[1:0]	2
0xBB01E0A8	SERI_LED_REFRESH_TIME.RESERVED[31:2]	30
0xBB01E0A8	SERI_LED_REFRESH_TIME.CFG_SERI_LED_REFRESH_TIME[1:0]	2
0xBB01E0C0	RGF_VER_LED.REGFILE_VER[31:0]	32
0xBB01E0C4	RSVD_LED [0].RSVD_MEM[31:0]	32
0xBB01E0C8	RSVD_LED [1].RSVD_MEM[31:0]	32
0xBB01E0CC	RSVD_LED [2].RSVD_MEM[31:0]	32
0xBB01E0D0	RSVD_LED [3].RSVD_MEM[31:0]	32
0xBB01E0D4	RSVD_LED [4].RSVD_MEM[31:0]	32
0xBB01E0D8	RSVD_LED [5].RSVD_MEM[31:0]	32
0xBB01E0DC	RSVD_LED [6].RSVD_MEM[31:0]	32
0xBB01E0E0	RSVD_LED [7].RSVD_MEM[31:0]	32
0xBB01E0E4	RSVD_LED [8].RSVD_MEM[31:0]	32
0xBB01E0E8	RSVD_LED [9].RSVD_MEM[31:0]	32
0xBB01E0EC	RSVD_LED [10].RSVD_MEM[31:0]	32
0xBB01E0F0	RSVD_LED [11].RSVD_MEM[31:0]	32
0xBB01E0F4	RSVD_LED [12].RSVD_MEM[31:0]	32
0xBB01E0F8	RSVD_LED [13].RSVD_MEM[31:0]	32
0xBB01E0FC	RSVD_LED [14].RSVD_MEM[31:0]	32
0xBB01E100	RSVD_LED [15].RSVD_MEM[31:0]	32
0xBB01E104	RLDP_BUZZER.RESERVED[31:1]	31

Address	Register	Len
0xBB01E104	RLDP_BUZZER.LED_LOOP_DET_BUZZER_EN[0:0]	1
0xBB01E108	PON_LED_CFG.RESERVED[31:2]	30
0xBB01E108	PON_LED_CFG.SWLED_PONN_ALARM[1:1]	1
0xBB01E108	PON_LED_CFG.SWLED_PON_WARN[0:0]	1
0xBB020000	P_TX_ERR_CNT [0].RESERVED[31:3]	29
0xBB020000	P_TX_ERR_CNT [0].TX_ERR_CNT[2:0]	3
0xBB020400	P_TX_ERR_CNT [1].RESERVED[31:3]	29
0xBB020400	P_TX_ERR_CNT [1].TX_ERR_CNT[2:0]	3
0xBB020800	P_TX_ERR_CNT [2].RESERVED[31:3]	29
0xBB020800	P_TX_ERR_CNT [2].TX_ERR_CNT[2:0]	3
0xBB020C00	P_TX_ERR_CNT [3].RESERVED[31:3]	29
0xBB020C00	P_TX_ERR_CNT [3].TX_ERR_CNT[2:0]	3
0xBB021000	P_TX_ERR_CNT [4].RESERVED[31:3]	29
0xBB021000	P_TX_ERR_CNT [4].TX_ERR_CNT[2:0]	3
0xBB021400	P_TX_ERR_CNT [5].RESERVED[31:3]	29
0xBB021400	P_TX_ERR_CNT [5].TX_ERR_CNT[2:0]	3
0xBB021800	P_TX_ERR_CNT [6].RESERVED[31:3]	29
0xBB021800	P_TX_ERR_CNT [6].TX_ERR_CNT[2:0]	3
0xBB020004	P_CGSTTIMER [0].RESERVED[31:1]	31
0xBB020004	P_CGSTTIMER [0].RX_DMA_ERR_FLAG[0:0]	1
0xBB020404	P_CGSTTIMER [1].RESERVED[31:1]	31
0xBB020404	P_CGSTTIMER [1].RX_DMA_ERR_FLAG[0:0]	1
0xBB020804	P_CGSTTIMER [2].RESERVED[31:1]	31
0xBB020804	P_CGSTTIMER [2].RX_DMA_ERR_FLAG[0:0]	1
0xBB020C04	P_CGSTTIMER [3].RESERVED[31:1]	31
0xBB020C04	P_CGSTTIMER [3].RX_DMA_ERR_FLAG[0:0]	1
0xBB021004	P_CGSTTIMER [4].RESERVED[31:1]	31
0xBB021004	P_CGSTTIMER [4].RX_DMA_ERR_FLAG[0:0]	1
0xBB021404	P_CGSTTIMER [5].RESERVED[31:1]	31
0xBB021404	P_CGSTTIMER [5].RX_DMA_ERR_FLAG[0:0]	1
0xBB021804	P_CGSTTIMER [6].RESERVED[31:1]	31
0xBB021804	P_CGSTTIMER [6].RX_DMA_ERR_FLAG[0:0]	1
0xBB020008	P_MISC [0].RESERVED[31:6]	26
0xBB020008	P_MISC [0].LATE_COL[5:5]	1
0xBB020008	P_MISC [0].SMALL_TAG_IPG[4:4]	1
0xBB020008	P_MISC [0].TX_ITFSP_MODE[3:3]	1
0xBB020008	P_MISC [0].RX_SPC[2:2]	1
0xBB020008	P_MISC [0].CRC_SKIP[1:1]	1
0xBB020008	P_MISC [0].MAC_LOOPBACK[0:0]	1
0xBB020408	P_MISC [1].RESERVED[31:6]	26
0xBB020408	P_MISC [1].LATE_COL[5:5]	1
0xBB020408	P_MISC [1].SMALL_TAG_IPG[4:4]	1
0xBB020408	P_MISC [1].TX_ITFSP_MODE[3:3]	1
0xBB020408	P_MISC [1].RX_SPC[2:2]	1
0xBB020408	P_MISC [1].CRC_SKIP[1:1]	1
0xBB020408	P_MISC [1].MAC_LOOPBACK[0:0]	1

Address	Register	Len
0xBB020808	P_MISC [2].RESERVED[31:6]	26
0xBB020808	P_MISC [2].LATE_COL[5:5]	1
0xBB020808	P_MISC [2].SMALL_TAG_IPG[4:4]	1
0xBB020808	P_MISC [2].TX_ITFSP_MODE[3:3]	1
0xBB020808	P_MISC [2].RX_SPC[2:2]	1
0xBB020808	P_MISC [2].CRC_SKIP[1:1]	1
0xBB020808	P_MISC [2].MAC_LOOPBACK[0:0]	1
0xBB020C08	P_MISC [3].RESERVED[31:6]	26
0xBB020C08	P_MISC [3].LATE_COL[5:5]	1
0xBB020C08	P_MISC [3].SMALL_TAG_IPG[4:4]	1
0xBB020C08	P_MISC [3].TX_ITFSP_MODE[3:3]	1
0xBB020C08	P_MISC [3].RX_SPC[2:2]	1
0xBB020C08	P_MISC [3].CRC_SKIP[1:1]	1
0xBB020C08	P_MISC [3].MAC_LOOPBACK[0:0]	1
0xBB021008	P_MISC [4].RESERVED[31:6]	26
0xBB021008	P_MISC [4].LATE_COL[5:5]	1
0xBB021008	P_MISC [4].SMALL_TAG_IPG[4:4]	1
0xBB021008	P_MISC [4].TX_ITFSP_MODE[3:3]	1
0xBB021008	P_MISC [4].RX_SPC[2:2]	1
0xBB021008	P_MISC [4].CRC_SKIP[1:1]	1
0xBB021008	P_MISC [4].MAC_LOOPBACK[0:0]	1
0xBB021408	P_MISC [5].RESERVED[31:6]	26
0xBB021408	P_MISC [5].LATE_COL[5:5]	1
0xBB021408	P_MISC [5].SMALL_TAG_IPG[4:4]	1
0xBB021408	P_MISC [5].TX_ITFSP_MODE[3:3]	1
0xBB021408	P_MISC [5].RX_SPC[2:2]	1
0xBB021408	P_MISC [5].CRC_SKIP[1:1]	1
0xBB021408	P_MISC [5].MAC_LOOPBACK[0:0]	1
0xBB021808	P_MISC [6].RESERVED[31:6]	26
0xBB021808	P_MISC [6].LATE_COL[5:5]	1
0xBB021808	P_MISC [6].SMALL_TAG_IPG[4:4]	1
0xBB021808	P_MISC [6].TX_ITFSP_MODE[3:3]	1
0xBB021808	P_MISC [6].RX_SPC[2:2]	1
0xBB021808	P_MISC [6].CRC_SKIP[1:1]	1
0xBB021808	P_MISC [6].MAC_LOOPBACK[0:0]	1
0xBB02000C	P_CFG_FRC_RATE [0].P_FORCE_RATE[31:0]	32
0xBB02040C	P_CFG_FRC_RATE [1].P_FORCE_RATE[31:0]	32
0xBB02080C	P_CFG_FRC_RATE [2].P_FORCE_RATE[31:0]	32
0xBB020C0C	P_CFG_FRC_RATE [3].P_FORCE_RATE[31:0]	32
0xBB02100C	P_CFG_FRC_RATE [4].P_FORCE_RATE[31:0]	32
0xBB02140C	P_CFG_FRC_RATE [5].P_FORCE_RATE[31:0]	32
0xBB02180C	P_CFG_FRC_RATE [6].P_FORCE_RATE[31:0]	32
0xBB020010	P_CUR_RATE [0].P_CURENT_RATE[31:0]	32
0xBB020410	P_CUR_RATE [1].P_CURENT_RATE[31:0]	32
0xBB020810	P_CUR_RATE [2].P_CURENT_RATE[31:0]	32
0xBB020C10	P_CUR_RATE [3].P_CURENT_RATE[31:0]	32

Address	Register	Len
0xBB021010	P_CUR_RATE [4].P_CURENT_RATE[31:0]	32
0xBB021410	P_CUR_RATE [5].P_CURENT_RATE[31:0]	32
0xBB021810	P_CUR_RATE [6].P_CURENT_RATE[31:0]	32
0xBB020014	EEE_EEEP_PORT_CFG [0].RESERVED[31:4]	28
0xBB020014	EEE_EEEP_PORT_CFG [0].EEE_EEEP_TX_STS[3:3]	1
0xBB020014	EEE_EEEP_PORT_CFG [0].EEE_EEEP_RX_STS[2:2]	1
0xBB020014	EEE_EEEP_PORT_CFG [0].RESERVED[1:0]	2
0xBB020414	EEE_EEEP_PORT_CFG [1].RESERVED[31:4]	28
0xBB020414	EEE_EEEP_PORT_CFG [1].EEE_EEEP_TX_STS[3:3]	1
0xBB020414	EEE_EEEP_PORT_CFG [1].EEE_EEEP_RX_STS[2:2]	1
0xBB020414	EEE_EEEP_PORT_CFG [1].RESERVED[1:0]	2
0xBB020814	EEE_EEEP_PORT_CFG [2].RESERVED[31:4]	28
0xBB020814	EEE_EEEP_PORT_CFG [2].EEE_EEEP_TX_STS[3:3]	1
0xBB020814	EEE_EEEP_PORT_CFG [2].EEE_EEEP_RX_STS[2:2]	1
0xBB020814	EEE_EEEP_PORT_CFG [2].RESERVED[1:0]	2
0xBB020C14	EEE_EEEP_PORT_CFG [3].RESERVED[31:4]	28
0xBB020C14	EEE_EEEP_PORT_CFG [3].EEE_EEEP_TX_STS[3:3]	1
0xBB020C14	EEE_EEEP_PORT_CFG [3].EEE_EEEP_RX_STS[2:2]	1
0xBB020C14	EEE_EEEP_PORT_CFG [3].RESERVED[1:0]	2
0xBB021014	EEE_EEEP_PORT_CFG [4].RESERVED[31:4]	28
0xBB021014	EEE_EEEP_PORT_CFG [4].EEE_EEEP_TX_STS[3:3]	1
0xBB021014	EEE_EEEP_PORT_CFG [4].EEE_EEEP_RX_STS[2:2]	1
0xBB021014	EEE_EEEP_PORT_CFG [4].RESERVED[1:0]	2
0xBB020018	P_EEECFG [0].RESERVED[31:11]	21
0xBB020018	P_EEECFG [0].EEE_FORCE[10:10]	1
0xBB020018	P_EEECFG [0].EEE_100M[9:9]	1
0xBB020018	P_EEECFG [0].EEE_GIGA[8:8]	1
0xBB020018	P_EEECFG [0].EEE_TX[7:7]	1
0xBB020018	P_EEECFG [0].EEE_RX[6:6]	1
0xBB020018	P_EEECFG [0].RESERVED[5:5]	1
0xBB020018	P_EEECFG [0].EEE_DSP_RX[4:4]	1
0xBB020018	P_EEECFG [0].EEE_LPI[3:3]	1
0xBB020018	P_EEECFG [0].EEE_PAUSE_INDICATOR[2:2]	1
0xBB020018	P_EEECFG [0].EEE_WAKE_REQ[1:1]	1
0xBB020018	P_EEECFG [0].EEE_SLEEP_REQ[0:0]	1
0xBB020418	P_EEECFG [1].RESERVED[31:11]	21
0xBB020418	P_EEECFG [1].EEE_FORCE[10:10]	1
0xBB020418	P_EEECFG [1].EEE_100M[9:9]	1
0xBB020418	P_EEECFG [1].EEE_GIGA[8:8]	1
0xBB020418	P_EEECFG [1].EEE_TX[7:7]	1
0xBB020418	P_EEECFG [1].EEE_RX[6:6]	1
0xBB020418	P_EEECFG [1].RESERVED[5:5]	1
0xBB020418	P_EEECFG [1].EEE_DSP_RX[4:4]	1
0xBB020418	P_EEECFG [1].EEE_LPI[3:3]	1
0xBB020418	P_EEECFG [1].EEE_PAUSE_INDICATOR[2:2]	1
0xBB020418	P_EEECFG [1].EEE_WAKE_REQ[1:1]	1

Address	Register	Len
0xBB020418	P_EEECFG [1].EEE_SLEEP_REQ[0:0]	1
0xBB020818	P_EEECFG [2].RESERVED[31:11]	21
0xBB020818	P_EEECFG [2].EEE_FORCE[10:10]	1
0xBB020818	P_EEECFG [2].EEE_100M[9:9]	1
0xBB020818	P_EEECFG [2].EEE_GIGA[8:8]	1
0xBB020818	P_EEECFG [2].EEE_TX[7:7]	1
0xBB020818	P_EEECFG [2].EEE_RX[6:6]	1
0xBB020818	P_EEECFG [2].RESERVED[5:5]	1
0xBB020818	P_EEECFG [2].EEE_DSP_RX[4:4]	1
0xBB020818	P_EEECFG [2].EEE_LPI[3:3]	1
0xBB020818	P_EEECFG [2].EEE_PAUSE_INDICATOR[2:2]	1
0xBB020818	P_EEECFG [2].EEE_WAKE_REQ[1:1]	1
0xBB020818	P_EEECFG [2].EEE_SLEEP_REQ[0:0]	1
0xBB020C18	P_EEECFG [3].RESERVED[31:11]	21
0xBB020C18	P_EEECFG [3].EEE_FORCE[10:10]	1
0xBB020C18	P_EEECFG [3].EEE_100M[9:9]	1
0xBB020C18	P_EEECFG [3].EEE_GIGA[8:8]	1
0xBB020C18	P_EEECFG [3].EEE_TX[7:7]	1
0xBB020C18	P_EEECFG [3].EEE_RX[6:6]	1
0xBB020C18	P_EEECFG [3].RESERVED[5:5]	1
0xBB020C18	P_EEECFG [3].EEE_DSP_RX[4:4]	1
0xBB020C18	P_EEECFG [3].EEE_LPI[3:3]	1
0xBB020C18	P_EEECFG [3].EEE_PAUSE_INDICATOR[2:2]	1
0xBB020C18	P_EEECFG [3].EEE_WAKE_REQ[1:1]	1
0xBB020C18	P_EEECFG [3].EEE_SLEEP_REQ[0:0]	1
0xBB021018	P_EEECFG [4].RESERVED[31:11]	21
0xBB021018	P_EEECFG [4].EEE_FORCE[10:10]	1
0xBB021018	P_EEECFG [4].EEE_100M[9:9]	1
0xBB021018	P_EEECFG [4].EEE_GIGA[8:8]	1
0xBB021018	P_EEECFG [4].EEE_TX[7:7]	1
0xBB021018	P_EEECFG [4].EEE_RX[6:6]	1
0xBB021018	P_EEECFG [4].RESERVED[5:5]	1
0xBB021018	P_EEECFG [4].EEE_DSP_RX[4:4]	1
0xBB021018	P_EEECFG [4].EEE_LPI[3:3]	1
0xBB021018	P_EEECFG [4].EEE_PAUSE_INDICATOR[2:2]	1
0xBB021018	P_EEECFG [4].EEE_WAKE_REQ[1:1]	1
0xBB021018	P_EEECFG [4].EEE_SLEEP_REQ[0:0]	1
0xBB02001C	P_EEETXMTR [0].P_EEETXMTR[31:0]	32
0xBB02041C	P_EEETXMTR [1].P_EEETXMTR[31:0]	32
0xBB02081C	P_EEETXMTR [2].P_EEETXMTR[31:0]	32
0xBB020C1C	P_EEETXMTR [3].P_EEETXMTR[31:0]	32
0xBB02101C	P_EEETXMTR [4].P_EEETXMTR[31:0]	32
0xBB020020	P_EEERXMTR [0].P_EEERXMTR[31:0]	32
0xBB020420	P_EEERXMTR [1].P_EEERXMTR[31:0]	32
0xBB020820	P_EEERXMTR [2].P_EEERXMTR[31:0]	32
0xBB020C20	P_EEERXMTR [3].P_EEERXMTR[31:0]	32



Address	Register	Len
0xBB021020	P_EEERXMTR [4].P_EEERXMTR[31:0]	32
0xBB020024	P_EEEP_CFG [0].RESERVED[31:2]	30
0xBB020024	P_EEEP_CFG [0].EEEP_TX_EN[1:1]	1
0xBB020024	P_EEEP_CFG [0].EEEP_RX_EN[0:0]	1
0xBB020424	P_EEEP_CFG [1].RESERVED[31:2]	30
0xBB020424	P_EEEP_CFG [1].EEEP_TX_EN[1:1]	1
0xBB020424	P_EEEP_CFG [1].EEEP_RX_EN[0:0]	1
0xBB020824	P_EEEP_CFG [2].RESERVED[31:2]	30
0xBB020824	P_EEEP_CFG [2].EEEP_TX_EN[1:1]	1
0xBB020824	P_EEEP_CFG [2].EEEP_RX_EN[0:0]	1
0xBB020C24	P_EEEP_CFG [3].RESERVED[31:2]	30
0xBB020C24	P_EEEP_CFG [3].EEEP_TX_EN[1:1]	1
0xBB020C24	P_EEEP_CFG [3].EEEP_RX_EN[0:0]	1
0xBB021024	P_EEEP_CFG [4].RESERVED[31:2]	30
0xBB021024	P_EEEP_CFG [4].EEEP_TX_EN[1:1]	1
0xBB021024	P_EEEP_CFG [4].EEEP_RX_EN[0:0]	1
0xBB020028	P_EEEPTXMTR [0].P_EEEPTXMTR[31:0]	32
0xBB020428	P_EEEPTXMTR [1].P_EEEPTXMTR[31:0]	32
0xBB020828	P_EEEPTXMTR [2].P_EEEPTXMTR[31:0]	32
0xBB020C28	P_EEEPTXMTR [3].P_EEEPTXMTR[31:0]	32
0xBB021028	P_EEEPTXMTR [4].P_EEEPTXMTR[31:0]	32
0xBB02002C	P_EEEPRXMTR [0].P_EEEPRXMTR[31:0]	32
0xBB02042C	P_EEEPRXMTR [1].P_EEEPRXMTR[31:0]	32
0xBB02082C	P_EEEPRXMTR [2].P_EEEPRXMTR[31:0]	32
0xBB020C2C	P_EEEPRXMTR [3].P_EEEPRXMTR[31:0]	32
0xBB02102C	P_EEEPRXMTR [4].P_EEEPRXMTR[31:0]	32
0xBB020030	VLAN_EGRESS_TAG [0].RESERVED[31:2]	30
0xBB020030	VLAN_EGRESS_TAG [0].EGRESS_MODE[1:0]	2
0xBB020430	VLAN_EGRESS_TAG [1].RESERVED[31:2]	30
0xBB020430	VLAN_EGRESS_TAG [1].EGRESS_MODE[1:0]	2
0xBB020830	VLAN_EGRESS_TAG [2].RESERVED[31:2]	30
0xBB020830	VLAN_EGRESS_TAG [2].EGRESS_MODE[1:0]	2
0xBB020C30	VLAN_EGRESS_TAG [3].RESERVED[31:2]	30
0xBB020C30	VLAN_EGRESS_TAG [3].EGRESS_MODE[1:0]	2
0xBB021030	VLAN_EGRESS_TAG [4].RESERVED[31:2]	30
0xBB021030	VLAN_EGRESS_TAG [4].EGRESS_MODE[1:0]	2
0xBB021430	VLAN_EGRESS_TAG [5].RESERVED[31:2]	30
0xBB021430	VLAN_EGRESS_TAG [5].EGRESS_MODE[1:0]	2
0xBB021830	VLAN_EGRESS_TAG [6].RESERVED[31:2]	30
0xBB021830	VLAN_EGRESS_TAG [6].EGRESS_MODE[1:0]	2
0xBB020034	IGR_BWCTRL_P_CTRL [0].RESERVED[31:19]	13
0xBB020034	IGR_BWCTRL_P_CTRL [0].RATE[18:2]	17
0xBB020034	IGR_BWCTRL_P_CTRL [0].MODE[1:1]	1
0xBB020034	IGR_BWCTRL_P_CTRL [0].IFG[0:0]	1
0xBB020434	IGR_BWCTRL_P_CTRL [1].RESERVED[31:19]	13
0xBB020434	IGR_BWCTRL_P_CTRL [1].RATE[18:2]	17

Address	Register	Len
0xBB020434	IGR_BWCTRL_P_CTRL [1].MODE[1:1]	1
0xBB020434	IGR_BWCTRL_P_CTRL [1].IFG[0:0]	1
0xBB020834	IGR_BWCTRL_P_CTRL [2].RESERVED[31:19]	13
0xBB020834	IGR_BWCTRL_P_CTRL [2].RATE[18:2]	17
0xBB020834	IGR_BWCTRL_P_CTRL [2].MODE[1:1]	1
0xBB020834	IGR_BWCTRL_P_CTRL [2].IFG[0:0]	1
0xBB020C34	IGR_BWCTRL_P_CTRL [3].RESERVED[31:19]	13
0xBB020C34	IGR_BWCTRL_P_CTRL [3].RATE[18:2]	17
0xBB020C34	IGR_BWCTRL_P_CTRL [3].MODE[1:1]	1
0xBB020C34	IGR_BWCTRL_P_CTRL [3].IFG[0:0]	1
0xBB021034	IGR_BWCTRL_P_CTRL [4].RESERVED[31:19]	13
0xBB021034	IGR_BWCTRL_P_CTRL [4].RATE[18:2]	17
0xBB021034	IGR_BWCTRL_P_CTRL [4].MODE[1:1]	1
0xBB021034	IGR_BWCTRL_P_CTRL [4].IFG[0:0]	1
0xBB021434	IGR_BWCTRL_P_CTRL [5].RESERVED[31:19]	13
0xBB021434	IGR_BWCTRL_P_CTRL [5].RATE[18:2]	17
0xBB021434	IGR_BWCTRL_P_CTRL [5].MODE[1:1]	1
0xBB021434	IGR_BWCTRL_P_CTRL [5].IFG[0:0]	1
0xBB021834	IGR_BWCTRL_P_CTRL [6].RESERVED[31:19]	13
0xBB021834	IGR_BWCTRL_P_CTRL [6].RATE[18:2]	17
0xBB021834	IGR_BWCTRL_P_CTRL [6].MODE[1:1]	1
0xBB021834	IGR_BWCTRL_P_CTRL [6].IFG[0:0]	1
0xBB020038	FC_P_DBG_PKT_PAGE_CNT [0].RESERVED[31:13]	19
0xBB020038	FC_P_DBG_PKT_PAGE_CNT [0].PKT_PAGE_CNT[12:0]	13
0xBB020438	FC_P_DBG_PKT_PAGE_CNT [1].RESERVED[31:13]	19
0xBB020438	FC_P_DBG_PKT_PAGE_CNT [1].PKT_PAGE_CNT[12:0]	13
0xBB020838	FC_P_DBG_PKT_PAGE_CNT [2].RESERVED[31:13]	19
0xBB020838	FC_P_DBG_PKT_PAGE_CNT [2].PKT_PAGE_CNT[12:0]	13
0xBB020C38	FC_P_DBG_PKT_PAGE_CNT [3].RESERVED[31:13]	19
0xBB020C38	FC_P_DBG_PKT_PAGE_CNT [3].PKT_PAGE_CNT[12:0]	13
0xBB021038	FC_P_DBG_PKT_PAGE_CNT [4].RESERVED[31:13]	19
0xBB021038	FC_P_DBG_PKT_PAGE_CNT [4].PKT_PAGE_CNT[12:0]	13
0xBB021438	FC_P_DBG_PKT_PAGE_CNT [5].RESERVED[31:13]	19
0xBB021438	FC_P_DBG_PKT_PAGE_CNT [5].PKT_PAGE_CNT[12:0]	13
0xBB021838	FC_P_DBG_PKT_PAGE_CNT [6].RESERVED[31:13]	19
0xBB021838	FC_P_DBG_PKT_PAGE_CNT [6].PKT_PAGE_CNT[12:0]	13
0xBB02003C	SC_P_CTRL_0 [0].RESERVED[31:24]	8
0xBB02003C	SC_P_CTRL_0 [0].CGST_TMR_H[23:20]	4
0xBB02003C	SC_P_CTRL_0 [0].CGST_SUST_TMR_LMT_H[19:16]	4
0xBB02003C	SC_P_CTRL_0 [0].RESERVED[15:8]	8
0xBB02003C	SC_P_CTRL_0 [0].CGST_TMR[7:4]	4
0xBB02003C	SC_P_CTRL_0 [0].CGST_SUST_TMR_LMT[3:0]	4
0xBB02043C	SC_P_CTRL_0 [1].RESERVED[31:24]	8
0xBB02043C	SC_P_CTRL_0 [1].CGST_TMR_H[23:20]	4
0xBB02043C	SC_P_CTRL_0 [1].CGST_SUST_TMR_LMT_H[19:16]	4
0xBB02043C	SC_P_CTRL_0 [1].RESERVED[15:8]	8

Address	Register	Len
0xBB02043C	SC_P_CTRL_0 [1].CGST_TMR[7:4]	4
0xBB02043C	SC_P_CTRL_0 [1].CGST_SUST_TMR_LMT[3:0]	4
0xBB02083C	SC_P_CTRL_0 [2].RESERVED[31:24]	8
0xBB02083C	SC_P_CTRL_0 [2].CGST_TMR_H[23:20]	4
0xBB02083C	SC_P_CTRL_0 [2].CGST_SUST_TMR_LMT_H[19:16]	4
0xBB02083C	SC_P_CTRL_0 [2].RESERVED[15:8]	8
0xBB02083C	SC_P_CTRL_0 [2].CGST_TMR[7:4]	4
0xBB02083C	SC_P_CTRL_0 [2].CGST_SUST_TMR_LMT[3:0]	4
0xBB020C3C	SC_P_CTRL_0 [3].RESERVED[31:24]	8
0xBB020C3C	SC_P_CTRL_0 [3].CGST_TMR_H[23:20]	4
0xBB020C3C	SC_P_CTRL_0 [3].CGST_SUST_TMR_LMT_H[19:16]	4
0xBB020C3C	SC_P_CTRL_0 [3].RESERVED[15:8]	8
0xBB020C3C	SC_P_CTRL_0 [3].CGST_TMR[7:4]	4
0xBB020C3C	SC_P_CTRL_0 [3].CGST_SUST_TMR_LMT[3:0]	4
0xBB02103C	SC_P_CTRL_0 [4].RESERVED[31:24]	8
0xBB02103C	SC_P_CTRL_0 [4].CGST_TMR_H[23:20]	4
0xBB02103C	SC_P_CTRL_0 [4].CGST_SUST_TMR_LMT_H[19:16]	4
0xBB02103C	SC_P_CTRL_0 [4].RESERVED[15:8]	8
0xBB02103C	SC_P_CTRL_0 [4].CGST_TMR[7:4]	4
0xBB02103C	SC_P_CTRL_0 [4].CGST_SUST_TMR_LMT[3:0]	4
0xBB02143C	SC_P_CTRL_0 [5].RESERVED[31:24]	8
0xBB02143C	SC_P_CTRL_0 [5].CGST_TMR_H[23:20]	4
0xBB02143C	SC_P_CTRL_0 [5].CGST_SUST_TMR_LMT_H[19:16]	4
0xBB02143C	SC_P_CTRL_0 [5].RESERVED[15:8]	8
0xBB02143C	SC_P_CTRL_0 [5].CGST_TMR[7:4]	4
0xBB02143C	SC_P_CTRL_0 [5].CGST_SUST_TMR_LMT[3:0]	4
0xBB02183C	SC_P_CTRL_0 [6].RESERVED[31:24]	8
0xBB02183C	SC_P_CTRL_0 [6].CGST_TMR_H[23:20]	4
0xBB02183C	SC_P_CTRL_0 [6].CGST_SUST_TMR_LMT_H[19:16]	4
0xBB02183C	SC_P_CTRL_0 [6].RESERVED[15:8]	8
0xBB02183C	SC_P_CTRL_0 [6].CGST_TMR[7:4]	4
0xBB02183C	SC_P_CTRL_0 [6].CGST_SUST_TMR_LMT[3:0]	4
0xBB020040	RMK_DOT1Q_RMK_EN_CTRL [0].RESERVED[31:1]	31
0xBB020040	RMK_DOT1Q_RMK_EN_CTRL [0].EN[0:0]	1
0xBB020440	RMK_DOT1Q_RMK_EN_CTRL [1].RESERVED[31:1]	31
0xBB020440	RMK_DOT1Q_RMK_EN_CTRL [1].EN[0:0]	1
0xBB020840	RMK_DOT1Q_RMK_EN_CTRL [2].RESERVED[31:1]	31
0xBB020840	RMK_DOT1Q_RMK_EN_CTRL [2].EN[0:0]	1
0xBB020C40	RMK_DOT1Q_RMK_EN_CTRL [3].RESERVED[31:1]	31
0xBB020C40	RMK_DOT1Q_RMK_EN_CTRL [3].EN[0:0]	1
0xBB021040	RMK_DOT1Q_RMK_EN_CTRL [4].RESERVED[31:1]	31
0xBB021040	RMK_DOT1Q_RMK_EN_CTRL [4].EN[0:0]	1
0xBB021440	RMK_DOT1Q_RMK_EN_CTRL [5].RESERVED[31:1]	31
0xBB021440	RMK_DOT1Q_RMK_EN_CTRL [5].EN[0:0]	1
0xBB021840	RMK_DOT1Q_RMK_EN_CTRL [6].RESERVED[31:1]	31
0xBB021840	RMK_DOT1Q_RMK_EN_CTRL [6].EN[0:0]	1

Address	Register	Len
0xBB020044	PORT_VM_EN [0].RESERVED[31:1]	31
0xBB020044	PORT_VM_EN [0].PORT_VM_EN[0:0]	1
0xBB020444	PORT_VM_EN [1].RESERVED[31:1]	31
0xBB020444	PORT_VM_EN [1].PORT_VM_EN[0:0]	1
0xBB020844	PORT_VM_EN [2].RESERVED[31:1]	31
0xBB020844	PORT_VM_EN [2].PORT_VM_EN[0:0]	1
0xBB020C44	PORT_VM_EN [3].RESERVED[31:1]	31
0xBB020C44	PORT_VM_EN [3].PORT_VM_EN[0:0]	1
0xBB021044	PORT_VM_EN [4].RESERVED[31:1]	31
0xBB021044	PORT_VM_EN [4].PORT_VM_EN[0:0]	1
0xBB021444	PORT_VM_EN [5].RESERVED[31:1]	31
0xBB021444	PORT_VM_EN [5].PORT_VM_EN[0:0]	1
0xBB021844	PORT_VM_EN [6].RESERVED[31:1]	31
0xBB021844	PORT_VM_EN [6].PORT_VM_EN[0:0]	1
0xBB020048	PORT_VM_RX [0].RESERVED[31:9]	23
0xBB020048	PORT_VM_RX [0].PORT_VM_RXDV[8:8]	1
0xBB020048	PORT_VM_RX [0].PORT_VM_RXD[7:0]	8
0xBB020448	PORT_VM_RX [1].RESERVED[31:9]	23
0xBB020448	PORT_VM_RX [1].PORT_VM_RXDV[8:8]	1
0xBB020448	PORT_VM_RX [1].PORT_VM_RXD[7:0]	8
0xBB020848	PORT_VM_RX [2].RESERVED[31:9]	23
0xBB020848	PORT_VM_RX [2].PORT_VM_RXDV[8:8]	1
0xBB020848	PORT_VM_RX [2].PORT_VM_RXD[7:0]	8
0xBB020C48	PORT_VM_RX [3].RESERVED[31:9]	23
0xBB020C48	PORT_VM_RX [3].PORT_VM_RXDV[8:8]	1
0xBB020C48	PORT_VM_RX [3].PORT_VM_RXD[7:0]	8
0xBB021048	PORT_VM_RX [4].RESERVED[31:9]	23
0xBB021048	PORT_VM_RX [4].PORT_VM_RXDV[8:8]	1
0xBB021048	PORT_VM_RX [4].PORT_VM_RXD[7:0]	8
0xBB021448	PORT_VM_RX [5].RESERVED[31:9]	23
0xBB021448	PORT_VM_RX [5].PORT_VM_RXDV[8:8]	1
0xBB021448	PORT_VM_RX [5].PORT_VM_RXD[7:0]	8
0xBB021848	PORT_VM_RX [6].RESERVED[31:9]	23
0xBB021848	PORT_VM_RX [6].PORT_VM_RXDV[8:8]	1
0xBB021848	PORT_VM_RX [6].PORT_VM_RXD[7:0]	8
0xBB02004C	PORT_VM_TX [0].RESERVED[31:9]	23
0xBB02004C	PORT_VM_TX [0].PORT_VM_TXEN[8:8]	1
0xBB02004C	PORT_VM_TX [0].PORT_VM_TXD[7:0]	8
0xBB02044C	PORT_VM_TX [1].RESERVED[31:9]	23
0xBB02044C	PORT_VM_TX [1].PORT_VM_TXEN[8:8]	1
0xBB02044C	PORT_VM_TX [1].PORT_VM_TXD[7:0]	8
0xBB02084C	PORT_VM_TX [2].RESERVED[31:9]	23
0xBB02084C	PORT_VM_TX [2].PORT_VM_TXEN[8:8]	1
0xBB02084C	PORT_VM_TX [2].PORT_VM_TXD[7:0]	8
0xBB020C4C	PORT_VM_TX [3].RESERVED[31:9]	23
0xBB020C4C	PORT_VM_TX [3].PORT_VM_TXEN[8:8]	1

Address	Register	Len
0xBB020C4C	PORT_VM_TX [3].PORT_VM_TXD[7:0]	8
0xBB02104C	PORT_VM_TX [4].RESERVED[31:9]	23
0xBB02104C	PORT_VM_TX [4].PORT_VM_TXEN[8:8]	1
0xBB02104C	PORT_VM_TX [4].PORT_VM_TXD[7:0]	8
0xBB02144C	PORT_VM_TX [5].RESERVED[31:9]	23
0xBB02144C	PORT_VM_TX [5].PORT_VM_TXEN[8:8]	1
0xBB02144C	PORT_VM_TX [5].PORT_VM_TXD[7:0]	8
0xBB02184C	PORT_VM_TX [6].RESERVED[31:9]	23
0xBB02184C	PORT_VM_TX [6].PORT_VM_TXEN[8:8]	1
0xBB02184C	PORT_VM_TX [6].PORT_VM_TXD[7:0]	8
0xBB020050	SPG_PORT_TX_GRP_CTRL [0].RESERVED[31:1]	31
0xBB020050	SPG_PORT_TX_GRP_CTRL [0].GRP_TX_PORT[0:0]	1
0xBB020450	SPG_PORT_TX_GRP_CTRL [1].RESERVED[31:1]	31
0xBB020450	SPG_PORT_TX_GRP_CTRL [1].GRP_TX_PORT[0:0]	1
0xBB020850	SPG_PORT_TX_GRP_CTRL [2].RESERVED[31:1]	31
0xBB020850	SPG_PORT_TX_GRP_CTRL [2].GRP_TX_PORT[0:0]	1
0xBB020C50	SPG_PORT_TX_GRP_CTRL [3].RESERVED[31:1]	31
0xBB020C50	SPG_PORT_TX_GRP_CTRL [3].GRP_TX_PORT[0:0]	1
0xBB021050	SPG_PORT_TX_GRP_CTRL [4].RESERVED[31:1]	31
0xBB021050	SPG_PORT_TX_GRP_CTRL [4].GRP_TX_PORT[0:0]	1
0xBB021450	SPG_PORT_TX_GRP_CTRL [5].RESERVED[31:1]	31
0xBB021450	SPG_PORT_TX_GRP_CTRL [5].GRP_TX_PORT[0:0]	1
0xBB021850	SPG_PORT_TX_GRP_CTRL [6].RESERVED[31:1]	31
0xBB021850	SPG_PORT_TX_GRP_CTRL [6].GRP_TX_PORT[0:0]	1
0xBB020054	SPG_PORT_STS [0].RESERVED[31:1]	31
0xBB020054	SPG_PORT_STS [0].TX_DONE_PORT[0:0]	1
0xBB020454	SPG_PORT_STS [1].RESERVED[31:1]	31
0xBB020454	SPG_PORT_STS [1].TX_DONE_PORT[0:0]	1
0xBB020854	SPG_PORT_STS [2].RESERVED[31:1]	31
0xBB020854	SPG_PORT_STS [2].TX_DONE_PORT[0:0]	1
0xBB020C54	SPG_PORT_STS [3].RESERVED[31:1]	31
0xBB020C54	SPG_PORT_STS [3].TX_DONE_PORT[0:0]	1
0xBB021054	SPG_PORT_STS [4].RESERVED[31:1]	31
0xBB021054	SPG_PORT_STS [4].TX_DONE_PORT[0:0]	1
0xBB021454	SPG_PORT_STS [5].RESERVED[31:1]	31
0xBB021454	SPG_PORT_STS [5].TX_DONE_PORT[0:0]	1
0xBB021854	SPG_PORT_STS [6].RESERVED[31:1]	31
0xBB021854	SPG_PORT_STS [6].TX_DONE_PORT[0:0]	1
0xBB020058	SPG_P_TX_GRP_CTRL [0].RESERVED[31:16]	16
0xBB020058	SPG_P_TX_GRP_CTRL [0].TX_FIRST[15:15]	1
0xBB020058	SPG_P_TX_GRP_CTRL [0].STS_GEN[14:14]	1
0xBB020058	SPG_P_TX_GRP_CTRL [0].STS_BUSY[13:13]	1
0xBB020058	SPG_P_TX_GRP_CTRL [0].CMD_SUSPEND[12:12]	1
0xBB020058	SPG_P_TX_GRP_CTRL [0].MODE_LEN_SEL[11:11]	1
0xBB020058	SPG_P_TX_GRP_CTRL [0].MODE_RANDOM_LEN[10:10]	1
0xBB020058	SPG_P_TX_GRP_CTRL [0].RESERVED[9:9]	1

Address	Register	Len
0xBB020058	SPG_P_TX_GRP_CTRL [0].MODE_BCINC[8:8]	1
0xBB020058	SPG_P_TX_GRP_CTRL [0].MODE_SAINC[7:7]	1
0xBB020058	SPG_P_TX_GRP_CTRL [0].MODE_DAINC[6:6]	1
0xBB020058	SPG_P_TX_GRP_CTRL [0].MODE_RANDOM[5:5]	1
0xBB020058	SPG_P_TX_GRP_CTRL [0].MODE_CRC[4:4]	1
0xBB020058	SPG_P_TX_GRP_CTRL [0].CMD_STOP[3:3]	1
0xBB020058	SPG_P_TX_GRP_CTRL [0].MODE_CONTINUE[2:2]	1
0xBB020058	SPG_P_TX_GRP_CTRL [0].MODE_PAUSE[1:1]	1
0xBB020058	SPG_P_TX_GRP_CTRL [0].CMD_START[0:0]	1
0xBB020458	SPG_P_TX_GRP_CTRL [1].RESERVED[31:16]	16
0xBB020458	SPG_P_TX_GRP_CTRL [1].TX_FIRST[15:15]	1
0xBB020458	SPG_P_TX_GRP_CTRL [1].STS_GEN[14:14]	1
0xBB020458	SPG_P_TX_GRP_CTRL [1].STS_BUSY[13:13]	1
0xBB020458	SPG_P_TX_GRP_CTRL [1].CMD_SUSPEND[12:12]	1
0xBB020458	SPG_P_TX_GRP_CTRL [1].MODE_LEN_SEL[11:11]	1
0xBB020458	SPG_P_TX_GRP_CTRL [1].MODE_RANDOM_LEN[10:10]	1
0xBB020458	SPG_P_TX_GRP_CTRL [1].RESERVED[9:9]	1
0xBB020458	SPG_P_TX_GRP_CTRL [1].MODE_BCINC[8:8]	1
0xBB020458	SPG_P_TX_GRP_CTRL [1].MODE_SAINC[7:7]	1
0xBB020458	SPG_P_TX_GRP_CTRL [1].MODE_DAINC[6:6]	1
0xBB020458	SPG_P_TX_GRP_CTRL [1].MODE_RANDOM[5:5]	1
0xBB020458	SPG_P_TX_GRP_CTRL [1].MODE_CRC[4:4]	1
0xBB020458	SPG_P_TX_GRP_CTRL [1].CMD_STOP[3:3]	1
0xBB020458	SPG_P_TX_GRP_CTRL [1].MODE_CONTINUE[2:2]	1
0xBB020458	SPG_P_TX_GRP_CTRL [1].MODE_PAUSE[1:1]	1
0xBB020458	SPG_P_TX_GRP_CTRL [1].CMD_START[0:0]	1
0xBB020858	SPG_P_TX_GRP_CTRL [2].RESERVED[31:16]	16
0xBB020858	SPG_P_TX_GRP_CTRL [2].TX_FIRST[15:15]	1
0xBB020858	SPG_P_TX_GRP_CTRL [2].STS_GEN[14:14]	1
0xBB020858	SPG_P_TX_GRP_CTRL [2].STS_BUSY[13:13]	1
0xBB020858	SPG_P_TX_GRP_CTRL [2].CMD_SUSPEND[12:12]	1
0xBB020858	SPG_P_TX_GRP_CTRL [2].MODE_LEN_SEL[11:11]	1
0xBB020858	SPG_P_TX_GRP_CTRL [2].MODE_RANDOM_LEN[10:10]	1
0xBB020858	SPG_P_TX_GRP_CTRL [2].RESERVED[9:9]	1
0xBB020858	SPG_P_TX_GRP_CTRL [2].MODE_BCINC[8:8]	1
0xBB020858	SPG_P_TX_GRP_CTRL [2].MODE_SAINC[7:7]	1
0xBB020858	SPG_P_TX_GRP_CTRL [2].MODE_DAINC[6:6]	1
0xBB020858	SPG_P_TX_GRP_CTRL [2].MODE_RANDOM[5:5]	1
0xBB020858	SPG_P_TX_GRP_CTRL [2].MODE_CRC[4:4]	1
0xBB020858	SPG_P_TX_GRP_CTRL [2].CMD_STOP[3:3]	1
0xBB020858	SPG_P_TX_GRP_CTRL [2].MODE_CONTINUE[2:2]	1
0xBB020858	SPG_P_TX_GRP_CTRL [2].MODE_PAUSE[1:1]	1
0xBB020858	SPG_P_TX_GRP_CTRL [2].CMD_START[0:0]	1
0xBB020C58	SPG_P_TX_GRP_CTRL [3].RESERVED[31:16]	16
0xBB020C58	SPG_P_TX_GRP_CTRL [3].TX_FIRST[15:15]	1
0xBB020C58	SPG_P_TX_GRP_CTRL [3].STS_GEN[14:14]	1

Address	Register	Len
0xBB020C58	SPG_P_TX_GRP_CTRL [3].STS_BUSY[13:13]	1
0xBB020C58	SPG_P_TX_GRP_CTRL [3].CMD_SUSPEND[12:12]	1
0xBB020C58	SPG_P_TX_GRP_CTRL [3].MODE_LEN_SEL[11:11]	1
0xBB020C58	SPG_P_TX_GRP_CTRL [3].MODE_RANDOM_LEN[10:10]	1
0xBB020C58	SPG_P_TX_GRP_CTRL [3].RESERVED[9:9]	1
0xBB020C58	SPG_P_TX_GRP_CTRL [3].MODE_BCINC[8:8]	1
0xBB020C58	SPG_P_TX_GRP_CTRL [3].MODE_SAINC[7:7]	1
0xBB020C58	SPG_P_TX_GRP_CTRL [3].MODE_DAINC[6:6]	1
0xBB020C58	SPG_P_TX_GRP_CTRL [3].MODE_RANDOM[5:5]	1
0xBB020C58	SPG_P_TX_GRP_CTRL [3].MODE_CRC[4:4]	1
0xBB020C58	SPG_P_TX_GRP_CTRL [3].CMD_STOP[3:3]	1
0xBB020C58	SPG_P_TX_GRP_CTRL [3].MODE_CONTINUE[2:2]	1
0xBB020C58	SPG_P_TX_GRP_CTRL [3].MODE_PAUSE[1:1]	1
0xBB020C58	SPG_P_TX_GRP_CTRL [3].CMD_START[0:0]	1
0xBB021058	SPG_P_TX_GRP_CTRL [4].RESERVED[31:16]	16
0xBB021058	SPG_P_TX_GRP_CTRL [4].TX_FIRST[15:15]	1
0xBB021058	SPG_P_TX_GRP_CTRL [4].STS_GEN[14:14]	1
0xBB021058	SPG_P_TX_GRP_CTRL [4].STS_BUSY[13:13]	1
0xBB021058	SPG_P_TX_GRP_CTRL [4].CMD_SUSPEND[12:12]	1
0xBB021058	SPG_P_TX_GRP_CTRL [4].MODE_LEN_SEL[11:11]	1
0xBB021058	SPG_P_TX_GRP_CTRL [4].MODE_RANDOM_LEN[10:10]	1
0xBB021058	SPG_P_TX_GRP_CTRL [4].RESERVED[9:9]	1
0xBB021058	SPG_P_TX_GRP_CTRL [4].MODE_BCINC[8:8]	1
0xBB021058	SPG_P_TX_GRP_CTRL [4].MODE_SAINC[7:7]	1
0xBB021058	SPG_P_TX_GRP_CTRL [4].MODE_DAINC[6:6]	1
0xBB021058	SPG_P_TX_GRP_CTRL [4].MODE_RANDOM[5:5]	1
0xBB021058	SPG_P_TX_GRP_CTRL [4].MODE_CRC[4:4]	1
0xBB021058	SPG_P_TX_GRP_CTRL [4].CMD_STOP[3:3]	1
0xBB021058	SPG_P_TX_GRP_CTRL [4].MODE_CONTINUE[2:2]	1
0xBB021058	SPG_P_TX_GRP_CTRL [4].MODE_PAUSE[1:1]	1
0xBB021058	SPG_P_TX_GRP_CTRL [4].CMD_START[0:0]	1
0xBB021458	SPG_P_TX_GRP_CTRL [5].RESERVED[31:16]	16
0xBB021458	SPG_P_TX_GRP_CTRL [5].TX_FIRST[15:15]	1
0xBB021458	SPG_P_TX_GRP_CTRL [5].STS_GEN[14:14]	1
0xBB021458	SPG_P_TX_GRP_CTRL [5].STS_BUSY[13:13]	1
0xBB021458	SPG_P_TX_GRP_CTRL [5].CMD_SUSPEND[12:12]	1
0xBB021458	SPG_P_TX_GRP_CTRL [5].MODE_LEN_SEL[11:11]	1
0xBB021458	SPG_P_TX_GRP_CTRL [5].MODE_RANDOM_LEN[10:10]	1
0xBB021458	SPG_P_TX_GRP_CTRL [5].RESERVED[9:9]	1
0xBB021458	SPG_P_TX_GRP_CTRL [5].MODE_BCINC[8:8]	1
0xBB021458	SPG_P_TX_GRP_CTRL [5].MODE_SAINC[7:7]	1
0xBB021458	SPG_P_TX_GRP_CTRL [5].MODE_DAINC[6:6]	1
0xBB021458	SPG_P_TX_GRP_CTRL [5].MODE_RANDOM[5:5]	1
0xBB021458	SPG_P_TX_GRP_CTRL [5].MODE_CRC[4:4]	1
0xBB021458	SPG_P_TX_GRP_CTRL [5].CMD_STOP[3:3]	1
0xBB021458	SPG_P_TX_GRP_CTRL [5].MODE_CONTINUE[2:2]	1



Address	Register	Len
0xBB021458	SPG_P_TX_GRP_CTRL [5].MODE_PAUSE[1:1]	1
0xBB021458	SPG_P_TX_GRP_CTRL [5].CMD_START[0:0]	1
0xBB021858	SPG_P_TX_GRP_CTRL [6].RESERVED[31:16]	16
0xBB021858	SPG_P_TX_GRP_CTRL [6].TX_FIRST[15:15]	1
0xBB021858	SPG_P_TX_GRP_CTRL [6].STS_GEN[14:14]	1
0xBB021858	SPG_P_TX_GRP_CTRL [6].STS_BUSY[13:13]	1
0xBB021858	SPG_P_TX_GRP_CTRL [6].CMD_SUSPEND[12:12]	1
0xBB021858	SPG_P_TX_GRP_CTRL [6].MODE_LEN_SEL[11:11]	1
0xBB021858	SPG_P_TX_GRP_CTRL [6].MODE_RANDOM_LEN[10:10]	1
0xBB021858	SPG_P_TX_GRP_CTRL [6].RESERVED[9:9]	1
0xBB021858	SPG_P_TX_GRP_CTRL [6].MODE_BCINC[8:8]	1
0xBB021858	SPG_P_TX_GRP_CTRL [6].MODE_SAINC[7:7]	1
0xBB021858	SPG_P_TX_GRP_CTRL [6].MODE_DAINC[6:6]	1
0xBB021858	SPG_P_TX_GRP_CTRL [6].MODE_RANDOM[5:5]	1
0xBB021858	SPG_P_TX_GRP_CTRL [6].MODE_CRC[4:4]	1
0xBB021858	SPG_P_TX_GRP_CTRL [6].CMD_STOP[3:3]	1
0xBB021858	SPG_P_TX_GRP_CTRL [6].MODE_CONTINUE[2:2]	1
0xBB021858	SPG_P_TX_GRP_CTRL [6].MODE_PAUSE[1:1]	1
0xBB021858	SPG_P_TX_GRP_CTRL [6].CMD_START[0:0]	1
0xBB02005C	SPG_P_LEN_CTRL [0].RESERVED[31:30]	2
0xBB02005C	SPG_P_LEN_CTRL [0].MAX_LEN[29:16]	14
0xBB02005C	SPG_P_LEN_CTRL [0].RESERVED[15:14]	2
0xBB02005C	SPG_P_LEN_CTRL [0].BYTE_LEN[13:0]	14
0xBB02045C	SPG_P_LEN_CTRL [1].RESERVED[31:30]	2
0xBB02045C	SPG_P_LEN_CTRL [1].MAX_LEN[29:16]	14
0xBB02045C	SPG_P_LEN_CTRL [1].RESERVED[15:14]	2
0xBB02045C	SPG_P_LEN_CTRL [1].BYTE_LEN[13:0]	14
0xBB02085C	SPG_P_LEN_CTRL [2].RESERVED[31:30]	2
0xBB02085C	SPG_P_LEN_CTRL [2].MAX_LEN[29:16]	14
0xBB02085C	SPG_P_LEN_CTRL [2].RESERVED[15:14]	2
0xBB02085C	SPG_P_LEN_CTRL [2].BYTE_LEN[13:0]	14
0xBB020C5C	SPG_P_LEN_CTRL [3].RESERVED[31:30]	2
0xBB020C5C	SPG_P_LEN_CTRL [3].MAX_LEN[29:16]	14
0xBB020C5C	SPG_P_LEN_CTRL [3].RESERVED[15:14]	2
0xBB020C5C	SPG_P_LEN_CTRL [3].BYTE_LEN[13:0]	14
0xBB02105C	SPG_P_LEN_CTRL [4].RESERVED[31:30]	2
0xBB02105C	SPG_P_LEN_CTRL [4].MAX_LEN[29:16]	14
0xBB02105C	SPG_P_LEN_CTRL [4].RESERVED[15:14]	2
0xBB02105C	SPG_P_LEN_CTRL [4].BYTE_LEN[13:0]	14
0xBB02145C	SPG_P_LEN_CTRL [5].RESERVED[31:30]	2
0xBB02145C	SPG_P_LEN_CTRL [5].MAX_LEN[29:16]	14
0xBB02145C	SPG_P_LEN_CTRL [5].RESERVED[15:14]	2
0xBB02145C	SPG_P_LEN_CTRL [5].BYTE_LEN[13:0]	14
0xBB02185C	SPG_P_LEN_CTRL [6].RESERVED[31:30]	2
0xBB02185C	SPG_P_LEN_CTRL [6].MAX_LEN[29:16]	14
0xBB02185C	SPG_P_LEN_CTRL [6].RESERVED[15:14]	2



Address	Register	Len
0xBB02185C	SPG_P_LEN_CTRL [6].BYTE_LEN[13:0]	14
0xBB020060	SPG_P_TX_CNT [0].RESERVED[31:24]	8
0xBB020060	SPG_P_TX_CNT [0].CNT[23:0]	24
0xBB020460	SPG_P_TX_CNT [1].RESERVED[31:24]	8
0xBB020460	SPG_P_TX_CNT [1].CNT[23:0]	24
0xBB020860	SPG_P_TX_CNT [2].RESERVED[31:24]	8
0xBB020860	SPG_P_TX_CNT [2].CNT[23:0]	24
0xBB020C60	SPG_P_TX_CNT [3].RESERVED[31:24]	8
0xBB020C60	SPG_P_TX_CNT [3].CNT[23:0]	24
0xBB021060	SPG_P_TX_CNT [4].RESERVED[31:24]	8
0xBB021060	SPG_P_TX_CNT [4].CNT[23:0]	24
0xBB021460	SPG_P_TX_CNT [5].RESERVED[31:24]	8
0xBB021460	SPG_P_TX_CNT [5].CNT[23:0]	24
0xBB021860	SPG_P_TX_CNT [6].RESERVED[31:24]	8
0xBB021860	SPG_P_TX_CNT [6].CNT[23:0]	24
0xBB020064	SPG_P_SA [0].RESERVED[31:16]	16
0xBB020064	SPG_P_SA [0].MAC_47_32[15:0]	16
0xBB020068	SPG_P_SA [0].MAC_31_0[31:0]	32
0xBB020464	SPG_P_SA [1].RESERVED[31:16]	16
0xBB020464	SPG_P_SA [1].MAC_47_32[15:0]	16
0xBB020468	SPG_P_SA [1].MAC_31_0[31:0]	32
0xBB020864	SPG_P_SA [2].RESERVED[31:16]	16
0xBB020864	SPG_P_SA [2].MAC_47_32[15:0]	16
0xBB020868	SPG_P_SA [2].MAC_31_0[31:0]	32
0xBB020C64	SPG_P_SA [3].RESERVED[31:16]	16
0xBB020C64	SPG_P_SA [3].MAC_47_32[15:0]	16
0xBB020C68	SPG_P_SA [3].MAC_31_0[31:0]	32
0xBB021064	SPG_P_SA [4].RESERVED[31:16]	16
0xBB021064	SPG_P_SA [4].MAC_47_32[15:0]	16
0xBB021068	SPG_P_SA [4].MAC_31_0[31:0]	32
0xBB021464	SPG_P_SA [5].RESERVED[31:16]	16
0xBB021464	SPG_P_SA [5].MAC_47_32[15:0]	16
0xBB021468	SPG_P_SA [5].MAC_31_0[31:0]	32
0xBB021864	SPG_P_SA [6].RESERVED[31:16]	16
0xBB021864	SPG_P_SA [6].MAC_47_32[15:0]	16
0xBB021868	SPG_P_SA [6].MAC_31_0[31:0]	32
0xBB02006C	SPG_P_DA [0].RESERVED[31:16]	16
0xBB02006C	SPG_P_DA [0].MAC_47_32[15:0]	16
0xBB020070	SPG_P_DA [0].MAC_31_0[31:0]	32
0xBB02046C	SPG_P_DA [1].RESERVED[31:16]	16
0xBB02046C	SPG_P_DA [1].MAC_47_32[15:0]	16
0xBB020470	SPG_P_DA [1].MAC_31_0[31:0]	32
0xBB02086C	SPG_P_DA [2].RESERVED[31:16]	16
0xBB02086C	SPG_P_DA [2].MAC_47_32[15:0]	16
0xBB020870	SPG_P_DA [2].MAC_31_0[31:0]	32
0xBB020C6C	SPG_P_DA [3].RESERVED[31:16]	16

Address	Register	Len
0xBB020C6C	SPG_P_DA [3].MAC_47_32[15:0]	16
0xBB020C70	SPG_P_DA [3].MAC_31_0[31:0]	32
0xBB02106C	SPG_P_DA [4].RESERVED[31:16]	16
0xBB02106C	SPG_P_DA [4].MAC_47_32[15:0]	16
0xBB021070	SPG_P_DA [4].MAC_31_0[31:0]	32
0xBB02146C	SPG_P_DA [5].RESERVED[31:16]	16
0xBB02146C	SPG_P_DA [5].MAC_47_32[15:0]	16
0xBB021470	SPG_P_DA [5].MAC_31_0[31:0]	32
0xBB02186C	SPG_P_DA [6].RESERVED[31:16]	16
0xBB02186C	SPG_P_DA [6].MAC_47_32[15:0]	16
0xBB021870	SPG_P_DA [6].MAC_31_0[31:0]	32
0xBB020074	SPG_PORT_USER_PKT [0].RESERVED[31:1]	31
0xBB020074	SPG_PORT_USER_PKT [0].EN[0:0]	1
0xBB020474	SPG_PORT_USER_PKT [1].RESERVED[31:1]	31
0xBB020474	SPG_PORT_USER_PKT [1].EN[0:0]	1
0xBB020874	SPG_PORT_USER_PKT [2].RESERVED[31:1]	31
0xBB020874	SPG_PORT_USER_PKT [2].EN[0:0]	1
0xBB020C74	SPG_PORT_USER_PKT [3].RESERVED[31:1]	31
0xBB020C74	SPG_PORT_USER_PKT [3].EN[0:0]	1
0xBB021074	SPG_PORT_USER_PKT [4].RESERVED[31:1]	31
0xBB021074	SPG_PORT_USER_PKT [4].EN[0:0]	1
0xBB021474	SPG_PORT_USER_PKT [5].RESERVED[31:1]	31
0xBB021474	SPG_PORT_USER_PKT [5].EN[0:0]	1
0xBB021874	SPG_PORT_USER_PKT [6].RESERVED[31:1]	31
0xBB021874	SPG_PORT_USER_PKT [6].EN[0:0]	1
0xBB020078	RGF_VER_PER_PORT_MAC [0].REGFILE_VER[31:0]	32
0xBB020478	RGF_VER_PER_PORT_MAC [1].REGFILE_VER[31:0]	32
0xBB020878	RGF_VER_PER_PORT_MAC [2].REGFILE_VER[31:0]	32
0xBB020C78	RGF_VER_PER_PORT_MAC [3].REGFILE_VER[31:0]	32
0xBB021078	RGF_VER_PER_PORT_MAC [4].REGFILE_VER[31:0]	32
0xBB021478	RGF_VER_PER_PORT_MAC [5].REGFILE_VER[31:0]	32
0xBB021878	RGF_VER_PER_PORT_MAC [6].REGFILE_VER[31:0]	32
0xBB02007C	RSVD_PER_PORT_MAC [0][0].RSVD_MEM[31:0]	32
0xBB020080	RSVD_PER_PORT_MAC [0][1].RSVD_MEM[31:0]	32
0xBB020084	RSVD_PER_PORT_MAC [0][2].RSVD_MEM[31:0]	32
0xBB020088	RSVD_PER_PORT_MAC [0][3].RSVD_MEM[31:0]	32
0xBB02008C	RSVD_PER_PORT_MAC [0][4].RSVD_MEM[31:0]	32
0xBB020090	RSVD_PER_PORT_MAC [0][5].RSVD_MEM[31:0]	32
0xBB020094	RSVD_PER_PORT_MAC [0][6].RSVD_MEM[31:0]	32
0xBB020098	RSVD_PER_PORT_MAC [0][7].RSVD_MEM[31:0]	32
0xBB02009C	RSVD_PER_PORT_MAC [0][8].RSVD_MEM[31:0]	32
0xBB0200A0	RSVD_PER_PORT_MAC [0][9].RSVD_MEM[31:0]	32
0xBB0200A4	RSVD_PER_PORT_MAC [0][10].RSVD_MEM[31:0]	32
0xBB0200A8	RSVD_PER_PORT_MAC [0][11].RSVD_MEM[31:0]	32
0xBB0200AC	RSVD_PER_PORT_MAC [0][12].RSVD_MEM[31:0]	32
0xBB0200B0	RSVD_PER_PORT_MAC [0][13].RSVD_MEM[31:0]	32

Address	Register	Len
0xBB0200B4	RSVD_PER_PORT_MAC [0][14].RSVD_MEM[31:0]	32
0xBB0200B8	RSVD_PER_PORT_MAC [0][15].RSVD_MEM[31:0]	32
0xBB02047C	RSVD_PER_PORT_MAC [1][0].RSVD_MEM[31:0]	32
0xBB020480	RSVD_PER_PORT_MAC [1][1].RSVD_MEM[31:0]	32
0xBB020484	RSVD_PER_PORT_MAC [1][2].RSVD_MEM[31:0]	32
0xBB020488	RSVD_PER_PORT_MAC [1][3].RSVD_MEM[31:0]	32
0xBB02048C	RSVD_PER_PORT_MAC [1][4].RSVD_MEM[31:0]	32
0xBB020490	RSVD_PER_PORT_MAC [1][5].RSVD_MEM[31:0]	32
0xBB020494	RSVD_PER_PORT_MAC [1][6].RSVD_MEM[31:0]	32
0xBB020498	RSVD_PER_PORT_MAC [1][7].RSVD_MEM[31:0]	32
0xBB02049C	RSVD_PER_PORT_MAC [1][8].RSVD_MEM[31:0]	32
0xBB0204A0	RSVD_PER_PORT_MAC [1][9].RSVD_MEM[31:0]	32
0xBB0204A4	RSVD_PER_PORT_MAC [1][10].RSVD_MEM[31:0]	32
0xBB0204A8	RSVD_PER_PORT_MAC [1][11].RSVD_MEM[31:0]	32
0xBB0204AC	RSVD_PER_PORT_MAC [1][12].RSVD_MEM[31:0]	32
0xBB0204B0	RSVD_PER_PORT_MAC [1][13].RSVD_MEM[31:0]	32
0xBB0204B4	RSVD_PER_PORT_MAC [1][14].RSVD_MEM[31:0]	32
0xBB0204B8	RSVD_PER_PORT_MAC [1][15].RSVD_MEM[31:0]	32
0xBB02087C	RSVD_PER_PORT_MAC [2][0].RSVD_MEM[31:0]	32
0xBB020880	RSVD_PER_PORT_MAC [2][1].RSVD_MEM[31:0]	32
0xBB020884	RSVD_PER_PORT_MAC [2][2].RSVD_MEM[31:0]	32
0xBB020888	RSVD_PER_PORT_MAC [2][3].RSVD_MEM[31:0]	32
0xBB02088C	RSVD_PER_PORT_MAC [2][4].RSVD_MEM[31:0]	32
0xBB020890	RSVD_PER_PORT_MAC [2][5].RSVD_MEM[31:0]	32
0xBB020894	RSVD_PER_PORT_MAC [2][6].RSVD_MEM[31:0]	32
0xBB020898	RSVD_PER_PORT_MAC [2][7].RSVD_MEM[31:0]	32
0xBB02089C	RSVD_PER_PORT_MAC [2][8].RSVD_MEM[31:0]	32
0xBB0208A0	RSVD_PER_PORT_MAC [2][9].RSVD_MEM[31:0]	32
0xBB0208A4	RSVD_PER_PORT_MAC [2][10].RSVD_MEM[31:0]	32
0xBB0208A8	RSVD_PER_PORT_MAC [2][11].RSVD_MEM[31:0]	32
0xBB0208AC	RSVD_PER_PORT_MAC [2][12].RSVD_MEM[31:0]	32
0xBB0208B0	RSVD_PER_PORT_MAC [2][13].RSVD_MEM[31:0]	32
0xBB0208B4	RSVD_PER_PORT_MAC [2][14].RSVD_MEM[31:0]	32
0xBB0208B8	RSVD_PER_PORT_MAC [2][15].RSVD_MEM[31:0]	32
0xBB020C7C	RSVD_PER_PORT_MAC [3][0].RSVD_MEM[31:0]	32
0xBB020C80	RSVD_PER_PORT_MAC [3][1].RSVD_MEM[31:0]	32
0xBB020C84	RSVD_PER_PORT_MAC [3][2].RSVD_MEM[31:0]	32
0xBB020C88	RSVD_PER_PORT_MAC [3][3].RSVD_MEM[31:0]	32
0xBB020C8C	RSVD_PER_PORT_MAC [3][4].RSVD_MEM[31:0]	32
0xBB020C90	RSVD_PER_PORT_MAC [3][5].RSVD_MEM[31:0]	32
0xBB020C94	RSVD_PER_PORT_MAC [3][6].RSVD_MEM[31:0]	32
0xBB020C98	RSVD_PER_PORT_MAC [3][7].RSVD_MEM[31:0]	32
0xBB020C9C	RSVD_PER_PORT_MAC [3][8].RSVD_MEM[31:0]	32
0xBB020CA0	RSVD_PER_PORT_MAC [3][9].RSVD_MEM[31:0]	32
0xBB020CA4	RSVD_PER_PORT_MAC [3][10].RSVD_MEM[31:0]	32
0xBB020CA8	RSVD_PER_PORT_MAC [3][11].RSVD_MEM[31:0]	32

Address	Register	Len
0xBB020CAC	RSVD_PER_PORT_MAC [3][12].RSVD_MEM[31:0]	32
0xBB020CB0	RSVD_PER_PORT_MAC [3][13].RSVD_MEM[31:0]	32
0xBB020CB4	RSVD_PER_PORT_MAC [3][14].RSVD_MEM[31:0]	32
0xBB020CB8	RSVD_PER_PORT_MAC [3][15].RSVD_MEM[31:0]	32
0xBB02107C	RSVD_PER_PORT_MAC [4][0].RSVD_MEM[31:0]	32
0xBB021080	RSVD_PER_PORT_MAC [4][1].RSVD_MEM[31:0]	32
0xBB021084	RSVD_PER_PORT_MAC [4][2].RSVD_MEM[31:0]	32
0xBB021088	RSVD_PER_PORT_MAC [4][3].RSVD_MEM[31:0]	32
0xBB02108C	RSVD_PER_PORT_MAC [4][4].RSVD_MEM[31:0]	32
0xBB021090	RSVD_PER_PORT_MAC [4][5].RSVD_MEM[31:0]	32
0xBB021094	RSVD_PER_PORT_MAC [4][6].RSVD_MEM[31:0]	32
0xBB021098	RSVD_PER_PORT_MAC [4][7].RSVD_MEM[31:0]	32
0xBB02109C	RSVD_PER_PORT_MAC [4][8].RSVD_MEM[31:0]	32
0xBB0210A0	RSVD_PER_PORT_MAC [4][9].RSVD_MEM[31:0]	32
0xBB0210A4	RSVD_PER_PORT_MAC [4][10].RSVD_MEM[31:0]	32
0xBB0210A8	RSVD_PER_PORT_MAC [4][11].RSVD_MEM[31:0]	32
0xBB0210AC	RSVD_PER_PORT_MAC [4][12].RSVD_MEM[31:0]	32
0xBB0210B0	RSVD_PER_PORT_MAC [4][13].RSVD_MEM[31:0]	32
0xBB0210B4	RSVD_PER_PORT_MAC [4][14].RSVD_MEM[31:0]	32
0xBB0210B8	RSVD_PER_PORT_MAC [4][15].RSVD_MEM[31:0]	32
0xBB02147C	RSVD_PER_PORT_MAC [5][0].RSVD_MEM[31:0]	32
0xBB021480	RSVD_PER_PORT_MAC [5][1].RSVD_MEM[31:0]	32
0xBB021484	RSVD_PER_PORT_MAC [5][2].RSVD_MEM[31:0]	32
0xBB021488	RSVD_PER_PORT_MAC [5][3].RSVD_MEM[31:0]	32
0xBB02148C	RSVD_PER_PORT_MAC [5][4].RSVD_MEM[31:0]	32
0xBB021490	RSVD_PER_PORT_MAC [5][5].RSVD_MEM[31:0]	32
0xBB021494	RSVD_PER_PORT_MAC [5][6].RSVD_MEM[31:0]	32
0xBB021498	RSVD_PER_PORT_MAC [5][7].RSVD_MEM[31:0]	32
0xBB02149C	RSVD_PER_PORT_MAC [5][8].RSVD_MEM[31:0]	32
0xBB0214A0	RSVD_PER_PORT_MAC [5][9].RSVD_MEM[31:0]	32
0xBB0214A4	RSVD_PER_PORT_MAC [5][10].RSVD_MEM[31:0]	32
0xBB0214A8	RSVD_PER_PORT_MAC [5][11].RSVD_MEM[31:0]	32
0xBB0214AC	RSVD_PER_PORT_MAC [5][12].RSVD_MEM[31:0]	32
0xBB0214B0	RSVD_PER_PORT_MAC [5][13].RSVD_MEM[31:0]	32
0xBB0214B4	RSVD_PER_PORT_MAC [5][14].RSVD_MEM[31:0]	32
0xBB0214B8	RSVD_PER_PORT_MAC [5][15].RSVD_MEM[31:0]	32
0xBB02187C	RSVD_PER_PORT_MAC [6][0].RSVD_MEM[31:0]	32
0xBB021880	RSVD_PER_PORT_MAC [6][1].RSVD_MEM[31:0]	32
0xBB021884	RSVD_PER_PORT_MAC [6][2].RSVD_MEM[31:0]	32
0xBB021888	RSVD_PER_PORT_MAC [6][3].RSVD_MEM[31:0]	32
0xBB02188C	RSVD_PER_PORT_MAC [6][4].RSVD_MEM[31:0]	32
0xBB021890	RSVD_PER_PORT_MAC [6][5].RSVD_MEM[31:0]	32
0xBB021894	RSVD_PER_PORT_MAC [6][6].RSVD_MEM[31:0]	32
0xBB021898	RSVD_PER_PORT_MAC [6][7].RSVD_MEM[31:0]	32
0xBB02189C	RSVD_PER_PORT_MAC [6][8].RSVD_MEM[31:0]	32
0xBB0218A0	RSVD_PER_PORT_MAC [6][9].RSVD_MEM[31:0]	32

Address	Register	Len
0xBB0218A4	RSVD_PER_PORT_MAC [6][10].RSVD_MEM[31:0]	32
0xBB0218A8	RSVD_PER_PORT_MAC [6][11].RSVD_MEM[31:0]	32
0xBB0218AC	RSVD_PER_PORT_MAC [6][12].RSVD_MEM[31:0]	32
0xBB0218B0	RSVD_PER_PORT_MAC [6][13].RSVD_MEM[31:0]	32
0xBB0218B4	RSVD_PER_PORT_MAC [6][14].RSVD_MEM[31:0]	32
0xBB0218B8	RSVD_PER_PORT_MAC [6][15].RSVD_MEM[31:0]	32
0xBB022000	WSDS_ANA_00.RESERVED[31:16]	16
0xBB022000	WSDS_ANA_00.REG_BG[15:14]	2
0xBB022000	WSDS_ANA_00.REG_SPDSEL[13:12]	2
0xBB022000	WSDS_ANA_00.REG_RX_SD_POR_SEL[11:11]	1
0xBB022000	WSDS_ANA_00.REG_CDR_BYPASS_SDM_INT[10:10]	1
0xBB022000	WSDS_ANA_00.REG_CDR_EN_LPF_MANUAL[9:9]	1
0xBB022000	WSDS_ANA_00.REG_LOOPBACK_EN[8:8]	1
0xBB022000	WSDS_ANA_00.REG_TX_EMP[7:5]	3
0xBB022000	WSDS_ANA_00.REG_CDR_RESET_MANUAL[4:4]	1
0xBB022000	WSDS_ANA_00.REG_CDR_RESET_SEL[3:3]	1
0xBB022000	WSDS_ANA_00.REG_RX_SEL_CDR_AFEN[2:2]	1
0xBB022000	WSDS_ANA_00.REG_CMU_BIG_KVCO_RX[1:1]	1
0xBB022000	WSDS_ANA_00.REG_CMU_BYPASS_PI_RX[0:0]	1
0xBB022004	WSDS_ANA_01.RESERVED[31:16]	16
0xBB022004	WSDS_ANA_01.REG_CDR_INT_INIT[15:2]	14
0xBB022004	WSDS_ANA_01.REG_CMU_BYPASS_R2[1:1]	1
0xBB022004	WSDS_ANA_01.REG_CDR_KD[0:0]	1
0xBB022008	WSDS_ANA_02.RESERVED[31:16]	16
0xBB022008	WSDS_ANA_02.REG_CDR_KI[15:13]	3
0xBB022008	WSDS_ANA_02.REG_EN_M_VALUE[12:9]	4
0xBB022008	WSDS_ANA_02.REG_ST_M_VALUE[8:4]	5
0xBB022008	WSDS_ANA_02.REG_CDR_KP1[3:1]	3
0xBB022008	WSDS_ANA_02.RESERVED[0:0]	1
0xBB02200C	WSDS_ANA_03.RESERVED[31:16]	16
0xBB02200C	WSDS_ANA_03.REG_PI_M_MODE[15:15]	1
0xBB02200C	WSDS_ANA_03.REG_SQU_TRI[14:14]	1
0xBB02200C	WSDS_ANA_03.REG_CDR_SEL_TESTOUT[13:12]	2
0xBB02200C	WSDS_ANA_03.RESERVED[11:7]	5
0xBB02200C	WSDS_ANA_03.REG_CDR_KP2[6:4]	3
0xBB02200C	WSDS_ANA_03.RESERVED[3:1]	3
0xBB02200C	WSDS_ANA_03.REG_CMU_EN_CKOOBS_RX[0:0]	1
0xBB022010	WSDS_ANA_04.RESERVED[31:8]	24
0xBB022010	WSDS_ANA_04.REG_BG_OFF[7:7]	1
0xBB022010	WSDS_ANA_04.REG_BG_POW[6:6]	1
0xBB022010	WSDS_ANA_04.REG_CKDEGLITCH[5:5]	1
0xBB022010	WSDS_ANA_04.REG_CKOOBS_AUX[4:4]	1
0xBB022010	WSDS_ANA_04.REG_CMU_CP_NEW_CP_RX[3:3]	1
0xBB022010	WSDS_ANA_04.REG_CMU_LDO_EN_RX[2:2]	1
0xBB022010	WSDS_ANA_04.REG_CMU_VC_DLY_RX[1:1]	1
0xBB022010	WSDS_ANA_04.RESERVED[0:0]	1

Address	Register	Len
0xBB022014	WSDS_ANA_05.RESERVED[31:16]	16
0xBB022014	WSDS_ANA_05.REG_ACC2_MANUAL[15:15]	1
0xBB022014	WSDS_ANA_05.REG_ACC2_PERIOD[14:5]	10
0xBB022014	WSDS_ANA_05.RESERVED[4:3]	2
0xBB022014	WSDS_ANA_05.REG_CMU_PI_I_SEL_RX[2:0]	3
0xBB022018	WSDS_ANA_06.RESERVED[31:8]	24
0xBB022018	WSDS_ANA_06.REG_CMU_SEL_CP_I_RX_40M[7:4]	4
0xBB022018	WSDS_ANA_06.REG_CMU_SEL_CP_I_RX_25M[3:0]	4
0xBB02201C	WSDS_ANA_07.RESERVED[31:15]	17
0xBB02201C	WSDS_ANA_07.REG_CMU_SEL_R1_RX_40M[14:12]	3
0xBB02201C	WSDS_ANA_07.REG_CMU_SEL_R1_RX_25M[11:9]	3
0xBB02201C	WSDS_ANA_07.REG_CMU_SEL_DIV4_RX[8:8]	1
0xBB02201C	WSDS_ANA_07.REG_CMU_SEL_FREF[7:7]	1
0xBB02201C	WSDS_ANA_07.REG_CMU_SEL_PREDIV_RX[6:5]	2
0xBB02201C	WSDS_ANA_07.REG_CMU_SEL_VCO_RX[4:4]	1
0xBB02201C	WSDS_ANA_07.RESERVED[3:2]	2
0xBB02201C	WSDS_ANA_07.REG_TX_SWING[1:0]	2
0xBB022020	WSDS_ANA_08.RESERVED[31:9]	23
0xBB022020	WSDS_ANA_08.REG_CMU_VSEL_LDO_A_RX[8:6]	3
0xBB022020	WSDS_ANA_08.REG_CMU_VSEL_LDO_D[5:3]	3
0xBB022020	WSDS_ANA_08.REG_COMINIT[2:2]	1
0xBB022020	WSDS_ANA_08.REG_COMWAKE[1:1]	1
0xBB022020	WSDS_ANA_08.REG_EN_CLKREQ[0:0]	1
0xBB022024	WSDS_ANA_09.RESERVED[31:4]	28
0xBB022024	WSDS_ANA_09.REG_EN_SATA[3:3]	1
0xBB022024	WSDS_ANA_09.REG_FORCE_RCVDET[2:2]	1
0xBB022024	WSDS_ANA_09.REG_IBRXSEL[1:0]	2
0xBB022028	WSDS_ANA_0A.RESERVED[31:16]	16
0xBB022028	WSDS_ANA_0A.REG_IBTXSEL[15:14]	2
0xBB022028	WSDS_ANA_0A.REG_OOBS_CALI[13:12]	2
0xBB022028	WSDS_ANA_0A.REG_OOBS_CALSEL[11:11]	1
0xBB022028	WSDS_ANA_0A.REG_OOBS_CKSEL[10:10]	1
0xBB022028	WSDS_ANA_0A.REG_OOBS_FORCECAL[9:9]	1
0xBB022028	WSDS_ANA_0A.REG_OOBS_FREQSEL[8:8]	1
0xBB022028	WSDS_ANA_0A.REG_OOBS_ISEL[7:7]	1
0xBB022028	WSDS_ANA_0A.REG_OOBS_NSQDLY[6:6]	1
0xBB022028	WSDS_ANA_0A.REG_OOBS_RXIDLE_MANUAL[5:5]	1
0xBB022028	WSDS_ANA_0A.REG_OOBS_SEL[4:4]	1
0xBB022028	WSDS_ANA_0A.REG_OOBS_SEN[3:0]	4
0xBB02202C	WSDS_ANA_0B.RESERVED[31:16]	16
0xBB02202C	WSDS_ANA_0B.REG_RX_DBG_SEL[15:14]	2
0xBB02202C	WSDS_ANA_0B.REG_RX_DCVS_SEL[13:13]	1
0xBB02202C	WSDS_ANA_0B.REG_RX_EN_KOFFSET[12:12]	1
0xBB02202C	WSDS_ANA_0B.REG_RX_EN_SELF[11:11]	1
0xBB02202C	WSDS_ANA_0B.REG_RX_EN_TEST[10:10]	1
0xBB02202C	WSDS_ANA_0B.REG_RX_EQ_EN_SLICER[9:9]	1

Address	Register	Len
0xBB02202C	WSDS_ANA_0B.REG_RX_EQ_GAIN[8:7]	2
0xBB02202C	WSDS_ANA_0B.REG_RX_EQ_HOLD[6:6]	1
0xBB02202C	WSDS_ANA_0B.REG_RX_EQ_SELREG[5:5]	1
0xBB02202C	WSDS_ANA_0B.REG_RX_EQ2SEL[4:3]	2
0xBB02202C	WSDS_ANA_0B.REG_RX_FORCERUN[2:2]	1
0xBB02202C	WSDS_ANA_0B.REG_RX_IDLE_SPD[1:1]	1
0xBB02202C	WSDS_ANA_0B.REG_RX_IQDSEL[0:0]	1
0xBB022030	WSDS_ANA_0C.RESERVED[31:16]	16
0xBB022030	WSDS_ANA_0C.REG_RX_EQ_IN[15:9]	7
0xBB022030	WSDS_ANA_0C.REG_RX_OFFSET_ADJR[8:5]	4
0xBB022030	WSDS_ANA_0C.REG_RX_OFFSET_AUTO_K[4:4]	1
0xBB022030	WSDS_ANA_0C.REG_RX_OFFSET_RANGE[3:2]	2
0xBB022030	WSDS_ANA_0C.REG_RX_PIENSEL[1:1]	1
0xBB022030	WSDS_ANA_0C.REG_RX_PS_AFE[0:0]	1
0xBB022034	WSDS_ANA_0D.RESERVED[31:16]	16
0xBB022034	WSDS_ANA_0D.REG_RX_PSAVE_SEL[15:15]	1
0xBB022034	WSDS_ANA_0D.REG_RX_SEL_RXIDLE[14:14]	1
0xBB022034	WSDS_ANA_0D.REG_RX_TIMER_BER[13:9]	5
0xBB022034	WSDS_ANA_0D.REG_RX_TIMER_EQ[8:4]	5
0xBB022034	WSDS_ANA_0D.REG_RXDSEL[3:2]	2
0xBB022034	WSDS_ANA_0D.REG_SERDES_MODE[1:0]	2
0xBB022038	WSDS_ANA_0E.RESERVED[31:16]	16
0xBB022038	WSDS_ANA_0E.REG_RX_TIMER_LPF[15:11]	5
0xBB022038	WSDS_ANA_0E.REG_TX_AMP[10:8]	3
0xBB022038	WSDS_ANA_0E.REG_TX_BAMP[7:5]	3
0xBB022038	WSDS_ANA_0E.REG_TX_BEAE[4:4]	1
0xBB022038	WSDS_ANA_0E.REG_TX_DLY[3:2]	2
0xBB022038	WSDS_ANA_0E.REG_TX_EN_EMPHAS[1:1]	1
0xBB022038	WSDS_ANA_0E.REG_TX_EN_TEST[0:0]	1
0xBB02203C	WSDS_ANA_0F.RESERVED[31:4]	28
0xBB02203C	WSDS_ANA_0F.REG_TX_EN_VCM_RES[3:3]	1
0xBB02203C	WSDS_ANA_0F.REG_TX_SEL_CKRD_DUTY[2:2]	1
0xBB02203C	WSDS_ANA_0F.REG_TX_SEL_VCM[1:0]	2
0xBB022040	WSDS_ANA_10.RESERVED[31:13]	19
0xBB022040	WSDS_ANA_10.REG_Z0_NADJR[12:9]	4
0xBB022040	WSDS_ANA_10.REG_Z0_NAUTO_K[8:8]	1
0xBB022040	WSDS_ANA_10.REG_Z0_PADJR[7:3]	5
0xBB022040	WSDS_ANA_10.REG_Z0_PAUTO_K[2:2]	1
0xBB022040	WSDS_ANA_10.REG_Z0_TEST[1:1]	1
0xBB022040	WSDS_ANA_10.REG_Z0_TUNE[0:0]	1
0xBB022044	WSDS_ANA_11.RESERVED[31:16]	16
0xBB022044	WSDS_ANA_11.REG_CMU_SEL_CP_RX[15:15]	1
0xBB022044	WSDS_ANA_11.REG_OOBS_SEN_VAR[14:10]	5
0xBB022044	WSDS_ANA_11.REG_SEL_IBLPF[9:9]	1
0xBB022044	WSDS_ANA_11.REG_RX50_LINK[8:8]	1
0xBB022044	WSDS_ANA_11.REG_TX_50_EN[7:7]	1



Address	Register	Len
0xBB022044	WSDS_ANA_11.RESERVED[6:0]	7
0xBB022048	WSDS_ANA_12.DMY0[31:0]	32
0xBB02204C	WSDS_ANA_13.DMY1[31:0]	32
0xBB022050	WSDS_ANA_14.RESERVED[31:14]	18
0xBB022050	WSDS_ANA_14.REG_CMU_CP_NEW_EN_TX[13:13]	1
0xBB022050	WSDS_ANA_14.REG_CMU_SEL_CP_I_TX[12:9]	4
0xBB022050	WSDS_ANA_14.REG_CMU_SEL_CP_TX[8:8]	1
0xBB022050	WSDS_ANA_14.REG_CMU_SEL_RS_TX[7:5]	3
0xBB022050	WSDS_ANA_14.REG_CMU_BIG_KVCO_TX[4:4]	1
0xBB022050	WSDS_ANA_14.REG_CMU_SEL_VCO_TX[3:3]	1
0xBB022050	WSDS_ANA_14.REG_CMU_LDO_EN_TX[2:2]	1
0xBB022050	WSDS_ANA_14.REG_CMU_VC_DLY_TX[1:1]	1
0xBB022050	WSDS_ANA_14.REG_CMU_BYPASS_PI_TX[0:0]	1
0xBB022054	WSDS_ANA_15.RESERVED[31:16]	16
0xBB022054	WSDS_ANA_15.REG_CMU_EN_GPHY[15:15]	1
0xBB022054	WSDS_ANA_15.REG_CMU_PI_I_SEL_TX[14:12]	3
0xBB022054	WSDS_ANA_15.REG_PREDIV_BYPASS_TX[11:11]	1
0xBB022054	WSDS_ANA_15.RESERVED[10:8]	3
0xBB022054	WSDS_ANA_15.REG_CMU_LDO_VREFSEL_TX[7:5]	3
0xBB022054	WSDS_ANA_15.REG_CMU_PREDIV_TX[4:0]	5
0xBB022058	WSDS_ANA_16.RESERVED[31:16]	16
0xBB022058	WSDS_ANA_16.REG_CMU_PREDIV_GPHY[15:13]	3
0xBB022058	WSDS_ANA_16.RESERVED[12:2]	11
0xBB022058	WSDS_ANA_16.REG_CMU_SEL_CP_GPHY[1:0]	2
0xBB02205C	WSDS_ANA_17.RESERVED[31:10]	22
0xBB02205C	WSDS_ANA_17.REG_CMU_POSTDIV_GPHY_40M[9:5]	5
0xBB02205C	WSDS_ANA_17.REG_CMU_POSTDIV_GPHY_25M[4:0]	5
0xBB022060	WSDS_ANA_18.RESERVED[31:16]	16
0xBB022060	WSDS_ANA_18.REG_BEN_SWING[15:13]	3
0xBB022060	WSDS_ANA_18.REG_BEN_SEL_CML[12:12]	1
0xBB022060	WSDS_ANA_18.REG_BEN_V20_SEL[11:10]	2
0xBB022060	WSDS_ANA_18.REG_RX_EN_I_SAMPLER[9:9]	1
0xBB022060	WSDS_ANA_18.RESERVED[8:8]	1
0xBB022060	WSDS_ANA_18.REG_CMU_TX_OFF[7:7]	1
0xBB022060	WSDS_ANA_18.REG_RX_KP1_2[6:4]	3
0xBB022060	WSDS_ANA_18.REG_RX_KP_DIV[3:2]	2
0xBB022060	WSDS_ANA_18.REG_TX_CLK_SEL[1:0]	2
0xBB022064	WSDS_ANA_19.RESERVED[31:14]	18
0xBB022064	WSDS_ANA_19.TX_DISABLE_OPTIC[13:13]	1
0xBB022064	WSDS_ANA_19.CKRDY_GPHY[12:12]	1
0xBB022064	WSDS_ANA_19.BER_NOTIFY[11:11]	1
0xBB022064	WSDS_ANA_19.REG_RX_EQ_FILTER_OUT[10:4]	7
0xBB022064	WSDS_ANA_19.REG_RX_OFFSET_CODE[3:0]	4
0xBB022068	WSDS_ANA_1A.RESERVED[31:16]	16
0xBB022068	WSDS_ANA_1A.REG_RX_SEL_SD[15:15]	1
0xBB022068	WSDS_ANA_1A.REG_TX_V20_SEL[14:13]	2



Address	Register	Len
0xBB022068	WSDS_ANA_1A.REG_DIVN_GPHY_REF[12:5]	8
0xBB022068	WSDS_ANA_1A.REG_RX_ACC2_MANUAL_2[4:4]	1
0xBB022068	WSDS_ANA_1A.REG_RX_SQU_TRI_2[3:3]	1
0xBB022068	WSDS_ANA_1A.REG_RX_KP2_2[2:0]	3
0xBB02206C	WSDS_ANA_1B.RESERVED[31:10]	22
0xBB02206C	WSDS_ANA_1B.REG_RX_ACC2_PERIOD_2[9:0]	10
0xBB022070	WSDS_ANA_1C.RESERVED[31:8]	24
0xBB022070	WSDS_ANA_1C.REG_RX_FILT_CONFIG[7:0]	8
0xBB022074	WSDS_ANA_1D.RESERVED[31:14]	18
0xBB022074	WSDS_ANA_1D.REG_RX_INT_INIT_2[13:0]	14
0xBB022078	WSDS_ANA_1E.RESERVED[31:16]	16
0xBB022078	WSDS_ANA_1E.REG_CMU_ADP_TIME_GPHY[15:13]	3
0xBB022078	WSDS_ANA_1E.REG_CMU_AUTO_K_GPHY[12:12]	1
0xBB022078	WSDS_ANA_1E.REG_CMU_CALIB_TIME_GPHY[11:9]	3
0xBB022078	WSDS_ANA_1E.REG_CMU_CP_TIME_GPHY[8:6]	3
0xBB022078	WSDS_ANA_1E.REG_CMU_DIVIDE_NUM_GPHY[5:0]	6
0xBB02207C	WSDS_ANA_1F.RESERVED[31:16]	16
0xBB02207C	WSDS_ANA_1F.REG_CMU_FLD_DSEL_GPHY[15:15]	1
0xBB02207C	WSDS_ANA_1F.REG_CMU_ICP_SEL_GPHY[14:11]	4
0xBB02207C	WSDS_ANA_1F.REG_CMU_INIT_TIME_GPHY[10:8]	3
0xBB02207C	WSDS_ANA_1F.REG_CMU_ISTANK_SEL_GPHY[7:6]	2
0xBB02207C	WSDS_ANA_1F.REG_CMU_LCBIAS_LPF_EN_GPHY[5:5]	1
0xBB02207C	WSDS_ANA_1F.REG_CMU_LCVCO_TR_GPHY[4:0]	5
0xBB022080	WSDS_ANA_20.RESERVED[31:10]	22
0xBB022080	WSDS_ANA_20.REG_CMU_LOCK_DN_LIMIT_GPHY[9:0]	10
0xBB022084	WSDS_ANA_21.RESERVED[31:10]	22
0xBB022084	WSDS_ANA_21.REG_CMU_LOCK_UP_LIMIT_GPHY[9:0]	10
0xBB022088	WSDS_ANA_22.RESERVED[31:15]	17
0xBB022088	WSDS_ANA_22.REG_CMU_N_PLL_GPHY[14:10]	5
0xBB022088	WSDS_ANA_22.REG_CMU_N_PLL_TX[9:2]	8
0xBB022088	WSDS_ANA_22.RESERVED[1:0]	2
0xBB02208C	WSDS_ANA_23.RESERVED[31:12]	20
0xBB02208C	WSDS_ANA_23.REG_CMU_SEL_R_GPHY[11:9]	3
0xBB02208C	WSDS_ANA_23.RESERVED[8:4]	5
0xBB02208C	WSDS_ANA_23.REG_CMU_VSEL_LREG_GPHY[3:1]	3
0xBB02208C	WSDS_ANA_23.REG_SEL_IBN[0:0]	1
0xBB022090	WSDS_ANA_24.RESERVED[31:14]	18
0xBB022090	WSDS_ANA_24.REG_FREF_SEL_GPHY[13:12]	2
0xBB022090	WSDS_ANA_24.REG_TTL_DRI_SEL[11:10]	2
0xBB022090	WSDS_ANA_24.REG_BEN_TTL_OUT[9:9]	1
0xBB022090	WSDS_ANA_24.REG_CMU_AUTO_MODE_GPHY[8:8]	1
0xBB022090	WSDS_ANA_24.REG_CMU_CALIB_LATE_GPHY[7:7]	1
0xBB022090	WSDS_ANA_24.REG_CMU_CALIB_MANUAL_GPHY[6:6]	1
0xBB022090	WSDS_ANA_24.REG_CMU_CP_ADJ_EN_GPHY[5:5]	1
0xBB022090	WSDS_ANA_24.REG_CMU_CP_EN_MANUAL_GPHY[4:4]	1
0xBB022090	WSDS_ANA_24.REG_CMU_EN_TX[3:3]	1

Address	Register	Len
0xBB022090	WSDS_ANA_24.REG_CMU_START_EN_GPHY_MANUAL[2:2]	1
0xBB022090	WSDS_ANA_24.REG_CMU_WD_ENABLE_GPHY[1:1]	1
0xBB022090	WSDS_ANA_24.REG_TX_DBG_SEL[0:0]	1
0xBB022094	WSDS_ANA_25.RESERVED[31:16]	16
0xBB022094	WSDS_ANA_25.REG_CMU_F390K_GPHY[15:14]	2
0xBB022094	WSDS_ANA_25.REG_CMU_LC_BUF_SEL_GPHY[13:12]	2
0xBB022094	WSDS_ANA_25.REG_CMU_TIME0_CK_GPHY[11:9]	3
0xBB022094	WSDS_ANA_25.REG_CMU_TIME2_RST_WIDTH_GPHY[8:7]	2
0xBB022094	WSDS_ANA_25.REG_CMU_TIME_RDY_CKOUT_GPHY[6:5]	2
0xBB022094	WSDS_ANA_25.REG_CMU_VCO_COARSE_GPHY[4:0]	5
0xBB022098	WSDS_DIG_00.RESERVED[31:12]	20
0xBB022098	WSDS_DIG_00.CFG_SFT_RSB_ANA[11:11]	1
0xBB022098	WSDS_DIG_00.CFG_SFT_RSTB_GPON[10:10]	1
0xBB022098	WSDS_DIG_00.CFG_SFT_RSTB_EPON[9:9]	1
0xBB022098	WSDS_DIG_00.CFG_SFT_RSTB[8:8]	1
0xBB022098	WSDS_DIG_00.CFG_FRCV_155M_EN[7:7]	1
0xBB022098	WSDS_DIG_00.CFG_FRC_155M_EN[6:6]	1
0xBB022098	WSDS_DIG_00.CFG_FRCV_125M_EN[5:5]	1
0xBB022098	WSDS_DIG_00.CFG_FRC_125M_EN[4:4]	1
0xBB022098	WSDS_DIG_00.CFG_FRCV_GMIICK_EN[3:3]	1
0xBB022098	WSDS_DIG_00.CFG_FRC_GMIICK_EN[2:2]	1
0xBB022098	WSDS_DIG_00.CFG_TXDIS_SEL[1:1]	1
0xBB022098	WSDS_DIG_00.CFG_STOP_CLK[0:0]	1
0xBB02209C	WSDS_DIG_01.RESERVED[31:16]	16
0xBB02209C	WSDS_DIG_01.CFG_FRC_CMUEN[15:14]	2
0xBB02209C	WSDS_DIG_01.CFG_FRC_CMUEN_TX[13:12]	2
0xBB02209C	WSDS_DIG_01.CFG_FRC_RX_OOBS_EN[11:10]	2
0xBB02209C	WSDS_DIG_01.CFG_FRC_V2ANALOG[9:8]	2
0xBB02209C	WSDS_DIG_01.CFG_FRC_PDOWN[7:6]	2
0xBB02209C	WSDS_DIG_01.CFG_FRC_RX_EN[5:4]	2
0xBB02209C	WSDS_DIG_01.CFG_FRC_NOTIFY[3:2]	2
0xBB02209C	WSDS_DIG_01.CFG_FRC_RXIDLE[1:0]	2
0xBB0220A0	WSDS_DIG_02.RESERVED[31:10]	22
0xBB0220A0	WSDS_DIG_02.CFG_FRCV_SEL_FX100[9:9]	1
0xBB0220A0	WSDS_DIG_02.CFG_FRC_SEL_FX100[8:8]	1
0xBB0220A0	WSDS_DIG_02.CFG_SDS_PHY_MODE[7:7]	1
0xBB0220A0	WSDS_DIG_02.FRC_REG4_EN[6:6]	1
0xBB0220A0	WSDS_DIG_02.FRC_REG4_FIB100[5:5]	1
0xBB0220A0	WSDS_DIG_02.CFG_LPI_GMII_SEL[4:4]	1
0xBB0220A0	WSDS_DIG_02.CFG_CMD_STOP_GLI_CLK[3:0]	4
0xBB0220A4	WSDS_DIG_03.RESERVED[31:7]	25
0xBB0220A4	WSDS_DIG_03.CFG_TXDIS_SEL_DLY[6:4]	3
0xBB0220A4	WSDS_DIG_03.CFG_D2ANLOG_SEL[3:0]	4
0xBB0220A8	WSDS_DIG_04.RESERVED[31:3]	29
0xBB0220A8	WSDS_DIG_04.CFG_AFE_LPK_EN[2:2]	1
0xBB0220A8	WSDS_DIG_04.CFG_DIG_LPK_EN[1:1]	1

Address	Register	Len
0xBB0220A8	WSDS_DIG_04.CFG_RMT_LPK_EN[0:0]	1
0xBB0220AC	WSDS_DIG_05.CFG_DMY0[31:0]	32
0xBB0220B0	WSDS_DIG_06.CFG_DMY1[31:0]	32
0xBB0220B4	WSDS_DIG_07.RESERVED[31:16]	16
0xBB0220B4	WSDS_DIG_07.CFG_DBG_TRAN_SEL[15:0]	16
0xBB0220B8	WSDS_DIG_08.RESERVED[31:8]	24
0xBB0220B8	WSDS_DIG_08.CFG_BYPASS_PI_RX[7:7]	1
0xBB0220B8	WSDS_DIG_08.RESERVED[6:6]	1
0xBB0220B8	WSDS_DIG_08.CFG_EN_CENTER_IN_RX[5:5]	1
0xBB0220B8	WSDS_DIG_08.RESERVED[4:4]	1
0xBB0220B8	WSDS_DIG_08.CFG_EN_SSC_RX[3:3]	1
0xBB0220B8	WSDS_DIG_08.RESERVED[2:2]	1
0xBB0220B8	WSDS_DIG_08.CFG_ORDER_RX[1:1]	1
0xBB0220B8	WSDS_DIG_08.RESERVED[0:0]	1
0xBB0220BC	WSDS_DIG_09.RESERVED[31:16]	16
0xBB0220BC	WSDS_DIG_09.CFG_SEL_MODE_RX[15:15]	1
0xBB0220BC	WSDS_DIG_09.RESERVED[14:14]	1
0xBB0220BC	WSDS_DIG_09.CFG_WTG_SEL_RX[13:11]	3
0xBB0220BC	WSDS_DIG_09.RESERVED[10:8]	3
0xBB0220BC	WSDS_DIG_09.CFG_FRC_POW_SSCD_RX[7:7]	1
0xBB0220BC	WSDS_DIG_09.RESERVED[6:6]	1
0xBB0220BC	WSDS_DIG_09.CFG_FRC_N_PLL_RX[5:5]	1
0xBB0220BC	WSDS_DIG_09.RESERVED[4:4]	1
0xBB0220BC	WSDS_DIG_09.CFG_FRC_PH_SEL_RX[3:3]	1
0xBB0220BC	WSDS_DIG_09.RESERVED[2:2]	1
0xBB0220BC	WSDS_DIG_09.CFG_FRCV_POW_SSCD_RX[1:1]	1
0xBB0220BC	WSDS_DIG_09.RESERVED[0:0]	1
0xBB0220C0	WSDS_DIG_0A.RESERVED[31:12]	20
0xBB0220C0	WSDS_DIG_0A.CFG_F_CODE_RX_25M[11:0]	12
0xBB0220C4	WSDS_DIG_0B.RESERVED[31:12]	20
0xBB0220C4	WSDS_DIG_0B.CFG_F_CODE_RX_40M[11:0]	12
0xBB0220C8	WSDS_DIG_0C.RESERVED[31:9]	23
0xBB0220C8	WSDS_DIG_0C.CFG_N_CODE_RX_25M[8:0]	9
0xBB0220CC	WSDS_DIG_0D.RESERVED[31:9]	23
0xBB0220CC	WSDS_DIG_0D.CFG_N_CODE_RX_40M[8:0]	9
0xBB0220D0	WSDS_DIG_0E.RESERVED[31:13]	19
0xBB0220D0	WSDS_DIG_0E.CFG_STEP_IN_RX[12:0]	13
0xBB0220D4	WSDS_DIG_0F.RESERVED[31:12]	20
0xBB0220D4	WSDS_DIG_0F.CFG_TBASE_RX[11:0]	12
0xBB0220D8	WSDS_DIG_10.RESERVED[31:9]	23
0xBB0220D8	WSDS_DIG_10.CFG_FRCV_N_PLL_RX[8:0]	9
0xBB0220DC	WSDS_DIG_11.RESERVED[31:16]	16
0xBB0220DC	WSDS_DIG_11.CFG_FRCV_PH_SEL_RX[15:0]	16
0xBB0220E0	WSDS_DIG_12.RESERVED[31:12]	20
0xBB0220E0	WSDS_DIG_12.CFG_WD_ENABLE_RX[11:11]	1
0xBB0220E0	WSDS_DIG_12.CFG_WD_ENABLE_TX[10:10]	1

Address	Register	Len
0xBB0220E0	WSDS_DIG_12.RESERVED[9:9]	1
0xBB0220E0	WSDS_DIG_12.CFG_F390K_RX[8:7]	2
0xBB0220E0	WSDS_DIG_12.CFG_F390K_TX[6:5]	2
0xBB0220E0	WSDS_DIG_12.RESERVED[4:3]	2
0xBB0220E0	WSDS_DIG_12.CFG_TIME0_CK_RX[2:0]	3
0xBB0220E4	WSDS_DIG_13.RESERVED[31:14]	18
0xBB0220E4	WSDS_DIG_13.CFG_TIME0_CK_TX[13:11]	3
0xBB0220E4	WSDS_DIG_13.RESERVED[10:8]	3
0xBB0220E4	WSDS_DIG_13.CFG_T_RDY_CKOUT_RX[7:6]	2
0xBB0220E4	WSDS_DIG_13.CFG_T_RDY_CKOUT_TX[5:4]	2
0xBB0220E4	WSDS_DIG_13.RESERVED[3:2]	2
0xBB0220E4	WSDS_DIG_13.CFG_T2_RST_WIDTH_RX[1:0]	2
0xBB0220E8	WSDS_DIG_14.RESERVED[31:16]	16
0xBB0220E8	WSDS_DIG_14.CFG_T2_RST_WIDTH_TX[15:14]	2
0xBB0220E8	WSDS_DIG_14.RESERVED[13:12]	2
0xBB0220E8	WSDS_DIG_14.CFG_FRC_CKRDY_RX[11:11]	1
0xBB0220E8	WSDS_DIG_14.CFG_FRC_CKRDY_TX[10:10]	1
0xBB0220E8	WSDS_DIG_14.RESERVED[9:9]	1
0xBB0220E8	WSDS_DIG_14.CFG_FRCV_CKRDY_RX[8:8]	1
0xBB0220E8	WSDS_DIG_14.CFG_FRCV_CKRDY_TX[7:7]	1
0xBB0220E8	WSDS_DIG_14.RESERVED[6:6]	1
0xBB0220E8	WSDS_DIG_14.CFG_FRC_N911_B_RX[5:5]	1
0xBB0220E8	WSDS_DIG_14.CFG_FRC_N911_B_TX[4:4]	1
0xBB0220E8	WSDS_DIG_14.RESERVED[3:3]	1
0xBB0220E8	WSDS_DIG_14.CFG_FRCV_N911_B_RX[2:2]	1
0xBB0220E8	WSDS_DIG_14.CFG_FRCV_N911_B_TX[1:1]	1
0xBB0220E8	WSDS_DIG_14.RESERVED[0:0]	1
0xBB0220EC	WSDS_DIG_15.RESERVED[31:4]	28
0xBB0220EC	WSDS_DIG_15.CFG_CLKREQB[3:3]	1
0xBB0220EC	WSDS_DIG_15.CFG_RCV_DETECT[2:2]	1
0xBB0220EC	WSDS_DIG_15.CFG_RXIDLE_D[1:1]	1
0xBB0220EC	WSDS_DIG_15.CFG_TXBEACON[0:0]	1
0xBB0220F0	WSDS_DIG_16.RESERVED[31:16]	16
0xBB0220F0	WSDS_DIG_16.CFG_WRAP_SDS_DBG_SEL[15:0]	16
0xBB0220F4	WSDS_DIG_17.RESERVED[31:2]	30
0xBB0220F4	WSDS_DIG_17.CFG_FRC_BYP_EPMC[1:0]	2
0xBB0220F8	WSDS_DIG_18.RESERVED[31:13]	19
0xBB0220F8	WSDS_DIG_18.BEN_OE[12:12]	1
0xBB0220F8	WSDS_DIG_18.TX_DISABLE_OPTIC_OE[11:11]	1
0xBB0220F8	WSDS_DIG_18.CFG_FRC_OPTIC_LOS_INV[10:10]	1
0xBB0220F8	WSDS_DIG_18.CFG_FRC_CDR_LOS_INV[9:9]	1
0xBB0220F8	WSDS_DIG_18.CFG_FRC_TX_DISABLE_OPTIC_INV[8:8]	1
0xBB0220F8	WSDS_DIG_18.CFG_FRC_TX_DISABLE_OPTIC[7:6]	2
0xBB0220F8	WSDS_DIG_18.CFG_FRC_TX_OPTIC_SD_INV[5:5]	1
0xBB0220F8	WSDS_DIG_18.CFG_FRC_TX_OPTIC_SD[4:3]	2
0xBB0220F8	WSDS_DIG_18.CFG_FRC_BEN_INV[2:2]	1

Address	Register	Len
0xBB0220F8	WSDS_DIG_18.CFG_FRC_BEN[1:0]	2
0xBB0220FC	WSDS_DIG_19.RESERVED[31:16]	16
0xBB0220FC	WSDS_DIG_19.CFG_PRBS_TYPE_SEL[15:0]	16
0xBB022100	WSDS_DIG_1A.RESERVED[31:1]	31
0xBB022100	WSDS_DIG_1A.CFG_PRBS_EN[0:0]	1
0xBB022104	WSDS_DIG_1B.RESERVED[31:16]	16
0xBB022104	WSDS_DIG_1B.CFG_PRBS_ERRORS[15:0]	16
0xBB022108	WSDS_DIG_1C.RESERVED[31:16]	16
0xBB022108	WSDS_DIG_1C.CFG_PRBS_STATUS[15:0]	16
0xBB02210C	WSDS_DIG_1D.RESERVED[31:15]	17
0xBB02210C	WSDS_DIG_1D.CFG_SFT_RSTB_INF[14:14]	1
0xBB02210C	WSDS_DIG_1D.CFG_FRC_CLK_EN[13:13]	1
0xBB02210C	WSDS_DIG_1D.CFG_FRCV_CLK_EN[12:12]	1
0xBB02210C	WSDS_DIG_1D.CFG_TX_WRPT_DN_SEL[11:9]	3
0xBB02210C	WSDS_DIG_1D.CFG_RX_WRPT_DN_SEL[8:6]	3
0xBB02210C	WSDS_DIG_1D.CFG_BEN_INV[5:5]	1
0xBB02210C	WSDS_DIG_1D.CFG_HAM_PTR[4:4]	1
0xBB02210C	WSDS_DIG_1D.CFG_ERRHAM_EN[3:3]	1
0xBB02210C	WSDS_DIG_1D.CFG_FREE_CNT_SEL[2:0]	3
0xBB022110	WSDS_DIG_1E.RESERVED[31:11]	21
0xBB022110	WSDS_DIG_1E.CFG_A2D16_INV[10:10]	1
0xBB022110	WSDS_DIG_1E.CFG_D2A16_INV[9:9]	1
0xBB022110	WSDS_DIG_1E.CFG_RSTB_BITERR_INV[8:8]	1
0xBB022110	WSDS_DIG_1E.CFG_FRCV_RSTB_BITERR[7:7]	1
0xBB022110	WSDS_DIG_1E.CFG_FRC_RSTB_BITERR[6:6]	1
0xBB022110	WSDS_DIG_1E.CFG_ANALOG2D_SEL[5:5]	1
0xBB022110	WSDS_DIG_1E.CFG_D2ANLOG_INF_SEL[4:4]	1
0xBB022110	WSDS_DIG_1E.CFG_622_START_SEL[3:0]	4
0xBB022114	WSDS_DIG_1F.RESERVED[31:26]	6
0xBB022114	WSDS_DIG_1F.CFG_CLR_T1_FULL[25:25]	1
0xBB022114	WSDS_DIG_1F.CFG_CLR_T0_FULL[24:24]	1
0xBB022114	WSDS_DIG_1F.CFG_T1_DIF_MIN[23:18]	6
0xBB022114	WSDS_DIG_1F.CFG_T1_DIF_MAX[17:12]	6
0xBB022114	WSDS_DIG_1F.CFG_T0_DIF_MIN[11:6]	6
0xBB022114	WSDS_DIG_1F.CFG_T0_DIF_MAX[5:0]	6
0xBB022118	WSDS_DIG_20.RESERVED[31:13]	19
0xBB022118	WSDS_DIG_20.CFG_CLR_R0_FULL[12:12]	1
0xBB022118	WSDS_DIG_20.CFG_R0_DIF_MIN[11:6]	6
0xBB022118	WSDS_DIG_20.CFG_R0_DIF_MAX[5:0]	6
0xBB02211C	WSDS_DIG_21.RESERVED[31:26]	6
0xBB02211C	WSDS_DIG_21.T1_FULL[25:25]	1
0xBB02211C	WSDS_DIG_21.T0_FULL[24:24]	1
0xBB02211C	WSDS_DIG_21.T1_DIF_MIN[23:18]	6
0xBB02211C	WSDS_DIG_21.T1_DIF_MAX[17:12]	6
0xBB02211C	WSDS_DIG_21.T0_DIF_MIN[11:6]	6
0xBB02211C	WSDS_DIG_21.T0_DIF_MAX[5:0]	6

Address	Register	Len
0xBB022120	WSDS_DIG_22.RESERVED[31:13]	19
0xBB022120	WSDS_DIG_22.R0_FULL[12:12]	1
0xBB022120	WSDS_DIG_22.R0_DIF_MIN[11:6]	6
0xBB022120	WSDS_DIG_22.R0_DIF_MAX[5:0]	6
0xBB022124	WSDS_DIG_23.CFG_SDSINF_DMYRD_0[31:0]	32
0xBB022128	WSDS_DIG_24.CFG_WRAP_DMYRD_0[31:0]	32
0xBB02212C	WSDS_DIG_25.CFG_WRAP_DMYRD_1[31:0]	32
0xBB022130	WSDS_DIG_26.CFG_WRAP_DMYRD_2[31:0]	32
0xBB022134	WSDS_DIG_27.CFG_WRAP_DMYRD_3[31:0]	32
0xBB022138	WSDS_DIG_28.CFG_WRAP_DMYRD_4[31:0]	32
0xBB02213C	WSDS_DIG_29.CFG_WRAP_DMY_0[31:0]	32
0xBB022140	WSDS_DIG_2A.CFG_WRAP_DMY_1[31:0]	32
0xBB022144	WSDS_DIG_2B.CFG_WRAP_DMY_2[31:0]	32
0xBB022148	WSDS_DIG_2C.CFG_WRAP_DMY_3[31:0]	32
0xBB02214C	RGF_VER_SDSREG.REGFILE_VER[31:0]	32
0xBB022150	RSVD_SDSREG [0].RSVD_MEM[31:0]	32
0xBB022154	RSVD_SDSREG [1].RSVD_MEM[31:0]	32
0xBB022158	RSVD_SDSREG [2].RSVD_MEM[31:0]	32
0xBB02215C	RSVD_SDSREG [3].RSVD_MEM[31:0]	32
0xBB022160	RSVD_SDSREG [4].RSVD_MEM[31:0]	32
0xBB022164	RSVD_SDSREG [5].RSVD_MEM[31:0]	32
0xBB022168	RSVD_SDSREG [6].RSVD_MEM[31:0]	32
0xBB02216C	RSVD_SDSREG [7].RSVD_MEM[31:0]	32
0xBB022170	RSVD_SDSREG [8].RSVD_MEM[31:0]	32
0xBB022174	RSVD_SDSREG [9].RSVD_MEM[31:0]	32
0xBB022178	RSVD_SDSREG [10].RSVD_MEM[31:0]	32
0xBB02217C	RSVD_SDSREG [11].RSVD_MEM[31:0]	32
0xBB022180	RSVD_SDSREG [12].RSVD_MEM[31:0]	32
0xBB022184	RSVD_SDSREG [13].RSVD_MEM[31:0]	32
0xBB022188	RSVD_SDSREG [14].RSVD_MEM[31:0]	32
0xBB02218C	RSVD_SDSREG [15].RSVD_MEM[31:0]	32
0xBB022800	SDS_REG0.RESERVED[31:15]	17
0xBB022800	SDS_REG0.DUMMY_00[14:14]	1
0xBB022800	SDS_REG0.BYP_8B10B[13:13]	1
0xBB022800	SDS_REG0.CDET[12:12]	1
0xBB022800	SDS_REG0.DIS_TMR_CMA[11:11]	1
0xBB022800	SDS_REG0.DUMMY_01[10:10]	1
0xBB022800	SDS_REG0.INV_HSI[9:9]	1
0xBB022800	SDS_REG0.INV_HSO[8:8]	1
0xBB022800	SDS_REG0.SDS_SDET_DEG[7:6]	2
0xBB022800	SDS_REG0.CODEC_LPK[5:5]	1
0xBB022800	SDS_REG0.AFE_LPK[4:4]	1
0xBB022800	SDS_REG0.REMOTE_LPK[3:3]	1
0xBB022800	SDS_REG0.SDS_TX_DOWN[2:2]	1
0xBB022800	SDS_REG0.SDS_EN_RX[1:1]	1
0xBB022800	SDS_REG0.SDS_EN_TX[0:0]	1

Address	Register	Len
0xBB022804	SDS_REG1.RESERVED[31:16]	16
0xBB022804	SDS_REG1.DUMMY_02[15:12]	4
0xBB022804	SDS_REG1.SDS_FRC_RX[11:8]	4
0xBB022804	SDS_REG1.DUMMY_03[7:4]	4
0xBB022804	SDS_REG1.SDS_FRC_TX[3:0]	4
0xBB022808	SDS_REG2.RESERVED[31:16]	16
0xBB022808	SDS_REG2.FRC_PRAMBLE[15:14]	2
0xBB022808	SDS_REG2.FRC_IPG[13:12]	2
0xBB022808	SDS_REG2.FRC_CGGOOD[11:10]	2
0xBB022808	SDS_REG2.SDS_FRC_AN[9:8]	2
0xBB022808	SDS_REG2.DUMMY_04[7:4]	4
0xBB022808	SDS_REG2.SDS_RESATRT_AN[3:0]	4
0xBB02280C	SDS_REG3.RESERVED[31:16]	16
0xBB02280C	SDS_REG3.WR_COFT_RSTB[15:15]	1
0xBB02280C	SDS_REG3.USE_25M_CLK[14:14]	1
0xBB02280C	SDS_REG3.MARK_CARR_EXT[13:13]	1
0xBB02280C	SDS_REG3.SEL_DEG[12:12]	1
0xBB02280C	SDS_REG3.REG_CALIB_OK_CNT[11:8]	4
0xBB02280C	SDS_REG3.EXT_PWR_CTL[7:7]	1
0xBB02280C	SDS_REG3.SOFT_RST[6:6]	1
0xBB02280C	SDS_REG3.CLR_SOFT_RSTB[5:5]	1
0xBB02280C	SDS_REG3.CMA_RQ[4:0]	5
0xBB022810	SDS_REG4.RESERVED[31:16]	16
0xBB022810	SDS_REG4.CFG_FRC_SDS_MODE[15:13]	3
0xBB022810	SDS_REG4.CFG_FRC_SDS_MODE_EN[12:12]	1
0xBB022810	SDS_REG4.CFG_UPD_RXD[11:8]	4
0xBB022810	SDS_REG4.CFG_UPD_TXD[7:4]	4
0xBB022810	SDS_REG4.CFG_UPD_RXD_DYN[3:3]	1
0xBB022810	SDS_REG4.CFG_EN_LINK_FIB1G[2:2]	1
0xBB022810	SDS_REG4.DUMMY_05[1:1]	1
0xBB022810	SDS_REG4.DUMMY_06[0:0]	1
0xBB022814	SDS_REG5.RESERVED[31:16]	16
0xBB022814	SDS_REG5.LPI_TRANSMIT_STYLE[15:15]	1
0xBB022814	SDS_REG5.DUMMY_07[14:12]	3
0xBB022814	SDS_REG5.DUMMY_08[11:11]	1
0xBB022814	SDS_REG5.DUMMY_09[10:10]	1
0xBB022814	SDS_REG5.DUMMY_0A[9:9]	1
0xBB022814	SDS_REG5.DUMMY_0B[8:8]	1
0xBB022814	SDS_REG5.DUMMY_0C[7:4]	4
0xBB022814	SDS_REG5.DUMMY_0D[3:0]	4
0xBB022818	SDS_REG6.RESERVED[31:16]	16
0xBB022818	SDS_REG6.DUMMY_0E[15:12]	4
0xBB022818	SDS_REG6.RX_BYPSRC[11:8]	4
0xBB022818	SDS_REG6.DUMMY_0F[7:4]	4
0xBB022818	SDS_REG6.TX_BYPSRC[3:0]	4
0xBB02281C	SDS_REG7.RESERVED[31:16]	16



Address	Register	Len
0xBB02281C	SDS_REG7.DUMMY_10[15:11]	5
0xBB02281C	SDS_REG7.CFG_LPI_CMD_MII[10:10]	1
0xBB02281C	SDS_REG7.CFG_MARK_RXSCR_ERR[9:9]	1
0xBB02281C	SDS_REG7.CFG_MARK_TXSCR_ERR[8:8]	1
0xBB02281C	SDS_REG7.BYP_START[7:4]	4
0xBB02281C	SDS_REG7.BYP_END[3:0]	4
0xBB022820	SDS_REG8.RESERVED[31:16]	16
0xBB022820	SDS_REG8.DUMMY_11[15:15]	1
0xBB022820	SDS_REG8.DUMMY_12[14:14]	1
0xBB022820	SDS_REG8.DUMMY_13[13:11]	3
0xBB022820	SDS_REG8.DUMMY_14[10:8]	3
0xBB022820	SDS_REG8.DUMMY_15[7:5]	3
0xBB022820	SDS_REG8.DUMMY_16[4:2]	3
0xBB022820	SDS_REG8.DUMMY_17[1:1]	1
0xBB022820	SDS_REG8.DUMMY_18[0:0]	1
0xBB022824	SDS_REG9.RESERVED[31:16]	16
0xBB022824	SDS_REG9.CFG_EEE_PROGRAM_0[15:0]	16
0xBB022828	SDS_REG10.RESERVED[31:16]	16
0xBB022828	SDS_REG10.DUMMY_19[15:0]	16
0xBB02282C	SDS_REG11.RESERVED[31:16]	16
0xBB02282C	SDS_REG11.DUMMY_1C[15:0]	16
0xBB022830	SDS_REG12.RESERVED[31:16]	16
0xBB022830	SDS_REG12.DUMMY_1D[15:8]	8
0xBB022830	SDS_REG12.ABLITY[7:4]	4
0xBB022830	SDS_REG12.DUMMY_1E[3:3]	1
0xBB022830	SDS_REG12.DUMMY_1F[2:2]	1
0xBB022830	SDS_REG12.DUMMY_20[1:1]	1
0xBB022830	SDS_REG12.SEND_NP_ON[0:0]	1
0xBB022834	SDS_REG13.RESERVED[31:16]	16
0xBB022834	SDS_REG13.DUMMY_21[15:8]	8
0xBB022834	SDS_REG13.DUMMY_22[7:0]	8
0xBB022838	SDS_REG14.RESERVED[31:16]	16
0xBB022838	SDS_REG14.CGF_SPDUP[15:15]	1
0xBB022838	SDS_REG14.DUMMY_23[14:10]	5
0xBB022838	SDS_REG14.CFG_SEL_ODD_BIT[9:9]	1
0xBB022838	SDS_REG14.CFG_FRC_LD_VALUE[8:8]	1
0xBB022838	SDS_REG14.CFG_FRC_LD[7:7]	1
0xBB022838	SDS_REG14.DUMMY_24[6:6]	1
0xBB022838	SDS_REG14.DUMMY_25[5:3]	3
0xBB022838	SDS_REG14.CFG_LINK_TMR_NORM_SEL[2:0]	3
0xBB02283C	SDS_REG15.RESERVED[31:16]	16
0xBB02283C	SDS_REG15.DUMMY_26[15:0]	16
0xBB022840	SDS_REG16.RESERVED[31:16]	16
0xBB022840	SDS_REG16.DUMMY_27[15:0]	16
0xBB022844	SDS_REG17.RESERVED[31:14]	18
0xBB022844	SDS_REG17.DUMMY_28[13:0]	14



Address	Register	Len
0xBB022848	SDS_REG18.RESERVED[31:16]	16
0xBB022848	SDS_REG18.DUMMY_29[15:0]	16
0xBB02284C	SDS_REG19.RESERVED[31:16]	16
0xBB02284C	SDS_REG19.DUMMY_2A[15:0]	16
0xBB022850	SDS_REG20.RESERVED[31:16]	16
0xBB022850	SDS_REG20.DUMMY_2B[15:0]	16
0xBB022854	SDS_REG21.RESERVED[31:16]	16
0xBB022854	SDS_REG21.DUMMY_2C[15:0]	16
0xBB022858	SDS_REG22.RESERVED[31:16]	16
0xBB022858	SDS_REG22.DUMMY_2D[15:0]	16
0xBB02285C	SDS_REG23.RESERVED[31:16]	16
0xBB02285C	SDS_REG23.DUMMY_2E[15:0]	16
0xBB022860	SDS_REG24.RESERVED[31:16]	16
0xBB022860	SDS_REG24.DUMMY_2F[15:0]	16
0xBB022864	SDS_REG25.RESERVED[31:16]	16
0xBB022864	SDS_REG25.DUMMY_30[15:0]	16
0xBB022868	SDS_REG26.RESERVED[31:16]	16
0xBB022868	SDS_REG26.CFG_DNG_OUT_ECO0[15:0]	16
0xBB02286C	SDS_REG27.RESERVED[31:16]	16
0xBB02286C	SDS_REG27.CFG_DNG_OUT_ECO1[15:0]	16
0xBB022870	SDS_REG28.RESERVED[31:16]	16
0xBB022870	SDS_REG28.DUMMY_31[15:12]	4
0xBB022870	SDS_REG28.DUMMY_32[11:11]	1
0xBB022870	SDS_REG28.DUMMY_33[10:10]	1
0xBB022870	SDS_REG28.CFG_SDS_DBG_SEL[9:0]	10
0xBB022874	SDS_REG29.CFG_SDS_DBG_OUT[31:0]	32
0xBB022878	DUMMY [0].DUMMY[31:0]	32
0xBB02287C	DUMMY [1].DUMMY[31:0]	32
0xBB022880	DUMMY [2].DUMMY[31:0]	32
0xBB022884	DUMMY [3].DUMMY[31:0]	32
0xBB022888	DUMMY [4].DUMMY[31:0]	32
0xBB02288C	DUMMY [5].DUMMY[31:0]	32
0xBB022890	DUMMY [6].DUMMY[31:0]	32
0xBB022894	DUMMY [7].DUMMY[31:0]	32
0xBB022898	DUMMY [8].DUMMY[31:0]	32
0xBB02289C	DUMMY [9].DUMMY[31:0]	32
0xBB0228A0	DUMMY [10].DUMMY[31:0]	32
0xBB0228A4	DUMMY [11].DUMMY[31:0]	32
0xBB0228A8	DUMMY [12].DUMMY[31:0]	32
0xBB0228AC	DUMMY [13].DUMMY[31:0]	32
0xBB0228B0	DUMMY [14].DUMMY[31:0]	32
0xBB0228B4	DUMMY [15].DUMMY[31:0]	32
0xBB0228B8	DUMMY [16].DUMMY[31:0]	32
0xBB0228BC	DUMMY [17].DUMMY[31:0]	32
0xBB0228C0	DUMMY [18].DUMMY[31:0]	32
0xBB0228C4	DUMMY [19].DUMMY[31:0]	32

Address	Register	Len
0xBB0228C8	DUMMY [20].DUMMY[31:0]	32
0xBB0228CC	DUMMY [21].DUMMY[31:0]	32
0xBB0228D0	DUMMY [22].DUMMY[31:0]	32
0xBB0228D4	DUMMY [23].DUMMY[31:0]	32
0xBB0228D8	DUMMY [24].DUMMY[31:0]	32
0xBB0228DC	DUMMY [25].DUMMY[31:0]	32
0xBB0228E0	DUMMY [26].DUMMY[31:0]	32
0xBB0228E4	DUMMY [27].DUMMY[31:0]	32
0xBB0228E8	DUMMY [28].DUMMY[31:0]	32
0xBB0228EC	DUMMY [29].DUMMY[31:0]	32
0xBB0228F0	DUMMY [30].DUMMY[31:0]	32
0xBB0228F4	DUMMY [31].DUMMY[31:0]	32
0xBB0228F8	DUMMY [32].DUMMY[31:0]	32
0xBB0228FC	DUMMY [33].DUMMY[31:0]	32
0xBB022900	DUMMY [34].DUMMY[31:0]	32
0xBB022904	DUMMY [35].DUMMY[31:0]	32
0xBB022908	DUMMY [36].DUMMY[31:0]	32
0xBB02290C	DUMMY [37].DUMMY[31:0]	32
0xBB022910	DUMMY [38].DUMMY[31:0]	32
0xBB022914	DUMMY [39].DUMMY[31:0]	32
0xBB022918	DUMMY [40].DUMMY[31:0]	32
0xBB02291C	DUMMY [41].DUMMY[31:0]	32
0xBB022920	DUMMY [42].DUMMY[31:0]	32
0xBB022924	DUMMY [43].DUMMY[31:0]	32
0xBB022928	DUMMY [44].DUMMY[31:0]	32
0xBB02292C	DUMMY [45].DUMMY[31:0]	32
0xBB022930	DUMMY [46].DUMMY[31:0]	32
0xBB022934	DUMMY [47].DUMMY[31:0]	32
0xBB022938	DUMMY [48].DUMMY[31:0]	32
0xBB02293C	DUMMY [49].DUMMY[31:0]	32
0xBB022940	DUMMY [50].DUMMY[31:0]	32
0xBB022944	DUMMY [51].DUMMY[31:0]	32
0xBB022948	DUMMY [52].DUMMY[31:0]	32
0xBB02294C	DUMMY [53].DUMMY[31:0]	32
0xBB022950	DUMMY [54].DUMMY[31:0]	32
0xBB022954	DUMMY [55].DUMMY[31:0]	32
0xBB022958	DUMMY [56].DUMMY[31:0]	32
0xBB02295C	DUMMY [57].DUMMY[31:0]	32
0xBB022960	DUMMY [58].DUMMY[31:0]	32
0xBB022964	DUMMY [59].DUMMY[31:0]	32
0xBB022968	DUMMY [60].DUMMY[31:0]	32
0xBB02296C	DUMMY [61].DUMMY[31:0]	32
0xBB022970	DUMMY [62].DUMMY[31:0]	32
0xBB022974	DUMMY [63].DUMMY[31:0]	32
0xBB022978	DUMMY [64].DUMMY[31:0]	32
0xBB02297C	DUMMY [65].DUMMY[31:0]	32

Address	Register	Len
0xBB022980	DUMMY [66].DUMMY[31:0]	32
0xBB022984	DUMMY [67].DUMMY[31:0]	32
0xBB022988	DUMMY [68].DUMMY[31:0]	32
0xBB02298C	DUMMY [69].DUMMY[31:0]	32
0xBB022990	DUMMY [70].DUMMY[31:0]	32
0xBB022994	DUMMY [71].DUMMY[31:0]	32
0xBB022998	DUMMY [72].DUMMY[31:0]	32
0xBB02299C	DUMMY [73].DUMMY[31:0]	32
0xBB0229A0	DUMMY [74].DUMMY[31:0]	32
0xBB0229A4	DUMMY [75].DUMMY[31:0]	32
0xBB0229A8	DUMMY [76].DUMMY[31:0]	32
0xBB0229AC	DUMMY [77].DUMMY[31:0]	32
0xBB0229B0	DUMMY [78].DUMMY[31:0]	32
0xBB0229B4	DUMMY [79].DUMMY[31:0]	32
0xBB0229B8	DUMMY [80].DUMMY[31:0]	32
0xBB0229BC	DUMMY [81].DUMMY[31:0]	32
0xBB0229C0	DUMMY [82].DUMMY[31:0]	32
0xBB0229C4	DUMMY [83].DUMMY[31:0]	32
0xBB0229C8	DUMMY [84].DUMMY[31:0]	32
0xBB0229CC	DUMMY [85].DUMMY[31:0]	32
0xBB0229D0	DUMMY [86].DUMMY[31:0]	32
0xBB0229D4	DUMMY [87].DUMMY[31:0]	32
0xBB0229D8	DUMMY [88].DUMMY[31:0]	32
0xBB0229DC	DUMMY [89].DUMMY[31:0]	32
0xBB0229E0	DUMMY [90].DUMMY[31:0]	32
0xBB0229E4	DUMMY [91].DUMMY[31:0]	32
0xBB0229E8	DUMMY [92].DUMMY[31:0]	32
0xBB0229EC	DUMMY [93].DUMMY[31:0]	32
0xBB0229F0	DUMMY [94].DUMMY[31:0]	32
0xBB0229F4	DUMMY [95].DUMMY[31:0]	32
0xBB0229F8	DUMMY [96].DUMMY[31:0]	32
0xBB0229FC	DUMMY [97].DUMMY[31:0]	32
0xBB022A00	SDS_EXT_REG0.RESERVED[31:16]	16
0xBB022A00	SDS_EXT_REG0.SDS_EXT_CFG0[15:0]	16
0xBB022A04	SDS_EXT_REG1.RESERVED[31:16]	16
0xBB022A04	SDS_EXT_REG1.SDS_EXT_CFG1[15:0]	16
0xBB022A08	SDS_EXT_REG2.RESERVED[31:16]	16
0xBB022A08	SDS_EXT_REG2.SDS_EXT_CFG2[15:0]	16
0xBB022A0C	SDS_EXT_REG3.RESERVED[31:16]	16
0xBB022A0C	SDS_EXT_REG3.SDS_EXT_CFG3[15:0]	16
0xBB022A10	SDS_EXT_REG4.RESERVED[31:16]	16
0xBB022A10	SDS_EXT_REG4.SDS_EXT_CFG4[15:0]	16
0xBB022A14	SDS_EXT_REG5.RESERVED[31:16]	16
0xBB022A14	SDS_EXT_REG5.SDS_EXT_CFG5[15:0]	16
0xBB022A18	SDS_EXT_REG6.RESERVED[31:16]	16
0xBB022A18	SDS_EXT_REG6.SDS_EXT_CFG6[15:0]	16

Address	Register	Len
0xBB022A1C	SDS_EXT_REG7.RESERVED[31:16]	16
0xBB022A1C	SDS_EXT_REG7.SDS_EXT_CFG7[15:0]	16
0xBB022A20	SDS_EXT_REG8.RESERVED[31:16]	16
0xBB022A20	SDS_EXT_REG8.SDS_EXT_CFG8[15:0]	16
0xBB022A24	SDS_EXT_REG9.RESERVED[31:16]	16
0xBB022A24	SDS_EXT_REG9.SDS_EXT_CFG9[15:0]	16
0xBB022A28	SDS_EXT_REG10.RESERVED[31:16]	16
0xBB022A28	SDS_EXT_REG10.SDS_EXT_CFG10[15:0]	16
0xBB022A2C	SDS_EXT_REG11.RESERVED[31:16]	16
0xBB022A2C	SDS_EXT_REG11.SDS_EXT_CFG11[15:0]	16
0xBB022A30	SDS_EXT_REG12.RESERVED[31:16]	16
0xBB022A30	SDS_EXT_REG12.SDS_EXT_CFG12[15:0]	16
0xBB022A34	SDS_EXT_REG13.RESERVED[31:16]	16
0xBB022A34	SDS_EXT_REG13.SDS_EXT_CFG13[15:0]	16
0xBB022A38	SDS_EXT_REG14.RESERVED[31:16]	16
0xBB022A38	SDS_EXT_REG14.SDS_EXT_CFG14[15:0]	16
0xBB022A3C	SDS_EXT_REG15.RESERVED[31:16]	16
0xBB022A3C	SDS_EXT_REG15.SDS_EXT_CFG15[15:0]	16
0xBB022A40	SDS_EXT_REG16.RESERVED[31:16]	16
0xBB022A40	SDS_EXT_REG16.SDS_EXT_CFG16[15:0]	16
0xBB022A44	SDS_EXT_REG24.RESERVED[31:16]	16
0xBB022A44	SDS_EXT_REG24.CFG_RG24X153[15:3]	13
0xBB022A44	SDS_EXT_REG24.CFG_SYMBOLERR_CNT[2:0]	3
0xBB022A48	SDS_EXT_REG25.RESERVED[31:16]	16
0xBB022A48	SDS_EXT_REG25.ALL_SYMBOLERR_CNT[15:8]	8
0xBB022A48	SDS_EXT_REG25.MUX_SYMBOLERR_CNT[7:0]	8
0xBB022A4C	SDS_EXT_REG26.RESERVED[31:16]	16
0xBB022A4C	SDS_EXT_REG26.P3_LONKDOWN_CNT[15:12]	4
0xBB022A4C	SDS_EXT_REG26.P2_LONKDOWN_CNT[11:8]	4
0xBB022A4C	SDS_EXT_REG26.P1_LONKDOWN_CNT[7:4]	4
0xBB022A4C	SDS_EXT_REG26.P0_LONKDOWN_CNT[3:0]	4
0xBB022A50	SDS_EXT_REG27.RESERVED[31:16]	16
0xBB022A50	SDS_EXT_REG27.CFG_DBG_STATUS_ECO_0[15:0]	16
0xBB022A54	SDS_EXT_REG28.RESERVED[31:16]	16
0xBB022A54	SDS_EXT_REG28.CFG_DBG_STATUS_ECO_1[15:0]	16
0xBB022A58	SDS_EXT_REG29.RESERVED[31:16]	16
0xBB022A58	SDS_EXT_REG29.CFG_DBG_STATUS_ECO_2[15:9]	7
0xBB022A58	SDS_EXT_REG29.SIGNOK_LAT[8:8]	1
0xBB022A58	SDS_EXT_REG29.LINKOK_LAT[7:4]	4
0xBB022A58	SDS_EXT_REG29.SYNOK_LAT[3:0]	4
0xBB022A5C	SDS_EXT_REG30.RESERVED[31:16]	16
0xBB022A5C	SDS_EXT_REG30.CFG_DBG_STATUS_ECO_3[15:9]	7
0xBB022A5C	SDS_EXT_REG30.SIGNOKLAT[8:8]	1
0xBB022A5C	SDS_EXT_REG30.LINKOKLAT[7:4]	4
0xBB022A5C	SDS_EXT_REG30.SYNOKLAT[3:0]	4
0xBB022A60	DUMMY [0].DUMMY[31:0]	32

Address	Register	Len
0xBB022A64	DUMMY [1].DUMMY[31:0]	32
0xBB022A68	DUMMY [2].DUMMY[31:0]	32
0xBB022A6C	DUMMY [3].DUMMY[31:0]	32
0xBB022A70	DUMMY [4].DUMMY[31:0]	32
0xBB022A74	DUMMY [5].DUMMY[31:0]	32
0xBB022A78	DUMMY [6].DUMMY[31:0]	32
0xBB022A7C	DUMMY [7].DUMMY[31:0]	32
0xBB022A80	DUMMY [8].DUMMY[31:0]	32
0xBB022A84	DUMMY [9].DUMMY[31:0]	32
0xBB022A88	DUMMY [10].DUMMY[31:0]	32
0xBB022A8C	DUMMY [11].DUMMY[31:0]	32
0xBB022A90	DUMMY [12].DUMMY[31:0]	32
0xBB022A94	DUMMY [13].DUMMY[31:0]	32
0xBB022A98	DUMMY [14].DUMMY[31:0]	32
0xBB022A9C	DUMMY [15].DUMMY[31:0]	32
0xBB022AA0	DUMMY [16].DUMMY[31:0]	32
0xBB022AA4	DUMMY [17].DUMMY[31:0]	32
0xBB022AA8	DUMMY [18].DUMMY[31:0]	32
0xBB022AAC	DUMMY [19].DUMMY[31:0]	32
0xBB022AB0	DUMMY [20].DUMMY[31:0]	32
0xBB022AB4	DUMMY [21].DUMMY[31:0]	32
0xBB022AB8	DUMMY [22].DUMMY[31:0]	32
0xBB022ABC	DUMMY [23].DUMMY[31:0]	32
0xBB022AC0	DUMMY [24].DUMMY[31:0]	32
0xBB022AC4	DUMMY [25].DUMMY[31:0]	32
0xBB022AC8	DUMMY [26].DUMMY[31:0]	32
0xBB022ACC	DUMMY [27].DUMMY[31:0]	32
0xBB022AD0	DUMMY [28].DUMMY[31:0]	32
0xBB022AD4	DUMMY [29].DUMMY[31:0]	32
0xBB022AD8	DUMMY [30].DUMMY[31:0]	32
0xBB022ADC	DUMMY [31].DUMMY[31:0]	32
0xBB022AE0	DUMMY [32].DUMMY[31:0]	32
0xBB022AE4	DUMMY [33].DUMMY[31:0]	32
0xBB022AE8	DUMMY [34].DUMMY[31:0]	32
0xBB022AEC	DUMMY [35].DUMMY[31:0]	32
0xBB022AF0	DUMMY [36].DUMMY[31:0]	32
0xBB022AF4	DUMMY [37].DUMMY[31:0]	32
0xBB022AF8	DUMMY [38].DUMMY[31:0]	32
0xBB022AFC	DUMMY [39].DUMMY[31:0]	32
0xBB022B00	DUMMY [40].DUMMY[31:0]	32
0xBB022B04	DUMMY [41].DUMMY[31:0]	32
0xBB022B08	DUMMY [42].DUMMY[31:0]	32
0xBB022B0C	DUMMY [43].DUMMY[31:0]	32
0xBB022B10	DUMMY [44].DUMMY[31:0]	32
0xBB022B14	DUMMY [45].DUMMY[31:0]	32
0xBB022B18	DUMMY [46].DUMMY[31:0]	32

Address	Register	Len
0xBB022B1C	DUMMY [47].DUMMY[31:0]	32
0xBB022B20	DUMMY [48].DUMMY[31:0]	32
0xBB022B24	DUMMY [49].DUMMY[31:0]	32
0xBB022B28	DUMMY [50].DUMMY[31:0]	32
0xBB022B2C	DUMMY [51].DUMMY[31:0]	32
0xBB022B30	DUMMY [52].DUMMY[31:0]	32
0xBB022B34	DUMMY [53].DUMMY[31:0]	32
0xBB022B38	DUMMY [54].DUMMY[31:0]	32
0xBB022B3C	DUMMY [55].DUMMY[31:0]	32
0xBB022B40	DUMMY [56].DUMMY[31:0]	32
0xBB022B44	DUMMY [57].DUMMY[31:0]	32
0xBB022B48	DUMMY [58].DUMMY[31:0]	32
0xBB022B4C	DUMMY [59].DUMMY[31:0]	32
0xBB022B50	DUMMY [60].DUMMY[31:0]	32
0xBB022B54	DUMMY [61].DUMMY[31:0]	32
0xBB022B58	DUMMY [62].DUMMY[31:0]	32
0xBB022B5C	DUMMY [63].DUMMY[31:0]	32
0xBB022B60	DUMMY [64].DUMMY[31:0]	32
0xBB022B64	DUMMY [65].DUMMY[31:0]	32
0xBB022B68	DUMMY [66].DUMMY[31:0]	32
0xBB022B6C	DUMMY [67].DUMMY[31:0]	32
0xBB022B70	DUMMY [68].DUMMY[31:0]	32
0xBB022B74	DUMMY [69].DUMMY[31:0]	32
0xBB022B78	DUMMY [70].DUMMY[31:0]	32
0xBB022B7C	DUMMY [71].DUMMY[31:0]	32
0xBB022B80	DUMMY [72].DUMMY[31:0]	32
0xBB022B84	DUMMY [73].DUMMY[31:0]	32
0xBB022B88	DUMMY [74].DUMMY[31:0]	32
0xBB022B8C	DUMMY [75].DUMMY[31:0]	32
0xBB022B90	DUMMY [76].DUMMY[31:0]	32
0xBB022B94	DUMMY [77].DUMMY[31:0]	32
0xBB022B98	DUMMY [78].DUMMY[31:0]	32
0xBB022B9C	DUMMY [79].DUMMY[31:0]	32
0xBB022BA0	DUMMY [80].DUMMY[31:0]	32
0xBB022BA4	DUMMY [81].DUMMY[31:0]	32
0xBB022BA8	DUMMY [82].DUMMY[31:0]	32
0xBB022BAC	DUMMY [83].DUMMY[31:0]	32
0xBB022BB0	DUMMY [84].DUMMY[31:0]	32
0xBB022BB4	DUMMY [85].DUMMY[31:0]	32
0xBB022BB8	DUMMY [86].DUMMY[31:0]	32
0xBB022BBC	DUMMY [87].DUMMY[31:0]	32
0xBB022BC0	DUMMY [88].DUMMY[31:0]	32
0xBB022BC4	DUMMY [89].DUMMY[31:0]	32
0xBB022BC8	DUMMY [90].DUMMY[31:0]	32
0xBB022BCC	DUMMY [91].DUMMY[31:0]	32
0xBB022BD0	DUMMY [92].DUMMY[31:0]	32

Address	Register	Len
0xBB022BD4	DUMMY [93].DUMMY[31:0]	32
0xBB022BD8	DUMMY [94].DUMMY[31:0]	32
0xBB022BDC	DUMMY [95].DUMMY[31:0]	32
0xBB022BE0	DUMMY [96].DUMMY[31:0]	32
0xBB022BE4	DUMMY [97].DUMMY[31:0]	32
0xBB022BE8	DUMMY [98].DUMMY[31:0]	32
0xBB022BEC	DUMMY [99].DUMMY[31:0]	32
0xBB022BF0	DUMMY [100].DUMMY[31:0]	32
0xBB022BF4	DUMMY [101].DUMMY[31:0]	32
0xBB022BF8	DUMMY [102].DUMMY[31:0]	32
0xBB022BFC	DUMMY [103].DUMMY[31:0]	32
0xBB022C00	FIB_REG0.RESERVED[31:16]	16
0xBB022C00	FIB_REG0.CFG_FIB_RST[15:15]	1
0xBB022C00	FIB_REG0.CFG_FIB_LPK[14:14]	1
0xBB022C00	FIB_REG0.CFG_FIB_SPD_RD_0[13:13]	1
0xBB022C00	FIB_REG0.CFG_FIB_ANEN[12:12]	1
0xBB022C00	FIB_REG0.CFG_FIB_PDOWN[11:11]	1
0xBB022C00	FIB_REG0.CFG_FIB_ISO[10:10]	1
0xBB022C00	FIB_REG0.CFG_FIB_RESTART[9:9]	1
0xBB022C00	FIB_REG0.CFG_FIB_FULLDUP[8:8]	1
0xBB022C00	FIB_REG0.RESERVED[7:7]	1
0xBB022C00	FIB_REG0.CFG_FIB_SPD_RD_1[6:6]	1
0xBB022C00	FIB_REG0.CFG_FIB_FRCTX[5:5]	1
0xBB022C00	FIB_REG0.RESERVED[4:0]	5
0xBB022C04	FIB_REG1.RESERVED[31:16]	16
0xBB022C04	FIB_REG1.CAPBILITY[15:6]	10
0xBB022C04	FIB_REG1.AN_COMPLETE[5:5]	1
0xBB022C04	FIB_REG1.R_FAULT[4:4]	1
0xBB022C04	FIB_REG1.NWAY_ABILITY[3:3]	1
0xBB022C04	FIB_REG1.LINK_STATUS[2:2]	1
0xBB022C04	FIB_REG1.JABBER_DETECT[1:1]	1
0xBB022C04	FIB_REG1.EXTENDED_CAPBILITY[0:0]	1
0xBB022C08	FIB_REG2.REALTEK_OUI[31:10]	22
0xBB022C08	FIB_REG2.MODEL_NO[9:4]	6
0xBB022C08	FIB_REG2.REVISION_NO[3:0]	4
0xBB022C0C	FIB_REG4.RESERVED[31:16]	16
0xBB022C0C	FIB_REG4.TX_CFG_REG[15:0]	16
0xBB022C10	FIB_REG5.RESERVED[31:16]	16
0xBB022C10	FIB_REG5.RX_CFG_REG[15:0]	16
0xBB022C14	FIB_REG6.RESERVED[31:3]	29
0xBB022C14	FIB_REG6.FIB_NP_EN[2:2]	1
0xBB022C14	FIB_REG6.RXPAGE[1:1]	1
0xBB022C14	FIB_REG6.RESERVED[0:0]	1
0xBB022C18	FIB_REG7.RESERVED[31:16]	16
0xBB022C18	FIB_REG7.MR_NP_TX[15:0]	16
0xBB022C1C	FIB_REG8.RESERVED[31:16]	16

Address	Register	Len
0xBB022C1C	FIB_REG8.MR_NP_TX[15:0]	16
0xBB022C20	DUMMY [0].DUMMY[31:0]	32
0xBB022C24	DUMMY [1].DUMMY[31:0]	32
0xBB022C28	DUMMY [2].DUMMY[31:0]	32
0xBB022C2C	DUMMY [3].DUMMY[31:0]	32
0xBB022C30	FIB_REG13.RESERVED[31:16]	16
0xBB022C30	FIB_REG13.INDR_FUNC[15:14]	2
0xBB022C30	FIB_REG13.DUMMY[13:5]	9
0xBB022C30	FIB_REG13.INDR_DEVAD[4:0]	5
0xBB022C34	FIB_REG14.RESERVED[31:16]	16
0xBB022C34	FIB_REG14.MMDRDBUS[15:0]	16
0xBB022C38	DUMMY.DUMMY[31:0]	32
0xBB022C3C	FIB_REG16.RESERVED[31:16]	16
0xBB022C3C	FIB_REG16.ANA_RG2X[15:0]	16
0xBB022C40	FIB_REG17.RESERVED[31:16]	16
0xBB022C40	FIB_REG17.ANA_RG3X[15:0]	16
0xBB022C44	FIB_REG18.RESERVED[31:16]	16
0xBB022C44	FIB_REG18.ANA_RG4X[15:0]	16
0xBB022C48	FIB_REG19.RESERVED[31:16]	16
0xBB022C48	FIB_REG19.ANA_RG5X[15:0]	16
0xBB022C4C	FIB_REG20.RESERVED[31:16]	16
0xBB022C4C	FIB_REG20.ANA_RG6X[15:0]	16
0xBB022C50	FIB_REG21.RESERVED[31:16]	16
0xBB022C50	FIB_REG21.ANA_RG7X[15:0]	16
0xBB022C54	FIB_REG22.RESERVED[31:16]	16
0xBB022C54	FIB_REG22.ANA_RG8X[15:0]	16
0xBB022C58	FIB_REG23.RESERVED[31:16]	16
0xBB022C58	FIB_REG23.ANA_RG9X[15:0]	16
0xBB022C5C	FIB_REG28.RESERVED[31:16]	16
0xBB022C5C	FIB_REG28.CFG_CONS1_MAX[15:12]	4
0xBB022C5C	FIB_REG28.CFG_CONS0_MAX[11:8]	4
0xBB022C5C	FIB_REG28.CFG_CNT_MIN[7:0]	8
0xBB022C60	FIB_REG29.RESERVED[31:16]	16
0xBB022C60	FIB_REG29.CFG_AUTO_DET_ON[15:15]	1
0xBB022C60	FIB_REG29.CFG_TOUT_MAX[14:9]	6
0xBB022C60	FIB_REG29.CFG_STATE_TMR[8:5]	4
0xBB022C60	FIB_REG29.CFG_TEST_TMR[4:0]	5
0xBB022C64	FIB_REG30.RESERVED[31:16]	16
0xBB022C64	FIB_REG30.CFG_RG30X1508[15:8]	8
0xBB022C64	FIB_REG30.CFG_LNK_ON_TMR[7:0]	8
0xBB022C68	DUMMY [0].DUMMY[31:0]	32
0xBB022C6C	DUMMY [1].DUMMY[31:0]	32
0xBB022C70	DUMMY [2].DUMMY[31:0]	32
0xBB022C74	DUMMY [3].DUMMY[31:0]	32
0xBB022C78	DUMMY [4].DUMMY[31:0]	32
0xBB022C7C	DUMMY [5].DUMMY[31:0]	32



Address	Register	Len
0xBB022C80	DUMMY [6].DUMMY[31:0]	32
0xBB022C84	DUMMY [7].DUMMY[31:0]	32
0xBB022C88	DUMMY [8].DUMMY[31:0]	32
0xBB022C8C	DUMMY [9].DUMMY[31:0]	32
0xBB022C90	DUMMY [10].DUMMY[31:0]	32
0xBB022C94	DUMMY [11].DUMMY[31:0]	32
0xBB022C98	DUMMY [12].DUMMY[31:0]	32
0xBB022C9C	DUMMY [13].DUMMY[31:0]	32
0xBB022CA0	DUMMY [14].DUMMY[31:0]	32
0xBB022CA4	DUMMY [15].DUMMY[31:0]	32
0xBB022CA8	DUMMY [16].DUMMY[31:0]	32
0xBB022CAC	DUMMY [17].DUMMY[31:0]	32
0xBB022CB0	DUMMY [18].DUMMY[31:0]	32
0xBB022CB4	DUMMY [19].DUMMY[31:0]	32
0xBB022CB8	DUMMY [20].DUMMY[31:0]	32
0xBB022CBC	DUMMY [21].DUMMY[31:0]	32
0xBB022CC0	DUMMY [22].DUMMY[31:0]	32
0xBB022CC4	DUMMY [23].DUMMY[31:0]	32
0xBB022CC8	DUMMY [24].DUMMY[31:0]	32
0xBB022CCC	DUMMY [25].DUMMY[31:0]	32
0xBB022CD0	DUMMY [26].DUMMY[31:0]	32
0xBB022CD4	DUMMY [27].DUMMY[31:0]	32
0xBB022CD8	DUMMY [28].DUMMY[31:0]	32
0xBB022CDC	DUMMY [29].DUMMY[31:0]	32
0xBB022CE0	DUMMY [30].DUMMY[31:0]	32
0xBB022CE4	DUMMY [31].DUMMY[31:0]	32
0xBB022CE8	DUMMY [32].DUMMY[31:0]	32
0xBB022CEC	DUMMY [33].DUMMY[31:0]	32
0xBB022CF0	DUMMY [34].DUMMY[31:0]	32
0xBB022CF4	DUMMY [35].DUMMY[31:0]	32
0xBB022CF8	DUMMY [36].DUMMY[31:0]	32
0xBB022CFC	DUMMY [37].DUMMY[31:0]	32
0xBB022D00	DUMMY [38].DUMMY[31:0]	32
0xBB022D04	DUMMY [39].DUMMY[31:0]	32
0xBB022D08	DUMMY [40].DUMMY[31:0]	32
0xBB022D0C	DUMMY [41].DUMMY[31:0]	32
0xBB022D10	DUMMY [42].DUMMY[31:0]	32
0xBB022D14	DUMMY [43].DUMMY[31:0]	32
0xBB022D18	DUMMY [44].DUMMY[31:0]	32
0xBB022D1C	DUMMY [45].DUMMY[31:0]	32
0xBB022D20	DUMMY [46].DUMMY[31:0]	32
0xBB022D24	DUMMY [47].DUMMY[31:0]	32
0xBB022D28	DUMMY [48].DUMMY[31:0]	32
0xBB022D2C	DUMMY [49].DUMMY[31:0]	32
0xBB022D30	DUMMY [50].DUMMY[31:0]	32
0xBB022D34	DUMMY [51].DUMMY[31:0]	32

Address	Register	Len
0xBB022D38	DUMMY [52].DUMMY[31:0]	32
0xBB022D3C	DUMMY [53].DUMMY[31:0]	32
0xBB022D40	DUMMY [54].DUMMY[31:0]	32
0xBB022D44	DUMMY [55].DUMMY[31:0]	32
0xBB022D48	DUMMY [56].DUMMY[31:0]	32
0xBB022D4C	DUMMY [57].DUMMY[31:0]	32
0xBB022D50	DUMMY [58].DUMMY[31:0]	32
0xBB022D54	DUMMY [59].DUMMY[31:0]	32
0xBB022D58	DUMMY [60].DUMMY[31:0]	32
0xBB022D5C	DUMMY [61].DUMMY[31:0]	32
0xBB022D60	DUMMY [62].DUMMY[31:0]	32
0xBB022D64	DUMMY [63].DUMMY[31:0]	32
0xBB022D68	DUMMY [64].DUMMY[31:0]	32
0xBB022D6C	DUMMY [65].DUMMY[31:0]	32
0xBB022D70	DUMMY [66].DUMMY[31:0]	32
0xBB022D74	DUMMY [67].DUMMY[31:0]	32
0xBB022D78	DUMMY [68].DUMMY[31:0]	32
0xBB022D7C	DUMMY [69].DUMMY[31:0]	32
0xBB022D80	DUMMY [70].DUMMY[31:0]	32
0xBB022D84	DUMMY [71].DUMMY[31:0]	32
0xBB022D88	DUMMY [72].DUMMY[31:0]	32
0xBB022D8C	DUMMY [73].DUMMY[31:0]	32
0xBB022D90	DUMMY [74].DUMMY[31:0]	32
0xBB022D94	DUMMY [75].DUMMY[31:0]	32
0xBB022D98	DUMMY [76].DUMMY[31:0]	32
0xBB022D9C	DUMMY [77].DUMMY[31:0]	32
0xBB022DA0	DUMMY [78].DUMMY[31:0]	32
0xBB022DA4	DUMMY [79].DUMMY[31:0]	32
0xBB022DA8	DUMMY [80].DUMMY[31:0]	32
0xBB022DAC	DUMMY [81].DUMMY[31:0]	32
0xBB022DB0	DUMMY [82].DUMMY[31:0]	32
0xBB022DB4	DUMMY [83].DUMMY[31:0]	32
0xBB022DB8	DUMMY [84].DUMMY[31:0]	32
0xBB022DBC	DUMMY [85].DUMMY[31:0]	32
0xBB022DC0	DUMMY [86].DUMMY[31:0]	32
0xBB022DC4	DUMMY [87].DUMMY[31:0]	32
0xBB022DC8	DUMMY [88].DUMMY[31:0]	32
0xBB022DCC	DUMMY [89].DUMMY[31:0]	32
0xBB022DD0	DUMMY [90].DUMMY[31:0]	32
0xBB022DD4	DUMMY [91].DUMMY[31:0]	32
0xBB022DD8	DUMMY [92].DUMMY[31:0]	32
0xBB022DDC	DUMMY [93].DUMMY[31:0]	32
0xBB022DE0	DUMMY [94].DUMMY[31:0]	32
0xBB022DE4	DUMMY [95].DUMMY[31:0]	32
0xBB022DE8	DUMMY [96].DUMMY[31:0]	32
0xBB022DEC	DUMMY [97].DUMMY[31:0]	32

Address	Register	Len
0xBB022DF0	DUMMY [98].DUMMY[31:0]	32
0xBB022DF4	DUMMY [99].DUMMY[31:0]	32
0xBB022DF8	DUMMY [100].DUMMY[31:0]	32
0xBB022DFC	DUMMY [101].DUMMY[31:0]	32
0xBB022E00	FIB_EXT_REG0.RESERVED[31:16]	16
0xBB022E00	FIB_EXT_REG0.CFG_FIB_RST[15:15]	1
0xBB022E00	FIB_EXT_REG0.CFG_FIB_LPK[14:14]	1
0xBB022E00	FIB_EXT_REG0.CFG_FIB_SPD_RD_0[13:13]	1
0xBB022E00	FIB_EXT_REG0.CFG_FIB_ANEN[12:12]	1
0xBB022E00	FIB_EXT_REG0.CFG_FIB_PDOWN[11:11]	1
0xBB022E00	FIB_EXT_REG0.CFG_FIB_ISO[10:10]	1
0xBB022E00	FIB_EXT_REG0.CFG_FIB_RESTART[9:9]	1
0xBB022E00	FIB_EXT_REG0.CFG_FIB_FULLDUP[8:8]	1
0xBB022E00	FIB_EXT_REG0.RESERVED[7:7]	1
0xBB022E00	FIB_EXT_REG0.CFG_FIB_SPD_RD_1[6:6]	1
0xBB022E00	FIB_EXT_REG0.CFG_FIB_FRCTX[5:5]	1
0xBB022E00	FIB_EXT_REG0.RESERVED[4:0]	5
0xBB022E04	FIB_EXT_REG1.RESERVED[31:16]	16
0xBB022E04	FIB_EXT_REG1.CAPBILITY[15:6]	10
0xBB022E04	FIB_EXT_REG1.AN_COMPLETE[5:5]	1
0xBB022E04	FIB_EXT_REG1.R_FAULT[4:4]	1
0xBB022E04	FIB_EXT_REG1.NWAY_ABILITY[3:3]	1
0xBB022E04	FIB_EXT_REG1.LINK_STATUS[2:2]	1
0xBB022E04	FIB_EXT_REG1.JABBER_DETECT[1:1]	1
0xBB022E04	FIB_EXT_REG1.EXTENDED_CAPBILITY[0:0]	1
0xBB022E08	FIB_EXT_REG2.REALTEK_OUI[31:10]	22
0xBB022E08	FIB_EXT_REG2.MODEL_NO[9:4]	6
0xBB022E08	FIB_EXT_REG2.REVISION_NO[3:0]	4
0xBB022E0C	FIB_EXT_REG4.RESERVED[31:16]	16
0xBB022E0C	FIB_EXT_REG4.TX_CFG_REG[15:0]	16
0xBB022E10	FIB_EXT_REG5.RESERVED[31:16]	16
0xBB022E10	FIB_EXT_REG5.RX_CFG_REG[15:0]	16
0xBB022E14	FIB_EXT_REG6.RESERVED[31:3]	29
0xBB022E14	FIB_EXT_REG6.FIB_NP_EN[2:2]	1
0xBB022E14	FIB_EXT_REG6.RXPAGE[1:1]	1
0xBB022E14	FIB_EXT_REG6.RESERVED[0:0]	1
0xBB022E18	FIB_EXT_REG7.RESERVED[31:16]	16
0xBB022E18	FIB_EXT_REG7.MR_NP_TX[15:0]	16
0xBB022E1C	FIB_EXT_REG8.RESERVED[31:16]	16
0xBB022E1C	FIB_EXT_REG8.MR_NP_TX[15:0]	16
0xBB022E20	DUMMY [0].DUMMY[31:0]	32
0xBB022E24	DUMMY [1].DUMMY[31:0]	32
0xBB022E28	DUMMY [2].DUMMY[31:0]	32
0xBB022E2C	DUMMY [3].DUMMY[31:0]	32
0xBB022E30	FIB_EXT_REG13.RESERVED[31:16]	16
0xBB022E30	FIB_EXT_REG13.INDR_FUNC[15:14]	2

Address	Register	Len
0xBB022E30	FIB_EXT_REG13.DUMMY[13:5]	9
0xBB022E30	FIB_EXT_REG13.INDR_DEVAD[4:0]	5
0xBB022E34	FIB_EXT_REG14.RESERVED[31:16]	16
0xBB022E34	FIB_EXT_REG14.MMDRDBUS[15:0]	16
0xBB022E38	DUMMY.DUMMY[31:0]	32
0xBB022E3C	FIB_EXT_REG16.RESERVED[31:16]	16
0xBB022E3C	FIB_EXT_REG16.ANA_RG2X[15:0]	16
0xBB022E40	FIB_EXT_REG17.RESERVED[31:16]	16
0xBB022E40	FIB_EXT_REG17.ANA_RG3X[15:0]	16
0xBB022E44	FIB_EXT_REG18.RESERVED[31:16]	16
0xBB022E44	FIB_EXT_REG18.ANA_RG4X[15:0]	16
0xBB022E48	FIB_EXT_REG19.RESERVED[31:16]	16
0xBB022E48	FIB_EXT_REG19.ANA_RG5X[15:0]	16
0xBB022E4C	FIB_EXT_REG20.RESERVED[31:16]	16
0xBB022E4C	FIB_EXT_REG20.ANA_RG6X[15:0]	16
0xBB022E50	FIB_EXT_REG21.RESERVED[31:16]	16
0xBB022E50	FIB_EXT_REG21.FIB_STS_0[15:13]	3
0xBB022E50	FIB_EXT_REG21.ANA_RG7X[12:4]	9
0xBB022E50	FIB_EXT_REG21.FIB_STS_1[3:0]	4
0xBB022E54	FIB_EXT_REG22.RESERVED[31:16]	16
0xBB022E54	FIB_EXT_REG22.ANA_RG8X[15:2]	14
0xBB022E54	FIB_EXT_REG22.FIB_STS_2[1:0]	2
0xBB022E58	FIB_EXT_REG23.RESERVED[31:16]	16
0xBB022E58	FIB_EXT_REG23.ANA_RG9X[15:0]	16
0xBB022E5C	FIB_EXT_REG24.RESERVED[31:16]	16
0xBB022E5C	FIB_EXT_REG24.ANA_RG10X[15:0]	16
0xBB022E60	FIB_EXT_REG25.RESERVED[31:16]	16
0xBB022E60	FIB_EXT_REG25.ANA_RG11[15:0]	16
0xBB022E64	FIB_EXT_REG26.RESERVED[31:16]	16
0xBB022E64	FIB_EXT_REG26.ANA_RG12[15:0]	16
0xBB022E68	FIB_EXT_REG27.RESERVED[31:16]	16
0xBB022E68	FIB_EXT_REG27.ANA_RG13[15:0]	16
0xBB022E6C	FIB_EXT_REG28.RESERVED[31:16]	16
0xBB022E6C	FIB_EXT_REG28.ANA_RG14[15:0]	16
0xBB022E70	FIB_EXT_REG29.RESERVED[31:16]	16
0xBB022E70	FIB_EXT_REG29.DBG_STS_OUT[15:0]	16
0xBB022E74	FIB_EXT_REG30.RESERVED[31:9]	23
0xBB022E74	FIB_EXT_REG30.SIGNSTAT[8:8]	1
0xBB022E74	FIB_EXT_REG30.LINKSTAT[7:4]	4
0xBB022E74	FIB_EXT_REG30.SYNCSTAT[3:0]	4
0xBB023000	DIGITAL_INTERFACE_SELECT.RESERVED[31:2]	30
0xBB023000	DIGITAL_INTERFACE_SELECT.ORG_COL[1:1]	1
0xBB023000	DIGITAL_INTERFACE_SELECT.ORG_CRS[0:0]	1
0xBB023004	I2C_CLOCK_DIV [0].RESERVED[31:19]	13
0xBB023004	I2C_CLOCK_DIV [0].I2C_DEV_ID[18:12]	7
0xBB023004	I2C_CLOCK_DIV [0].I2C_AW[11:11]	1

Address	Register	Len
0xBB023004	I2C_CLOCK_DIV [0].I2C_DW[10:10]	1
0xBB023004	I2C_CLOCK_DIV [0].I2C_CLOCK_DIV[9:0]	10
0xBB023008	I2C_CLOCK_DIV [1].RESERVED[31:19]	13
0xBB023008	I2C_CLOCK_DIV [1].I2C_DEV_ID[18:12]	7
0xBB023008	I2C_CLOCK_DIV [1].I2C_AW[11:11]	1
0xBB023008	I2C_CLOCK_DIV [1].I2C_DW[10:10]	1
0xBB023008	I2C_CLOCK_DIV [1].I2C_CLOCK_DIV[9:0]	10
0xBB02300C	REGCTRL_GLB.RESERVED[31:30]	2
0xBB02300C	REGCTRL_GLB.PHY_OCP_TOF[29:25]	5
0xBB02300C	REGCTRL_GLB.PHY_OCP_TO[24:17]	8
0xBB02300C	REGCTRL_GLB.PHY_ACK_TO[16:1]	16
0xBB02300C	REGCTRL_GLB.SMI_EN[0:0]	1
0xBB023010	IOPAD_CFG.RESERVED[31:27]	5
0xBB023010	IOPAD_CFG.RGM_DP[26:24]	3
0xBB023010	IOPAD_CFG.RGM_DN[23:21]	3
0xBB023010	IOPAD_CFG.RGM_SEL33[20:20]	1
0xBB023010	IOPAD_CFG.DRI_LED[19:19]	1
0xBB023010	IOPAD_CFG.DRI_EXCK[18:18]	1
0xBB023010	IOPAD_CFG.DRI_EXDT[17:17]	1
0xBB023010	IOPAD_CFG.DRI_IFCK[16:16]	1
0xBB023010	IOPAD_CFG.DRI_IFDT[15:15]	1
0xBB023010	IOPAD_CFG.DRI_SLIC_CHK[14:14]	1
0xBB023010	IOPAD_CFG.DRI_SLIC_DT[13:13]	1
0xBB023010	IOPAD_CFG.DRI_SPI_CHK[12:12]	1
0xBB023010	IOPAD_CFG.DRI_SPI_DT[11:11]	1
0xBB023010	IOPAD_CFG.DRI_OTH[10:10]	1
0xBB023010	IOPAD_CFG.SR_EXCK[9:9]	1
0xBB023010	IOPAD_CFG.SR_EXDT[8:8]	1
0xBB023010	IOPAD_CFG.SR_IFCK[7:7]	1
0xBB023010	IOPAD_CFG.SR_IFDT[6:6]	1
0xBB023010	IOPAD_CFG.SR_SLIC_CHK[5:5]	1
0xBB023010	IOPAD_CFG.SR_SLIC_DT[4:4]	1
0xBB023010	IOPAD_CFG.SR_LED[3:3]	1
0xBB023010	IOPAD_CFG.SR_SPI_CHK[2:2]	1
0xBB023010	IOPAD_CFG.SR_SPI_DT[1:1]	1
0xBB023010	IOPAD_CFG.SR_OTH[0:0]	1
0xBB023014	IO_LED_EN.RESERVED[31:20]	12
0xBB023014	IO_LED_EN.EXT_USBLED_EN[19:18]	2
0xBB023014	IO_LED_EN.SERI_LED_EN[17:17]	1
0xBB023014	IO_LED_EN.PARA_LED_EN[16:7]	10
0xBB023014	IO_LED_EN.EXTLED_EN[6:5]	2
0xBB023014	IO_LED_EN.PONLED_EN[4:3]	2
0xBB023014	IO_LED_EN.SATALED_EN[2:2]	1
0xBB023014	IO_LED_EN.USBLED_EN[1:0]	2
0xBB023018	IO_MODE_EN.RESERVED[31:24]	8
0xBB023018	IO_MODE_EN.PTP_IO_EN[23:23]	1

Address	Register	Len
0xBB023018	IO_MODE_EN.NFBI_EN[22:22]	1
0xBB023018	IO_MODE_EN.EXT_INTRPT_EN[21:21]	1
0xBB023018	IO_MODE_EN.OEM_EN[20:19]	2
0xBB023018	IO_MODE_EN.SLIC_PCM_EN[18:18]	1
0xBB023018	IO_MODE_EN.SLIC_SPI_EN[17:17]	1
0xBB023018	IO_MODE_EN.SLIC_ZSI_EN[16:16]	1
0xBB023018	IO_MODE_EN.SLIC_ISI_EN[15:15]	1
0xBB023018	IO_MODE_EN.I2C_EN[14:13]	2
0xBB023018	IO_MODE_EN.INTRPT_EN[12:11]	2
0xBB023018	IO_MODE_EN.MDX_M_EN[10:9]	2
0xBB023018	IO_MODE_EN.MDX_S_EN[8:8]	1
0xBB023018	IO_MODE_EN.SATA_MDC_EN[7:7]	1
0xBB023018	IO_MODE_EN.SPI_EN[6:6]	1
0xBB023018	IO_MODE_EN.UART_EN[5:3]	3
0xBB023018	IO_MODE_EN.SIO_EN[2:1]	2
0xBB023018	IO_MODE_EN.RESERVED[0:0]	1
0xBB02301C	RAM_DVS_CFG0.RESERVED[31:20]	12
0xBB02301C	RAM_DVS_CFG0.CFG_PBRAM_DVSE[19:19]	1
0xBB02301C	RAM_DVS_CFG0.CFG_PBRAM_DVS[18:15]	4
0xBB02301C	RAM_DVS_CFG0.CFG_OUTQGRAM_DVSE[14:14]	1
0xBB02301C	RAM_DVS_CFG0.CFG_OUTQGRAM_DVS[13:10]	4
0xBB02301C	RAM_DVS_CFG0.CFG_MIBRAM_DVSE[9:9]	1
0xBB02301C	RAM_DVS_CFG0.CFG_MIBRAM_DVS[8:5]	4
0xBB02301C	RAM_DVS_CFG0.CFG_L2RAM_DVSE[4:4]	1
0xBB02301C	RAM_DVS_CFG0.CFG_L2RAM_DVS[3:0]	4
0xBB023020	RAM_DVS_CFG1.RESERVED[31:20]	12
0xBB023020	RAM_DVS_CFG1.CFG_INQGRAM_DVSE[19:19]	1
0xBB023020	RAM_DVS_CFG1.CFG_INQGRAM_DVS[18:15]	4
0xBB023020	RAM_DVS_CFG1.CFG_HSARAM_DVSE[14:14]	1
0xBB023020	RAM_DVS_CFG1.CFG_HSARAM_DVS[13:10]	4
0xBB023020	RAM_DVS_CFG1.CFG_CVLANRAM_DVSE[9:9]	1
0xBB023020	RAM_DVS_CFG1.CFG_CVLANRAM_DVS[8:5]	4
0xBB023020	RAM_DVS_CFG1.CFG_ACTRAM_DVSE[4:4]	1
0xBB023020	RAM_DVS_CFG1.CFG_ACTRAM_DVS[3:0]	4
0xBB023024	RAM_DVS_CFG2.RESERVED[31:20]	12
0xBB023024	RAM_DVS_CFG2.PIRRAM_DVSE[19:19]	1
0xBB023024	RAM_DVS_CFG2.PIRRAM_DVS[18:15]	4
0xBB023024	RAM_DVS_CFG2.DBARAM_DVSE[14:14]	1
0xBB023024	RAM_DVS_CFG2.DBARAM_DVS[13:10]	4
0xBB023024	RAM_DVS_CFG2.QCNTRAM_DVSE[9:9]	1
0xBB023024	RAM_DVS_CFG2.QCNTRAM_DVS[8:5]	4
0xBB023024	RAM_DVS_CFG2.PTRRAM_DVSE[4:4]	1
0xBB023024	RAM_DVS_CFG2.PTRRAM_DVS[3:0]	4
0xBB023028	RAM_DVS_CFG3.RESERVED[31:20]	12
0xBB023028	RAM_DVS_CFG3.US_FRAGRAM_DVSE[19:19]	1
0xBB023028	RAM_DVS_CFG3.US_FRAGRAM_DVS[18:15]	4

Address	Register	Len
0xBB023028	RAM_DVS_CFG3.US_DATARAM_DVSE[14:14]	1
0xBB023028	RAM_DVS_CFG3.US_DATARAM_DVS[13:10]	4
0xBB023028	RAM_DVS_CFG3.LBRAM_DVSE[9:9]	1
0xBB023028	RAM_DVS_CFG3.LBRAM_DVS[8:5]	4
0xBB023028	RAM_DVS_CFG3.CIRRAM_DVSE[4:4]	1
0xBB023028	RAM_DVS_CFG3.CIRRAM_DVS[3:0]	4
0xBB02302C	RAM_DVS_CFG4.RESERVED[31:30]	2
0xBB02302C	RAM_DVS_CFG4.BS3_TFARP1_DVSE[29:29]	1
0xBB02302C	RAM_DVS_CFG4.BS3_TFARP1_DVS[28:25]	4
0xBB02302C	RAM_DVS_CFG4.BS3_TFARP0_DVSE[24:24]	1
0xBB02302C	RAM_DVS_CFG4.BS3_TFARP0_DVS[23:20]	4
0xBB02302C	RAM_DVS_CFG4.BS2_L4T_DVSE[19:19]	1
0xBB02302C	RAM_DVS_CFG4.BS2_L4T_DVS[18:15]	4
0xBB02302C	RAM_DVS_CFG4.BS2_ARP_DVSE[14:14]	1
0xBB02302C	RAM_DVS_CFG4.BS2_ARP_DVS[13:10]	4
0xBB02302C	RAM_DVS_CFG4.BS1_1_DVSE[9:9]	1
0xBB02302C	RAM_DVS_CFG4.BS1_1_DVS[8:5]	4
0xBB02302C	RAM_DVS_CFG4.BS1_0_DVSE[4:4]	1
0xBB02302C	RAM_DVS_CFG4.BS1_0_DVS[3:0]	4
0xBB023030	RAM_DVS_CFG5.RESERVED[31:15]	17
0xBB023030	RAM_DVS_CFG5.BS4_NB_DVSE[14:14]	1
0xBB023030	RAM_DVS_CFG5.BS4_NB_DVS[13:10]	4
0xBB023030	RAM_DVS_CFG5.BS3_TFL41_DVSE[9:9]	1
0xBB023030	RAM_DVS_CFG5.BS3_TFL41_DVS[8:5]	4
0xBB023030	RAM_DVS_CFG5.BS3_TFL40_DVSE[4:4]	1
0xBB023030	RAM_DVS_CFG5.BS3_TFL40_DVS[3:0]	4
0xBB023034	GLB_MAC_MISC.RESERVED[31:3]	29
0xBB023034	GLB_MAC_MISC.EEEP_DEFER_TXLPI[2:2]	1
0xBB023034	GLB_MAC_MISC.RX_DMA_SRC[1:1]	1
0xBB023034	GLB_MAC_MISC.RX_NEW_DMA[0:0]	1
0xBB023038	HTRAM_DVS_CFG.RESERVED[31:16]	16
0xBB023038	HTRAM_DVS_CFG.CFG_HTRAM_DVSE_3[15:15]	1
0xBB023038	HTRAM_DVS_CFG.CFG_HTRAM_DVS_3[14:12]	3
0xBB023038	HTRAM_DVS_CFG.CFG_HTRAM_DVSE_2[11:11]	1
0xBB023038	HTRAM_DVS_CFG.CFG_HTRAM_DVS_2[10:8]	3
0xBB023038	HTRAM_DVS_CFG.CFG_HTRAM_DVSE_1[7:7]	1
0xBB023038	HTRAM_DVS_CFG.CFG_HTRAM_DVS_1[6:4]	3
0xBB023038	HTRAM_DVS_CFG.CFG_HTRAM_DVSE_0[3:3]	1
0xBB023038	HTRAM_DVS_CFG.CFG_HTRAM_DVS_0[2:0]	3
0xBB02303C	HWPKT_GEN_STA.RESERVED[31:16]	16
0xBB02303C	HWPKT_GEN_STA.HWPKT_GEN_SUS[15:8]	8
0xBB02303C	HWPKT_GEN_STA.HWPKT_GEN_STATUS[7:0]	8
0xBB023040	FPGA_VER_MAC.FPGA_VER_MAC[31:0]	32
0xBB023044	MAC_CPU_TAG_CTRL.RESERVED[31:9]	23
0xBB023044	MAC_CPU_TAG_CTRL.TRAP_TAGET_INSERT_EN[8:8]	1
0xBB023044	MAC_CPU_TAG_CTRL.RESERVED[7:1]	7

Address	Register	Len
0xBB023044	MAC_CPU_TAG_CTRL.TAG_FORMAT[0:0]	1
0xBB023048	MAC_CPU_TAG_AWARE_CTRL [0].EN[0:0]	1
0xBB023048	MAC_CPU_TAG_AWARE_CTRL [1].EN[1:1]	1
0xBB023048	MAC_CPU_TAG_AWARE_CTRL [2].EN[2:2]	1
0xBB023048	MAC_CPU_TAG_AWARE_CTRL [3].EN[3:3]	1
0xBB023048	MAC_CPU_TAG_AWARE_CTRL [4].EN[4:4]	1
0xBB023048	MAC_CPU_TAG_AWARE_CTRL [5].EN[5:5]	1
0xBB023048	MAC_CPU_TAG_AWARE_CTRL [6].EN[6:6]	1
0xBB02304C	MAX_LENGTH_CFG0.RESERVED[31:14]	18
0xBB02304C	MAX_LENGTH_CFG0.ACCEPT_MAX_LENGTH_CFG0[13:0]	14
0xBB023050	MAX_LENGTH_LIMINT_IPG.RESERVED[31:14]	18
0xBB023050	MAX_LENGTH_LIMINT_IPG.PAGES_BEFORE_FCDROP[13:6]	8
0xBB023050	MAX_LENGTH_LIMINT_IPG.CHECK_MIN_IPG_RXDV[5:5]	1
0xBB023050	MAX_LENGTH_LIMINT_IPG.LIMIT_IPG_CFG[4:0]	5
0xBB023054	IOL_RXDROP_CFG.RESERVED[31:9]	23
0xBB023054	IOL_RXDROP_CFG.RX_IOL_MAX_LENGTH_CFG[8:8]	1
0xBB023054	IOL_RXDROP_CFG.RX_IOL_ERROR_LENGTH_CFG[7:7]	1
0xBB023054	IOL_RXDROP_CFG.RX_NODROP_PAUSE_CFG[6:6]	1
0xBB023054	IOL_RXDROP_CFG.RX_DV_CNT_CFG[5:0]	6
0xBB023058	CFG_BACKPRESSURE.RESERVED[31:4]	28
0xBB023058	CFG_BACKPRESSURE.LONGTXE[3:3]	1
0xBB023058	CFG_BACKPRESSURE.EN_BYPASS_ERROR[2:2]	1
0xBB023058	CFG_BACKPRESSURE.EN_BACKPRESSURE[1:1]	1
0xBB023058	CFG_BACKPRESSURE.EN_48_PASS_1[0:0]	1
0xBB02305C	CFG_UNHIOL.RESERVED[31:10]	22
0xBB02305C	CFG_UNHIOL.DIS_ITFSP_OP[9:9]	1
0xBB02305C	CFG_UNHIOL.DIS_SKIP_FP[8:8]	1
0xBB02305C	CFG_UNHIOL.ITFSP_REG[7:5]	3
0xBB02305C	CFG_UNHIOL.IOL_16DROP[4:4]	1
0xBB02305C	CFG_UNHIOL.IOL_BACKOFF[3:3]	1
0xBB02305C	CFG_UNHIOL.BACKOFF_RANDOM_TIME[2:2]	1
0xBB02305C	CFG_UNHIOL.DISABLE_BACK_OFF[1:1]	1
0xBB02305C	CFG_UNHIOL.IPG_COMPENSATION[0:0]	1
0xBB023060	SWITCH_MAC.RESERVED[31:16]	16
0xBB023060	SWITCH_MAC.SWITCH_MAC5[15:8]	8
0xBB023060	SWITCH_MAC.SWITCH_MAC4[7:0]	8
0xBB023064	SWITCH_MAC.SWITCH_MAC3[31:24]	8
0xBB023064	SWITCH_MAC.SWITCH_MAC2[23:16]	8
0xBB023064	SWITCH_MAC.SWITCH_MAC1[15:8]	8
0xBB023064	SWITCH_MAC.SWITCH_MAC0[7:0]	8
0xBB023068	SWITCH_CTRL.RESERVED[31:2]	30
0xBB023068	SWITCH_CTRL.SHORT_IPG[1:1]	1
0xBB023068	SWITCH_CTRL.PAUSE_MAX128[0:0]	1
0xBB02306C	INBW_BOUND.RESERVED[31:8]	24
0xBB02306C	INBW_BOUND.HBOUND[7:4]	4
0xBB02306C	INBW_BOUND.LBOUND[3:0]	4



Address	Register	Len
0xBB023070	MAX_FIFO_SIZE.RESERVED[31:4]	28
0xBB023070	MAX_FIFO_SIZE.MAX_FIFO_SIZE[3:0]	4
0xBB023074	EEE_TX_THR_GIGA.RESERVED[31:16]	16
0xBB023074	EEE_TX_THR_GIGA.TX_RATE_EEE_GIGA[15:0]	16
0xBB023078	EEE_TX_THR_FE.RESERVED[31:16]	16
0xBB023078	EEE_TX_THR_FE.TX_RATE_EEE_100M[15:0]	16
0xBB02307C	EEE_RX_FC_REG.RESERVED[31:11]	21
0xBB02307C	EEE_RX_FC_REG.EEE_HALF_DUP_EN[10:10]	1
0xBB02307C	EEE_RX_FC_REG.RX_PGCNT[9:0]	10
0xBB023080	EEE_MISC.RESERVED[31:8]	24
0xBB023080	EEE_MISC.EEE_REQ_SET1[7:7]	1
0xBB023080	EEE_MISC.EEE_REQ_SET0[6:6]	1
0xBB023080	EEE_MISC.EEE_WAKE_SET1[5:5]	1
0xBB023080	EEE_MISC.EEE_WAKE_SET0[4:4]	1
0xBB023080	EEE_MISC.EEE_TU_GIGA[3:2]	2
0xBB023080	EEE_MISC.EEE_TU_100M[1:0]	2
0xBB023084	EEE_GIGA_CTRL0.RESERVED[31:24]	8
0xBB023084	EEE_GIGA_CTRL0.EEE_TW_500M[23:16]	8
0xBB023084	EEE_GIGA_CTRL0.EEE_TW_GIGA[15:8]	8
0xBB023084	EEE_GIGA_CTRL0.EEE_TR_GIGA[7:0]	8
0xBB023088	EEE_GIGA_CTRL1.RESERVED[31:16]	16
0xBB023088	EEE_GIGA_CTRL1.EEE_TD_GIGA[15:8]	8
0xBB023088	EEE_GIGA_CTRL1.EEE_TP_GIGA[7:0]	8
0xBB02308C	EEE_100M_CTRL0.RESERVED[31:16]	16
0xBB02308C	EEE_100M_CTRL0.EEE_TW_100M[15:8]	8
0xBB02308C	EEE_100M_CTRL0.EEE_TR_100M[7:0]	8
0xBB023090	EEE_100M_CTRL1.RESERVED[31:16]	16
0xBB023090	EEE_100M_CTRL1.EEE_TD_100M[15:8]	8
0xBB023090	EEE_100M_CTRL1.EEE_TP_100M[7:0]	8
0xBB023094	EEE_BURSTSIZE.RESERVED[31:16]	16
0xBB023094	EEE_BURSTSIZE.EEE_BURSTSIZE[15:0]	16
0xBB023098	EEE_IFG_CFG.RESERVED[31:1]	31
0xBB023098	EEE_IFG_CFG.EEE_INC_IFG[0:0]	1
0xBB02309C	EEE_RXIDLE.RESERVED[31:18]	14
0xBB02309C	EEE_RXIDLE.WAIT_RX_IDLE_GELITE[17:17]	1
0xBB02309C	EEE_RXIDLE.WAIT_RX_IDLE_GE[16:16]	1
0xBB02309C	EEE_RXIDLE.WAIT_RX_IDLE_TIMER_GELITE[15:8]	8
0xBB02309C	EEE_RXIDLE.WAIT_RX_IDLE_TIMER_GE[7:0]	8
0xBB0230A0	EEE_DECISION_WINDOW.RESERVED[31:24]	8
0xBB0230A0	EEE_DECISION_WINDOW.EEE_DECISION_WINDOW_100M[23:16]	8
0xBB0230A0	EEE_DECISION_WINDOW.EEE_DECISION_WINDOW_500M[15:8]	8
0xBB0230A0	EEE_DECISION_WINDOW.EEE_DECISION_WINDOW_GE[7:0]	8
0xBB0230A4	PS_LINKID_GATCLK_CTRL.RESERVED[31:6]	26
0xBB0230A4	PS_LINKID_GATCLK_CTRL.LINKID_TIME[5:4]	2
0xBB0230A4	PS_LINKID_GATCLK_CTRL.RESERVED[3:0]	4
0xBB0230A8	EEEP_CFG.RESERVED[31:4]	28

Address	Register	Len
0xBB0230A8	EEEE_CFG.EEEP_SLAVE_EN[3:3]	1
0xBB0230A8	EEEE_CFG.EEEP_100M[2:2]	1
0xBB0230A8	EEEE_CFG.EEEP_500M[1:1]	1
0xBB0230A8	EEEE_CFG.EEEP_GIGA[0:0]	1
0xBB0230AC	EEEE_TIMER_UNIT_CTRL.RESERVED[31:6]	26
0xBB0230AC	EEEE_TIMER_UNIT_CTRL.TIMER_UNIT_GIGA[5:4]	2
0xBB0230AC	EEEE_TIMER_UNIT_CTRL.TIMER_UNIT_500M[3:2]	2
0xBB0230AC	EEEE_TIMER_UNIT_CTRL.TIMER_UNIT_100M[1:0]	2
0xBB0230B0	EEEE_TX_TIMER_GIGA_CTRL.RESERVED[31:16]	16
0xBB0230B0	EEEE_TX_TIMER_GIGA_CTRL.TX_IDLE_TIMER_GIGA[15:8]	8
0xBB0230B0	EEEE_TX_TIMER_GIGA_CTRL.TX_WAKE_TIMER_GIGA[7:0]	8
0xBB0230B4	EEEE_TX_TIMER_500M_CTRL.RESERVED[31:16]	16
0xBB0230B4	EEEE_TX_TIMER_500M_CTRL.TX_IDLE_TIMER_500M[15:8]	8
0xBB0230B4	EEEE_TX_TIMER_500M_CTRL.TX_WAKE_TIMER_500M[7:0]	8
0xBB0230B8	EEEE_TX_TIMER_100M_CTRL.RESERVED[31:16]	16
0xBB0230B8	EEEE_TX_TIMER_100M_CTRL.TX_IDLE_TIMER_100M[15:8]	8
0xBB0230B8	EEEE_TX_TIMER_100M_CTRL.TX_WAKE_TIMER_100M[7:0]	8
0xBB0230BC	EEEE_TX_GIGA_CTRL.RESERVED[31:25]	7
0xBB0230BC	EEEE_TX_GIGA_CTRL.TX_RATE_THR_GIGA[24:9]	16
0xBB0230BC	EEEE_TX_GIGA_CTRL.TX_RATE_TIMER_GIGA[8:1]	8
0xBB0230BC	EEEE_TX_GIGA_CTRL.TX_RATE_EN_GIGA[0:0]	1
0xBB0230C0	EEEE_TX_500M_CTRL.RESERVED[31:25]	7
0xBB0230C0	EEEE_TX_500M_CTRL.TX_RATE_THR_500M[24:9]	16
0xBB0230C0	EEEE_TX_500M_CTRL.TX_RATE_TIMER_500M[8:1]	8
0xBB0230C0	EEEE_TX_500M_CTRL.TX_RATE_EN_500M[0:0]	1
0xBB0230C4	EEEE_TX_100M_CTRL.RESERVED[31:25]	7
0xBB0230C4	EEEE_TX_100M_CTRL.TX_RATE_THR_100M[24:9]	16
0xBB0230C4	EEEE_TX_100M_CTRL.TX_RATE_TIMER_100M[8:1]	8
0xBB0230C4	EEEE_TX_100M_CTRL.TX_RATE_EN_100M[0:0]	1
0xBB0230C8	EEEE_RX_RATE_GIGA_CTRL.RESERVED[31:24]	8
0xBB0230C8	EEEE_RX_RATE_GIGA_CTRL.RX_RATE_THR_GIGA[23:8]	16
0xBB0230C8	EEEE_RX_RATE_GIGA_CTRL.RX_RATE_TIMER_GIGA[7:0]	8
0xBB0230CC	EEEE_RX_RATE_500M_CTRL.RESERVED[31:24]	8
0xBB0230CC	EEEE_RX_RATE_500M_CTRL.RX_RATE_THR_500M[23:8]	16
0xBB0230CC	EEEE_RX_RATE_500M_CTRL.RX_RATE_TIMER_500M[7:0]	8
0xBB0230D0	EEEE_RX_RATE_100M_CTRL.RESERVED[31:24]	8
0xBB0230D0	EEEE_RX_RATE_100M_CTRL.RX_RATE_THR_100M[23:8]	16
0xBB0230D0	EEEE_RX_RATE_100M_CTRL.RX_RATE_TIMER_100M[7:0]	8
0xBB0230D4	EEEE_RX_SLEEP_STEP_CTRL.RESERVED[31:16]	16
0xBB0230D4	EEEE_RX_SLEEP_STEP_CTRL.RX_SLEEP_STEP_CURRENT[15:8]	8
0xBB0230D4	EEEE_RX_SLEEP_STEP_CTRL.RX_SLEEP_STEP_MAX[7:0]	8
0xBB0230D8	EEEE_RX_WAKE_TIMER_GIGA_CTRL.RESERVED[31:16]	16
0xBB0230D8	EEEE_RX_WAKE_TIMER_GIGA_CTRL.RX_WAKE_TIMER_GIGA_MASTER[15:8]	8
0xBB0230D8	EEEE_RX_WAKE_TIMER_GIGA_CTRL.RX_WAKE_TIMER_GIGA_SLAVE[7:0]	8
0xBB0230DC	EEEE_RX_TIMER_GIGA_CTRL.RX_IDLE_TIMER_GIGA[31:24]	8
0xBB0230DC	EEEE_RX_TIMER_GIGA_CTRL.RX_MIN_SLEEP_TIMER_GIGA[23:16]	8

Address	Register	Len
0xBB0230DC	EEEP_RX_TIMER_GIGA_CTRL.RX_SLEEP_TIMER_GIGA[15:8]	8
0xBB0230DC	EEEP_RX_TIMER_GIGA_CTRL.RX_PAUSE_ON_TIMER_GIGA[7:0]	8
0xBB0230E0	EEEP_RX_WAKE_TIMER_500M_CTRL.RESERVED[31:16]	16
0xBB0230E0	EEEP_RX_WAKE_TIMER_500M_CTRL.RX_WAKE_TIMER_500M_MASTER[15:8]	8
0xBB0230E0	EEEP_RX_WAKE_TIMER_500M_CTRL.RX_WAKE_TIMER_500M_SLAVE[7:0]	8
0xBB0230E4	EEEP_RX_TIMER_500M_CTRL.RX_IDLE_TIMER_500M[31:24]	8
0xBB0230E4	EEEP_RX_TIMER_500M_CTRL.RX_MIN_SLEEP_TIMER_500M[23:16]	8
0xBB0230E4	EEEP_RX_TIMER_500M_CTRL.RX_SLEEP_TIMER_500M[15:8]	8
0xBB0230E4	EEEP_RX_TIMER_500M_CTRL.RX_PAUSE_ON_TIMER_500M[7:0]	8
0xBB0230E8	EEEP_RX_WAKE_TIMER_100M_CTRL.RESERVED[31:8]	24
0xBB0230E8	EEEP_RX_WAKE_TIMER_100M_CTRL.RX_WAKE_TIMER_100M[7:0]	8
0xBB0230EC	EEEP_RX_TIMER_100M_CTRL.RX_IDLE_TIMER_100M[31:24]	8
0xBB0230EC	EEEP_RX_TIMER_100M_CTRL.RX_MIN_SLEEP_TIMER_100M[23:16]	8
0xBB0230EC	EEEP_RX_TIMER_100M_CTRL.RX_SLEEP_TIMER_100M[15:8]	8
0xBB0230EC	EEEP_RX_TIMER_100M_CTRL.RX_PAUSE_ON_TIMER_100M[7:0]	8
0xBB0230F0	SVLAN_UPLINK_PMSK [0].EN[0:0]	1
0xBB0230F0	SVLAN_UPLINK_PMSK [1].EN[1:1]	1
0xBB0230F0	SVLAN_UPLINK_PMSK [2].EN[2:2]	1
0xBB0230F0	SVLAN_UPLINK_PMSK [3].EN[3:3]	1
0xBB0230F0	SVLAN_UPLINK_PMSK [4].EN[4:4]	1
0xBB0230F0	SVLAN_UPLINK_PMSK [5].EN[5:5]	1
0xBB0230F0	SVLAN_UPLINK_PMSK [6].EN[6:6]	1
0xBB0230F4	SVLAN_LOOK_UP_TYPE.RESERVED[31:7]	25
0xBB0230F4	SVLAN_LOOK_UP_TYPE.TYPE[6:0]	7
0xBB0230F8	SVLAN_CFG.RESERVED[31:16]	16
0xBB0230F8	SVLAN_CFG.VS_TPID[15:0]	16
0xBB0230FC	MIR_CTRL.RESERVED[31:13]	19
0xBB0230FC	MIR_CTRL.MIR_SRC_PMSK[12:6]	7
0xBB0230FC	MIR_CTRL.MIR_ISO[5:5]	1
0xBB0230FC	MIR_CTRL.MIR_TX[4:4]	1
0xBB0230FC	MIR_CTRL.MIR_RX[3:3]	1
0xBB0230FC	MIR_CTRL.MIR_MONITOR_PORT[2:0]	3
0xBB023100	FC_CTRL.RESERVED[31:4]	28
0xBB023100	FC_CTRL.FC_JUMBO_SIZE[3:2]	2
0xBB023100	FC_CTRL.FC_JUMBO_MODE[1:1]	1
0xBB023100	FC_CTRL.FC_TYPE[0:0]	1
0xBB023104	FC_DROP_ALL_TH.RESERVED[31:13]	19
0xBB023104	FC_DROP_ALL_TH.TH[12:0]	13
0xBB023108	FC_PAUSE_ALL_TH.RESERVED[31:13]	19
0xBB023108	FC_PAUSE_ALL_TH.TH[12:0]	13
0xBB02310C	FC_GLB_FCOFF_HI_TH.RESERVED[31:29]	3
0xBB02310C	FC_GLB_FCOFF_HI_TH.ON_TH[28:16]	13
0xBB02310C	FC_GLB_FCOFF_HI_TH.RESERVED[15:13]	3
0xBB02310C	FC_GLB_FCOFF_HI_TH.OFF_TH[12:0]	13
0xBB023110	FC_GLB_FCOFF_LO_TH.RESERVED[31:29]	3
0xBB023110	FC_GLB_FCOFF_LO_TH.ON_TH[28:16]	13

Address	Register	Len
0xBB023110	FC_GLB_FCOFF_LO_TH.RESERVED[15:13]	3
0xBB023110	FC_GLB_FCOFF_LO_TH.OFF_TH[12:0]	13
0xBB023114	FC_GLB_HI_TH.RESERVED[31:29]	3
0xBB023114	FC_GLB_HI_TH.ON_TH[28:16]	13
0xBB023114	FC_GLB_HI_TH.RESERVED[15:13]	3
0xBB023114	FC_GLB_HI_TH.OFF_TH[12:0]	13
0xBB023118	FC_GLB_LO_TH.RESERVED[31:29]	3
0xBB023118	FC_GLB_LO_TH.ON_TH[28:16]	13
0xBB023118	FC_GLB_LO_TH.RESERVED[15:13]	3
0xBB023118	FC_GLB_LO_TH.OFF_TH[12:0]	13
0xBB02311C	FC_P_HI_TH.RESERVED[31:29]	3
0xBB02311C	FC_P_HI_TH.ON_TH[28:16]	13
0xBB02311C	FC_P_HI_TH.RESERVED[15:13]	3
0xBB02311C	FC_P_HI_TH.OFF_TH[12:0]	13
0xBB023120	FC_P_LO_TH.RESERVED[31:29]	3
0xBB023120	FC_P_LO_TH.ON_TH[28:16]	13
0xBB023120	FC_P_LO_TH.RESERVED[15:13]	3
0xBB023120	FC_P_LO_TH.OFF_TH[12:0]	13
0xBB023124	FC_P_FCOFF_HI_TH.RESERVED[31:29]	3
0xBB023124	FC_P_FCOFF_HI_TH.ON_TH[28:16]	13
0xBB023124	FC_P_FCOFF_HI_TH.RESERVED[15:13]	3
0xBB023124	FC_P_FCOFF_HI_TH.OFF_TH[12:0]	13
0xBB023128	FC_P_FCOFF_LO_TH.RESERVED[31:29]	3
0xBB023128	FC_P_FCOFF_LO_TH.ON_TH[28:16]	13
0xBB023128	FC_P_FCOFF_LO_TH.RESERVED[15:13]	3
0xBB023128	FC_P_FCOFF_LO_TH.OFF_TH[12:0]	13
0xBB02312C	FC_JUMBO_GLB_HI_TH.RESERVED[31:29]	3
0xBB02312C	FC_JUMBO_GLB_HI_TH.ON_TH[28:16]	13
0xBB02312C	FC_JUMBO_GLB_HI_TH.RESERVED[15:13]	3
0xBB02312C	FC_JUMBO_GLB_HI_TH.OFF_TH[12:0]	13
0xBB023130	FC_JUMBO_GLB_LO_TH.RESERVED[31:29]	3
0xBB023130	FC_JUMBO_GLB_LO_TH.ON_TH[28:16]	13
0xBB023130	FC_JUMBO_GLB_LO_TH.RESERVED[15:13]	3
0xBB023130	FC_JUMBO_GLB_LO_TH.OFF_TH[12:0]	13
0xBB023134	FC_JUMBO_P_HI_TH.RESERVED[31:29]	3
0xBB023134	FC_JUMBO_P_HI_TH.ON_TH[28:16]	13
0xBB023134	FC_JUMBO_P_HI_TH.RESERVED[15:13]	3
0xBB023134	FC_JUMBO_P_HI_TH.OFF_TH[12:0]	13
0xBB023138	FC_JUMBO_P_LO_TH.RESERVED[31:29]	3
0xBB023138	FC_JUMBO_P_LO_TH.ON_TH[28:16]	13
0xBB023138	FC_JUMBO_P_LO_TH.RESERVED[15:13]	3
0xBB023138	FC_JUMBO_P_LO_TH.OFF_TH[12:0]	13
0xBB02313C	CLR_MAX_USED_PAGE_CNT.RESERVED[31:1]	31
0xBB02313C	CLR_MAX_USED_PAGE_CNT.CLR_MAX_USED_PAGE_CNT[0:0]	1
0xBB023140	FC_TL_USED_PAGE_CNT.RESERVED[31:29]	3
0xBB023140	FC_TL_USED_PAGE_CNT.TL_MAX_USED_PAGE_CNT[28:16]	13

Address	Register	Len
0xBB023140	FC_TL_USED_PAGE_CNT.RESERVED[15:13]	3
0xBB023140	FC_TL_USED_PAGE_CNT.TL_USED_PAGE_CNT[12:0]	13
0xBB023144	FC_PUB_USED_PAGE_CNT.RESERVED[31:29]	3
0xBB023144	FC_PUB_USED_PAGE_CNT.PUB_MAX_USED_PAGE_CNT[28:16]	13
0xBB023144	FC_PUB_USED_PAGE_CNT.RESERVED[15:13]	3
0xBB023144	FC_PUB_USED_PAGE_CNT.PUB_USED_PAGE_CNT[12:0]	13
0xBB023148	FC_PUB_FCOFF_USED_PAGE_CNT.RESERVED[31:29]	3
0xBB023148	FC_PUB_FCOFF_USED_PAGE_CNT.PUB_FCOFF_MAX_USED_PAGE_CNT[28:16]	13
0xBB023148	FC_PUB_FCOFF_USED_PAGE_CNT.RESERVED[15:13]	3
0xBB023148	FC_PUB_FCOFF_USED_PAGE_CNT.PUB_FCOFF_USED_PAGE_CNT[12:0]	13
0xBB02314C	FC_PUB_JUMBO_USED_PAGE_CNT.RESERVED[31:29]	3
0xBB02314C	FC_PUB_JUMBO_USED_PAGE_CNT.PUB_JUMBO_MAX_USED_PAGE_CNT[28:16]	13
0xBB02314C	FC_PUB_JUMBO_USED_PAGE_CNT.RESERVED[15:13]	3
0xBB02314C	FC_PUB_JUMBO_USED_PAGE_CNT.PUB_JUMBO_USED_PAGE_CNT[12:0]	13
0xBB023150	FC_P_USED_PAGE_CNT [0].RESERVED[31:29]	3
0xBB023150	FC_P_USED_PAGE_CNT [0].P_MAX_USED_PAGE_CNT[28:16]	13
0xBB023150	FC_P_USED_PAGE_CNT [0].RESERVED[15:13]	3
0xBB023150	FC_P_USED_PAGE_CNT [0].P_USED_PAGE_CNT[12:0]	13
0xBB023154	FC_P_USED_PAGE_CNT [1].RESERVED[31:29]	3
0xBB023154	FC_P_USED_PAGE_CNT [1].P_MAX_USED_PAGE_CNT[28:16]	13
0xBB023154	FC_P_USED_PAGE_CNT [1].RESERVED[15:13]	3
0xBB023154	FC_P_USED_PAGE_CNT [1].P_USED_PAGE_CNT[12:0]	13
0xBB023158	FC_P_USED_PAGE_CNT [2].RESERVED[31:29]	3
0xBB023158	FC_P_USED_PAGE_CNT [2].P_MAX_USED_PAGE_CNT[28:16]	13
0xBB023158	FC_P_USED_PAGE_CNT [2].RESERVED[15:13]	3
0xBB023158	FC_P_USED_PAGE_CNT [2].P_USED_PAGE_CNT[12:0]	13
0xBB02315C	FC_P_USED_PAGE_CNT [3].RESERVED[31:29]	3
0xBB02315C	FC_P_USED_PAGE_CNT [3].P_MAX_USED_PAGE_CNT[28:16]	13
0xBB02315C	FC_P_USED_PAGE_CNT [3].RESERVED[15:13]	3
0xBB02315C	FC_P_USED_PAGE_CNT [3].P_USED_PAGE_CNT[12:0]	13
0xBB023160	FC_P_USED_PAGE_CNT [4].RESERVED[31:29]	3
0xBB023160	FC_P_USED_PAGE_CNT [4].P_MAX_USED_PAGE_CNT[28:16]	13
0xBB023160	FC_P_USED_PAGE_CNT [4].RESERVED[15:13]	3
0xBB023160	FC_P_USED_PAGE_CNT [4].P_USED_PAGE_CNT[12:0]	13
0xBB023164	FC_P_USED_PAGE_CNT [5].RESERVED[31:29]	3
0xBB023164	FC_P_USED_PAGE_CNT [5].P_MAX_USED_PAGE_CNT[28:16]	13
0xBB023164	FC_P_USED_PAGE_CNT [5].RESERVED[15:13]	3
0xBB023164	FC_P_USED_PAGE_CNT [5].P_USED_PAGE_CNT[12:0]	13
0xBB023168	FC_P_USED_PAGE_CNT [6].RESERVED[31:29]	3
0xBB023168	FC_P_USED_PAGE_CNT [6].P_MAX_USED_PAGE_CNT[28:16]	13
0xBB023168	FC_P_USED_PAGE_CNT [6].RESERVED[15:13]	3
0xBB023168	FC_P_USED_PAGE_CNT [6].P_USED_PAGE_CNT[12:0]	13
0xBB02316C	FC_PON_GLB_HI_TH.RESERVED[31:29]	3
0xBB02316C	FC_PON_GLB_HI_TH.ON_TH[28:16]	13
0xBB02316C	FC_PON_GLB_HI_TH.RESERVED[15:13]	3
0xBB02316C	FC_PON_GLB_HI_TH.OFF_TH[12:0]	13

Address	Register	Len
0xBB023170	FC_PON_GLB_LO_TH.RESERVED[31:29]	3
0xBB023170	FC_PON_GLB_LO_TH.ON_TH[28:16]	13
0xBB023170	FC_PON_GLB_LO_TH.RESERVED[15:13]	3
0xBB023170	FC_PON_GLB_LO_TH.OFF_TH[12:0]	13
0xBB023174	FC_PON_P_HI_TH.RESERVED[31:29]	3
0xBB023174	FC_PON_P_HI_TH.ON_TH[28:16]	13
0xBB023174	FC_PON_P_HI_TH.RESERVED[15:13]	3
0xBB023174	FC_PON_P_HI_TH.OFF_TH[12:0]	13
0xBB023178	FC_PON_P_LO_TH.RESERVED[31:29]	3
0xBB023178	FC_PON_P_LO_TH.ON_TH[28:16]	13
0xBB023178	FC_PON_P_LO_TH.RESERVED[15:13]	3
0xBB023178	FC_PON_P_LO_TH.OFF_TH[12:0]	13
0xBB02317C	FC_PON_Q_EGR_DROP_IDX [0].IDX[2:0]	3
0xBB02317C	FC_PON_Q_EGR_DROP_IDX [1].IDX[5:3]	3
0xBB02317C	FC_PON_Q_EGR_DROP_IDX [2].IDX[8:6]	3
0xBB02317C	FC_PON_Q_EGR_DROP_IDX [3].IDX[11:9]	3
0xBB02317C	FC_PON_Q_EGR_DROP_IDX [4].IDX[14:12]	3
0xBB02317C	FC_PON_Q_EGR_DROP_IDX [5].IDX[17:15]	3
0xBB02317C	FC_PON_Q_EGR_DROP_IDX [6].IDX[20:18]	3
0xBB02317C	FC_PON_Q_EGR_DROP_IDX [7].IDX[23:21]	3
0xBB02317C	FC_PON_Q_EGR_DROP_IDX [8].IDX[26:24]	3
0xBB02317C	FC_PON_Q_EGR_DROP_IDX [9].IDX[29:27]	3
0xBB023180	FC_PON_Q_EGR_DROP_IDX [10].IDX[2:0]	3
0xBB023180	FC_PON_Q_EGR_DROP_IDX [11].IDX[5:3]	3
0xBB023180	FC_PON_Q_EGR_DROP_IDX [12].IDX[8:6]	3
0xBB023180	FC_PON_Q_EGR_DROP_IDX [13].IDX[11:9]	3
0xBB023180	FC_PON_Q_EGR_DROP_IDX [14].IDX[14:12]	3
0xBB023180	FC_PON_Q_EGR_DROP_IDX [15].IDX[17:15]	3
0xBB023180	FC_PON_Q_EGR_DROP_IDX [16].IDX[20:18]	3
0xBB023180	FC_PON_Q_EGR_DROP_IDX [17].IDX[23:21]	3
0xBB023180	FC_PON_Q_EGR_DROP_IDX [18].IDX[26:24]	3
0xBB023180	FC_PON_Q_EGR_DROP_IDX [19].IDX[29:27]	3
0xBB023184	FC_PON_Q_EGR_DROP_IDX [20].IDX[2:0]	3
0xBB023184	FC_PON_Q_EGR_DROP_IDX [21].IDX[5:3]	3
0xBB023184	FC_PON_Q_EGR_DROP_IDX [22].IDX[8:6]	3
0xBB023184	FC_PON_Q_EGR_DROP_IDX [23].IDX[11:9]	3
0xBB023184	FC_PON_Q_EGR_DROP_IDX [24].IDX[14:12]	3
0xBB023184	FC_PON_Q_EGR_DROP_IDX [25].IDX[17:15]	3
0xBB023184	FC_PON_Q_EGR_DROP_IDX [26].IDX[20:18]	3
0xBB023184	FC_PON_Q_EGR_DROP_IDX [27].IDX[23:21]	3
0xBB023184	FC_PON_Q_EGR_DROP_IDX [28].IDX[26:24]	3
0xBB023184	FC_PON_Q_EGR_DROP_IDX [29].IDX[29:27]	3
0xBB023188	FC_PON_Q_EGR_DROP_IDX [30].IDX[2:0]	3
0xBB023188	FC_PON_Q_EGR_DROP_IDX [31].IDX[5:3]	3
0xBB023188	FC_PON_Q_EGR_DROP_IDX [32].IDX[8:6]	3
0xBB023188	FC_PON_Q_EGR_DROP_IDX [33].IDX[11:9]	3

Address	Register	Len
0xBB023188	FC_PON_Q_EGR_DROP_IDX [34].IDX[14:12]	3
0xBB023188	FC_PON_Q_EGR_DROP_IDX [35].IDX[17:15]	3
0xBB023188	FC_PON_Q_EGR_DROP_IDX [36].IDX[20:18]	3
0xBB023188	FC_PON_Q_EGR_DROP_IDX [37].IDX[23:21]	3
0xBB023188	FC_PON_Q_EGR_DROP_IDX [38].IDX[26:24]	3
0xBB023188	FC_PON_Q_EGR_DROP_IDX [39].IDX[29:27]	3
0xBB02318C	FC_PON_Q_EGR_DROP_IDX [40].IDX[2:0]	3
0xBB02318C	FC_PON_Q_EGR_DROP_IDX [41].IDX[5:3]	3
0xBB02318C	FC_PON_Q_EGR_DROP_IDX [42].IDX[8:6]	3
0xBB02318C	FC_PON_Q_EGR_DROP_IDX [43].IDX[11:9]	3
0xBB02318C	FC_PON_Q_EGR_DROP_IDX [44].IDX[14:12]	3
0xBB02318C	FC_PON_Q_EGR_DROP_IDX [45].IDX[17:15]	3
0xBB02318C	FC_PON_Q_EGR_DROP_IDX [46].IDX[20:18]	3
0xBB02318C	FC_PON_Q_EGR_DROP_IDX [47].IDX[23:21]	3
0xBB02318C	FC_PON_Q_EGR_DROP_IDX [48].IDX[26:24]	3
0xBB02318C	FC_PON_Q_EGR_DROP_IDX [49].IDX[29:27]	3
0xBB023190	FC_PON_Q_EGR_DROP_IDX [50].IDX[2:0]	3
0xBB023190	FC_PON_Q_EGR_DROP_IDX [51].IDX[5:3]	3
0xBB023190	FC_PON_Q_EGR_DROP_IDX [52].IDX[8:6]	3
0xBB023190	FC_PON_Q_EGR_DROP_IDX [53].IDX[11:9]	3
0xBB023190	FC_PON_Q_EGR_DROP_IDX [54].IDX[14:12]	3
0xBB023190	FC_PON_Q_EGR_DROP_IDX [55].IDX[17:15]	3
0xBB023190	FC_PON_Q_EGR_DROP_IDX [56].IDX[20:18]	3
0xBB023190	FC_PON_Q_EGR_DROP_IDX [57].IDX[23:21]	3
0xBB023190	FC_PON_Q_EGR_DROP_IDX [58].IDX[26:24]	3
0xBB023190	FC_PON_Q_EGR_DROP_IDX [59].IDX[29:27]	3
0xBB023194	FC_PON_Q_EGR_DROP_IDX [60].IDX[2:0]	3
0xBB023194	FC_PON_Q_EGR_DROP_IDX [61].IDX[5:3]	3
0xBB023194	FC_PON_Q_EGR_DROP_IDX [62].IDX[8:6]	3
0xBB023194	FC_PON_Q_EGR_DROP_IDX [63].IDX[11:9]	3
0xBB023194	FC_PON_Q_EGR_DROP_IDX [64].IDX[14:12]	3
0xBB023194	FC_PON_Q_EGR_DROP_IDX [65].IDX[17:15]	3
0xBB023194	FC_PON_Q_EGR_DROP_IDX [66].IDX[20:18]	3
0xBB023194	FC_PON_Q_EGR_DROP_IDX [67].IDX[23:21]	3
0xBB023194	FC_PON_Q_EGR_DROP_IDX [68].IDX[26:24]	3
0xBB023194	FC_PON_Q_EGR_DROP_IDX [69].IDX[29:27]	3
0xBB023198	FC_PON_Q_EGR_DROP_IDX [70].IDX[2:0]	3
0xBB023198	FC_PON_Q_EGR_DROP_IDX [71].IDX[5:3]	3
0xBB023198	FC_PON_Q_EGR_DROP_IDX [72].IDX[8:6]	3
0xBB023198	FC_PON_Q_EGR_DROP_IDX [73].IDX[11:9]	3
0xBB023198	FC_PON_Q_EGR_DROP_IDX [74].IDX[14:12]	3
0xBB023198	FC_PON_Q_EGR_DROP_IDX [75].IDX[17:15]	3
0xBB023198	FC_PON_Q_EGR_DROP_IDX [76].IDX[20:18]	3
0xBB023198	FC_PON_Q_EGR_DROP_IDX [77].IDX[23:21]	3
0xBB023198	FC_PON_Q_EGR_DROP_IDX [78].IDX[26:24]	3
0xBB023198	FC_PON_Q_EGR_DROP_IDX [79].IDX[29:27]	3



Address	Register	Len
0xBB02319C	FC_PON_Q_EGR_DROP_IDX [80].IDX[2:0]	3
0xBB02319C	FC_PON_Q_EGR_DROP_IDX [81].IDX[5:3]	3
0xBB02319C	FC_PON_Q_EGR_DROP_IDX [82].IDX[8:6]	3
0xBB02319C	FC_PON_Q_EGR_DROP_IDX [83].IDX[11:9]	3
0xBB02319C	FC_PON_Q_EGR_DROP_IDX [84].IDX[14:12]	3
0xBB02319C	FC_PON_Q_EGR_DROP_IDX [85].IDX[17:15]	3
0xBB02319C	FC_PON_Q_EGR_DROP_IDX [86].IDX[20:18]	3
0xBB02319C	FC_PON_Q_EGR_DROP_IDX [87].IDX[23:21]	3
0xBB02319C	FC_PON_Q_EGR_DROP_IDX [88].IDX[26:24]	3
0xBB02319C	FC_PON_Q_EGR_DROP_IDX [89].IDX[29:27]	3
0xBB0231A0	FC_PON_Q_EGR_DROP_IDX [90].IDX[2:0]	3
0xBB0231A0	FC_PON_Q_EGR_DROP_IDX [91].IDX[5:3]	3
0xBB0231A0	FC_PON_Q_EGR_DROP_IDX [92].IDX[8:6]	3
0xBB0231A0	FC_PON_Q_EGR_DROP_IDX [93].IDX[11:9]	3
0xBB0231A0	FC_PON_Q_EGR_DROP_IDX [94].IDX[14:12]	3
0xBB0231A0	FC_PON_Q_EGR_DROP_IDX [95].IDX[17:15]	3
0xBB0231A0	FC_PON_Q_EGR_DROP_IDX [96].IDX[20:18]	3
0xBB0231A0	FC_PON_Q_EGR_DROP_IDX [97].IDX[23:21]	3
0xBB0231A0	FC_PON_Q_EGR_DROP_IDX [98].IDX[26:24]	3
0xBB0231A0	FC_PON_Q_EGR_DROP_IDX [99].IDX[29:27]	3
0xBB0231A4	FC_PON_Q_EGR_DROP_IDX [100].IDX[2:0]	3
0xBB0231A4	FC_PON_Q_EGR_DROP_IDX [101].IDX[5:3]	3
0xBB0231A4	FC_PON_Q_EGR_DROP_IDX [102].IDX[8:6]	3
0xBB0231A4	FC_PON_Q_EGR_DROP_IDX [103].IDX[11:9]	3
0xBB0231A4	FC_PON_Q_EGR_DROP_IDX [104].IDX[14:12]	3
0xBB0231A4	FC_PON_Q_EGR_DROP_IDX [105].IDX[17:15]	3
0xBB0231A4	FC_PON_Q_EGR_DROP_IDX [106].IDX[20:18]	3
0xBB0231A4	FC_PON_Q_EGR_DROP_IDX [107].IDX[23:21]	3
0xBB0231A4	FC_PON_Q_EGR_DROP_IDX [108].IDX[26:24]	3
0xBB0231A4	FC_PON_Q_EGR_DROP_IDX [109].IDX[29:27]	3
0xBB0231A8	FC_PON_Q_EGR_DROP_IDX [110].IDX[2:0]	3
0xBB0231A8	FC_PON_Q_EGR_DROP_IDX [111].IDX[5:3]	3
0xBB0231A8	FC_PON_Q_EGR_DROP_IDX [112].IDX[8:6]	3
0xBB0231A8	FC_PON_Q_EGR_DROP_IDX [113].IDX[11:9]	3
0xBB0231A8	FC_PON_Q_EGR_DROP_IDX [114].IDX[14:12]	3
0xBB0231A8	FC_PON_Q_EGR_DROP_IDX [115].IDX[17:15]	3
0xBB0231A8	FC_PON_Q_EGR_DROP_IDX [116].IDX[20:18]	3
0xBB0231A8	FC_PON_Q_EGR_DROP_IDX [117].IDX[23:21]	3
0xBB0231A8	FC_PON_Q_EGR_DROP_IDX [118].IDX[26:24]	3
0xBB0231A8	FC_PON_Q_EGR_DROP_IDX [119].IDX[29:27]	3
0xBB0231AC	FC_PON_Q_EGR_DROP_IDX [120].IDX[2:0]	3
0xBB0231AC	FC_PON_Q_EGR_DROP_IDX [121].IDX[5:3]	3
0xBB0231AC	FC_PON_Q_EGR_DROP_IDX [122].IDX[8:6]	3
0xBB0231AC	FC_PON_Q_EGR_DROP_IDX [123].IDX[11:9]	3
0xBB0231AC	FC_PON_Q_EGR_DROP_IDX [124].IDX[14:12]	3
0xBB0231AC	FC_PON_Q_EGR_DROP_IDX [125].IDX[17:15]	3



Address	Register	Len
0xBB0231AC	FC_PON_Q_EGR_DROP_IDX [126].IDX[20:18]	3
0xBB0231AC	FC_PON_Q_EGR_DROP_IDX [127].IDX[23:21]	3
0xBB0231B0	FC_PON_Q_EGR_DROP_TH [0].TH[12:0]	13
0xBB0231B0	FC_PON_Q_EGR_DROP_TH [1].TH[25:13]	13
0xBB0231B4	FC_PON_Q_EGR_DROP_TH [2].TH[12:0]	13
0xBB0231B4	FC_PON_Q_EGR_DROP_TH [3].TH[25:13]	13
0xBB0231B8	FC_PON_Q_EGR_DROP_TH [4].TH[12:0]	13
0xBB0231B8	FC_PON_Q_EGR_DROP_TH [5].TH[25:13]	13
0xBB0231BC	FC_PON_Q_EGR_DROP_TH [6].TH[12:0]	13
0xBB0231BC	FC_PON_Q_EGR_DROP_TH [7].TH[25:13]	13
0xBB0231C0	FC_PON_Q_EGR_GAP_TH.RESERVED[31:13]	19
0xBB0231C0	FC_PON_Q_EGR_GAP_TH.TH[12:0]	13
0xBB0231C4	FC_PON_Q_USED_PAGE_CTRL.RESERVED[31:8]	24
0xBB0231C4	FC_PON_Q_USED_PAGE_CTRL.CLR_MAX_PAGE_CNT[7:7]	1
0xBB0231C4	FC_PON_Q_USED_PAGE_CTRL.QID[6:0]	7
0xBB0231C8	FC_PON_Q_USED_PAGE_CNT.RESERVED[31:29]	3
0xBB0231C8	FC_PON_Q_USED_PAGE_CNT.Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB0231C8	FC_PON_Q_USED_PAGE_CNT.RESERVED[15:13]	3
0xBB0231C8	FC_PON_Q_USED_PAGE_CNT.Q_USED_PAGE_CNT[12:0]	13
0xBB0231CC	RMK_1Q_CTRL [0].INTPRI_1Q[2:0]	3
0xBB0231CC	RMK_1Q_CTRL [1].INTPRI_1Q[5:3]	3
0xBB0231CC	RMK_1Q_CTRL [2].INTPRI_1Q[8:6]	3
0xBB0231CC	RMK_1Q_CTRL [3].INTPRI_1Q[11:9]	3
0xBB0231CC	RMK_1Q_CTRL [4].INTPRI_1Q[14:12]	3
0xBB0231CC	RMK_1Q_CTRL [5].INTPRI_1Q[17:15]	3
0xBB0231CC	RMK_1Q_CTRL [6].INTPRI_1Q[20:18]	3
0xBB0231CC	RMK_1Q_CTRL [7].INTPRI_1Q[23:21]	3
0xBB0231D0	RMK_DSCP_RMK_EN_CTRL [0].RESERVED[31:1]	31
0xBB0231D0	RMK_DSCP_RMK_EN_CTRL [0].EN[0:0]	1
0xBB0231D4	RMK_DSCP_RMK_EN_CTRL [1].RESERVED[31:1]	31
0xBB0231D4	RMK_DSCP_RMK_EN_CTRL [1].EN[0:0]	1
0xBB0231D8	RMK_DSCP_RMK_EN_CTRL [2].RESERVED[31:1]	31
0xBB0231D8	RMK_DSCP_RMK_EN_CTRL [2].EN[0:0]	1
0xBB0231DC	RMK_DSCP_RMK_EN_CTRL [3].RESERVED[31:1]	31
0xBB0231DC	RMK_DSCP_RMK_EN_CTRL [3].EN[0:0]	1
0xBB0231E0	RMK_DSCP_RMK_EN_CTRL [4].RESERVED[31:1]	31
0xBB0231E0	RMK_DSCP_RMK_EN_CTRL [4].EN[0:0]	1
0xBB0231E4	RMK_DSCP_RMK_EN_CTRL [5].RESERVED[31:1]	31
0xBB0231E4	RMK_DSCP_RMK_EN_CTRL [5].EN[0:0]	1
0xBB0231E8	RMK_DSCP_RMK_EN_CTRL [6].RESERVED[31:1]	31
0xBB0231E8	RMK_DSCP_RMK_EN_CTRL [6].EN[0:0]	1
0xBB0231EC	RLDP_CTRL_0.RESERVED[31:1]	31
0xBB0231EC	RLDP_CTRL_0.ACT_RUNOUTDSC[0:0]	1
0xBB0231F0	SPG_GLB_CTRL.PAUSE_TIME[31:16]	16
0xBB0231F0	SPG_GLB_CTRL.RESERVED[15:3]	13
0xBB0231F0	SPG_GLB_CTRL.BYPASS_FC_MODE[2:2]	1

Address	Register	Len
0xBB0231F0	SPG_GLB_CTRL.CMD_STOP[1:1]	1
0xBB0231F0	SPG_GLB_CTRL.CMD_START[0:0]	1
0xBB0231F4	SPG_PAYLOAD [0].PAYLOAD[7:0]	8
0xBB0231F4	SPG_PAYLOAD [1].PAYLOAD[15:8]	8
0xBB0231F4	SPG_PAYLOAD [2].PAYLOAD[23:16]	8
0xBB0231F4	SPG_PAYLOAD [3].PAYLOAD[31:24]	8
0xBB0231F8	SPG_PAYLOAD [4].PAYLOAD[7:0]	8
0xBB0231F8	SPG_PAYLOAD [5].PAYLOAD[15:8]	8
0xBB0231F8	SPG_PAYLOAD [6].PAYLOAD[23:16]	8
0xBB0231F8	SPG_PAYLOAD [7].PAYLOAD[31:24]	8
0xBB0231FC	SPG_PAYLOAD [8].PAYLOAD[7:0]	8
0xBB0231FC	SPG_PAYLOAD [9].PAYLOAD[15:8]	8
0xBB0231FC	SPG_PAYLOAD [10].PAYLOAD[23:16]	8
0xBB0231FC	SPG_PAYLOAD [11].PAYLOAD[31:24]	8
0xBB023200	SPG_PAYLOAD [12].PAYLOAD[7:0]	8
0xBB023200	SPG_PAYLOAD [13].PAYLOAD[15:8]	8
0xBB023200	SPG_PAYLOAD [14].PAYLOAD[23:16]	8
0xBB023200	SPG_PAYLOAD [15].PAYLOAD[31:24]	8
0xBB023204	SPG_PAYLOAD [16].PAYLOAD[7:0]	8
0xBB023204	SPG_PAYLOAD [17].PAYLOAD[15:8]	8
0xBB023204	SPG_PAYLOAD [18].PAYLOAD[23:16]	8
0xBB023204	SPG_PAYLOAD [19].PAYLOAD[31:24]	8
0xBB023208	SPG_PAYLOAD [20].PAYLOAD[7:0]	8
0xBB023208	SPG_PAYLOAD [21].PAYLOAD[15:8]	8
0xBB023208	SPG_PAYLOAD [22].PAYLOAD[23:16]	8
0xBB023208	SPG_PAYLOAD [23].PAYLOAD[31:24]	8
0xBB02320C	SPG_PAYLOAD [24].PAYLOAD[7:0]	8
0xBB02320C	SPG_PAYLOAD [25].PAYLOAD[15:8]	8
0xBB02320C	SPG_PAYLOAD [26].PAYLOAD[23:16]	8
0xBB02320C	SPG_PAYLOAD [27].PAYLOAD[31:24]	8
0xBB023210	SPG_PAYLOAD [28].PAYLOAD[7:0]	8
0xBB023210	SPG_PAYLOAD [29].PAYLOAD[15:8]	8
0xBB023210	SPG_PAYLOAD [30].PAYLOAD[23:16]	8
0xBB023210	SPG_PAYLOAD [31].PAYLOAD[31:24]	8
0xBB023214	SPG_PAYLOAD [32].PAYLOAD[7:0]	8
0xBB023214	SPG_PAYLOAD [33].PAYLOAD[15:8]	8
0xBB023214	SPG_PAYLOAD [34].PAYLOAD[23:16]	8
0xBB023214	SPG_PAYLOAD [35].PAYLOAD[31:24]	8
0xBB023218	SPG_PAYLOAD [36].PAYLOAD[7:0]	8
0xBB023218	SPG_PAYLOAD [37].PAYLOAD[15:8]	8
0xBB023218	SPG_PAYLOAD [38].PAYLOAD[23:16]	8
0xBB023218	SPG_PAYLOAD [39].PAYLOAD[31:24]	8
0xBB02321C	SPG_PAYLOAD [40].PAYLOAD[7:0]	8
0xBB02321C	SPG_PAYLOAD [41].PAYLOAD[15:8]	8
0xBB02321C	SPG_PAYLOAD [42].PAYLOAD[23:16]	8
0xBB02321C	SPG_PAYLOAD [43].PAYLOAD[31:24]	8

Address	Register	Len
0xBB023220	SPG_PAYLOAD [44].PAYLOAD[7:0]	8
0xBB023220	SPG_PAYLOAD [45].PAYLOAD[15:8]	8
0xBB023220	SPG_PAYLOAD [46].PAYLOAD[23:16]	8
0xBB023220	SPG_PAYLOAD [47].PAYLOAD[31:24]	8
0xBB023224	PARSER_FIELD_SELECTOR_CTRL [0].RESERVED[31:11]	21
0xBB023224	PARSER_FIELD_SELECTOR_CTRL [0].OFFSET[10:3]	8
0xBB023224	PARSER_FIELD_SELECTOR_CTRL [0].FMT[2:0]	3
0xBB023228	PARSER_FIELD_SELECTOR_CTRL [1].RESERVED[31:11]	21
0xBB023228	PARSER_FIELD_SELECTOR_CTRL [1].OFFSET[10:3]	8
0xBB023228	PARSER_FIELD_SELECTOR_CTRL [1].FMT[2:0]	3
0xBB02322C	PARSER_FIELD_SELECTOR_CTRL [2].RESERVED[31:11]	21
0xBB02322C	PARSER_FIELD_SELECTOR_CTRL [2].OFFSET[10:3]	8
0xBB02322C	PARSER_FIELD_SELECTOR_CTRL [2].FMT[2:0]	3
0xBB023230	PARSER_FIELD_SELECTOR_CTRL [3].RESERVED[31:11]	21
0xBB023230	PARSER_FIELD_SELECTOR_CTRL [3].OFFSET[10:3]	8
0xBB023230	PARSER_FIELD_SELECTOR_CTRL [3].FMT[2:0]	3
0xBB023234	PARSER_FIELD_SELECTOR_CTRL [4].RESERVED[31:11]	21
0xBB023234	PARSER_FIELD_SELECTOR_CTRL [4].OFFSET[10:3]	8
0xBB023234	PARSER_FIELD_SELECTOR_CTRL [4].FMT[2:0]	3
0xBB023238	PARSER_FIELD_SELECTOR_CTRL [5].RESERVED[31:11]	21
0xBB023238	PARSER_FIELD_SELECTOR_CTRL [5].OFFSET[10:3]	8
0xBB023238	PARSER_FIELD_SELECTOR_CTRL [5].FMT[2:0]	3
0xBB02323C	PARSER_FIELD_SELECTOR_CTRL [6].RESERVED[31:11]	21
0xBB02323C	PARSER_FIELD_SELECTOR_CTRL [6].OFFSET[10:3]	8
0xBB02323C	PARSER_FIELD_SELECTOR_CTRL [6].FMT[2:0]	3
0xBB023240	PARSER_FIELD_SELECTOR_CTRL [7].RESERVED[31:11]	21
0xBB023240	PARSER_FIELD_SELECTOR_CTRL [7].OFFSET[10:3]	8
0xBB023240	PARSER_FIELD_SELECTOR_CTRL [7].FMT[2:0]	3
0xBB023244	PARSER_FIELD_SELECTOR_CTRL [8].RESERVED[31:11]	21
0xBB023244	PARSER_FIELD_SELECTOR_CTRL [8].OFFSET[10:3]	8
0xBB023244	PARSER_FIELD_SELECTOR_CTRL [8].FMT[2:0]	3
0xBB023248	PARSER_FIELD_SELECTOR_CTRL [9].RESERVED[31:11]	21
0xBB023248	PARSER_FIELD_SELECTOR_CTRL [9].OFFSET[10:3]	8
0xBB023248	PARSER_FIELD_SELECTOR_CTRL [9].FMT[2:0]	3
0xBB02324C	PARSER_FIELD_SELECTOR_CTRL [10].RESERVED[31:11]	21
0xBB02324C	PARSER_FIELD_SELECTOR_CTRL [10].OFFSET[10:3]	8
0xBB02324C	PARSER_FIELD_SELECTOR_CTRL [10].FMT[2:0]	3
0xBB023250	PARSER_FIELD_SELECTOR_CTRL [11].RESERVED[31:11]	21
0xBB023250	PARSER_FIELD_SELECTOR_CTRL [11].OFFSET[10:3]	8
0xBB023250	PARSER_FIELD_SELECTOR_CTRL [11].FMT[2:0]	3
0xBB023254	PARSER_FIELD_SELECTOR_CTRL [12].RESERVED[31:11]	21
0xBB023254	PARSER_FIELD_SELECTOR_CTRL [12].OFFSET[10:3]	8
0xBB023254	PARSER_FIELD_SELECTOR_CTRL [12].FMT[2:0]	3
0xBB023258	PARSER_FIELD_SELECTOR_CTRL [13].RESERVED[31:11]	21
0xBB023258	PARSER_FIELD_SELECTOR_CTRL [13].OFFSET[10:3]	8
0xBB023258	PARSER_FIELD_SELECTOR_CTRL [13].FMT[2:0]	3

Address	Register	Len
0xBB02325C	PARSER_FIELD_SELTOR_CTRL [14].RESERVED[31:11]	21
0xBB02325C	PARSER_FIELD_SELTOR_CTRL [14].OFFSET[10:3]	8
0xBB02325C	PARSER_FIELD_SELTOR_CTRL [14].FMT[2:0]	3
0xBB023260	PARSER_FIELD_SELTOR_CTRL [15].RESERVED[31:11]	21
0xBB023260	PARSER_FIELD_SELTOR_CTRL [15].OFFSET[10:3]	8
0xBB023260	PARSER_FIELD_SELTOR_CTRL [15].FMT[2:0]	3
0xBB023264	PON_PORT_CTRL.RESERVED[31:6]	26
0xBB023264	PON_PORT_CTRL.BW_THRESHOLD[5:0]	6
0xBB023268	PONMAC_DRN_CTRL.RESERVED[31:9]	23
0xBB023268	PONMAC_DRN_CTRL.PON_DRN_SEL[8:8]	1
0xBB023268	PONMAC_DRN_CTRL.PON_DRN_IDX[7:1]	7
0xBB023268	PONMAC_DRN_CTRL.PON_DRN_EN[0:0]	1
0xBB02326C	RGF_VER_SWCORE.REGFILE_VER[31:0]	32
0xBB023270	RSVD_SWCORE [0].RSVD_MEM[31:0]	32
0xBB023274	RSVD_SWCORE [1].RSVD_MEM[31:0]	32
0xBB023278	RSVD_SWCORE [2].RSVD_MEM[31:0]	32
0xBB02327C	RSVD_SWCORE [3].RSVD_MEM[31:0]	32
0xBB023280	RSVD_SWCORE [4].RSVD_MEM[31:0]	32
0xBB023284	RSVD_SWCORE [5].RSVD_MEM[31:0]	32
0xBB023288	RSVD_SWCORE [6].RSVD_MEM[31:0]	32
0xBB02328C	RSVD_SWCORE [7].RSVD_MEM[31:0]	32
0xBB023290	RSVD_SWCORE [8].RSVD_MEM[31:0]	32
0xBB023294	RSVD_SWCORE [9].RSVD_MEM[31:0]	32
0xBB023298	RSVD_SWCORE [10].RSVD_MEM[31:0]	32
0xBB02329C	RSVD_SWCORE [11].RSVD_MEM[31:0]	32
0xBB0232A0	RSVD_SWCORE [12].RSVD_MEM[31:0]	32
0xBB0232A4	RSVD_SWCORE [13].RSVD_MEM[31:0]	32
0xBB0232A8	RSVD_SWCORE [14].RSVD_MEM[31:0]	32
0xBB0232AC	RSVD_SWCORE [15].RSVD_MEM[31:0]	32
0xBB0232B0	CHANGE_DUPLEX_CTRL.RESERVED[31:8]	24
0xBB0232B0	CHANGE_DUPLEX_CTRL.CFG_CHG_DUP_EN[7:7]	1
0xBB0232B0	CHANGE_DUPLEX_CTRL.CFG_CHG_DUP_THR[6:2]	5
0xBB0232B0	CHANGE_DUPLEX_CTRL.CFG_CHG_DUP_CONGEST[1:1]	1
0xBB0232B0	CHANGE_DUPLEX_CTRL.CFG_CHG_DUP_REF[0:0]	1
0xBB025000	METER_TB_CTRL.RESERVED[31:17]	15
0xBB025000	METER_TB_CTRL.METER_OP[16:16]	1
0xBB025000	METER_TB_CTRL.TICK_PERIOD[15:8]	8
0xBB025000	METER_TB_CTRL.TKN[7:0]	8
0xBB025004	METER_GLB_CTRL [0].RESERVED[31:17]	15
0xBB025004	METER_GLB_CTRL [0].RATE[16:0]	17
0xBB025008	METER_GLB_CTRL [0].RESERVED[31:17]	15
0xBB025008	METER_GLB_CTRL [0].BUCKET_SIZE[16:1]	16
0xBB025008	METER_GLB_CTRL [0].IFG[0:0]	1
0xBB02500C	METER_GLB_CTRL [1].RESERVED[31:17]	15
0xBB02500C	METER_GLB_CTRL [1].RATE[16:0]	17
0xBB025010	METER_GLB_CTRL [1].RESERVED[31:17]	15

Address	Register	Len
0xBB025010	METER_GLB_CTRL [1].BUCKET_SIZE[16:1]	16
0xBB025010	METER_GLB_CTRL [1].IFG[0:0]	1
0xBB025014	METER_GLB_CTRL [2].RESERVED[31:17]	15
0xBB025014	METER_GLB_CTRL [2].RATE[16:0]	17
0xBB025018	METER_GLB_CTRL [2].RESERVED[31:17]	15
0xBB025018	METER_GLB_CTRL [2].BUCKET_SIZE[16:1]	16
0xBB025018	METER_GLB_CTRL [2].IFG[0:0]	1
0xBB02501C	METER_GLB_CTRL [3].RESERVED[31:17]	15
0xBB02501C	METER_GLB_CTRL [3].RATE[16:0]	17
0xBB025020	METER_GLB_CTRL [3].RESERVED[31:17]	15
0xBB025020	METER_GLB_CTRL [3].BUCKET_SIZE[16:1]	16
0xBB025020	METER_GLB_CTRL [3].IFG[0:0]	1
0xBB025024	METER_GLB_CTRL [4].RESERVED[31:17]	15
0xBB025024	METER_GLB_CTRL [4].RATE[16:0]	17
0xBB025028	METER_GLB_CTRL [4].RESERVED[31:17]	15
0xBB025028	METER_GLB_CTRL [4].BUCKET_SIZE[16:1]	16
0xBB025028	METER_GLB_CTRL [4].IFG[0:0]	1
0xBB02502C	METER_GLB_CTRL [5].RESERVED[31:17]	15
0xBB02502C	METER_GLB_CTRL [5].RATE[16:0]	17
0xBB025030	METER_GLB_CTRL [5].RESERVED[31:17]	15
0xBB025030	METER_GLB_CTRL [5].BUCKET_SIZE[16:1]	16
0xBB025030	METER_GLB_CTRL [5].IFG[0:0]	1
0xBB025034	METER_GLB_CTRL [6].RESERVED[31:17]	15
0xBB025034	METER_GLB_CTRL [6].RATE[16:0]	17
0xBB025038	METER_GLB_CTRL [6].RESERVED[31:17]	15
0xBB025038	METER_GLB_CTRL [6].BUCKET_SIZE[16:1]	16
0xBB025038	METER_GLB_CTRL [6].IFG[0:0]	1
0xBB02503C	METER_GLB_CTRL [7].RESERVED[31:17]	15
0xBB02503C	METER_GLB_CTRL [7].RATE[16:0]	17
0xBB025040	METER_GLB_CTRL [7].RESERVED[31:17]	15
0xBB025040	METER_GLB_CTRL [7].BUCKET_SIZE[16:1]	16
0xBB025040	METER_GLB_CTRL [7].IFG[0:0]	1
0xBB025044	METER_GLB_CTRL [8].RESERVED[31:17]	15
0xBB025044	METER_GLB_CTRL [8].RATE[16:0]	17
0xBB025048	METER_GLB_CTRL [8].RESERVED[31:17]	15
0xBB025048	METER_GLB_CTRL [8].BUCKET_SIZE[16:1]	16
0xBB025048	METER_GLB_CTRL [8].IFG[0:0]	1
0xBB02504C	METER_GLB_CTRL [9].RESERVED[31:17]	15
0xBB02504C	METER_GLB_CTRL [9].RATE[16:0]	17
0xBB025050	METER_GLB_CTRL [9].RESERVED[31:17]	15
0xBB025050	METER_GLB_CTRL [9].BUCKET_SIZE[16:1]	16
0xBB025050	METER_GLB_CTRL [9].IFG[0:0]	1
0xBB025054	METER_GLB_CTRL [10].RESERVED[31:17]	15
0xBB025054	METER_GLB_CTRL [10].RATE[16:0]	17
0xBB025058	METER_GLB_CTRL [10].RESERVED[31:17]	15
0xBB025058	METER_GLB_CTRL [10].BUCKET_SIZE[16:1]	16

Address	Register	Len
0xBB025058	METER_GLB_CTRL [10].IFG[0:0]	1
0xBB02505C	METER_GLB_CTRL [11].RESERVED[31:17]	15
0xBB02505C	METER_GLB_CTRL [11].RATE[16:0]	17
0xBB025060	METER_GLB_CTRL [11].RESERVED[31:17]	15
0xBB025060	METER_GLB_CTRL [11].BUCKET_SIZE[16:1]	16
0xBB025060	METER_GLB_CTRL [11].IFG[0:0]	1
0xBB025064	METER_GLB_CTRL [12].RESERVED[31:17]	15
0xBB025064	METER_GLB_CTRL [12].RATE[16:0]	17
0xBB025068	METER_GLB_CTRL [12].RESERVED[31:17]	15
0xBB025068	METER_GLB_CTRL [12].BUCKET_SIZE[16:1]	16
0xBB025068	METER_GLB_CTRL [12].IFG[0:0]	1
0xBB02506C	METER_GLB_CTRL [13].RESERVED[31:17]	15
0xBB02506C	METER_GLB_CTRL [13].RATE[16:0]	17
0xBB025070	METER_GLB_CTRL [13].RESERVED[31:17]	15
0xBB025070	METER_GLB_CTRL [13].BUCKET_SIZE[16:1]	16
0xBB025070	METER_GLB_CTRL [13].IFG[0:0]	1
0xBB025074	METER_GLB_CTRL [14].RESERVED[31:17]	15
0xBB025074	METER_GLB_CTRL [14].RATE[16:0]	17
0xBB025078	METER_GLB_CTRL [14].RESERVED[31:17]	15
0xBB025078	METER_GLB_CTRL [14].BUCKET_SIZE[16:1]	16
0xBB025078	METER_GLB_CTRL [14].IFG[0:0]	1
0xBB02507C	METER_GLB_CTRL [15].RESERVED[31:17]	15
0xBB02507C	METER_GLB_CTRL [15].RATE[16:0]	17
0xBB025080	METER_GLB_CTRL [15].RESERVED[31:17]	15
0xBB025080	METER_GLB_CTRL [15].BUCKET_SIZE[16:1]	16
0xBB025080	METER_GLB_CTRL [15].IFG[0:0]	1
0xBB025084	METER_GLB_CTRL [16].RESERVED[31:17]	15
0xBB025084	METER_GLB_CTRL [16].RATE[16:0]	17
0xBB025088	METER_GLB_CTRL [16].RESERVED[31:17]	15
0xBB025088	METER_GLB_CTRL [16].BUCKET_SIZE[16:1]	16
0xBB025088	METER_GLB_CTRL [16].IFG[0:0]	1
0xBB02508C	METER_GLB_CTRL [17].RESERVED[31:17]	15
0xBB02508C	METER_GLB_CTRL [17].RATE[16:0]	17
0xBB025090	METER_GLB_CTRL [17].RESERVED[31:17]	15
0xBB025090	METER_GLB_CTRL [17].BUCKET_SIZE[16:1]	16
0xBB025090	METER_GLB_CTRL [17].IFG[0:0]	1
0xBB025094	METER_GLB_CTRL [18].RESERVED[31:17]	15
0xBB025094	METER_GLB_CTRL [18].RATE[16:0]	17
0xBB025098	METER_GLB_CTRL [18].RESERVED[31:17]	15
0xBB025098	METER_GLB_CTRL [18].BUCKET_SIZE[16:1]	16
0xBB025098	METER_GLB_CTRL [18].IFG[0:0]	1
0xBB02509C	METER_GLB_CTRL [19].RESERVED[31:17]	15
0xBB02509C	METER_GLB_CTRL [19].RATE[16:0]	17
0xBB0250A0	METER_GLB_CTRL [19].RESERVED[31:17]	15
0xBB0250A0	METER_GLB_CTRL [19].BUCKET_SIZE[16:1]	16
0xBB0250A0	METER_GLB_CTRL [19].IFG[0:0]	1

Address	Register	Len
0xBB0250A4	METER_GLB_CTRL [20].RESERVED[31:17]	15
0xBB0250A4	METER_GLB_CTRL [20].RATE[16:0]	17
0xBB0250A8	METER_GLB_CTRL [20].RESERVED[31:17]	15
0xBB0250A8	METER_GLB_CTRL [20].BUCKET_SIZE[16:1]	16
0xBB0250A8	METER_GLB_CTRL [20].IFG[0:0]	1
0xBB0250AC	METER_GLB_CTRL [21].RESERVED[31:17]	15
0xBB0250AC	METER_GLB_CTRL [21].RATE[16:0]	17
0xBB0250B0	METER_GLB_CTRL [21].RESERVED[31:17]	15
0xBB0250B0	METER_GLB_CTRL [21].BUCKET_SIZE[16:1]	16
0xBB0250B0	METER_GLB_CTRL [21].IFG[0:0]	1
0xBB0250B4	METER_GLB_CTRL [22].RESERVED[31:17]	15
0xBB0250B4	METER_GLB_CTRL [22].RATE[16:0]	17
0xBB0250B8	METER_GLB_CTRL [22].RESERVED[31:17]	15
0xBB0250B8	METER_GLB_CTRL [22].BUCKET_SIZE[16:1]	16
0xBB0250B8	METER_GLB_CTRL [22].IFG[0:0]	1
0xBB0250BC	METER_GLB_CTRL [23].RESERVED[31:17]	15
0xBB0250BC	METER_GLB_CTRL [23].RATE[16:0]	17
0xBB0250C0	METER_GLB_CTRL [23].RESERVED[31:17]	15
0xBB0250C0	METER_GLB_CTRL [23].BUCKET_SIZE[16:1]	16
0xBB0250C0	METER_GLB_CTRL [23].IFG[0:0]	1
0xBB0250C4	METER_GLB_CTRL [24].RESERVED[31:17]	15
0xBB0250C4	METER_GLB_CTRL [24].RATE[16:0]	17
0xBB0250C8	METER_GLB_CTRL [24].RESERVED[31:17]	15
0xBB0250C8	METER_GLB_CTRL [24].BUCKET_SIZE[16:1]	16
0xBB0250C8	METER_GLB_CTRL [24].IFG[0:0]	1
0xBB0250CC	METER_GLB_CTRL [25].RESERVED[31:17]	15
0xBB0250CC	METER_GLB_CTRL [25].RATE[16:0]	17
0xBB0250D0	METER_GLB_CTRL [25].RESERVED[31:17]	15
0xBB0250D0	METER_GLB_CTRL [25].BUCKET_SIZE[16:1]	16
0xBB0250D0	METER_GLB_CTRL [25].IFG[0:0]	1
0xBB0250D4	METER_GLB_CTRL [26].RESERVED[31:17]	15
0xBB0250D4	METER_GLB_CTRL [26].RATE[16:0]	17
0xBB0250D8	METER_GLB_CTRL [26].RESERVED[31:17]	15
0xBB0250D8	METER_GLB_CTRL [26].BUCKET_SIZE[16:1]	16
0xBB0250D8	METER_GLB_CTRL [26].IFG[0:0]	1
0xBB0250DC	METER_GLB_CTRL [27].RESERVED[31:17]	15
0xBB0250DC	METER_GLB_CTRL [27].RATE[16:0]	17
0xBB0250E0	METER_GLB_CTRL [27].RESERVED[31:17]	15
0xBB0250E0	METER_GLB_CTRL [27].BUCKET_SIZE[16:1]	16
0xBB0250E0	METER_GLB_CTRL [27].IFG[0:0]	1
0xBB0250E4	METER_GLB_CTRL [28].RESERVED[31:17]	15
0xBB0250E4	METER_GLB_CTRL [28].RATE[16:0]	17
0xBB0250E8	METER_GLB_CTRL [28].RESERVED[31:17]	15
0xBB0250E8	METER_GLB_CTRL [28].BUCKET_SIZE[16:1]	16
0xBB0250E8	METER_GLB_CTRL [28].IFG[0:0]	1
0xBB0250EC	METER_GLB_CTRL [29].RESERVED[31:17]	15



Address	Register	Len
0xBB0250EC	METER_GLB_CTRL [29].RATE[16:0]	17
0xBB0250F0	METER_GLB_CTRL [29].RESERVED[31:17]	15
0xBB0250F0	METER_GLB_CTRL [29].BUCKET_SIZE[16:1]	16
0xBB0250F0	METER_GLB_CTRL [29].IFG[0:0]	1
0xBB0250F4	METER_GLB_CTRL [30].RESERVED[31:17]	15
0xBB0250F4	METER_GLB_CTRL [30].RATE[16:0]	17
0xBB0250F8	METER_GLB_CTRL [30].RESERVED[31:17]	15
0xBB0250F8	METER_GLB_CTRL [30].BUCKET_SIZE[16:1]	16
0xBB0250F8	METER_GLB_CTRL [30].IFG[0:0]	1
0xBB0250FC	METER_GLB_CTRL [31].RESERVED[31:17]	15
0xBB0250FC	METER_GLB_CTRL [31].RATE[16:0]	17
0xBB025100	METER_GLB_CTRL [31].RESERVED[31:17]	15
0xBB025100	METER_GLB_CTRL [31].BUCKET_SIZE[16:1]	16
0xBB025100	METER_GLB_CTRL [31].IFG[0:0]	1
0xBB025104	METER_LB_EXCEED_STS [0].LB_EXCEED[0:0]	1
0xBB025104	METER_LB_EXCEED_STS [1].LB_EXCEED[1:1]	1
0xBB025104	METER_LB_EXCEED_STS [2].LB_EXCEED[2:2]	1
0xBB025104	METER_LB_EXCEED_STS [3].LB_EXCEED[3:3]	1
0xBB025104	METER_LB_EXCEED_STS [4].LB_EXCEED[4:4]	1
0xBB025104	METER_LB_EXCEED_STS [5].LB_EXCEED[5:5]	1
0xBB025104	METER_LB_EXCEED_STS [6].LB_EXCEED[6:6]	1
0xBB025104	METER_LB_EXCEED_STS [7].LB_EXCEED[7:7]	1
0xBB025104	METER_LB_EXCEED_STS [8].LB_EXCEED[8:8]	1
0xBB025104	METER_LB_EXCEED_STS [9].LB_EXCEED[9:9]	1
0xBB025104	METER_LB_EXCEED_STS [10].LB_EXCEED[10:10]	1
0xBB025104	METER_LB_EXCEED_STS [11].LB_EXCEED[11:11]	1
0xBB025104	METER_LB_EXCEED_STS [12].LB_EXCEED[12:12]	1
0xBB025104	METER_LB_EXCEED_STS [13].LB_EXCEED[13:13]	1
0xBB025104	METER_LB_EXCEED_STS [14].LB_EXCEED[14:14]	1
0xBB025104	METER_LB_EXCEED_STS [15].LB_EXCEED[15:15]	1
0xBB025104	METER_LB_EXCEED_STS [16].LB_EXCEED[16:16]	1
0xBB025104	METER_LB_EXCEED_STS [17].LB_EXCEED[17:17]	1
0xBB025104	METER_LB_EXCEED_STS [18].LB_EXCEED[18:18]	1
0xBB025104	METER_LB_EXCEED_STS [19].LB_EXCEED[19:19]	1
0xBB025104	METER_LB_EXCEED_STS [20].LB_EXCEED[20:20]	1
0xBB025104	METER_LB_EXCEED_STS [21].LB_EXCEED[21:21]	1
0xBB025104	METER_LB_EXCEED_STS [22].LB_EXCEED[22:22]	1
0xBB025104	METER_LB_EXCEED_STS [23].LB_EXCEED[23:23]	1
0xBB025104	METER_LB_EXCEED_STS [24].LB_EXCEED[24:24]	1
0xBB025104	METER_LB_EXCEED_STS [25].LB_EXCEED[25:25]	1
0xBB025104	METER_LB_EXCEED_STS [26].LB_EXCEED[26:26]	1
0xBB025104	METER_LB_EXCEED_STS [27].LB_EXCEED[27:27]	1
0xBB025104	METER_LB_EXCEED_STS [28].LB_EXCEED[28:28]	1
0xBB025104	METER_LB_EXCEED_STS [29].LB_EXCEED[29:29]	1
0xBB025104	METER_LB_EXCEED_STS [30].LB_EXCEED[30:30]	1
0xBB025104	METER_LB_EXCEED_STS [31].LB_EXCEED[31:31]	1



Address	Register	Len
0xBB025108	PON_TB_CTRL.RESERVED[31:17]	15
0xBB025108	PON_TB_CTRL.METER_OP[16:16]	1
0xBB025108	PON_TB_CTRL.TICK_PERIOD[15:8]	8
0xBB025108	PON_TB_CTRL.TKN[7:0]	8
0xBB02510C	METER_PKT_RATE.SHMTR_PKT_RATE[31:0]	32
0xBB025110	RGF_VER_ALE_METER.REGFILE_VER[31:0]	32
0xBB025114	RSVD_ALE_METER [0].RSVD_MEM[31:0]	32
0xBB025118	RSVD_ALE_METER [1].RSVD_MEM[31:0]	32
0xBB02511C	RSVD_ALE_METER [2].RSVD_MEM[31:0]	32
0xBB025120	RSVD_ALE_METER [3].RSVD_MEM[31:0]	32
0xBB025124	RSVD_ALE_METER [4].RSVD_MEM[31:0]	32
0xBB025128	RSVD_ALE_METER [5].RSVD_MEM[31:0]	32
0xBB02512C	RSVD_ALE_METER [6].RSVD_MEM[31:0]	32
0xBB025130	RSVD_ALE_METER [7].RSVD_MEM[31:0]	32
0xBB025134	RSVD_ALE_METER [8].RSVD_MEM[31:0]	32
0xBB025138	RSVD_ALE_METER [9].RSVD_MEM[31:0]	32
0xBB02513C	RSVD_ALE_METER [10].RSVD_MEM[31:0]	32
0xBB025140	RSVD_ALE_METER [11].RSVD_MEM[31:0]	32
0xBB025144	RSVD_ALE_METER [12].RSVD_MEM[31:0]	32
0xBB025148	RSVD_ALE_METER [13].RSVD_MEM[31:0]	32
0xBB02514C	RSVD_ALE_METER [14].RSVD_MEM[31:0]	32
0xBB025150	RSVD_ALE_METER [15].RSVD_MEM[31:0]	32
0xBB026000	DOS_EN [0].EN[0:0]	1
0xBB026000	DOS_EN [1].EN[1:1]	1
0xBB026000	DOS_EN [2].EN[2:2]	1
0xBB026000	DOS_EN [3].EN[3:3]	1
0xBB026000	DOS_EN [4].EN[4:4]	1
0xBB026000	DOS_EN [5].EN[5:5]	1
0xBB026000	DOS_EN [6].EN[6:6]	1
0xBB026004	DOS_CFG.DOS_ICMPFLOOD_ACT[31:31]	1
0xBB026004	DOS_CFG.DOS_FINFLOOD_ACT[30:30]	1
0xBB026004	DOS_CFG.DOS_SYNFLOOD_ACT[29:29]	1
0xBB026004	DOS_CFG.DOS_SYNWITHDATA_ACT[28:28]	1
0xBB026004	DOS_CFG.DOS_UDPBOMB_ACT[27:27]	1
0xBB026004	DOS_CFG.DOS_PINGOFDEATH_ACT[26:26]	1
0xBB026004	DOS_CFG.DOS_ICMPFRAGMENT_ACT[25:25]	1
0xBB026004	DOS_CFG.DOS_TCPFRAGERERROR_ACT[24:24]	1
0xBB026004	DOS_CFG.DOS_TCPSHORTHDR_ACT[23:23]	1
0xBB026004	DOS_CFG.DOS_SYN1024_ACT[22:22]	1
0xBB026004	DOS_CFG.DOS_NULLSCAN_ACT[21:21]	1
0xBB026004	DOS_CFG.DOS_XMASCAN_ACT[20:20]	1
0xBB026004	DOS_CFG.DOS_SYNFINSCAN_ACT[19:19]	1
0xBB026004	DOS_CFG.DOS_BLATATTACKS_ACT[18:18]	1
0xBB026004	DOS_CFG.DOS_LANDATTACKS_ACT[17:17]	1
0xBB026004	DOS_CFG.DOS_DAEQSA_ACT[16:16]	1
0xBB026004	DOS_CFG.DOS_ICMPFLOOD[15:15]	1

Address	Register	Len
0xBB026004	DOS_CFG.DOS_FINFLOOD[14:14]	1
0xBB026004	DOS_CFG.DOS_SYNFLOOD[13:13]	1
0xBB026004	DOS_CFG.DOS_SYNWITHDATA[12:12]	1
0xBB026004	DOS_CFG.DOS_UDPBOMB[11:11]	1
0xBB026004	DOS_CFG.DOS_PINGOFDEATH[10:10]	1
0xBB026004	DOS_CFG.DOS_ICMPFRAGMENT[9:9]	1
0xBB026004	DOS_CFG.DOS_TCPFRAGERROR[8:8]	1
0xBB026004	DOS_CFG.DOS_TCPSHORTHDR[7:7]	1
0xBB026004	DOS_CFG.DOS_SYN1024[6:6]	1
0xBB026004	DOS_CFG.DOS_NULLSCAN[5:5]	1
0xBB026004	DOS_CFG.DOS_XMASCAN[4:4]	1
0xBB026004	DOS_CFG.DOS_SYNFINSCAN[3:3]	1
0xBB026004	DOS_CFG.DOS_BLATATTACKS[2:2]	1
0xBB026004	DOS_CFG.DOS_LANDATTACKS[1:1]	1
0xBB026004	DOS_CFG.DOS_DAEQSA[0:0]	1
0xBB026008	DOS_SYNFLOOD_TH.RESERVED[31:8]	24
0xBB026008	DOS_SYNFLOOD_TH.TH[7:0]	8
0xBB02600C	DOS_FINFLOOD_TH.RESERVED[31:8]	24
0xBB02600C	DOS_FINFLOOD_TH.TH[7:0]	8
0xBB026010	DOS_ICMPFLOOD_TH.RESERVED[31:8]	24
0xBB026010	DOS_ICMPFLOOD_TH.TH[7:0]	8
0xBB026014	RGF_VER_ALE_RMA_ATTACK.REGFILE_VER[31:0]	32
0xBB026018	RSVD_ALE_RMA_ATTACK [0].RSVD_MEM[31:0]	32
0xBB02601C	RSVD_ALE_RMA_ATTACK [1].RSVD_MEM[31:0]	32
0xBB026020	RSVD_ALE_RMA_ATTACK [2].RSVD_MEM[31:0]	32
0xBB026024	RSVD_ALE_RMA_ATTACK [3].RSVD_MEM[31:0]	32
0xBB026028	RSVD_ALE_RMA_ATTACK [4].RSVD_MEM[31:0]	32
0xBB02602C	RSVD_ALE_RMA_ATTACK [5].RSVD_MEM[31:0]	32
0xBB026030	RSVD_ALE_RMA_ATTACK [6].RSVD_MEM[31:0]	32
0xBB026034	RSVD_ALE_RMA_ATTACK [7].RSVD_MEM[31:0]	32
0xBB026038	RSVD_ALE_RMA_ATTACK [8].RSVD_MEM[31:0]	32
0xBB02603C	RSVD_ALE_RMA_ATTACK [9].RSVD_MEM[31:0]	32
0xBB026040	RSVD_ALE_RMA_ATTACK [10].RSVD_MEM[31:0]	32
0xBB026044	RSVD_ALE_RMA_ATTACK [11].RSVD_MEM[31:0]	32
0xBB026048	RSVD_ALE_RMA_ATTACK [12].RSVD_MEM[31:0]	32
0xBB02604C	RSVD_ALE_RMA_ATTACK [13].RSVD_MEM[31:0]	32
0xBB026050	RSVD_ALE_RMA_ATTACK [14].RSVD_MEM[31:0]	32
0xBB026054	RSVD_ALE_RMA_ATTACK [15].RSVD_MEM[31:0]	32
0xBB027000	PISO_P_MODE0_CTRL [0].PORTMASK[12:0]	13
0xBB027000	PISO_P_MODE0_CTRL [1].PORTMASK[25:13]	13
0xBB027004	PISO_P_MODE0_CTRL [2].PORTMASK[12:0]	13
0xBB027004	PISO_P_MODE0_CTRL [3].PORTMASK[25:13]	13
0xBB027008	PISO_P_MODE0_CTRL [4].PORTMASK[12:0]	13
0xBB027008	PISO_P_MODE0_CTRL [5].PORTMASK[25:13]	13
0xBB02700C	PISO_P_MODE0_CTRL [6].PORTMASK[12:0]	13
0xBB027010	PISO_P_MODE1_CTRL [0].PORTMASK[12:0]	13

Address	Register	Len
0xBB027010	PISO_P_MODE1_CTRL [1].PORTMASK[25:13]	13
0xBB027014	PISO_P_MODE1_CTRL [2].PORTMASK[12:0]	13
0xBB027014	PISO_P_MODE1_CTRL [3].PORTMASK[25:13]	13
0xBB027018	PISO_P_MODE1_CTRL [4].PORTMASK[12:0]	13
0xBB027018	PISO_P_MODE1_CTRL [5].PORTMASK[25:13]	13
0xBB02701C	PISO_P_MODE1_CTRL [6].PORTMASK[12:0]	13
0xBB027020	PISO_EXT_MODE0_CTRL [0].PORTMASK[12:0]	13
0xBB027020	PISO_EXT_MODE0_CTRL [1].PORTMASK[25:13]	13
0xBB027024	PISO_EXT_MODE0_CTRL [2].PORTMASK[12:0]	13
0xBB027024	PISO_EXT_MODE0_CTRL [3].PORTMASK[25:13]	13
0xBB027028	PISO_EXT_MODE0_CTRL [4].PORTMASK[12:0]	13
0xBB02702C	PISO_EXT_MODE1_CTRL [0].PORTMASK[12:0]	13
0xBB02702C	PISO_EXT_MODE1_CTRL [1].PORTMASK[25:13]	13
0xBB027030	PISO_EXT_MODE1_CTRL [2].PORTMASK[12:0]	13
0xBB027030	PISO_EXT_MODE1_CTRL [3].PORTMASK[25:13]	13
0xBB027034	PISO_EXT_MODE1_CTRL [4].PORTMASK[12:0]	13
0xBB027038	PISO_CTRL.RESERVED[31:2]	30
0xBB027038	PISO_CTRL.CTAG_SEL[1:1]	1
0xBB027038	PISO_CTRL.L34_SEL[0:0]	1
0xBB02703C	RGF_VER_ALE_PISO.REGFILE_VER[31:0]	32
0xBB027040	RSVD_ALE_PISO [0].RSVD_MEM[31:0]	32
0xBB027044	RSVD_ALE_PISO [1].RSVD_MEM[31:0]	32
0xBB027048	RSVD_ALE_PISO [2].RSVD_MEM[31:0]	32
0xBB02704C	RSVD_ALE_PISO [3].RSVD_MEM[31:0]	32
0xBB027050	RSVD_ALE_PISO [4].RSVD_MEM[31:0]	32
0xBB027054	RSVD_ALE_PISO [5].RSVD_MEM[31:0]	32
0xBB027058	RSVD_ALE_PISO [6].RSVD_MEM[31:0]	32
0xBB02705C	RSVD_ALE_PISO [7].RSVD_MEM[31:0]	32
0xBB027060	RSVD_ALE_PISO [8].RSVD_MEM[31:0]	32
0xBB027064	RSVD_ALE_PISO [9].RSVD_MEM[31:0]	32
0xBB027068	RSVD_ALE_PISO [10].RSVD_MEM[31:0]	32
0xBB02706C	RSVD_ALE_PISO [11].RSVD_MEM[31:0]	32
0xBB027070	RSVD_ALE_PISO [12].RSVD_MEM[31:0]	32
0xBB027074	RSVD_ALE_PISO [13].RSVD_MEM[31:0]	32
0xBB027078	RSVD_ALE_PISO [14].RSVD_MEM[31:0]	32
0xBB02707C	RSVD_ALE_PISO [15].RSVD_MEM[31:0]	32
0xBB028000	HSB_CTRL.RESERVED[31:5]	27
0xBB028000	HSB_CTRL.LATCH_MODE[4:2]	3
0xBB028000	HSB_CTRL.SEL[1:1]	1
0xBB028000	HSB_CTRL.VALID[0:0]	1
0xBB028040	HSB_DATA [0].DATA[31:0]	32
0xBB028044	HSB_DATA [1].DATA[31:0]	32
0xBB028048	HSB_DATA [2].DATA[31:0]	32
0xBB02804C	HSB_DATA [3].DATA[31:0]	32
0xBB028050	HSB_DATA [4].DATA[31:0]	32
0xBB028054	HSB_DATA [5].DATA[31:0]	32

Address	Register	Len
0xBB028058	HSB_DATA [6].DATA[31:0]	32
0xBB02805C	HSB_DATA [7].DATA[31:0]	32
0xBB028060	HSB_DATA [8].DATA[31:0]	32
0xBB028064	HSB_DATA [9].DATA[31:0]	32
0xBB028068	HSB_DATA [10].DATA[31:0]	32
0xBB02806C	HSB_DATA [11].DATA[31:0]	32
0xBB028070	HSB_DATA [12].DATA[31:0]	32
0xBB028074	HSB_DATA [13].DATA[31:0]	32
0xBB028078	HSB_DATA [14].DATA[31:0]	32
0xBB02807C	HSB_DATA [15].DATA[31:0]	32
0xBB028080	HSB_DATA [16].DATA[31:0]	32
0xBB028084	HSB_DATA [17].DATA[31:0]	32
0xBB028088	HSB_DATA [18].DATA[31:0]	32
0xBB02808C	HSB_DATA [19].DATA[31:0]	32
0xBB0280C0	HSA_DATA [0].DATA[31:0]	32
0xBB0280C4	HSA_DATA [1].DATA[31:0]	32
0xBB0280C8	HSA_DATA [2].DATA[31:0]	32
0xBB0280CC	HSA_DATA [3].DATA[31:0]	32
0xBB0280D0	HSA_DATA [4].DATA[31:0]	32
0xBB0280D4	HSA_DATA [5].DATA[31:0]	32
0xBB0280D8	HSA_DATA [6].DATA[31:0]	32
0xBB0280DC	HSA_DATA [7].DATA[31:0]	32
0xBB0280E0	HSA_DATA [8].DATA[31:0]	32
0xBB0280E4	HSA_DATA [9].DATA[31:0]	32
0xBB0280E8	HSA_DATA [10].DATA[31:0]	32
0xBB0280EC	HSA_DATA [11].DATA[31:0]	32
0xBB0280F0	HSA_DATA [12].DATA[31:0]	32
0xBB02A000	SVLAN_SP2C [0].RESERVED[31:22]	10
0xBB02A000	SVLAN_SP2C [0].VID[21:10]	12
0xBB02A000	SVLAN_SP2C [0].DST_PORT[9:7]	3
0xBB02A000	SVLAN_SP2C [0].SVIDX[6:1]	6
0xBB02A000	SVLAN_SP2C [0].VALID[0:0]	1
0xBB02A004	SVLAN_SP2C [1].RESERVED[31:22]	10
0xBB02A004	SVLAN_SP2C [1].VID[21:10]	12
0xBB02A004	SVLAN_SP2C [1].DST_PORT[9:7]	3
0xBB02A004	SVLAN_SP2C [1].SVIDX[6:1]	6
0xBB02A004	SVLAN_SP2C [1].VALID[0:0]	1
0xBB02A008	SVLAN_SP2C [2].RESERVED[31:22]	10
0xBB02A008	SVLAN_SP2C [2].VID[21:10]	12
0xBB02A008	SVLAN_SP2C [2].DST_PORT[9:7]	3
0xBB02A008	SVLAN_SP2C [2].SVIDX[6:1]	6
0xBB02A008	SVLAN_SP2C [2].VALID[0:0]	1
0xBB02A00C	SVLAN_SP2C [3].RESERVED[31:22]	10
0xBB02A00C	SVLAN_SP2C [3].VID[21:10]	12
0xBB02A00C	SVLAN_SP2C [3].DST_PORT[9:7]	3
0xBB02A00C	SVLAN_SP2C [3].SVIDX[6:1]	6

Address	Register	Len
0xBB02A00C	SVLAN_SP2C [3].VALID[0:0]	1
0xBB02A010	SVLAN_SP2C [4].RESERVED[31:22]	10
0xBB02A010	SVLAN_SP2C [4].VID[21:10]	12
0xBB02A010	SVLAN_SP2C [4].DST_PORT[9:7]	3
0xBB02A010	SVLAN_SP2C [4].SVIDX[6:1]	6
0xBB02A010	SVLAN_SP2C [4].VALID[0:0]	1
0xBB02A014	SVLAN_SP2C [5].RESERVED[31:22]	10
0xBB02A014	SVLAN_SP2C [5].VID[21:10]	12
0xBB02A014	SVLAN_SP2C [5].DST_PORT[9:7]	3
0xBB02A014	SVLAN_SP2C [5].SVIDX[6:1]	6
0xBB02A014	SVLAN_SP2C [5].VALID[0:0]	1
0xBB02A018	SVLAN_SP2C [6].RESERVED[31:22]	10
0xBB02A018	SVLAN_SP2C [6].VID[21:10]	12
0xBB02A018	SVLAN_SP2C [6].DST_PORT[9:7]	3
0xBB02A018	SVLAN_SP2C [6].SVIDX[6:1]	6
0xBB02A018	SVLAN_SP2C [6].VALID[0:0]	1
0xBB02A01C	SVLAN_SP2C [7].RESERVED[31:22]	10
0xBB02A01C	SVLAN_SP2C [7].VID[21:10]	12
0xBB02A01C	SVLAN_SP2C [7].DST_PORT[9:7]	3
0xBB02A01C	SVLAN_SP2C [7].SVIDX[6:1]	6
0xBB02A01C	SVLAN_SP2C [7].VALID[0:0]	1
0xBB02A020	SVLAN_SP2C [8].RESERVED[31:22]	10
0xBB02A020	SVLAN_SP2C [8].VID[21:10]	12
0xBB02A020	SVLAN_SP2C [8].DST_PORT[9:7]	3
0xBB02A020	SVLAN_SP2C [8].SVIDX[6:1]	6
0xBB02A020	SVLAN_SP2C [8].VALID[0:0]	1
0xBB02A024	SVLAN_SP2C [9].RESERVED[31:22]	10
0xBB02A024	SVLAN_SP2C [9].VID[21:10]	12
0xBB02A024	SVLAN_SP2C [9].DST_PORT[9:7]	3
0xBB02A024	SVLAN_SP2C [9].SVIDX[6:1]	6
0xBB02A024	SVLAN_SP2C [9].VALID[0:0]	1
0xBB02A028	SVLAN_SP2C [10].RESERVED[31:22]	10
0xBB02A028	SVLAN_SP2C [10].VID[21:10]	12
0xBB02A028	SVLAN_SP2C [10].DST_PORT[9:7]	3
0xBB02A028	SVLAN_SP2C [10].SVIDX[6:1]	6
0xBB02A028	SVLAN_SP2C [10].VALID[0:0]	1
0xBB02A02C	SVLAN_SP2C [11].RESERVED[31:22]	10
0xBB02A02C	SVLAN_SP2C [11].VID[21:10]	12
0xBB02A02C	SVLAN_SP2C [11].DST_PORT[9:7]	3
0xBB02A02C	SVLAN_SP2C [11].SVIDX[6:1]	6
0xBB02A02C	SVLAN_SP2C [11].VALID[0:0]	1
0xBB02A030	SVLAN_SP2C [12].RESERVED[31:22]	10
0xBB02A030	SVLAN_SP2C [12].VID[21:10]	12
0xBB02A030	SVLAN_SP2C [12].DST_PORT[9:7]	3
0xBB02A030	SVLAN_SP2C [12].SVIDX[6:1]	6
0xBB02A030	SVLAN_SP2C [12].VALID[0:0]	1

Address	Register	Len
0xBB02A034	SVLAN_SP2C [13].RESERVED[31:22]	10
0xBB02A034	SVLAN_SP2C [13].VID[21:10]	12
0xBB02A034	SVLAN_SP2C [13].DST_PORT[9:7]	3
0xBB02A034	SVLAN_SP2C [13].SVIDX[6:1]	6
0xBB02A034	SVLAN_SP2C [13].VALID[0:0]	1
0xBB02A038	SVLAN_SP2C [14].RESERVED[31:22]	10
0xBB02A038	SVLAN_SP2C [14].VID[21:10]	12
0xBB02A038	SVLAN_SP2C [14].DST_PORT[9:7]	3
0xBB02A038	SVLAN_SP2C [14].SVIDX[6:1]	6
0xBB02A038	SVLAN_SP2C [14].VALID[0:0]	1
0xBB02A03C	SVLAN_SP2C [15].RESERVED[31:22]	10
0xBB02A03C	SVLAN_SP2C [15].VID[21:10]	12
0xBB02A03C	SVLAN_SP2C [15].DST_PORT[9:7]	3
0xBB02A03C	SVLAN_SP2C [15].SVIDX[6:1]	6
0xBB02A03C	SVLAN_SP2C [15].VALID[0:0]	1
0xBB02A040	SVLAN_SP2C [16].RESERVED[31:22]	10
0xBB02A040	SVLAN_SP2C [16].VID[21:10]	12
0xBB02A040	SVLAN_SP2C [16].DST_PORT[9:7]	3
0xBB02A040	SVLAN_SP2C [16].SVIDX[6:1]	6
0xBB02A040	SVLAN_SP2C [16].VALID[0:0]	1
0xBB02A044	SVLAN_SP2C [17].RESERVED[31:22]	10
0xBB02A044	SVLAN_SP2C [17].VID[21:10]	12
0xBB02A044	SVLAN_SP2C [17].DST_PORT[9:7]	3
0xBB02A044	SVLAN_SP2C [17].SVIDX[6:1]	6
0xBB02A044	SVLAN_SP2C [17].VALID[0:0]	1
0xBB02A048	SVLAN_SP2C [18].RESERVED[31:22]	10
0xBB02A048	SVLAN_SP2C [18].VID[21:10]	12
0xBB02A048	SVLAN_SP2C [18].DST_PORT[9:7]	3
0xBB02A048	SVLAN_SP2C [18].SVIDX[6:1]	6
0xBB02A048	SVLAN_SP2C [18].VALID[0:0]	1
0xBB02A04C	SVLAN_SP2C [19].RESERVED[31:22]	10
0xBB02A04C	SVLAN_SP2C [19].VID[21:10]	12
0xBB02A04C	SVLAN_SP2C [19].DST_PORT[9:7]	3
0xBB02A04C	SVLAN_SP2C [19].SVIDX[6:1]	6
0xBB02A04C	SVLAN_SP2C [19].VALID[0:0]	1
0xBB02A050	SVLAN_SP2C [20].RESERVED[31:22]	10
0xBB02A050	SVLAN_SP2C [20].VID[21:10]	12
0xBB02A050	SVLAN_SP2C [20].DST_PORT[9:7]	3
0xBB02A050	SVLAN_SP2C [20].SVIDX[6:1]	6
0xBB02A050	SVLAN_SP2C [20].VALID[0:0]	1
0xBB02A054	SVLAN_SP2C [21].RESERVED[31:22]	10
0xBB02A054	SVLAN_SP2C [21].VID[21:10]	12
0xBB02A054	SVLAN_SP2C [21].DST_PORT[9:7]	3
0xBB02A054	SVLAN_SP2C [21].SVIDX[6:1]	6
0xBB02A054	SVLAN_SP2C [21].VALID[0:0]	1
0xBB02A058	SVLAN_SP2C [22].RESERVED[31:22]	10

Address	Register	Len
0xBB02A058	SVLAN_SP2C [22].VID[21:10]	12
0xBB02A058	SVLAN_SP2C [22].DST_PORT[9:7]	3
0xBB02A058	SVLAN_SP2C [22].SVIDX[6:1]	6
0xBB02A058	SVLAN_SP2C [22].VALID[0:0]	1
0xBB02A05C	SVLAN_SP2C [23].RESERVED[31:22]	10
0xBB02A05C	SVLAN_SP2C [23].VID[21:10]	12
0xBB02A05C	SVLAN_SP2C [23].DST_PORT[9:7]	3
0xBB02A05C	SVLAN_SP2C [23].SVIDX[6:1]	6
0xBB02A05C	SVLAN_SP2C [23].VALID[0:0]	1
0xBB02A060	SVLAN_SP2C [24].RESERVED[31:22]	10
0xBB02A060	SVLAN_SP2C [24].VID[21:10]	12
0xBB02A060	SVLAN_SP2C [24].DST_PORT[9:7]	3
0xBB02A060	SVLAN_SP2C [24].SVIDX[6:1]	6
0xBB02A060	SVLAN_SP2C [24].VALID[0:0]	1
0xBB02A064	SVLAN_SP2C [25].RESERVED[31:22]	10
0xBB02A064	SVLAN_SP2C [25].VID[21:10]	12
0xBB02A064	SVLAN_SP2C [25].DST_PORT[9:7]	3
0xBB02A064	SVLAN_SP2C [25].SVIDX[6:1]	6
0xBB02A064	SVLAN_SP2C [25].VALID[0:0]	1
0xBB02A068	SVLAN_SP2C [26].RESERVED[31:22]	10
0xBB02A068	SVLAN_SP2C [26].VID[21:10]	12
0xBB02A068	SVLAN_SP2C [26].DST_PORT[9:7]	3
0xBB02A068	SVLAN_SP2C [26].SVIDX[6:1]	6
0xBB02A068	SVLAN_SP2C [26].VALID[0:0]	1
0xBB02A06C	SVLAN_SP2C [27].RESERVED[31:22]	10
0xBB02A06C	SVLAN_SP2C [27].VID[21:10]	12
0xBB02A06C	SVLAN_SP2C [27].DST_PORT[9:7]	3
0xBB02A06C	SVLAN_SP2C [27].SVIDX[6:1]	6
0xBB02A06C	SVLAN_SP2C [27].VALID[0:0]	1
0xBB02A070	SVLAN_SP2C [28].RESERVED[31:22]	10
0xBB02A070	SVLAN_SP2C [28].VID[21:10]	12
0xBB02A070	SVLAN_SP2C [28].DST_PORT[9:7]	3
0xBB02A070	SVLAN_SP2C [28].SVIDX[6:1]	6
0xBB02A070	SVLAN_SP2C [28].VALID[0:0]	1
0xBB02A074	SVLAN_SP2C [29].RESERVED[31:22]	10
0xBB02A074	SVLAN_SP2C [29].VID[21:10]	12
0xBB02A074	SVLAN_SP2C [29].DST_PORT[9:7]	3
0xBB02A074	SVLAN_SP2C [29].SVIDX[6:1]	6
0xBB02A074	SVLAN_SP2C [29].VALID[0:0]	1
0xBB02A078	SVLAN_SP2C [30].RESERVED[31:22]	10
0xBB02A078	SVLAN_SP2C [30].VID[21:10]	12
0xBB02A078	SVLAN_SP2C [30].DST_PORT[9:7]	3
0xBB02A078	SVLAN_SP2C [30].SVIDX[6:1]	6
0xBB02A078	SVLAN_SP2C [30].VALID[0:0]	1
0xBB02A07C	SVLAN_SP2C [31].RESERVED[31:22]	10
0xBB02A07C	SVLAN_SP2C [31].VID[21:10]	12



Address	Register	Len
0xBB02A07C	SVLAN_SP2C [31].DST_PORT[9:7]	3
0xBB02A07C	SVLAN_SP2C [31].SVIDX[6:1]	6
0xBB02A07C	SVLAN_SP2C [31].VALID[0:0]	1
0xBB02A080	SVLAN_SP2C [32].RESERVED[31:22]	10
0xBB02A080	SVLAN_SP2C [32].VID[21:10]	12
0xBB02A080	SVLAN_SP2C [32].DST_PORT[9:7]	3
0xBB02A080	SVLAN_SP2C [32].SVIDX[6:1]	6
0xBB02A080	SVLAN_SP2C [32].VALID[0:0]	1
0xBB02A084	SVLAN_SP2C [33].RESERVED[31:22]	10
0xBB02A084	SVLAN_SP2C [33].VID[21:10]	12
0xBB02A084	SVLAN_SP2C [33].DST_PORT[9:7]	3
0xBB02A084	SVLAN_SP2C [33].SVIDX[6:1]	6
0xBB02A084	SVLAN_SP2C [33].VALID[0:0]	1
0xBB02A088	SVLAN_SP2C [34].RESERVED[31:22]	10
0xBB02A088	SVLAN_SP2C [34].VID[21:10]	12
0xBB02A088	SVLAN_SP2C [34].DST_PORT[9:7]	3
0xBB02A088	SVLAN_SP2C [34].SVIDX[6:1]	6
0xBB02A088	SVLAN_SP2C [34].VALID[0:0]	1
0xBB02A08C	SVLAN_SP2C [35].RESERVED[31:22]	10
0xBB02A08C	SVLAN_SP2C [35].VID[21:10]	12
0xBB02A08C	SVLAN_SP2C [35].DST_PORT[9:7]	3
0xBB02A08C	SVLAN_SP2C [35].SVIDX[6:1]	6
0xBB02A08C	SVLAN_SP2C [35].VALID[0:0]	1
0xBB02A090	SVLAN_SP2C [36].RESERVED[31:22]	10
0xBB02A090	SVLAN_SP2C [36].VID[21:10]	12
0xBB02A090	SVLAN_SP2C [36].DST_PORT[9:7]	3
0xBB02A090	SVLAN_SP2C [36].SVIDX[6:1]	6
0xBB02A090	SVLAN_SP2C [36].VALID[0:0]	1
0xBB02A094	SVLAN_SP2C [37].RESERVED[31:22]	10
0xBB02A094	SVLAN_SP2C [37].VID[21:10]	12
0xBB02A094	SVLAN_SP2C [37].DST_PORT[9:7]	3
0xBB02A094	SVLAN_SP2C [37].SVIDX[6:1]	6
0xBB02A094	SVLAN_SP2C [37].VALID[0:0]	1
0xBB02A098	SVLAN_SP2C [38].RESERVED[31:22]	10
0xBB02A098	SVLAN_SP2C [38].VID[21:10]	12
0xBB02A098	SVLAN_SP2C [38].DST_PORT[9:7]	3
0xBB02A098	SVLAN_SP2C [38].SVIDX[6:1]	6
0xBB02A098	SVLAN_SP2C [38].VALID[0:0]	1
0xBB02A09C	SVLAN_SP2C [39].RESERVED[31:22]	10
0xBB02A09C	SVLAN_SP2C [39].VID[21:10]	12
0xBB02A09C	SVLAN_SP2C [39].DST_PORT[9:7]	3
0xBB02A09C	SVLAN_SP2C [39].SVIDX[6:1]	6
0xBB02A09C	SVLAN_SP2C [39].VALID[0:0]	1
0xBB02A0A0	SVLAN_SP2C [40].RESERVED[31:22]	10
0xBB02A0A0	SVLAN_SP2C [40].VID[21:10]	12
0xBB02A0A0	SVLAN_SP2C [40].DST_PORT[9:7]	3



Address	Register	Len
0xBB02A0A0	SVLAN_SP2C [40].SVIDX[6:1]	6
0xBB02A0A0	SVLAN_SP2C [40].VALID[0:0]	1
0xBB02A0A4	SVLAN_SP2C [41].RESERVED[31:22]	10
0xBB02A0A4	SVLAN_SP2C [41].VID[21:10]	12
0xBB02A0A4	SVLAN_SP2C [41].DST_PORT[9:7]	3
0xBB02A0A4	SVLAN_SP2C [41].SVIDX[6:1]	6
0xBB02A0A4	SVLAN_SP2C [41].VALID[0:0]	1
0xBB02A0A8	SVLAN_SP2C [42].RESERVED[31:22]	10
0xBB02A0A8	SVLAN_SP2C [42].VID[21:10]	12
0xBB02A0A8	SVLAN_SP2C [42].DST_PORT[9:7]	3
0xBB02A0A8	SVLAN_SP2C [42].SVIDX[6:1]	6
0xBB02A0A8	SVLAN_SP2C [42].VALID[0:0]	1
0xBB02A0AC	SVLAN_SP2C [43].RESERVED[31:22]	10
0xBB02A0AC	SVLAN_SP2C [43].VID[21:10]	12
0xBB02A0AC	SVLAN_SP2C [43].DST_PORT[9:7]	3
0xBB02A0AC	SVLAN_SP2C [43].SVIDX[6:1]	6
0xBB02A0AC	SVLAN_SP2C [43].VALID[0:0]	1
0xBB02A0B0	SVLAN_SP2C [44].RESERVED[31:22]	10
0xBB02A0B0	SVLAN_SP2C [44].VID[21:10]	12
0xBB02A0B0	SVLAN_SP2C [44].DST_PORT[9:7]	3
0xBB02A0B0	SVLAN_SP2C [44].SVIDX[6:1]	6
0xBB02A0B0	SVLAN_SP2C [44].VALID[0:0]	1
0xBB02A0B4	SVLAN_SP2C [45].RESERVED[31:22]	10
0xBB02A0B4	SVLAN_SP2C [45].VID[21:10]	12
0xBB02A0B4	SVLAN_SP2C [45].DST_PORT[9:7]	3
0xBB02A0B4	SVLAN_SP2C [45].SVIDX[6:1]	6
0xBB02A0B4	SVLAN_SP2C [45].VALID[0:0]	1
0xBB02A0B8	SVLAN_SP2C [46].RESERVED[31:22]	10
0xBB02A0B8	SVLAN_SP2C [46].VID[21:10]	12
0xBB02A0B8	SVLAN_SP2C [46].DST_PORT[9:7]	3
0xBB02A0B8	SVLAN_SP2C [46].SVIDX[6:1]	6
0xBB02A0B8	SVLAN_SP2C [46].VALID[0:0]	1
0xBB02A0BC	SVLAN_SP2C [47].RESERVED[31:22]	10
0xBB02A0BC	SVLAN_SP2C [47].VID[21:10]	12
0xBB02A0BC	SVLAN_SP2C [47].DST_PORT[9:7]	3
0xBB02A0BC	SVLAN_SP2C [47].SVIDX[6:1]	6
0xBB02A0BC	SVLAN_SP2C [47].VALID[0:0]	1
0xBB02A0C0	SVLAN_SP2C [48].RESERVED[31:22]	10
0xBB02A0C0	SVLAN_SP2C [48].VID[21:10]	12
0xBB02A0C0	SVLAN_SP2C [48].DST_PORT[9:7]	3
0xBB02A0C0	SVLAN_SP2C [48].SVIDX[6:1]	6
0xBB02A0C0	SVLAN_SP2C [48].VALID[0:0]	1
0xBB02A0C4	SVLAN_SP2C [49].RESERVED[31:22]	10
0xBB02A0C4	SVLAN_SP2C [49].VID[21:10]	12
0xBB02A0C4	SVLAN_SP2C [49].DST_PORT[9:7]	3
0xBB02A0C4	SVLAN_SP2C [49].SVIDX[6:1]	6

Address	Register	Len
0xBB02A0C4	SVLAN_SP2C [49].VALID[0:0]	1
0xBB02A0C8	SVLAN_SP2C [50].RESERVED[31:22]	10
0xBB02A0C8	SVLAN_SP2C [50].VID[21:10]	12
0xBB02A0C8	SVLAN_SP2C [50].DST_PORT[9:7]	3
0xBB02A0C8	SVLAN_SP2C [50].SVIDX[6:1]	6
0xBB02A0C8	SVLAN_SP2C [50].VALID[0:0]	1
0xBB02A0CC	SVLAN_SP2C [51].RESERVED[31:22]	10
0xBB02A0CC	SVLAN_SP2C [51].VID[21:10]	12
0xBB02A0CC	SVLAN_SP2C [51].DST_PORT[9:7]	3
0xBB02A0CC	SVLAN_SP2C [51].SVIDX[6:1]	6
0xBB02A0CC	SVLAN_SP2C [51].VALID[0:0]	1
0xBB02A0D0	SVLAN_SP2C [52].RESERVED[31:22]	10
0xBB02A0D0	SVLAN_SP2C [52].VID[21:10]	12
0xBB02A0D0	SVLAN_SP2C [52].DST_PORT[9:7]	3
0xBB02A0D0	SVLAN_SP2C [52].SVIDX[6:1]	6
0xBB02A0D0	SVLAN_SP2C [52].VALID[0:0]	1
0xBB02A0D4	SVLAN_SP2C [53].RESERVED[31:22]	10
0xBB02A0D4	SVLAN_SP2C [53].VID[21:10]	12
0xBB02A0D4	SVLAN_SP2C [53].DST_PORT[9:7]	3
0xBB02A0D4	SVLAN_SP2C [53].SVIDX[6:1]	6
0xBB02A0D4	SVLAN_SP2C [53].VALID[0:0]	1
0xBB02A0D8	SVLAN_SP2C [54].RESERVED[31:22]	10
0xBB02A0D8	SVLAN_SP2C [54].VID[21:10]	12
0xBB02A0D8	SVLAN_SP2C [54].DST_PORT[9:7]	3
0xBB02A0D8	SVLAN_SP2C [54].SVIDX[6:1]	6
0xBB02A0D8	SVLAN_SP2C [54].VALID[0:0]	1
0xBB02A0DC	SVLAN_SP2C [55].RESERVED[31:22]	10
0xBB02A0DC	SVLAN_SP2C [55].VID[21:10]	12
0xBB02A0DC	SVLAN_SP2C [55].DST_PORT[9:7]	3
0xBB02A0DC	SVLAN_SP2C [55].SVIDX[6:1]	6
0xBB02A0DC	SVLAN_SP2C [55].VALID[0:0]	1
0xBB02A0E0	SVLAN_SP2C [56].RESERVED[31:22]	10
0xBB02A0E0	SVLAN_SP2C [56].VID[21:10]	12
0xBB02A0E0	SVLAN_SP2C [56].DST_PORT[9:7]	3
0xBB02A0E0	SVLAN_SP2C [56].SVIDX[6:1]	6
0xBB02A0E0	SVLAN_SP2C [56].VALID[0:0]	1
0xBB02A0E4	SVLAN_SP2C [57].RESERVED[31:22]	10
0xBB02A0E4	SVLAN_SP2C [57].VID[21:10]	12
0xBB02A0E4	SVLAN_SP2C [57].DST_PORT[9:7]	3
0xBB02A0E4	SVLAN_SP2C [57].SVIDX[6:1]	6
0xBB02A0E4	SVLAN_SP2C [57].VALID[0:0]	1
0xBB02A0E8	SVLAN_SP2C [58].RESERVED[31:22]	10
0xBB02A0E8	SVLAN_SP2C [58].VID[21:10]	12
0xBB02A0E8	SVLAN_SP2C [58].DST_PORT[9:7]	3
0xBB02A0E8	SVLAN_SP2C [58].SVIDX[6:1]	6
0xBB02A0E8	SVLAN_SP2C [58].VALID[0:0]	1

Address	Register	Len
0xBB02A0EC	SVLAN_SP2C [59].RESERVED[31:22]	10
0xBB02A0EC	SVLAN_SP2C [59].VID[21:10]	12
0xBB02A0EC	SVLAN_SP2C [59].DST_PORT[9:7]	3
0xBB02A0EC	SVLAN_SP2C [59].SVIDX[6:1]	6
0xBB02A0EC	SVLAN_SP2C [59].VALID[0:0]	1
0xBB02A0F0	SVLAN_SP2C [60].RESERVED[31:22]	10
0xBB02A0F0	SVLAN_SP2C [60].VID[21:10]	12
0xBB02A0F0	SVLAN_SP2C [60].DST_PORT[9:7]	3
0xBB02A0F0	SVLAN_SP2C [60].SVIDX[6:1]	6
0xBB02A0F0	SVLAN_SP2C [60].VALID[0:0]	1
0xBB02A0F4	SVLAN_SP2C [61].RESERVED[31:22]	10
0xBB02A0F4	SVLAN_SP2C [61].VID[21:10]	12
0xBB02A0F4	SVLAN_SP2C [61].DST_PORT[9:7]	3
0xBB02A0F4	SVLAN_SP2C [61].SVIDX[6:1]	6
0xBB02A0F4	SVLAN_SP2C [61].VALID[0:0]	1
0xBB02A0F8	SVLAN_SP2C [62].RESERVED[31:22]	10
0xBB02A0F8	SVLAN_SP2C [62].VID[21:10]	12
0xBB02A0F8	SVLAN_SP2C [62].DST_PORT[9:7]	3
0xBB02A0F8	SVLAN_SP2C [62].SVIDX[6:1]	6
0xBB02A0F8	SVLAN_SP2C [62].VALID[0:0]	1
0xBB02A0FC	SVLAN_SP2C [63].RESERVED[31:22]	10
0xBB02A0FC	SVLAN_SP2C [63].VID[21:10]	12
0xBB02A0FC	SVLAN_SP2C [63].DST_PORT[9:7]	3
0xBB02A0FC	SVLAN_SP2C [63].SVIDX[6:1]	6
0xBB02A0FC	SVLAN_SP2C [63].VALID[0:0]	1
0xBB02A100	SVLAN_SP2C [64].RESERVED[31:22]	10
0xBB02A100	SVLAN_SP2C [64].VID[21:10]	12
0xBB02A100	SVLAN_SP2C [64].DST_PORT[9:7]	3
0xBB02A100	SVLAN_SP2C [64].SVIDX[6:1]	6
0xBB02A100	SVLAN_SP2C [64].VALID[0:0]	1
0xBB02A104	SVLAN_SP2C [65].RESERVED[31:22]	10
0xBB02A104	SVLAN_SP2C [65].VID[21:10]	12
0xBB02A104	SVLAN_SP2C [65].DST_PORT[9:7]	3
0xBB02A104	SVLAN_SP2C [65].SVIDX[6:1]	6
0xBB02A104	SVLAN_SP2C [65].VALID[0:0]	1
0xBB02A108	SVLAN_SP2C [66].RESERVED[31:22]	10
0xBB02A108	SVLAN_SP2C [66].VID[21:10]	12
0xBB02A108	SVLAN_SP2C [66].DST_PORT[9:7]	3
0xBB02A108	SVLAN_SP2C [66].SVIDX[6:1]	6
0xBB02A108	SVLAN_SP2C [66].VALID[0:0]	1
0xBB02A10C	SVLAN_SP2C [67].RESERVED[31:22]	10
0xBB02A10C	SVLAN_SP2C [67].VID[21:10]	12
0xBB02A10C	SVLAN_SP2C [67].DST_PORT[9:7]	3
0xBB02A10C	SVLAN_SP2C [67].SVIDX[6:1]	6
0xBB02A10C	SVLAN_SP2C [67].VALID[0:0]	1
0xBB02A110	SVLAN_SP2C [68].RESERVED[31:22]	10

Address	Register	Len
0xBB02A110	SVLAN_SP2C [68].VID[21:10]	12
0xBB02A110	SVLAN_SP2C [68].DST_PORT[9:7]	3
0xBB02A110	SVLAN_SP2C [68].SVIDX[6:1]	6
0xBB02A110	SVLAN_SP2C [68].VALID[0:0]	1
0xBB02A114	SVLAN_SP2C [69].RESERVED[31:22]	10
0xBB02A114	SVLAN_SP2C [69].VID[21:10]	12
0xBB02A114	SVLAN_SP2C [69].DST_PORT[9:7]	3
0xBB02A114	SVLAN_SP2C [69].SVIDX[6:1]	6
0xBB02A114	SVLAN_SP2C [69].VALID[0:0]	1
0xBB02A118	SVLAN_SP2C [70].RESERVED[31:22]	10
0xBB02A118	SVLAN_SP2C [70].VID[21:10]	12
0xBB02A118	SVLAN_SP2C [70].DST_PORT[9:7]	3
0xBB02A118	SVLAN_SP2C [70].SVIDX[6:1]	6
0xBB02A118	SVLAN_SP2C [70].VALID[0:0]	1
0xBB02A11C	SVLAN_SP2C [71].RESERVED[31:22]	10
0xBB02A11C	SVLAN_SP2C [71].VID[21:10]	12
0xBB02A11C	SVLAN_SP2C [71].DST_PORT[9:7]	3
0xBB02A11C	SVLAN_SP2C [71].SVIDX[6:1]	6
0xBB02A11C	SVLAN_SP2C [71].VALID[0:0]	1
0xBB02A120	SVLAN_SP2C [72].RESERVED[31:22]	10
0xBB02A120	SVLAN_SP2C [72].VID[21:10]	12
0xBB02A120	SVLAN_SP2C [72].DST_PORT[9:7]	3
0xBB02A120	SVLAN_SP2C [72].SVIDX[6:1]	6
0xBB02A120	SVLAN_SP2C [72].VALID[0:0]	1
0xBB02A124	SVLAN_SP2C [73].RESERVED[31:22]	10
0xBB02A124	SVLAN_SP2C [73].VID[21:10]	12
0xBB02A124	SVLAN_SP2C [73].DST_PORT[9:7]	3
0xBB02A124	SVLAN_SP2C [73].SVIDX[6:1]	6
0xBB02A124	SVLAN_SP2C [73].VALID[0:0]	1
0xBB02A128	SVLAN_SP2C [74].RESERVED[31:22]	10
0xBB02A128	SVLAN_SP2C [74].VID[21:10]	12
0xBB02A128	SVLAN_SP2C [74].DST_PORT[9:7]	3
0xBB02A128	SVLAN_SP2C [74].SVIDX[6:1]	6
0xBB02A128	SVLAN_SP2C [74].VALID[0:0]	1
0xBB02A12C	SVLAN_SP2C [75].RESERVED[31:22]	10
0xBB02A12C	SVLAN_SP2C [75].VID[21:10]	12
0xBB02A12C	SVLAN_SP2C [75].DST_PORT[9:7]	3
0xBB02A12C	SVLAN_SP2C [75].SVIDX[6:1]	6
0xBB02A12C	SVLAN_SP2C [75].VALID[0:0]	1
0xBB02A130	SVLAN_SP2C [76].RESERVED[31:22]	10
0xBB02A130	SVLAN_SP2C [76].VID[21:10]	12
0xBB02A130	SVLAN_SP2C [76].DST_PORT[9:7]	3
0xBB02A130	SVLAN_SP2C [76].SVIDX[6:1]	6
0xBB02A130	SVLAN_SP2C [76].VALID[0:0]	1
0xBB02A134	SVLAN_SP2C [77].RESERVED[31:22]	10
0xBB02A134	SVLAN_SP2C [77].VID[21:10]	12

Address	Register	Len
0xBB02A134	SVLAN_SP2C [77].DST_PORT[9:7]	3
0xBB02A134	SVLAN_SP2C [77].SVIDX[6:1]	6
0xBB02A134	SVLAN_SP2C [77].VALID[0:0]	1
0xBB02A138	SVLAN_SP2C [78].RESERVED[31:22]	10
0xBB02A138	SVLAN_SP2C [78].VID[21:10]	12
0xBB02A138	SVLAN_SP2C [78].DST_PORT[9:7]	3
0xBB02A138	SVLAN_SP2C [78].SVIDX[6:1]	6
0xBB02A138	SVLAN_SP2C [78].VALID[0:0]	1
0xBB02A13C	SVLAN_SP2C [79].RESERVED[31:22]	10
0xBB02A13C	SVLAN_SP2C [79].VID[21:10]	12
0xBB02A13C	SVLAN_SP2C [79].DST_PORT[9:7]	3
0xBB02A13C	SVLAN_SP2C [79].SVIDX[6:1]	6
0xBB02A13C	SVLAN_SP2C [79].VALID[0:0]	1
0xBB02A140	SVLAN_SP2C [80].RESERVED[31:22]	10
0xBB02A140	SVLAN_SP2C [80].VID[21:10]	12
0xBB02A140	SVLAN_SP2C [80].DST_PORT[9:7]	3
0xBB02A140	SVLAN_SP2C [80].SVIDX[6:1]	6
0xBB02A140	SVLAN_SP2C [80].VALID[0:0]	1
0xBB02A144	SVLAN_SP2C [81].RESERVED[31:22]	10
0xBB02A144	SVLAN_SP2C [81].VID[21:10]	12
0xBB02A144	SVLAN_SP2C [81].DST_PORT[9:7]	3
0xBB02A144	SVLAN_SP2C [81].SVIDX[6:1]	6
0xBB02A144	SVLAN_SP2C [81].VALID[0:0]	1
0xBB02A148	SVLAN_SP2C [82].RESERVED[31:22]	10
0xBB02A148	SVLAN_SP2C [82].VID[21:10]	12
0xBB02A148	SVLAN_SP2C [82].DST_PORT[9:7]	3
0xBB02A148	SVLAN_SP2C [82].SVIDX[6:1]	6
0xBB02A148	SVLAN_SP2C [82].VALID[0:0]	1
0xBB02A14C	SVLAN_SP2C [83].RESERVED[31:22]	10
0xBB02A14C	SVLAN_SP2C [83].VID[21:10]	12
0xBB02A14C	SVLAN_SP2C [83].DST_PORT[9:7]	3
0xBB02A14C	SVLAN_SP2C [83].SVIDX[6:1]	6
0xBB02A14C	SVLAN_SP2C [83].VALID[0:0]	1
0xBB02A150	SVLAN_SP2C [84].RESERVED[31:22]	10
0xBB02A150	SVLAN_SP2C [84].VID[21:10]	12
0xBB02A150	SVLAN_SP2C [84].DST_PORT[9:7]	3
0xBB02A150	SVLAN_SP2C [84].SVIDX[6:1]	6
0xBB02A150	SVLAN_SP2C [84].VALID[0:0]	1
0xBB02A154	SVLAN_SP2C [85].RESERVED[31:22]	10
0xBB02A154	SVLAN_SP2C [85].VID[21:10]	12
0xBB02A154	SVLAN_SP2C [85].DST_PORT[9:7]	3
0xBB02A154	SVLAN_SP2C [85].SVIDX[6:1]	6
0xBB02A154	SVLAN_SP2C [85].VALID[0:0]	1
0xBB02A158	SVLAN_SP2C [86].RESERVED[31:22]	10
0xBB02A158	SVLAN_SP2C [86].VID[21:10]	12
0xBB02A158	SVLAN_SP2C [86].DST_PORT[9:7]	3

Address	Register	Len
0xBB02A158	SVLAN_SP2C [86].SVIDX[6:1]	6
0xBB02A158	SVLAN_SP2C [86].VALID[0:0]	1
0xBB02A15C	SVLAN_SP2C [87].RESERVED[31:22]	10
0xBB02A15C	SVLAN_SP2C [87].VID[21:10]	12
0xBB02A15C	SVLAN_SP2C [87].DST_PORT[9:7]	3
0xBB02A15C	SVLAN_SP2C [87].SVIDX[6:1]	6
0xBB02A15C	SVLAN_SP2C [87].VALID[0:0]	1
0xBB02A160	SVLAN_SP2C [88].RESERVED[31:22]	10
0xBB02A160	SVLAN_SP2C [88].VID[21:10]	12
0xBB02A160	SVLAN_SP2C [88].DST_PORT[9:7]	3
0xBB02A160	SVLAN_SP2C [88].SVIDX[6:1]	6
0xBB02A160	SVLAN_SP2C [88].VALID[0:0]	1
0xBB02A164	SVLAN_SP2C [89].RESERVED[31:22]	10
0xBB02A164	SVLAN_SP2C [89].VID[21:10]	12
0xBB02A164	SVLAN_SP2C [89].DST_PORT[9:7]	3
0xBB02A164	SVLAN_SP2C [89].SVIDX[6:1]	6
0xBB02A164	SVLAN_SP2C [89].VALID[0:0]	1
0xBB02A168	SVLAN_SP2C [90].RESERVED[31:22]	10
0xBB02A168	SVLAN_SP2C [90].VID[21:10]	12
0xBB02A168	SVLAN_SP2C [90].DST_PORT[9:7]	3
0xBB02A168	SVLAN_SP2C [90].SVIDX[6:1]	6
0xBB02A168	SVLAN_SP2C [90].VALID[0:0]	1
0xBB02A16C	SVLAN_SP2C [91].RESERVED[31:22]	10
0xBB02A16C	SVLAN_SP2C [91].VID[21:10]	12
0xBB02A16C	SVLAN_SP2C [91].DST_PORT[9:7]	3
0xBB02A16C	SVLAN_SP2C [91].SVIDX[6:1]	6
0xBB02A16C	SVLAN_SP2C [91].VALID[0:0]	1
0xBB02A170	SVLAN_SP2C [92].RESERVED[31:22]	10
0xBB02A170	SVLAN_SP2C [92].VID[21:10]	12
0xBB02A170	SVLAN_SP2C [92].DST_PORT[9:7]	3
0xBB02A170	SVLAN_SP2C [92].SVIDX[6:1]	6
0xBB02A170	SVLAN_SP2C [92].VALID[0:0]	1
0xBB02A174	SVLAN_SP2C [93].RESERVED[31:22]	10
0xBB02A174	SVLAN_SP2C [93].VID[21:10]	12
0xBB02A174	SVLAN_SP2C [93].DST_PORT[9:7]	3
0xBB02A174	SVLAN_SP2C [93].SVIDX[6:1]	6
0xBB02A174	SVLAN_SP2C [93].VALID[0:0]	1
0xBB02A178	SVLAN_SP2C [94].RESERVED[31:22]	10
0xBB02A178	SVLAN_SP2C [94].VID[21:10]	12
0xBB02A178	SVLAN_SP2C [94].DST_PORT[9:7]	3
0xBB02A178	SVLAN_SP2C [94].SVIDX[6:1]	6
0xBB02A178	SVLAN_SP2C [94].VALID[0:0]	1
0xBB02A17C	SVLAN_SP2C [95].RESERVED[31:22]	10
0xBB02A17C	SVLAN_SP2C [95].VID[21:10]	12
0xBB02A17C	SVLAN_SP2C [95].DST_PORT[9:7]	3
0xBB02A17C	SVLAN_SP2C [95].SVIDX[6:1]	6

Address	Register	Len
0xBB02A17C	SVLAN_SP2C [95].VALID[0:0]	1
0xBB02A180	SVLAN_SP2C [96].RESERVED[31:22]	10
0xBB02A180	SVLAN_SP2C [96].VID[21:10]	12
0xBB02A180	SVLAN_SP2C [96].DST_PORT[9:7]	3
0xBB02A180	SVLAN_SP2C [96].SVIDX[6:1]	6
0xBB02A180	SVLAN_SP2C [96].VALID[0:0]	1
0xBB02A184	SVLAN_SP2C [97].RESERVED[31:22]	10
0xBB02A184	SVLAN_SP2C [97].VID[21:10]	12
0xBB02A184	SVLAN_SP2C [97].DST_PORT[9:7]	3
0xBB02A184	SVLAN_SP2C [97].SVIDX[6:1]	6
0xBB02A184	SVLAN_SP2C [97].VALID[0:0]	1
0xBB02A188	SVLAN_SP2C [98].RESERVED[31:22]	10
0xBB02A188	SVLAN_SP2C [98].VID[21:10]	12
0xBB02A188	SVLAN_SP2C [98].DST_PORT[9:7]	3
0xBB02A188	SVLAN_SP2C [98].SVIDX[6:1]	6
0xBB02A188	SVLAN_SP2C [98].VALID[0:0]	1
0xBB02A18C	SVLAN_SP2C [99].RESERVED[31:22]	10
0xBB02A18C	SVLAN_SP2C [99].VID[21:10]	12
0xBB02A18C	SVLAN_SP2C [99].DST_PORT[9:7]	3
0xBB02A18C	SVLAN_SP2C [99].SVIDX[6:1]	6
0xBB02A18C	SVLAN_SP2C [99].VALID[0:0]	1
0xBB02A190	SVLAN_SP2C [100].RESERVED[31:22]	10
0xBB02A190	SVLAN_SP2C [100].VID[21:10]	12
0xBB02A190	SVLAN_SP2C [100].DST_PORT[9:7]	3
0xBB02A190	SVLAN_SP2C [100].SVIDX[6:1]	6
0xBB02A190	SVLAN_SP2C [100].VALID[0:0]	1
0xBB02A194	SVLAN_SP2C [101].RESERVED[31:22]	10
0xBB02A194	SVLAN_SP2C [101].VID[21:10]	12
0xBB02A194	SVLAN_SP2C [101].DST_PORT[9:7]	3
0xBB02A194	SVLAN_SP2C [101].SVIDX[6:1]	6
0xBB02A194	SVLAN_SP2C [101].VALID[0:0]	1
0xBB02A198	SVLAN_SP2C [102].RESERVED[31:22]	10
0xBB02A198	SVLAN_SP2C [102].VID[21:10]	12
0xBB02A198	SVLAN_SP2C [102].DST_PORT[9:7]	3
0xBB02A198	SVLAN_SP2C [102].SVIDX[6:1]	6
0xBB02A198	SVLAN_SP2C [102].VALID[0:0]	1
0xBB02A19C	SVLAN_SP2C [103].RESERVED[31:22]	10
0xBB02A19C	SVLAN_SP2C [103].VID[21:10]	12
0xBB02A19C	SVLAN_SP2C [103].DST_PORT[9:7]	3
0xBB02A19C	SVLAN_SP2C [103].SVIDX[6:1]	6
0xBB02A19C	SVLAN_SP2C [103].VALID[0:0]	1
0xBB02A1A0	SVLAN_SP2C [104].RESERVED[31:22]	10
0xBB02A1A0	SVLAN_SP2C [104].VID[21:10]	12
0xBB02A1A0	SVLAN_SP2C [104].DST_PORT[9:7]	3
0xBB02A1A0	SVLAN_SP2C [104].SVIDX[6:1]	6
0xBB02A1A0	SVLAN_SP2C [104].VALID[0:0]	1



Address	Register	Len
0xBB02A1A4	SVLAN_SP2C [105].RESERVED[31:22]	10
0xBB02A1A4	SVLAN_SP2C [105].VID[21:10]	12
0xBB02A1A4	SVLAN_SP2C [105].DST_PORT[9:7]	3
0xBB02A1A4	SVLAN_SP2C [105].SVIDX[6:1]	6
0xBB02A1A4	SVLAN_SP2C [105].VALID[0:0]	1
0xBB02A1A8	SVLAN_SP2C [106].RESERVED[31:22]	10
0xBB02A1A8	SVLAN_SP2C [106].VID[21:10]	12
0xBB02A1A8	SVLAN_SP2C [106].DST_PORT[9:7]	3
0xBB02A1A8	SVLAN_SP2C [106].SVIDX[6:1]	6
0xBB02A1A8	SVLAN_SP2C [106].VALID[0:0]	1
0xBB02A1AC	SVLAN_SP2C [107].RESERVED[31:22]	10
0xBB02A1AC	SVLAN_SP2C [107].VID[21:10]	12
0xBB02A1AC	SVLAN_SP2C [107].DST_PORT[9:7]	3
0xBB02A1AC	SVLAN_SP2C [107].SVIDX[6:1]	6
0xBB02A1AC	SVLAN_SP2C [107].VALID[0:0]	1
0xBB02A1B0	SVLAN_SP2C [108].RESERVED[31:22]	10
0xBB02A1B0	SVLAN_SP2C [108].VID[21:10]	12
0xBB02A1B0	SVLAN_SP2C [108].DST_PORT[9:7]	3
0xBB02A1B0	SVLAN_SP2C [108].SVIDX[6:1]	6
0xBB02A1B0	SVLAN_SP2C [108].VALID[0:0]	1
0xBB02A1B4	SVLAN_SP2C [109].RESERVED[31:22]	10
0xBB02A1B4	SVLAN_SP2C [109].VID[21:10]	12
0xBB02A1B4	SVLAN_SP2C [109].DST_PORT[9:7]	3
0xBB02A1B4	SVLAN_SP2C [109].SVIDX[6:1]	6
0xBB02A1B4	SVLAN_SP2C [109].VALID[0:0]	1
0xBB02A1B8	SVLAN_SP2C [110].RESERVED[31:22]	10
0xBB02A1B8	SVLAN_SP2C [110].VID[21:10]	12
0xBB02A1B8	SVLAN_SP2C [110].DST_PORT[9:7]	3
0xBB02A1B8	SVLAN_SP2C [110].SVIDX[6:1]	6
0xBB02A1B8	SVLAN_SP2C [110].VALID[0:0]	1
0xBB02A1BC	SVLAN_SP2C [111].RESERVED[31:22]	10
0xBB02A1BC	SVLAN_SP2C [111].VID[21:10]	12
0xBB02A1BC	SVLAN_SP2C [111].DST_PORT[9:7]	3
0xBB02A1BC	SVLAN_SP2C [111].SVIDX[6:1]	6
0xBB02A1BC	SVLAN_SP2C [111].VALID[0:0]	1
0xBB02A1C0	SVLAN_SP2C [112].RESERVED[31:22]	10
0xBB02A1C0	SVLAN_SP2C [112].VID[21:10]	12
0xBB02A1C0	SVLAN_SP2C [112].DST_PORT[9:7]	3
0xBB02A1C0	SVLAN_SP2C [112].SVIDX[6:1]	6
0xBB02A1C0	SVLAN_SP2C [112].VALID[0:0]	1
0xBB02A1C4	SVLAN_SP2C [113].RESERVED[31:22]	10
0xBB02A1C4	SVLAN_SP2C [113].VID[21:10]	12
0xBB02A1C4	SVLAN_SP2C [113].DST_PORT[9:7]	3
0xBB02A1C4	SVLAN_SP2C [113].SVIDX[6:1]	6
0xBB02A1C4	SVLAN_SP2C [113].VALID[0:0]	1
0xBB02A1C8	SVLAN_SP2C [114].RESERVED[31:22]	10



Address	Register	Len
0xBB02A1C8	SVLAN_SP2C [114].VID[21:10]	12
0xBB02A1C8	SVLAN_SP2C [114].DST_PORT[9:7]	3
0xBB02A1C8	SVLAN_SP2C [114].SVIDX[6:1]	6
0xBB02A1C8	SVLAN_SP2C [114].VALID[0:0]	1
0xBB02A1CC	SVLAN_SP2C [115].RESERVED[31:22]	10
0xBB02A1CC	SVLAN_SP2C [115].VID[21:10]	12
0xBB02A1CC	SVLAN_SP2C [115].DST_PORT[9:7]	3
0xBB02A1CC	SVLAN_SP2C [115].SVIDX[6:1]	6
0xBB02A1CC	SVLAN_SP2C [115].VALID[0:0]	1
0xBB02A1D0	SVLAN_SP2C [116].RESERVED[31:22]	10
0xBB02A1D0	SVLAN_SP2C [116].VID[21:10]	12
0xBB02A1D0	SVLAN_SP2C [116].DST_PORT[9:7]	3
0xBB02A1D0	SVLAN_SP2C [116].SVIDX[6:1]	6
0xBB02A1D0	SVLAN_SP2C [116].VALID[0:0]	1
0xBB02A1D4	SVLAN_SP2C [117].RESERVED[31:22]	10
0xBB02A1D4	SVLAN_SP2C [117].VID[21:10]	12
0xBB02A1D4	SVLAN_SP2C [117].DST_PORT[9:7]	3
0xBB02A1D4	SVLAN_SP2C [117].SVIDX[6:1]	6
0xBB02A1D4	SVLAN_SP2C [117].VALID[0:0]	1
0xBB02A1D8	SVLAN_SP2C [118].RESERVED[31:22]	10
0xBB02A1D8	SVLAN_SP2C [118].VID[21:10]	12
0xBB02A1D8	SVLAN_SP2C [118].DST_PORT[9:7]	3
0xBB02A1D8	SVLAN_SP2C [118].SVIDX[6:1]	6
0xBB02A1D8	SVLAN_SP2C [118].VALID[0:0]	1
0xBB02A1DC	SVLAN_SP2C [119].RESERVED[31:22]	10
0xBB02A1DC	SVLAN_SP2C [119].VID[21:10]	12
0xBB02A1DC	SVLAN_SP2C [119].DST_PORT[9:7]	3
0xBB02A1DC	SVLAN_SP2C [119].SVIDX[6:1]	6
0xBB02A1DC	SVLAN_SP2C [119].VALID[0:0]	1
0xBB02A1E0	SVLAN_SP2C [120].RESERVED[31:22]	10
0xBB02A1E0	SVLAN_SP2C [120].VID[21:10]	12
0xBB02A1E0	SVLAN_SP2C [120].DST_PORT[9:7]	3
0xBB02A1E0	SVLAN_SP2C [120].SVIDX[6:1]	6
0xBB02A1E0	SVLAN_SP2C [120].VALID[0:0]	1
0xBB02A1E4	SVLAN_SP2C [121].RESERVED[31:22]	10
0xBB02A1E4	SVLAN_SP2C [121].VID[21:10]	12
0xBB02A1E4	SVLAN_SP2C [121].DST_PORT[9:7]	3
0xBB02A1E4	SVLAN_SP2C [121].SVIDX[6:1]	6
0xBB02A1E4	SVLAN_SP2C [121].VALID[0:0]	1
0xBB02A1E8	SVLAN_SP2C [122].RESERVED[31:22]	10
0xBB02A1E8	SVLAN_SP2C [122].VID[21:10]	12
0xBB02A1E8	SVLAN_SP2C [122].DST_PORT[9:7]	3
0xBB02A1E8	SVLAN_SP2C [122].SVIDX[6:1]	6
0xBB02A1E8	SVLAN_SP2C [122].VALID[0:0]	1
0xBB02A1EC	SVLAN_SP2C [123].RESERVED[31:22]	10
0xBB02A1EC	SVLAN_SP2C [123].VID[21:10]	12

Address	Register	Len
0xBB02A1EC	SVLAN_SP2C [123].DST_PORT[9:7]	3
0xBB02A1EC	SVLAN_SP2C [123].SVIDX[6:1]	6
0xBB02A1EC	SVLAN_SP2C [123].VALID[0:0]	1
0xBB02A1F0	SVLAN_SP2C [124].RESERVED[31:22]	10
0xBB02A1F0	SVLAN_SP2C [124].VID[21:10]	12
0xBB02A1F0	SVLAN_SP2C [124].DST_PORT[9:7]	3
0xBB02A1F0	SVLAN_SP2C [124].SVIDX[6:1]	6
0xBB02A1F0	SVLAN_SP2C [124].VALID[0:0]	1
0xBB02A1F4	SVLAN_SP2C [125].RESERVED[31:22]	10
0xBB02A1F4	SVLAN_SP2C [125].VID[21:10]	12
0xBB02A1F4	SVLAN_SP2C [125].DST_PORT[9:7]	3
0xBB02A1F4	SVLAN_SP2C [125].SVIDX[6:1]	6
0xBB02A1F4	SVLAN_SP2C [125].VALID[0:0]	1
0xBB02A1F8	SVLAN_SP2C [126].RESERVED[31:22]	10
0xBB02A1F8	SVLAN_SP2C [126].VID[21:10]	12
0xBB02A1F8	SVLAN_SP2C [126].DST_PORT[9:7]	3
0xBB02A1F8	SVLAN_SP2C [126].SVIDX[6:1]	6
0xBB02A1F8	SVLAN_SP2C [126].VALID[0:0]	1
0xBB02A1FC	SVLAN_SP2C [127].RESERVED[31:22]	10
0xBB02A1FC	SVLAN_SP2C [127].VID[21:10]	12
0xBB02A1FC	SVLAN_SP2C [127].DST_PORT[9:7]	3
0xBB02A1FC	SVLAN_SP2C [127].SVIDX[6:1]	6
0xBB02A1FC	SVLAN_SP2C [127].VALID[0:0]	1
0xBB02A200	RMK_P_DSCP_SEL [0].SEL[0:0]	1
0xBB02A200	RMK_P_DSCP_SEL [1].SEL[1:1]	1
0xBB02A200	RMK_P_DSCP_SEL [2].SEL[2:2]	1
0xBB02A200	RMK_P_DSCP_SEL [3].SEL[3:3]	1
0xBB02A200	RMK_P_DSCP_SEL [4].SEL[4:4]	1
0xBB02A200	RMK_P_DSCP_SEL [5].SEL[5:5]	1
0xBB02A200	RMK_P_DSCP_SEL [6].SEL[6:6]	1
0xBB02A204	DBG_HSA_EP.RESERVED[31:3]	29
0xBB02A204	DBG_HSA_EP.DBG_HSA_EP[2:0]	3
0xBB02A208	L34_IPMC_TRAN_TBL [0].RESERVED[31:11]	21
0xBB02A208	L34_IPMC_TRAN_TBL [0].NETIF_IDX[10:8]	3
0xBB02A208	L34_IPMC_TRAN_TBL [0].EN_SIP_TRANS[7:7]	1
0xBB02A208	L34_IPMC_TRAN_TBL [0].EXT_IP_IDX[6:4]	3
0xBB02A208	L34_IPMC_TRAN_TBL [0].IS_PPPOE_IF[3:3]	1
0xBB02A208	L34_IPMC_TRAN_TBL [0].PPPOE_IDX[2:0]	3
0xBB02A20C	L34_IPMC_TRAN_TBL [1].RESERVED[31:11]	21
0xBB02A20C	L34_IPMC_TRAN_TBL [1].NETIF_IDX[10:8]	3
0xBB02A20C	L34_IPMC_TRAN_TBL [1].EN_SIP_TRANS[7:7]	1
0xBB02A20C	L34_IPMC_TRAN_TBL [1].EXT_IP_IDX[6:4]	3
0xBB02A20C	L34_IPMC_TRAN_TBL [1].IS_PPPOE_IF[3:3]	1
0xBB02A20C	L34_IPMC_TRAN_TBL [1].PPPOE_IDX[2:0]	3
0xBB02A210	L34_IPMC_TRAN_TBL [2].RESERVED[31:11]	21
0xBB02A210	L34_IPMC_TRAN_TBL [2].NETIF_IDX[10:8]	3

Address	Register	Len
0xBB02A210	L34_IPMC_TRAN_TBL [2].EN_SIP_TRANS[7:7]	1
0xBB02A210	L34_IPMC_TRAN_TBL [2].EXT_IP_IDX[6:4]	3
0xBB02A210	L34_IPMC_TRAN_TBL [2].IS_PPPOE_IF[3:3]	1
0xBB02A210	L34_IPMC_TRAN_TBL [2].PPPOE_IDX[2:0]	3
0xBB02A214	L34_IPMC_TRAN_TBL [3].RESERVED[31:11]	21
0xBB02A214	L34_IPMC_TRAN_TBL [3].NETIF_IDX[10:8]	3
0xBB02A214	L34_IPMC_TRAN_TBL [3].EN_SIP_TRANS[7:7]	1
0xBB02A214	L34_IPMC_TRAN_TBL [3].EXT_IP_IDX[6:4]	3
0xBB02A214	L34_IPMC_TRAN_TBL [3].IS_PPPOE_IF[3:3]	1
0xBB02A214	L34_IPMC_TRAN_TBL [3].PPPOE_IDX[2:0]	3
0xBB02A218	L34_IPMC_TRAN_TBL [4].RESERVED[31:11]	21
0xBB02A218	L34_IPMC_TRAN_TBL [4].NETIF_IDX[10:8]	3
0xBB02A218	L34_IPMC_TRAN_TBL [4].EN_SIP_TRANS[7:7]	1
0xBB02A218	L34_IPMC_TRAN_TBL [4].EXT_IP_IDX[6:4]	3
0xBB02A218	L34_IPMC_TRAN_TBL [4].IS_PPPOE_IF[3:3]	1
0xBB02A218	L34_IPMC_TRAN_TBL [4].PPPOE_IDX[2:0]	3
0xBB02A21C	L34_IPMC_TRAN_TBL [5].RESERVED[31:11]	21
0xBB02A21C	L34_IPMC_TRAN_TBL [5].NETIF_IDX[10:8]	3
0xBB02A21C	L34_IPMC_TRAN_TBL [5].EN_SIP_TRANS[7:7]	1
0xBB02A21C	L34_IPMC_TRAN_TBL [5].EXT_IP_IDX[6:4]	3
0xBB02A21C	L34_IPMC_TRAN_TBL [5].IS_PPPOE_IF[3:3]	1
0xBB02A21C	L34_IPMC_TRAN_TBL [5].PPPOE_IDX[2:0]	3
0xBB02A220	L34_IPMC_TRAN_TBL [6].RESERVED[31:11]	21
0xBB02A220	L34_IPMC_TRAN_TBL [6].NETIF_IDX[10:8]	3
0xBB02A220	L34_IPMC_TRAN_TBL [6].EN_SIP_TRANS[7:7]	1
0xBB02A220	L34_IPMC_TRAN_TBL [6].EXT_IP_IDX[6:4]	3
0xBB02A220	L34_IPMC_TRAN_TBL [6].IS_PPPOE_IF[3:3]	1
0xBB02A220	L34_IPMC_TRAN_TBL [6].PPPOE_IDX[2:0]	3
0xBB02A224	L34_IPMC_TRAN_TBL [7].RESERVED[31:11]	21
0xBB02A224	L34_IPMC_TRAN_TBL [7].NETIF_IDX[10:8]	3
0xBB02A224	L34_IPMC_TRAN_TBL [7].EN_SIP_TRANS[7:7]	1
0xBB02A224	L34_IPMC_TRAN_TBL [7].EXT_IP_IDX[6:4]	3
0xBB02A224	L34_IPMC_TRAN_TBL [7].IS_PPPOE_IF[3:3]	1
0xBB02A224	L34_IPMC_TRAN_TBL [7].PPPOE_IDX[2:0]	3
0xBB02A228	L34_IPMC_TRAN_TBL [8].RESERVED[31:11]	21
0xBB02A228	L34_IPMC_TRAN_TBL [8].NETIF_IDX[10:8]	3
0xBB02A228	L34_IPMC_TRAN_TBL [8].EN_SIP_TRANS[7:7]	1
0xBB02A228	L34_IPMC_TRAN_TBL [8].EXT_IP_IDX[6:4]	3
0xBB02A228	L34_IPMC_TRAN_TBL [8].IS_PPPOE_IF[3:3]	1
0xBB02A228	L34_IPMC_TRAN_TBL [8].PPPOE_IDX[2:0]	3
0xBB02A22C	L34_IPMC_TRAN_TBL [9].RESERVED[31:11]	21
0xBB02A22C	L34_IPMC_TRAN_TBL [9].NETIF_IDX[10:8]	3
0xBB02A22C	L34_IPMC_TRAN_TBL [9].EN_SIP_TRANS[7:7]	1
0xBB02A22C	L34_IPMC_TRAN_TBL [9].EXT_IP_IDX[6:4]	3
0xBB02A22C	L34_IPMC_TRAN_TBL [9].IS_PPPOE_IF[3:3]	1
0xBB02A22C	L34_IPMC_TRAN_TBL [9].PPPOE_IDX[2:0]	3

Address	Register	Len
0xBB02A230	L34_IPMC_TRAN_TBL [10].RESERVED[31:11]	21
0xBB02A230	L34_IPMC_TRAN_TBL [10].NETIF_IDX[10:8]	3
0xBB02A230	L34_IPMC_TRAN_TBL [10].EN_SIP_TRANS[7:7]	1
0xBB02A230	L34_IPMC_TRAN_TBL [10].EXT_IP_IDX[6:4]	3
0xBB02A230	L34_IPMC_TRAN_TBL [10].IS_PPPOE_IF[3:3]	1
0xBB02A230	L34_IPMC_TRAN_TBL [10].PPPOE_IDX[2:0]	3
0xBB02A234	L34_IPMC_TRAN_TBL [11].RESERVED[31:11]	21
0xBB02A234	L34_IPMC_TRAN_TBL [11].NETIF_IDX[10:8]	3
0xBB02A234	L34_IPMC_TRAN_TBL [11].EN_SIP_TRANS[7:7]	1
0xBB02A234	L34_IPMC_TRAN_TBL [11].EXT_IP_IDX[6:4]	3
0xBB02A234	L34_IPMC_TRAN_TBL [11].IS_PPPOE_IF[3:3]	1
0xBB02A234	L34_IPMC_TRAN_TBL [11].PPPOE_IDX[2:0]	3
0xBB02A238	L34_IPMC_TRAN_TBL [12].RESERVED[31:11]	21
0xBB02A238	L34_IPMC_TRAN_TBL [12].NETIF_IDX[10:8]	3
0xBB02A238	L34_IPMC_TRAN_TBL [12].EN_SIP_TRANS[7:7]	1
0xBB02A238	L34_IPMC_TRAN_TBL [12].EXT_IP_IDX[6:4]	3
0xBB02A238	L34_IPMC_TRAN_TBL [12].IS_PPPOE_IF[3:3]	1
0xBB02A238	L34_IPMC_TRAN_TBL [12].PPPOE_IDX[2:0]	3
0xBB02A23C	L34_IPMC_TRAN_TBL [13].RESERVED[31:11]	21
0xBB02A23C	L34_IPMC_TRAN_TBL [13].NETIF_IDX[10:8]	3
0xBB02A23C	L34_IPMC_TRAN_TBL [13].EN_SIP_TRANS[7:7]	1
0xBB02A23C	L34_IPMC_TRAN_TBL [13].EXT_IP_IDX[6:4]	3
0xBB02A23C	L34_IPMC_TRAN_TBL [13].IS_PPPOE_IF[3:3]	1
0xBB02A23C	L34_IPMC_TRAN_TBL [13].PPPOE_IDX[2:0]	3
0xBB02A240	L34_IPMC_TRAN_TBL [14].RESERVED[31:11]	21
0xBB02A240	L34_IPMC_TRAN_TBL [14].NETIF_IDX[10:8]	3
0xBB02A240	L34_IPMC_TRAN_TBL [14].EN_SIP_TRANS[7:7]	1
0xBB02A240	L34_IPMC_TRAN_TBL [14].EXT_IP_IDX[6:4]	3
0xBB02A240	L34_IPMC_TRAN_TBL [14].IS_PPPOE_IF[3:3]	1
0xBB02A240	L34_IPMC_TRAN_TBL [14].PPPOE_IDX[2:0]	3
0xBB02A244	L34_IPMC_TRAN_TBL [15].RESERVED[31:11]	21
0xBB02A244	L34_IPMC_TRAN_TBL [15].NETIF_IDX[10:8]	3
0xBB02A244	L34_IPMC_TRAN_TBL [15].EN_SIP_TRANS[7:7]	1
0xBB02A244	L34_IPMC_TRAN_TBL [15].EXT_IP_IDX[6:4]	3
0xBB02A244	L34_IPMC_TRAN_TBL [15].IS_PPPOE_IF[3:3]	1
0xBB02A244	L34_IPMC_TRAN_TBL [15].PPPOE_IDX[2:0]	3
0xBB02A248	L34_IPMC_TTL_CFG.RESERVED[31:1]	31
0xBB02A248	L34_IPMC_TTL_CFG.IP_MCST_TTL_1[0:0]	1
0xBB02A24C	RGF_VER_ALE_HSA.REGFILE_VER[31:0]	32
0xBB02A250	RSVD_ALE_HSA [0].RSVD_MEM[31:0]	32
0xBB02A254	RSVD_ALE_HSA [1].RSVD_MEM[31:0]	32
0xBB02A258	RSVD_ALE_HSA [2].RSVD_MEM[31:0]	32
0xBB02A25C	RSVD_ALE_HSA [3].RSVD_MEM[31:0]	32
0xBB02A260	RSVD_ALE_HSA [4].RSVD_MEM[31:0]	32
0xBB02A264	RSVD_ALE_HSA [5].RSVD_MEM[31:0]	32
0xBB02A268	RSVD_ALE_HSA [6].RSVD_MEM[31:0]	32

Address	Register	Len
0xBB02A26C	RSVD_ALE_HSA [7].RSVD_MEM[31:0]	32
0xBB02A270	RSVD_ALE_HSA [8].RSVD_MEM[31:0]	32
0xBB02A274	RSVD_ALE_HSA [9].RSVD_MEM[31:0]	32
0xBB02A278	RSVD_ALE_HSA [10].RSVD_MEM[31:0]	32
0xBB02A27C	RSVD_ALE_HSA [11].RSVD_MEM[31:0]	32
0xBB02A280	RSVD_ALE_HSA [12].RSVD_MEM[31:0]	32
0xBB02A284	RSVD_ALE_HSA [13].RSVD_MEM[31:0]	32
0xBB02A288	RSVD_ALE_HSA [14].RSVD_MEM[31:0]	32
0xBB02A28C	RSVD_ALE_HSA [15].RSVD_MEM[31:0]	32
0xBB02A290	HSA_TX_DBG [0].DBG_HSA_BUS[31:0]	32
0xBB02A294	HSA_TX_DBG [1].DBG_HSA_BUS[31:0]	32
0xBB02A298	HSA_TX_DBG [2].DBG_HSA_BUS[31:0]	32
0xBB02A29C	HSA_TX_DBG [3].DBG_HSA_BUS[31:0]	32
0xBB02A2A0	HSA_TX_DBG [4].DBG_HSA_BUS[31:0]	32
0xBB02A2A4	HSA_TX_DBG [5].DBG_HSA_BUS[31:0]	32
0xBB02A2A8	HSA_TX_DBG [6].DBG_HSA_BUS[31:0]	32
0xBB02A2AC	HSA_TX_DBG [7].DBG_HSA_BUS[31:0]	32
0xBB02A2B0	HSA_TX_DBG [8].DBG_HSA_BUS[31:0]	32
0xBB02A2B4	HSA_TX_DBG [9].DBG_HSA_BUS[31:0]	32
0xBB02A2B8	HSA_TX_DBG [10].DBG_HSA_BUS[31:0]	32
0xBB02A2BC	HSA_TX_DBG [11].DBG_HSA_BUS[31:0]	32
0xBB02A2C0	HSA_TX_DBG [12].DBG_HSA_BUS[31:0]	32
0xBB02A2C4	HSA_TX_DBG [13].DBG_HSA_BUS[31:0]	32
0xBB02A2C8	HSA_TX_DBG [14].DBG_HSA_BUS[31:0]	32
0xBB02A2CC	HSA_TX_DBG [15].DBG_HSA_BUS[31:0]	32
0xBB02A2D0	HSARAM_5_CFG.RESERVED[31:5]	27
0xBB02A2D0	HSARAM_5_CFG.HSARAM_5_DVSE[4:4]	1
0xBB02A2D0	HSARAM_5_CFG.HSARAM_5_DVS[3:0]	4
0xBB02A2D4	DBG_EP_CFG.RESERVED[31:3]	29
0xBB02A2D4	DBG_EP_CFG.DBG_EP[2:0]	3
0xBB02A2D8	TRUNK_DROP_CFG.RESERVED[31:1]	31
0xBB02A2D8	TRUNK_DROP_CFG.TRUNK_DROP[0:0]	1
0xBB02A2DC	PAUSE_ALL_LW_CFG.RESERVED[31:1]	31
0xBB02A2DC	PAUSE_ALL_LW_CFG.PAUSE_ALL_LW[0:0]	1
0xBB02A2E0	HYS_PUSAL_CFG.RESERVED[31:1]	31
0xBB02A2E0	HYS_PUSAL_CFG.HYS_PUSAL[0:0]	1
0xBB02D000	FC_Q_EGR_DROP_TH [0].TH[12:0]	13
0xBB02D000	FC_Q_EGR_DROP_TH [1].TH[25:13]	13
0xBB02D004	FC_Q_EGR_DROP_TH [2].TH[12:0]	13
0xBB02D004	FC_Q_EGR_DROP_TH [3].TH[25:13]	13
0xBB02D008	FC_Q_EGR_DROP_TH [4].TH[12:0]	13
0xBB02D008	FC_Q_EGR_DROP_TH [5].TH[25:13]	13
0xBB02D00C	FC_Q_EGR_DROP_TH [6].TH[12:0]	13
0xBB02D00C	FC_Q_EGR_DROP_TH [7].TH[25:13]	13
0xBB02D010	FC_P_EGR_DROP_TH [0].TH[12:0]	13
0xBB02D010	FC_P_EGR_DROP_TH [1].TH[25:13]	13

Address	Register	Len
0xBB02D014	FC_P_EGR_DROP_TH [2].TH[12:0]	13
0xBB02D014	FC_P_EGR_DROP_TH [3].TH[25:13]	13
0xBB02D018	FC_P_EGR_DROP_TH [4].TH[12:0]	13
0xBB02D018	FC_P_EGR_DROP_TH [5].TH[25:13]	13
0xBB02D01C	FC_P_EGR_DROP_TH [6].TH[12:0]	13
0xBB02D020	FC_Q_EGR_GAP_TH.RESERVED[31:13]	19
0xBB02D020	FC_Q_EGR_GAP_TH.TH[12:0]	13
0xBB02D024	FC_P_EGR_GAP_TH.RESERVED[31:13]	19
0xBB02D024	FC_P_EGR_GAP_TH.TH[12:0]	13
0xBB02D028	FC_DBG_CTRL.RESERVED[31:14]	18
0xBB02D028	FC_DBG_CTRL.PORT_NO[13:10]	4
0xBB02D028	FC_DBG_CTRL.CLR_TOTAL_PKT_CNT[9:9]	1
0xBB02D028	FC_DBG_CTRL.CLR_PE_MAX_PAGE_CNT[8:8]	1
0xBB02D028	FC_DBG_CTRL.CLR_Q_MAX_PAGE_CNT[7:0]	8
0xBB02D02C	FC_TOTAL_PAGE_CNT.RESERVED[31:16]	16
0xBB02D02C	FC_TOTAL_PAGE_CNT.TOTAL_PAGE_CNT[15:0]	16
0xBB02D030	FC_PE_USED_PAGE_CNT [0].RESERVED[31:29]	3
0xBB02D030	FC_PE_USED_PAGE_CNT [0].PE_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D030	FC_PE_USED_PAGE_CNT [0].RESERVED[15:13]	3
0xBB02D030	FC_PE_USED_PAGE_CNT [0].PE_USED_PAGE_CNT[12:0]	13
0xBB02D034	FC_PE_USED_PAGE_CNT [1].RESERVED[31:29]	3
0xBB02D034	FC_PE_USED_PAGE_CNT [1].PE_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D034	FC_PE_USED_PAGE_CNT [1].RESERVED[15:13]	3
0xBB02D034	FC_PE_USED_PAGE_CNT [1].PE_USED_PAGE_CNT[12:0]	13
0xBB02D038	FC_PE_USED_PAGE_CNT [2].RESERVED[31:29]	3
0xBB02D038	FC_PE_USED_PAGE_CNT [2].PE_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D038	FC_PE_USED_PAGE_CNT [2].RESERVED[15:13]	3
0xBB02D038	FC_PE_USED_PAGE_CNT [2].PE_USED_PAGE_CNT[12:0]	13
0xBB02D03C	FC_PE_USED_PAGE_CNT [3].RESERVED[31:29]	3
0xBB02D03C	FC_PE_USED_PAGE_CNT [3].PE_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D03C	FC_PE_USED_PAGE_CNT [3].RESERVED[15:13]	3
0xBB02D03C	FC_PE_USED_PAGE_CNT [3].PE_USED_PAGE_CNT[12:0]	13
0xBB02D040	FC_PE_USED_PAGE_CNT [4].RESERVED[31:29]	3
0xBB02D040	FC_PE_USED_PAGE_CNT [4].PE_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D040	FC_PE_USED_PAGE_CNT [4].RESERVED[15:13]	3
0xBB02D040	FC_PE_USED_PAGE_CNT [4].PE_USED_PAGE_CNT[12:0]	13
0xBB02D044	FC_PE_USED_PAGE_CNT [5].RESERVED[31:29]	3
0xBB02D044	FC_PE_USED_PAGE_CNT [5].PE_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D044	FC_PE_USED_PAGE_CNT [5].RESERVED[15:13]	3
0xBB02D044	FC_PE_USED_PAGE_CNT [5].PE_USED_PAGE_CNT[12:0]	13
0xBB02D048	FC_PE_USED_PAGE_CNT [6].RESERVED[31:29]	3
0xBB02D048	FC_PE_USED_PAGE_CNT [6].PE_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D048	FC_PE_USED_PAGE_CNT [6].RESERVED[15:13]	3
0xBB02D048	FC_PE_USED_PAGE_CNT [6].PE_USED_PAGE_CNT[12:0]	13
0xBB02D04C	FC_Q_USED_PAGE_CNT [0][0].RESERVED[31:29]	3
0xBB02D04C	FC_Q_USED_PAGE_CNT [0][0].Q_MAX_USED_PAGE_CNT[28:16]	13

Address	Register	Len
0xBB02D04C	FC_Q_USED_PAGE_CNT [0][0].RESERVED[15:13]	3
0xBB02D04C	FC_Q_USED_PAGE_CNT [0][0].Q_USED_PAGE_CNT[12:0]	13
0xBB02D050	FC_Q_USED_PAGE_CNT [0][1].RESERVED[31:29]	3
0xBB02D050	FC_Q_USED_PAGE_CNT [0][1].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D050	FC_Q_USED_PAGE_CNT [0][1].RESERVED[15:13]	3
0xBB02D050	FC_Q_USED_PAGE_CNT [0][1].Q_USED_PAGE_CNT[12:0]	13
0xBB02D054	FC_Q_USED_PAGE_CNT [0][2].RESERVED[31:29]	3
0xBB02D054	FC_Q_USED_PAGE_CNT [0][2].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D054	FC_Q_USED_PAGE_CNT [0][2].RESERVED[15:13]	3
0xBB02D054	FC_Q_USED_PAGE_CNT [0][2].Q_USED_PAGE_CNT[12:0]	13
0xBB02D058	FC_Q_USED_PAGE_CNT [0][3].RESERVED[31:29]	3
0xBB02D058	FC_Q_USED_PAGE_CNT [0][3].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D058	FC_Q_USED_PAGE_CNT [0][3].RESERVED[15:13]	3
0xBB02D058	FC_Q_USED_PAGE_CNT [0][3].Q_USED_PAGE_CNT[12:0]	13
0xBB02D05C	FC_Q_USED_PAGE_CNT [0][4].RESERVED[31:29]	3
0xBB02D05C	FC_Q_USED_PAGE_CNT [0][4].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D05C	FC_Q_USED_PAGE_CNT [0][4].RESERVED[15:13]	3
0xBB02D05C	FC_Q_USED_PAGE_CNT [0][4].Q_USED_PAGE_CNT[12:0]	13
0xBB02D060	FC_Q_USED_PAGE_CNT [0][5].RESERVED[31:29]	3
0xBB02D060	FC_Q_USED_PAGE_CNT [0][5].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D060	FC_Q_USED_PAGE_CNT [0][5].RESERVED[15:13]	3
0xBB02D060	FC_Q_USED_PAGE_CNT [0][5].Q_USED_PAGE_CNT[12:0]	13
0xBB02D064	FC_Q_USED_PAGE_CNT [0][6].RESERVED[31:29]	3
0xBB02D064	FC_Q_USED_PAGE_CNT [0][6].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D064	FC_Q_USED_PAGE_CNT [0][6].RESERVED[15:13]	3
0xBB02D064	FC_Q_USED_PAGE_CNT [0][6].Q_USED_PAGE_CNT[12:0]	13
0xBB02D068	FC_Q_USED_PAGE_CNT [0][7].RESERVED[31:29]	3
0xBB02D068	FC_Q_USED_PAGE_CNT [0][7].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D068	FC_Q_USED_PAGE_CNT [0][7].RESERVED[15:13]	3
0xBB02D068	FC_Q_USED_PAGE_CNT [0][7].Q_USED_PAGE_CNT[12:0]	13
0xBB02D06C	FC_Q_USED_PAGE_CNT [1][0].RESERVED[31:29]	3
0xBB02D06C	FC_Q_USED_PAGE_CNT [1][0].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D06C	FC_Q_USED_PAGE_CNT [1][0].RESERVED[15:13]	3
0xBB02D06C	FC_Q_USED_PAGE_CNT [1][0].Q_USED_PAGE_CNT[12:0]	13
0xBB02D070	FC_Q_USED_PAGE_CNT [1][1].RESERVED[31:29]	3
0xBB02D070	FC_Q_USED_PAGE_CNT [1][1].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D070	FC_Q_USED_PAGE_CNT [1][1].RESERVED[15:13]	3
0xBB02D070	FC_Q_USED_PAGE_CNT [1][1].Q_USED_PAGE_CNT[12:0]	13
0xBB02D074	FC_Q_USED_PAGE_CNT [1][2].RESERVED[31:29]	3
0xBB02D074	FC_Q_USED_PAGE_CNT [1][2].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D074	FC_Q_USED_PAGE_CNT [1][2].RESERVED[15:13]	3
0xBB02D074	FC_Q_USED_PAGE_CNT [1][2].Q_USED_PAGE_CNT[12:0]	13
0xBB02D078	FC_Q_USED_PAGE_CNT [1][3].RESERVED[31:29]	3
0xBB02D078	FC_Q_USED_PAGE_CNT [1][3].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D078	FC_Q_USED_PAGE_CNT [1][3].RESERVED[15:13]	3
0xBB02D078	FC_Q_USED_PAGE_CNT [1][3].Q_USED_PAGE_CNT[12:0]	13



Address	Register	Len
0xBB02D07C	FC_Q_USED_PAGE_CNT [1][4].RESERVED[31:29]	3
0xBB02D07C	FC_Q_USED_PAGE_CNT [1][4].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D07C	FC_Q_USED_PAGE_CNT [1][4].RESERVED[15:13]	3
0xBB02D07C	FC_Q_USED_PAGE_CNT [1][4].Q_USED_PAGE_CNT[12:0]	13
0xBB02D080	FC_Q_USED_PAGE_CNT [1][5].RESERVED[31:29]	3
0xBB02D080	FC_Q_USED_PAGE_CNT [1][5].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D080	FC_Q_USED_PAGE_CNT [1][5].RESERVED[15:13]	3
0xBB02D080	FC_Q_USED_PAGE_CNT [1][5].Q_USED_PAGE_CNT[12:0]	13
0xBB02D084	FC_Q_USED_PAGE_CNT [1][6].RESERVED[31:29]	3
0xBB02D084	FC_Q_USED_PAGE_CNT [1][6].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D084	FC_Q_USED_PAGE_CNT [1][6].RESERVED[15:13]	3
0xBB02D084	FC_Q_USED_PAGE_CNT [1][6].Q_USED_PAGE_CNT[12:0]	13
0xBB02D088	FC_Q_USED_PAGE_CNT [1][7].RESERVED[31:29]	3
0xBB02D088	FC_Q_USED_PAGE_CNT [1][7].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D088	FC_Q_USED_PAGE_CNT [1][7].RESERVED[15:13]	3
0xBB02D088	FC_Q_USED_PAGE_CNT [1][7].Q_USED_PAGE_CNT[12:0]	13
0xBB02D08C	FC_Q_USED_PAGE_CNT [2][0].RESERVED[31:29]	3
0xBB02D08C	FC_Q_USED_PAGE_CNT [2][0].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D08C	FC_Q_USED_PAGE_CNT [2][0].RESERVED[15:13]	3
0xBB02D08C	FC_Q_USED_PAGE_CNT [2][0].Q_USED_PAGE_CNT[12:0]	13
0xBB02D090	FC_Q_USED_PAGE_CNT [2][1].RESERVED[31:29]	3
0xBB02D090	FC_Q_USED_PAGE_CNT [2][1].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D090	FC_Q_USED_PAGE_CNT [2][1].RESERVED[15:13]	3
0xBB02D090	FC_Q_USED_PAGE_CNT [2][1].Q_USED_PAGE_CNT[12:0]	13
0xBB02D094	FC_Q_USED_PAGE_CNT [2][2].RESERVED[31:29]	3
0xBB02D094	FC_Q_USED_PAGE_CNT [2][2].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D094	FC_Q_USED_PAGE_CNT [2][2].RESERVED[15:13]	3
0xBB02D094	FC_Q_USED_PAGE_CNT [2][2].Q_USED_PAGE_CNT[12:0]	13
0xBB02D098	FC_Q_USED_PAGE_CNT [2][3].RESERVED[31:29]	3
0xBB02D098	FC_Q_USED_PAGE_CNT [2][3].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D098	FC_Q_USED_PAGE_CNT [2][3].RESERVED[15:13]	3
0xBB02D098	FC_Q_USED_PAGE_CNT [2][3].Q_USED_PAGE_CNT[12:0]	13
0xBB02D09C	FC_Q_USED_PAGE_CNT [2][4].RESERVED[31:29]	3
0xBB02D09C	FC_Q_USED_PAGE_CNT [2][4].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D09C	FC_Q_USED_PAGE_CNT [2][4].RESERVED[15:13]	3
0xBB02D09C	FC_Q_USED_PAGE_CNT [2][4].Q_USED_PAGE_CNT[12:0]	13
0xBB02D0A0	FC_Q_USED_PAGE_CNT [2][5].RESERVED[31:29]	3
0xBB02D0A0	FC_Q_USED_PAGE_CNT [2][5].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D0A0	FC_Q_USED_PAGE_CNT [2][5].RESERVED[15:13]	3
0xBB02D0A0	FC_Q_USED_PAGE_CNT [2][5].Q_USED_PAGE_CNT[12:0]	13
0xBB02D0A4	FC_Q_USED_PAGE_CNT [2][6].RESERVED[31:29]	3
0xBB02D0A4	FC_Q_USED_PAGE_CNT [2][6].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D0A4	FC_Q_USED_PAGE_CNT [2][6].RESERVED[15:13]	3
0xBB02D0A4	FC_Q_USED_PAGE_CNT [2][6].Q_USED_PAGE_CNT[12:0]	13
0xBB02D0A8	FC_Q_USED_PAGE_CNT [2][7].RESERVED[31:29]	3
0xBB02D0A8	FC_Q_USED_PAGE_CNT [2][7].Q_MAX_USED_PAGE_CNT[28:16]	13



Address	Register	Len
0xBB02D0A8	FC_Q_USED_PAGE_CNT [2][7].RESERVED[15:13]	3
0xBB02D0A8	FC_Q_USED_PAGE_CNT [2][7].Q_USED_PAGE_CNT[12:0]	13
0xBB02D0AC	FC_Q_USED_PAGE_CNT [3][0].RESERVED[31:29]	3
0xBB02D0AC	FC_Q_USED_PAGE_CNT [3][0].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D0AC	FC_Q_USED_PAGE_CNT [3][0].RESERVED[15:13]	3
0xBB02D0AC	FC_Q_USED_PAGE_CNT [3][0].Q_USED_PAGE_CNT[12:0]	13
0xBB02D0B0	FC_Q_USED_PAGE_CNT [3][1].RESERVED[31:29]	3
0xBB02D0B0	FC_Q_USED_PAGE_CNT [3][1].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D0B0	FC_Q_USED_PAGE_CNT [3][1].RESERVED[15:13]	3
0xBB02D0B0	FC_Q_USED_PAGE_CNT [3][1].Q_USED_PAGE_CNT[12:0]	13
0xBB02D0B4	FC_Q_USED_PAGE_CNT [3][2].RESERVED[31:29]	3
0xBB02D0B4	FC_Q_USED_PAGE_CNT [3][2].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D0B4	FC_Q_USED_PAGE_CNT [3][2].RESERVED[15:13]	3
0xBB02D0B4	FC_Q_USED_PAGE_CNT [3][2].Q_USED_PAGE_CNT[12:0]	13
0xBB02D0B8	FC_Q_USED_PAGE_CNT [3][3].RESERVED[31:29]	3
0xBB02D0B8	FC_Q_USED_PAGE_CNT [3][3].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D0B8	FC_Q_USED_PAGE_CNT [3][3].RESERVED[15:13]	3
0xBB02D0B8	FC_Q_USED_PAGE_CNT [3][3].Q_USED_PAGE_CNT[12:0]	13
0xBB02D0BC	FC_Q_USED_PAGE_CNT [3][4].RESERVED[31:29]	3
0xBB02D0BC	FC_Q_USED_PAGE_CNT [3][4].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D0BC	FC_Q_USED_PAGE_CNT [3][4].RESERVED[15:13]	3
0xBB02D0BC	FC_Q_USED_PAGE_CNT [3][4].Q_USED_PAGE_CNT[12:0]	13
0xBB02D0C0	FC_Q_USED_PAGE_CNT [3][5].RESERVED[31:29]	3
0xBB02D0C0	FC_Q_USED_PAGE_CNT [3][5].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D0C0	FC_Q_USED_PAGE_CNT [3][5].RESERVED[15:13]	3
0xBB02D0C0	FC_Q_USED_PAGE_CNT [3][5].Q_USED_PAGE_CNT[12:0]	13
0xBB02D0C4	FC_Q_USED_PAGE_CNT [3][6].RESERVED[31:29]	3
0xBB02D0C4	FC_Q_USED_PAGE_CNT [3][6].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D0C4	FC_Q_USED_PAGE_CNT [3][6].RESERVED[15:13]	3
0xBB02D0C4	FC_Q_USED_PAGE_CNT [3][6].Q_USED_PAGE_CNT[12:0]	13
0xBB02D0C8	FC_Q_USED_PAGE_CNT [3][7].RESERVED[31:29]	3
0xBB02D0C8	FC_Q_USED_PAGE_CNT [3][7].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D0C8	FC_Q_USED_PAGE_CNT [3][7].RESERVED[15:13]	3
0xBB02D0C8	FC_Q_USED_PAGE_CNT [3][7].Q_USED_PAGE_CNT[12:0]	13
0xBB02D0CC	FC_Q_USED_PAGE_CNT [4][0].RESERVED[31:29]	3
0xBB02D0CC	FC_Q_USED_PAGE_CNT [4][0].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D0CC	FC_Q_USED_PAGE_CNT [4][0].RESERVED[15:13]	3
0xBB02D0CC	FC_Q_USED_PAGE_CNT [4][0].Q_USED_PAGE_CNT[12:0]	13
0xBB02D0D0	FC_Q_USED_PAGE_CNT [4][1].RESERVED[31:29]	3
0xBB02D0D0	FC_Q_USED_PAGE_CNT [4][1].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D0D0	FC_Q_USED_PAGE_CNT [4][1].RESERVED[15:13]	3
0xBB02D0D0	FC_Q_USED_PAGE_CNT [4][1].Q_USED_PAGE_CNT[12:0]	13
0xBB02D0D4	FC_Q_USED_PAGE_CNT [4][2].RESERVED[31:29]	3
0xBB02D0D4	FC_Q_USED_PAGE_CNT [4][2].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D0D4	FC_Q_USED_PAGE_CNT [4][2].RESERVED[15:13]	3
0xBB02D0D4	FC_Q_USED_PAGE_CNT [4][2].Q_USED_PAGE_CNT[12:0]	13

Address	Register	Len
0xBB02D0D8	FC_Q_USED_PAGE_CNT [4][3].RESERVED[31:29]	3
0xBB02D0D8	FC_Q_USED_PAGE_CNT [4][3].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D0D8	FC_Q_USED_PAGE_CNT [4][3].RESERVED[15:13]	3
0xBB02D0D8	FC_Q_USED_PAGE_CNT [4][3].Q_USED_PAGE_CNT[12:0]	13
0xBB02D0DC	FC_Q_USED_PAGE_CNT [4][4].RESERVED[31:29]	3
0xBB02D0DC	FC_Q_USED_PAGE_CNT [4][4].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D0DC	FC_Q_USED_PAGE_CNT [4][4].RESERVED[15:13]	3
0xBB02D0DC	FC_Q_USED_PAGE_CNT [4][4].Q_USED_PAGE_CNT[12:0]	13
0xBB02D0E0	FC_Q_USED_PAGE_CNT [4][5].RESERVED[31:29]	3
0xBB02D0E0	FC_Q_USED_PAGE_CNT [4][5].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D0E0	FC_Q_USED_PAGE_CNT [4][5].RESERVED[15:13]	3
0xBB02D0E0	FC_Q_USED_PAGE_CNT [4][5].Q_USED_PAGE_CNT[12:0]	13
0xBB02D0E4	FC_Q_USED_PAGE_CNT [4][6].RESERVED[31:29]	3
0xBB02D0E4	FC_Q_USED_PAGE_CNT [4][6].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D0E4	FC_Q_USED_PAGE_CNT [4][6].RESERVED[15:13]	3
0xBB02D0E4	FC_Q_USED_PAGE_CNT [4][6].Q_USED_PAGE_CNT[12:0]	13
0xBB02D0E8	FC_Q_USED_PAGE_CNT [4][7].RESERVED[31:29]	3
0xBB02D0E8	FC_Q_USED_PAGE_CNT [4][7].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D0E8	FC_Q_USED_PAGE_CNT [4][7].RESERVED[15:13]	3
0xBB02D0E8	FC_Q_USED_PAGE_CNT [4][7].Q_USED_PAGE_CNT[12:0]	13
0xBB02D0EC	FC_Q_USED_PAGE_CNT [5][0].RESERVED[31:29]	3
0xBB02D0EC	FC_Q_USED_PAGE_CNT [5][0].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D0EC	FC_Q_USED_PAGE_CNT [5][0].RESERVED[15:13]	3
0xBB02D0EC	FC_Q_USED_PAGE_CNT [5][0].Q_USED_PAGE_CNT[12:0]	13
0xBB02D0F0	FC_Q_USED_PAGE_CNT [5][1].RESERVED[31:29]	3
0xBB02D0F0	FC_Q_USED_PAGE_CNT [5][1].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D0F0	FC_Q_USED_PAGE_CNT [5][1].RESERVED[15:13]	3
0xBB02D0F0	FC_Q_USED_PAGE_CNT [5][1].Q_USED_PAGE_CNT[12:0]	13
0xBB02D0F4	FC_Q_USED_PAGE_CNT [5][2].RESERVED[31:29]	3
0xBB02D0F4	FC_Q_USED_PAGE_CNT [5][2].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D0F4	FC_Q_USED_PAGE_CNT [5][2].RESERVED[15:13]	3
0xBB02D0F4	FC_Q_USED_PAGE_CNT [5][2].Q_USED_PAGE_CNT[12:0]	13
0xBB02D0F8	FC_Q_USED_PAGE_CNT [5][3].RESERVED[31:29]	3
0xBB02D0F8	FC_Q_USED_PAGE_CNT [5][3].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D0F8	FC_Q_USED_PAGE_CNT [5][3].RESERVED[15:13]	3
0xBB02D0F8	FC_Q_USED_PAGE_CNT [5][3].Q_USED_PAGE_CNT[12:0]	13
0xBB02D0FC	FC_Q_USED_PAGE_CNT [5][4].RESERVED[31:29]	3
0xBB02D0FC	FC_Q_USED_PAGE_CNT [5][4].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D0FC	FC_Q_USED_PAGE_CNT [5][4].RESERVED[15:13]	3
0xBB02D0FC	FC_Q_USED_PAGE_CNT [5][4].Q_USED_PAGE_CNT[12:0]	13
0xBB02D100	FC_Q_USED_PAGE_CNT [5][5].RESERVED[31:29]	3
0xBB02D100	FC_Q_USED_PAGE_CNT [5][5].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D100	FC_Q_USED_PAGE_CNT [5][5].RESERVED[15:13]	3
0xBB02D100	FC_Q_USED_PAGE_CNT [5][5].Q_USED_PAGE_CNT[12:0]	13
0xBB02D104	FC_Q_USED_PAGE_CNT [5][6].RESERVED[31:29]	3
0xBB02D104	FC_Q_USED_PAGE_CNT [5][6].Q_MAX_USED_PAGE_CNT[28:16]	13

Address	Register	Len
0xBB02D104	FC_Q_USED_PAGE_CNT [5][6].RESERVED[15:13]	3
0xBB02D104	FC_Q_USED_PAGE_CNT [5][6].Q_USED_PAGE_CNT[12:0]	13
0xBB02D108	FC_Q_USED_PAGE_CNT [5][7].RESERVED[31:29]	3
0xBB02D108	FC_Q_USED_PAGE_CNT [5][7].Q_MAX_USED_PAGE_CNT[28:16]	13
0xBB02D108	FC_Q_USED_PAGE_CNT [5][7].RESERVED[15:13]	3
0xBB02D108	FC_Q_USED_PAGE_CNT [5][7].Q_USED_PAGE_CNT[12:0]	13
0xBB02D10C	TH_TX_PREFET.RESERVED[31:8]	24
0xBB02D10C	TH_TX_PREFET.CFG_TH_TX_PREFET[7:0]	8
0xBB02D110	LOW_QUEUE_TH.RESERVED[31:13]	19
0xBB02D110	LOW_QUEUE_TH.LOW_QUEUE_TH[12:0]	13
0xBB02D114	HIGH_QUEUE_MSK [0].HIGH_QUEUE_MSK[7:0]	8
0xBB02D114	HIGH_QUEUE_MSK [1].HIGH_QUEUE_MSK[15:8]	8
0xBB02D114	HIGH_QUEUE_MSK [2].HIGH_QUEUE_MSK[23:16]	8
0xBB02D114	HIGH_QUEUE_MSK [3].HIGH_QUEUE_MSK[31:24]	8
0xBB02D118	HIGH_QUEUE_MSK [4].HIGH_QUEUE_MSK[7:0]	8
0xBB02D118	HIGH_QUEUE_MSK [5].HIGH_QUEUE_MSK[15:8]	8
0xBB02D118	HIGH_QUEUE_MSK [6].HIGH_QUEUE_MSK[23:16]	8
0xBB02D11C	P_QUEUE_EMPTY.RESERVED[31:7]	25
0xBB02D11C	P_QUEUE_EMPTY.EMPTY[6:0]	7
0xBB02D120	QUEUE_SEL_IND.RESERVED[31:19]	13
0xBB02D120	QUEUE_SEL_IND.CIR_SEL_IND[18:13]	6
0xBB02D120	QUEUE_SEL_IND.PIR_SEL_IND[12:7]	6
0xBB02D120	QUEUE_SEL_IND.QCNT_SEL_IND[6:0]	7
0xBB02D124	QUEUE_SEL_IND_DATA.CIR_QIN[31:16]	16
0xBB02D124	QUEUE_SEL_IND_DATA.PIR_QIN[15:0]	16
0xBB02D128	GPON_DPRU_RPT_PRD.RESERVED[31:5]	27
0xBB02D128	GPON_DPRU_RPT_PRD.RPT_PRD[4:0]	5
0xBB02D12C	PON_PIR_CIR_IFG.RESERVED[31:2]	30
0xBB02D12C	PON_PIR_CIR_IFG.DBA_IFG[1:1]	1
0xBB02D12C	PON_PIR_CIR_IFG.PIR_CIR_IFG[0:0]	1
0xBB02D130	RGF_VER_EGR_OUTQ.REGFILE_VER[31:0]	32
0xBB02D134	RSVD_EGR_OUTQ [0].RSVD_MEM[31:0]	32
0xBB02D138	RSVD_EGR_OUTQ [1].RSVD_MEM[31:0]	32
0xBB02D13C	RSVD_EGR_OUTQ [2].RSVD_MEM[31:0]	32
0xBB02D140	RSVD_EGR_OUTQ [3].RSVD_MEM[31:0]	32
0xBB02D144	RSVD_EGR_OUTQ [4].RSVD_MEM[31:0]	32
0xBB02D148	RSVD_EGR_OUTQ [5].RSVD_MEM[31:0]	32
0xBB02D14C	RSVD_EGR_OUTQ [6].RSVD_MEM[31:0]	32
0xBB02D150	RSVD_EGR_OUTQ [7].RSVD_MEM[31:0]	32
0xBB02D154	RSVD_EGR_OUTQ [8].RSVD_MEM[31:0]	32
0xBB02D158	RSVD_EGR_OUTQ [9].RSVD_MEM[31:0]	32
0xBB02D15C	RSVD_EGR_OUTQ [10].RSVD_MEM[31:0]	32
0xBB02D160	RSVD_EGR_OUTQ [11].RSVD_MEM[31:0]	32
0xBB02D164	RSVD_EGR_OUTQ [12].RSVD_MEM[31:0]	32
0xBB02D168	RSVD_EGR_OUTQ [13].RSVD_MEM[31:0]	32
0xBB02D16C	RSVD_EGR_OUTQ [14].RSVD_MEM[31:0]	32

Address	Register	Len
0xBB02D170	RSVD_EGR_OUTQ [15].RSVD_MEM[31:0]	32
0xBB02D800	WFQ_CTRL.RESERVED[31:17]	15
0xBB02D800	WFQ_CTRL.WFQ_IFG[16:16]	1
0xBB02D800	WFQ_CTRL.WFQ_BURSTSIZE[15:0]	16
0xBB02D804	EGR_BWCTRL_P_CTRL [0].RESERVED[31:18]	14
0xBB02D804	EGR_BWCTRL_P_CTRL [0].RATE[17:1]	17
0xBB02D804	EGR_BWCTRL_P_CTRL [0].IFG[0:0]	1
0xBB02D808	EGR_BWCTRL_P_CTRL [1].RESERVED[31:18]	14
0xBB02D808	EGR_BWCTRL_P_CTRL [1].RATE[17:1]	17
0xBB02D808	EGR_BWCTRL_P_CTRL [1].IFG[0:0]	1
0xBB02D80C	EGR_BWCTRL_P_CTRL [2].RESERVED[31:18]	14
0xBB02D80C	EGR_BWCTRL_P_CTRL [2].RATE[17:1]	17
0xBB02D80C	EGR_BWCTRL_P_CTRL [2].IFG[0:0]	1
0xBB02D810	EGR_BWCTRL_P_CTRL [3].RESERVED[31:18]	14
0xBB02D810	EGR_BWCTRL_P_CTRL [3].RATE[17:1]	17
0xBB02D810	EGR_BWCTRL_P_CTRL [3].IFG[0:0]	1
0xBB02D814	EGR_BWCTRL_P_CTRL [4].RESERVED[31:18]	14
0xBB02D814	EGR_BWCTRL_P_CTRL [4].RATE[17:1]	17
0xBB02D814	EGR_BWCTRL_P_CTRL [4].IFG[0:0]	1
0xBB02D818	EGR_BWCTRL_P_CTRL [5].RESERVED[31:18]	14
0xBB02D818	EGR_BWCTRL_P_CTRL [5].RATE[17:1]	17
0xBB02D818	EGR_BWCTRL_P_CTRL [5].IFG[0:0]	1
0xBB02D81C	EGR_BWCTRL_P_CTRL [6].RESERVED[31:18]	14
0xBB02D81C	EGR_BWCTRL_P_CTRL [6].RATE[17:1]	17
0xBB02D81C	EGR_BWCTRL_P_CTRL [6].IFG[0:0]	1
0xBB02D820	LINE_RATE_1G.RESERVED[31:17]	15
0xBB02D820	LINE_RATE_1G.RATE[16:0]	17
0xBB02D824	LINE_RATE_500M.RESERVED[31:17]	15
0xBB02D824	LINE_RATE_500M.RATE[16:0]	17
0xBB02D828	LINE_RATE_100M.RESERVED[31:17]	15
0xBB02D828	LINE_RATE_100M.RATE[16:0]	17
0xBB02D82C	LINE_RATE_10M.RESERVED[31:17]	15
0xBB02D82C	LINE_RATE_10M.RATE[16:0]	17
0xBB02D830	WFQ_PORT_CFG0 [0].WEIGHT0[15:0]	16
0xBB02D830	WFQ_PORT_CFG0 [1].WEIGHT0[31:16]	16
0xBB02D834	WFQ_PORT_CFG0 [2].WEIGHT0[15:0]	16
0xBB02D834	WFQ_PORT_CFG0 [3].WEIGHT0[31:16]	16
0xBB02D838	WFQ_PORT_CFG0 [4].WEIGHT0[15:0]	16
0xBB02D838	WFQ_PORT_CFG0 [5].WEIGHT0[31:16]	16
0xBB02D83C	WFQ_PORT_CFG0 [6].WEIGHT0[15:0]	16
0xBB02D840	WFQ_PORT_CFG1_7 [0][1].WEIGHT1_7[9:0]	10
0xBB02D840	WFQ_PORT_CFG1_7 [0][2].WEIGHT1_7[19:10]	10
0xBB02D840	WFQ_PORT_CFG1_7 [0][3].WEIGHT1_7[29:20]	10
0xBB02D844	WFQ_PORT_CFG1_7 [0][4].WEIGHT1_7[9:0]	10
0xBB02D844	WFQ_PORT_CFG1_7 [0][5].WEIGHT1_7[19:10]	10
0xBB02D844	WFQ_PORT_CFG1_7 [0][6].WEIGHT1_7[29:20]	10

Address	Register	Len
0xBB02D848	WFQ_PORT_CFG1_7 [0][7].WEIGHT1_7[9:0]	10
0xBB02D84C	WFQ_PORT_CFG1_7 [1][1].WEIGHT1_7[9:0]	10
0xBB02D84C	WFQ_PORT_CFG1_7 [1][2].WEIGHT1_7[19:10]	10
0xBB02D84C	WFQ_PORT_CFG1_7 [1][3].WEIGHT1_7[29:20]	10
0xBB02D850	WFQ_PORT_CFG1_7 [1][4].WEIGHT1_7[9:0]	10
0xBB02D850	WFQ_PORT_CFG1_7 [1][5].WEIGHT1_7[19:10]	10
0xBB02D850	WFQ_PORT_CFG1_7 [1][6].WEIGHT1_7[29:20]	10
0xBB02D854	WFQ_PORT_CFG1_7 [1][7].WEIGHT1_7[9:0]	10
0xBB02D858	WFQ_PORT_CFG1_7 [2][1].WEIGHT1_7[9:0]	10
0xBB02D858	WFQ_PORT_CFG1_7 [2][2].WEIGHT1_7[19:10]	10
0xBB02D858	WFQ_PORT_CFG1_7 [2][3].WEIGHT1_7[29:20]	10
0xBB02D85C	WFQ_PORT_CFG1_7 [2][4].WEIGHT1_7[9:0]	10
0xBB02D85C	WFQ_PORT_CFG1_7 [2][5].WEIGHT1_7[19:10]	10
0xBB02D85C	WFQ_PORT_CFG1_7 [2][6].WEIGHT1_7[29:20]	10
0xBB02D860	WFQ_PORT_CFG1_7 [2][7].WEIGHT1_7[9:0]	10
0xBB02D864	WFQ_PORT_CFG1_7 [3][1].WEIGHT1_7[9:0]	10
0xBB02D864	WFQ_PORT_CFG1_7 [3][2].WEIGHT1_7[19:10]	10
0xBB02D864	WFQ_PORT_CFG1_7 [3][3].WEIGHT1_7[29:20]	10
0xBB02D868	WFQ_PORT_CFG1_7 [3][4].WEIGHT1_7[9:0]	10
0xBB02D868	WFQ_PORT_CFG1_7 [3][5].WEIGHT1_7[19:10]	10
0xBB02D868	WFQ_PORT_CFG1_7 [3][6].WEIGHT1_7[29:20]	10
0xBB02D86C	WFQ_PORT_CFG1_7 [3][7].WEIGHT1_7[9:0]	10
0xBB02D870	WFQ_PORT_CFG1_7 [4][1].WEIGHT1_7[9:0]	10
0xBB02D870	WFQ_PORT_CFG1_7 [4][2].WEIGHT1_7[19:10]	10
0xBB02D870	WFQ_PORT_CFG1_7 [4][3].WEIGHT1_7[29:20]	10
0xBB02D874	WFQ_PORT_CFG1_7 [4][4].WEIGHT1_7[9:0]	10
0xBB02D874	WFQ_PORT_CFG1_7 [4][5].WEIGHT1_7[19:10]	10
0xBB02D874	WFQ_PORT_CFG1_7 [4][6].WEIGHT1_7[29:20]	10
0xBB02D878	WFQ_PORT_CFG1_7 [4][7].WEIGHT1_7[9:0]	10
0xBB02D87C	WFQ_PORT_CFG1_7 [5][1].WEIGHT1_7[9:0]	10
0xBB02D87C	WFQ_PORT_CFG1_7 [5][2].WEIGHT1_7[19:10]	10
0xBB02D87C	WFQ_PORT_CFG1_7 [5][3].WEIGHT1_7[29:20]	10
0xBB02D880	WFQ_PORT_CFG1_7 [5][4].WEIGHT1_7[9:0]	10
0xBB02D880	WFQ_PORT_CFG1_7 [5][5].WEIGHT1_7[19:10]	10
0xBB02D880	WFQ_PORT_CFG1_7 [5][6].WEIGHT1_7[29:20]	10
0xBB02D884	WFQ_PORT_CFG1_7 [5][7].WEIGHT1_7[9:0]	10
0xBB02D888	WFQ_PORT_CFG1_7 [6][1].WEIGHT1_7[9:0]	10
0xBB02D888	WFQ_PORT_CFG1_7 [6][2].WEIGHT1_7[19:10]	10
0xBB02D888	WFQ_PORT_CFG1_7 [6][3].WEIGHT1_7[29:20]	10
0xBB02D88C	WFQ_PORT_CFG1_7 [6][4].WEIGHT1_7[9:0]	10
0xBB02D88C	WFQ_PORT_CFG1_7 [6][5].WEIGHT1_7[19:10]	10
0xBB02D88C	WFQ_PORT_CFG1_7 [6][6].WEIGHT1_7[29:20]	10
0xBB02D890	WFQ_PORT_CFG1_7 [6][7].WEIGHT1_7[9:0]	10
0xBB02D894	WFQ_TYPE_PORT_CFG [0][0].QUEUE_TYPE[0:0]	1
0xBB02D894	WFQ_TYPE_PORT_CFG [0][1].QUEUE_TYPE[1:1]	1
0xBB02D894	WFQ_TYPE_PORT_CFG [0][2].QUEUE_TYPE[2:2]	1

Address	Register	Len
0xBB02D894	WFQ_TYPE_PORT_CFG [0][3].QUEUE_TYPE[3:3]	1
0xBB02D894	WFQ_TYPE_PORT_CFG [0][4].QUEUE_TYPE[4:4]	1
0xBB02D894	WFQ_TYPE_PORT_CFG [0][5].QUEUE_TYPE[5:5]	1
0xBB02D894	WFQ_TYPE_PORT_CFG [0][6].QUEUE_TYPE[6:6]	1
0xBB02D894	WFQ_TYPE_PORT_CFG [0][7].QUEUE_TYPE[7:7]	1
0xBB02D898	WFQ_TYPE_PORT_CFG [1][0].QUEUE_TYPE[0:0]	1
0xBB02D898	WFQ_TYPE_PORT_CFG [1][1].QUEUE_TYPE[1:1]	1
0xBB02D898	WFQ_TYPE_PORT_CFG [1][2].QUEUE_TYPE[2:2]	1
0xBB02D898	WFQ_TYPE_PORT_CFG [1][3].QUEUE_TYPE[3:3]	1
0xBB02D898	WFQ_TYPE_PORT_CFG [1][4].QUEUE_TYPE[4:4]	1
0xBB02D898	WFQ_TYPE_PORT_CFG [1][5].QUEUE_TYPE[5:5]	1
0xBB02D898	WFQ_TYPE_PORT_CFG [1][6].QUEUE_TYPE[6:6]	1
0xBB02D898	WFQ_TYPE_PORT_CFG [1][7].QUEUE_TYPE[7:7]	1
0xBB02D89C	WFQ_TYPE_PORT_CFG [2][0].QUEUE_TYPE[0:0]	1
0xBB02D89C	WFQ_TYPE_PORT_CFG [2][1].QUEUE_TYPE[1:1]	1
0xBB02D89C	WFQ_TYPE_PORT_CFG [2][2].QUEUE_TYPE[2:2]	1
0xBB02D89C	WFQ_TYPE_PORT_CFG [2][3].QUEUE_TYPE[3:3]	1
0xBB02D89C	WFQ_TYPE_PORT_CFG [2][4].QUEUE_TYPE[4:4]	1
0xBB02D89C	WFQ_TYPE_PORT_CFG [2][5].QUEUE_TYPE[5:5]	1
0xBB02D89C	WFQ_TYPE_PORT_CFG [2][6].QUEUE_TYPE[6:6]	1
0xBB02D89C	WFQ_TYPE_PORT_CFG [2][7].QUEUE_TYPE[7:7]	1
0xBB02D8A0	WFQ_TYPE_PORT_CFG [3][0].QUEUE_TYPE[0:0]	1
0xBB02D8A0	WFQ_TYPE_PORT_CFG [3][1].QUEUE_TYPE[1:1]	1
0xBB02D8A0	WFQ_TYPE_PORT_CFG [3][2].QUEUE_TYPE[2:2]	1
0xBB02D8A0	WFQ_TYPE_PORT_CFG [3][3].QUEUE_TYPE[3:3]	1
0xBB02D8A0	WFQ_TYPE_PORT_CFG [3][4].QUEUE_TYPE[4:4]	1
0xBB02D8A0	WFQ_TYPE_PORT_CFG [3][5].QUEUE_TYPE[5:5]	1
0xBB02D8A0	WFQ_TYPE_PORT_CFG [3][6].QUEUE_TYPE[6:6]	1
0xBB02D8A0	WFQ_TYPE_PORT_CFG [3][7].QUEUE_TYPE[7:7]	1
0xBB02D8A4	WFQ_TYPE_PORT_CFG [4][0].QUEUE_TYPE[0:0]	1
0xBB02D8A4	WFQ_TYPE_PORT_CFG [4][1].QUEUE_TYPE[1:1]	1
0xBB02D8A4	WFQ_TYPE_PORT_CFG [4][2].QUEUE_TYPE[2:2]	1
0xBB02D8A4	WFQ_TYPE_PORT_CFG [4][3].QUEUE_TYPE[3:3]	1
0xBB02D8A4	WFQ_TYPE_PORT_CFG [4][4].QUEUE_TYPE[4:4]	1
0xBB02D8A4	WFQ_TYPE_PORT_CFG [4][5].QUEUE_TYPE[5:5]	1
0xBB02D8A4	WFQ_TYPE_PORT_CFG [4][6].QUEUE_TYPE[6:6]	1
0xBB02D8A4	WFQ_TYPE_PORT_CFG [4][7].QUEUE_TYPE[7:7]	1
0xBB02D8A8	WFQ_TYPE_PORT_CFG [5][0].QUEUE_TYPE[0:0]	1
0xBB02D8A8	WFQ_TYPE_PORT_CFG [5][1].QUEUE_TYPE[1:1]	1
0xBB02D8A8	WFQ_TYPE_PORT_CFG [5][2].QUEUE_TYPE[2:2]	1
0xBB02D8A8	WFQ_TYPE_PORT_CFG [5][3].QUEUE_TYPE[3:3]	1
0xBB02D8A8	WFQ_TYPE_PORT_CFG [5][4].QUEUE_TYPE[4:4]	1
0xBB02D8A8	WFQ_TYPE_PORT_CFG [5][5].QUEUE_TYPE[5:5]	1
0xBB02D8A8	WFQ_TYPE_PORT_CFG [5][6].QUEUE_TYPE[6:6]	1
0xBB02D8A8	WFQ_TYPE_PORT_CFG [5][7].QUEUE_TYPE[7:7]	1
0xBB02D8AC	WFQ_TYPE_PORT_CFG [6][0].QUEUE_TYPE[0:0]	1



Address	Register	Len
0xBB02D8AC	WFQ_TYPE_PORT_CFG [6][1].QUEUE_TYPE[1:1]	1
0xBB02D8AC	WFQ_TYPE_PORT_CFG [6][2].QUEUE_TYPE[2:2]	1
0xBB02D8AC	WFQ_TYPE_PORT_CFG [6][3].QUEUE_TYPE[3:3]	1
0xBB02D8AC	WFQ_TYPE_PORT_CFG [6][4].QUEUE_TYPE[4:4]	1
0xBB02D8AC	WFQ_TYPE_PORT_CFG [6][5].QUEUE_TYPE[5:5]	1
0xBB02D8AC	WFQ_TYPE_PORT_CFG [6][6].QUEUE_TYPE[6:6]	1
0xBB02D8AC	WFQ_TYPE_PORT_CFG [6][7].QUEUE_TYPE[7:7]	1
0xBB02D8B0	APR_EN_PORT_CFG [0][0].EN[0:0]	1
0xBB02D8B0	APR_EN_PORT_CFG [0][1].EN[1:1]	1
0xBB02D8B0	APR_EN_PORT_CFG [0][2].EN[2:2]	1
0xBB02D8B0	APR_EN_PORT_CFG [0][3].EN[3:3]	1
0xBB02D8B0	APR_EN_PORT_CFG [0][4].EN[4:4]	1
0xBB02D8B0	APR_EN_PORT_CFG [0][5].EN[5:5]	1
0xBB02D8B0	APR_EN_PORT_CFG [0][6].EN[6:6]	1
0xBB02D8B0	APR_EN_PORT_CFG [0][7].EN[7:7]	1
0xBB02D8B4	APR_EN_PORT_CFG [1][0].EN[0:0]	1
0xBB02D8B4	APR_EN_PORT_CFG [1][1].EN[1:1]	1
0xBB02D8B4	APR_EN_PORT_CFG [1][2].EN[2:2]	1
0xBB02D8B4	APR_EN_PORT_CFG [1][3].EN[3:3]	1
0xBB02D8B4	APR_EN_PORT_CFG [1][4].EN[4:4]	1
0xBB02D8B4	APR_EN_PORT_CFG [1][5].EN[5:5]	1
0xBB02D8B4	APR_EN_PORT_CFG [1][6].EN[6:6]	1
0xBB02D8B4	APR_EN_PORT_CFG [1][7].EN[7:7]	1
0xBB02D8B8	APR_EN_PORT_CFG [2][0].EN[0:0]	1
0xBB02D8B8	APR_EN_PORT_CFG [2][1].EN[1:1]	1
0xBB02D8B8	APR_EN_PORT_CFG [2][2].EN[2:2]	1
0xBB02D8B8	APR_EN_PORT_CFG [2][3].EN[3:3]	1
0xBB02D8B8	APR_EN_PORT_CFG [2][4].EN[4:4]	1
0xBB02D8B8	APR_EN_PORT_CFG [2][5].EN[5:5]	1
0xBB02D8B8	APR_EN_PORT_CFG [2][6].EN[6:6]	1
0xBB02D8B8	APR_EN_PORT_CFG [2][7].EN[7:7]	1
0xBB02D8BC	APR_EN_PORT_CFG [3][0].EN[0:0]	1
0xBB02D8BC	APR_EN_PORT_CFG [3][1].EN[1:1]	1
0xBB02D8BC	APR_EN_PORT_CFG [3][2].EN[2:2]	1
0xBB02D8BC	APR_EN_PORT_CFG [3][3].EN[3:3]	1
0xBB02D8BC	APR_EN_PORT_CFG [3][4].EN[4:4]	1
0xBB02D8BC	APR_EN_PORT_CFG [3][5].EN[5:5]	1
0xBB02D8BC	APR_EN_PORT_CFG [3][6].EN[6:6]	1
0xBB02D8BC	APR_EN_PORT_CFG [3][7].EN[7:7]	1
0xBB02D8C0	APR_EN_PORT_CFG [4][0].EN[0:0]	1
0xBB02D8C0	APR_EN_PORT_CFG [4][1].EN[1:1]	1
0xBB02D8C0	APR_EN_PORT_CFG [4][2].EN[2:2]	1
0xBB02D8C0	APR_EN_PORT_CFG [4][3].EN[3:3]	1
0xBB02D8C0	APR_EN_PORT_CFG [4][4].EN[4:4]	1
0xBB02D8C0	APR_EN_PORT_CFG [4][5].EN[5:5]	1
0xBB02D8C0	APR_EN_PORT_CFG [4][6].EN[6:6]	1

Address	Register	Len
0xBB02D8C0	APR_EN_PORT_CFG [4][7].EN[7:7]	1
0xBB02D8C4	APR_EN_PORT_CFG [5][0].EN[0:0]	1
0xBB02D8C4	APR_EN_PORT_CFG [5][1].EN[1:1]	1
0xBB02D8C4	APR_EN_PORT_CFG [5][2].EN[2:2]	1
0xBB02D8C4	APR_EN_PORT_CFG [5][3].EN[3:3]	1
0xBB02D8C4	APR_EN_PORT_CFG [5][4].EN[4:4]	1
0xBB02D8C4	APR_EN_PORT_CFG [5][5].EN[5:5]	1
0xBB02D8C4	APR_EN_PORT_CFG [5][6].EN[6:6]	1
0xBB02D8C4	APR_EN_PORT_CFG [5][7].EN[7:7]	1
0xBB02D8C8	APR_EN_PORT_CFG [6][0].EN[0:0]	1
0xBB02D8C8	APR_EN_PORT_CFG [6][1].EN[1:1]	1
0xBB02D8C8	APR_EN_PORT_CFG [6][2].EN[2:2]	1
0xBB02D8C8	APR_EN_PORT_CFG [6][3].EN[3:3]	1
0xBB02D8C8	APR_EN_PORT_CFG [6][4].EN[4:4]	1
0xBB02D8C8	APR_EN_PORT_CFG [6][5].EN[5:5]	1
0xBB02D8C8	APR_EN_PORT_CFG [6][6].EN[6:6]	1
0xBB02D8C8	APR_EN_PORT_CFG [6][7].EN[7:7]	1
0xBB02D8CC	CPU_PORT_RATE_CFG.RESERVED[31:1]	31
0xBB02D8CC	CPU_PORT_RATE_CFG.BYPASS_LINE_RATE[0:0]	1
0xBB02D8D0	APR_METER_PORT_CFG [0][0].IDX[2:0]	3
0xBB02D8D0	APR_METER_PORT_CFG [0][1].IDX[5:3]	3
0xBB02D8D0	APR_METER_PORT_CFG [0][2].IDX[8:6]	3
0xBB02D8D0	APR_METER_PORT_CFG [0][3].IDX[11:9]	3
0xBB02D8D0	APR_METER_PORT_CFG [0][4].IDX[14:12]	3
0xBB02D8D0	APR_METER_PORT_CFG [0][5].IDX[17:15]	3
0xBB02D8D0	APR_METER_PORT_CFG [0][6].IDX[20:18]	3
0xBB02D8D0	APR_METER_PORT_CFG [0][7].IDX[23:21]	3
0xBB02D8D4	APR_METER_PORT_CFG [1][0].IDX[2:0]	3
0xBB02D8D4	APR_METER_PORT_CFG [1][1].IDX[5:3]	3
0xBB02D8D4	APR_METER_PORT_CFG [1][2].IDX[8:6]	3
0xBB02D8D4	APR_METER_PORT_CFG [1][3].IDX[11:9]	3
0xBB02D8D4	APR_METER_PORT_CFG [1][4].IDX[14:12]	3
0xBB02D8D4	APR_METER_PORT_CFG [1][5].IDX[17:15]	3
0xBB02D8D4	APR_METER_PORT_CFG [1][6].IDX[20:18]	3
0xBB02D8D4	APR_METER_PORT_CFG [1][7].IDX[23:21]	3
0xBB02D8D8	APR_METER_PORT_CFG [2][0].IDX[2:0]	3
0xBB02D8D8	APR_METER_PORT_CFG [2][1].IDX[5:3]	3
0xBB02D8D8	APR_METER_PORT_CFG [2][2].IDX[8:6]	3
0xBB02D8D8	APR_METER_PORT_CFG [2][3].IDX[11:9]	3
0xBB02D8D8	APR_METER_PORT_CFG [2][4].IDX[14:12]	3
0xBB02D8D8	APR_METER_PORT_CFG [2][5].IDX[17:15]	3
0xBB02D8D8	APR_METER_PORT_CFG [2][6].IDX[20:18]	3
0xBB02D8D8	APR_METER_PORT_CFG [2][7].IDX[23:21]	3
0xBB02D8DC	APR_METER_PORT_CFG [3][0].IDX[2:0]	3
0xBB02D8DC	APR_METER_PORT_CFG [3][1].IDX[5:3]	3
0xBB02D8DC	APR_METER_PORT_CFG [3][2].IDX[8:6]	3



Address	Register	Len
0xBB02D8DC	APR_METER_PORT_CFG [3][3].IDX[11:9]	3
0xBB02D8DC	APR_METER_PORT_CFG [3][4].IDX[14:12]	3
0xBB02D8DC	APR_METER_PORT_CFG [3][5].IDX[17:15]	3
0xBB02D8DC	APR_METER_PORT_CFG [3][6].IDX[20:18]	3
0xBB02D8DC	APR_METER_PORT_CFG [3][7].IDX[23:21]	3
0xBB02D8E0	APR_METER_PORT_CFG [4][0].IDX[2:0]	3
0xBB02D8E0	APR_METER_PORT_CFG [4][1].IDX[5:3]	3
0xBB02D8E0	APR_METER_PORT_CFG [4][2].IDX[8:6]	3
0xBB02D8E0	APR_METER_PORT_CFG [4][3].IDX[11:9]	3
0xBB02D8E0	APR_METER_PORT_CFG [4][4].IDX[14:12]	3
0xBB02D8E0	APR_METER_PORT_CFG [4][5].IDX[17:15]	3
0xBB02D8E0	APR_METER_PORT_CFG [4][6].IDX[20:18]	3
0xBB02D8E0	APR_METER_PORT_CFG [4][7].IDX[23:21]	3
0xBB02D8E4	APR_METER_PORT_CFG [5][0].IDX[2:0]	3
0xBB02D8E4	APR_METER_PORT_CFG [5][1].IDX[5:3]	3
0xBB02D8E4	APR_METER_PORT_CFG [5][2].IDX[8:6]	3
0xBB02D8E4	APR_METER_PORT_CFG [5][3].IDX[11:9]	3
0xBB02D8E4	APR_METER_PORT_CFG [5][4].IDX[14:12]	3
0xBB02D8E4	APR_METER_PORT_CFG [5][5].IDX[17:15]	3
0xBB02D8E4	APR_METER_PORT_CFG [5][6].IDX[20:18]	3
0xBB02D8E4	APR_METER_PORT_CFG [5][7].IDX[23:21]	3
0xBB02D8E8	APR_METER_PORT_CFG [6][0].IDX[2:0]	3
0xBB02D8E8	APR_METER_PORT_CFG [6][1].IDX[5:3]	3
0xBB02D8E8	APR_METER_PORT_CFG [6][2].IDX[8:6]	3
0xBB02D8E8	APR_METER_PORT_CFG [6][3].IDX[11:9]	3
0xBB02D8E8	APR_METER_PORT_CFG [6][4].IDX[14:12]	3
0xBB02D8E8	APR_METER_PORT_CFG [6][5].IDX[17:15]	3
0xBB02D8E8	APR_METER_PORT_CFG [6][6].IDX[20:18]	3
0xBB02D8E8	APR_METER_PORT_CFG [6][7].IDX[23:21]	3
0xBB02D8EC	MOCIR_TH_H.RESERVED[31:17]	15
0xBB02D8EC	MOCIR_TH_H.MOCIR_TH_H[16:0]	17
0xBB02D8F0	MOCIR_TH_L.RESERVED[31:17]	15
0xBB02D8F0	MOCIR_TH_L.MOCIR_TH_L[16:0]	17
0xBB02D8F4	MOCIR_BPT.RESERVED[31:8]	24
0xBB02D8F4	MOCIR_BPT.MOCIR_BPT[7:0]	8
0xBB02D8F8	MOCIR_FRC_MD.MOCIR_FRC_MD[31:0]	32
0xBB02D8FC	MOCIR_FRC_VAL.MOCIR_FRC_VAL[31:0]	32
0xBB02D900	PON_CFG.RESERVED[31:19]	13
0xBB02D900	PON_CFG.PON_REV[18:18]	1
0xBB02D900	PON_CFG.PIR_EXCEED_DROP[17:17]	1
0xBB02D900	PON_CFG.EGR_RATE[16:0]	17
0xBB02D904	PON_QID_CIR_RATE [0].RATE[16:0]	17
0xBB02D908	PON_QID_CIR_RATE [1].RATE[16:0]	17
0xBB02D90C	PON_QID_CIR_RATE [2].RATE[16:0]	17
0xBB02D910	PON_QID_CIR_RATE [3].RATE[16:0]	17
0xBB02D914	PON_QID_CIR_RATE [4].RATE[16:0]	17

Address	Register	Len
0xBB02D918	PON_QID_CIR_RATE [5].RATE[16:0]	17
0xBB02D91C	PON_QID_CIR_RATE [6].RATE[16:0]	17
0xBB02D920	PON_QID_CIR_RATE [7].RATE[16:0]	17
0xBB02D924	PON_QID_CIR_RATE [8].RATE[16:0]	17
0xBB02D928	PON_QID_CIR_RATE [9].RATE[16:0]	17
0xBB02D92C	PON_QID_CIR_RATE [10].RATE[16:0]	17
0xBB02D930	PON_QID_CIR_RATE [11].RATE[16:0]	17
0xBB02D934	PON_QID_CIR_RATE [12].RATE[16:0]	17
0xBB02D938	PON_QID_CIR_RATE [13].RATE[16:0]	17
0xBB02D93C	PON_QID_CIR_RATE [14].RATE[16:0]	17
0xBB02D940	PON_QID_CIR_RATE [15].RATE[16:0]	17
0xBB02D944	PON_QID_CIR_RATE [16].RATE[16:0]	17
0xBB02D948	PON_QID_CIR_RATE [17].RATE[16:0]	17
0xBB02D94C	PON_QID_CIR_RATE [18].RATE[16:0]	17
0xBB02D950	PON_QID_CIR_RATE [19].RATE[16:0]	17
0xBB02D954	PON_QID_CIR_RATE [20].RATE[16:0]	17
0xBB02D958	PON_QID_CIR_RATE [21].RATE[16:0]	17
0xBB02D95C	PON_QID_CIR_RATE [22].RATE[16:0]	17
0xBB02D960	PON_QID_CIR_RATE [23].RATE[16:0]	17
0xBB02D964	PON_QID_CIR_RATE [24].RATE[16:0]	17
0xBB02D968	PON_QID_CIR_RATE [25].RATE[16:0]	17
0xBB02D96C	PON_QID_CIR_RATE [26].RATE[16:0]	17
0xBB02D970	PON_QID_CIR_RATE [27].RATE[16:0]	17
0xBB02D974	PON_QID_CIR_RATE [28].RATE[16:0]	17
0xBB02D978	PON_QID_CIR_RATE [29].RATE[16:0]	17
0xBB02D97C	PON_QID_CIR_RATE [30].RATE[16:0]	17
0xBB02D980	PON_QID_CIR_RATE [31].RATE[16:0]	17
0xBB02D984	PON_QID_CIR_RATE [32].RATE[16:0]	17
0xBB02D988	PON_QID_CIR_RATE [33].RATE[16:0]	17
0xBB02D98C	PON_QID_CIR_RATE [34].RATE[16:0]	17
0xBB02D990	PON_QID_CIR_RATE [35].RATE[16:0]	17
0xBB02D994	PON_QID_CIR_RATE [36].RATE[16:0]	17
0xBB02D998	PON_QID_CIR_RATE [37].RATE[16:0]	17
0xBB02D99C	PON_QID_CIR_RATE [38].RATE[16:0]	17
0xBB02D9A0	PON_QID_CIR_RATE [39].RATE[16:0]	17
0xBB02D9A4	PON_QID_CIR_RATE [40].RATE[16:0]	17
0xBB02D9A8	PON_QID_CIR_RATE [41].RATE[16:0]	17
0xBB02D9AC	PON_QID_CIR_RATE [42].RATE[16:0]	17
0xBB02D9B0	PON_QID_CIR_RATE [43].RATE[16:0]	17
0xBB02D9B4	PON_QID_CIR_RATE [44].RATE[16:0]	17
0xBB02D9B8	PON_QID_CIR_RATE [45].RATE[16:0]	17
0xBB02D9BC	PON_QID_CIR_RATE [46].RATE[16:0]	17
0xBB02D9C0	PON_QID_CIR_RATE [47].RATE[16:0]	17
0xBB02D9C4	PON_QID_CIR_RATE [48].RATE[16:0]	17
0xBB02D9C8	PON_QID_CIR_RATE [49].RATE[16:0]	17
0xBB02D9CC	PON_QID_CIR_RATE [50].RATE[16:0]	17

Address	Register	Len
0xBB02D9D0	PON_QID_CIR_RATE [51].RATE[16:0]	17
0xBB02D9D4	PON_QID_CIR_RATE [52].RATE[16:0]	17
0xBB02D9D8	PON_QID_CIR_RATE [53].RATE[16:0]	17
0xBB02D9DC	PON_QID_CIR_RATE [54].RATE[16:0]	17
0xBB02D9E0	PON_QID_CIR_RATE [55].RATE[16:0]	17
0xBB02D9E4	PON_QID_CIR_RATE [56].RATE[16:0]	17
0xBB02D9E8	PON_QID_CIR_RATE [57].RATE[16:0]	17
0xBB02D9EC	PON_QID_CIR_RATE [58].RATE[16:0]	17
0xBB02D9F0	PON_QID_CIR_RATE [59].RATE[16:0]	17
0xBB02D9F4	PON_QID_CIR_RATE [60].RATE[16:0]	17
0xBB02D9F8	PON_QID_CIR_RATE [61].RATE[16:0]	17
0xBB02D9FC	PON_QID_CIR_RATE [62].RATE[16:0]	17
0xBB02DA00	PON_QID_CIR_RATE [63].RATE[16:0]	17
0xBB02DA04	PON_QID_CIR_RATE [64].RATE[16:0]	17
0xBB02DA08	PON_QID_CIR_RATE [65].RATE[16:0]	17
0xBB02DA0C	PON_QID_CIR_RATE [66].RATE[16:0]	17
0xBB02DA10	PON_QID_CIR_RATE [67].RATE[16:0]	17
0xBB02DA14	PON_QID_CIR_RATE [68].RATE[16:0]	17
0xBB02DA18	PON_QID_CIR_RATE [69].RATE[16:0]	17
0xBB02DA1C	PON_QID_CIR_RATE [70].RATE[16:0]	17
0xBB02DA20	PON_QID_CIR_RATE [71].RATE[16:0]	17
0xBB02DA24	PON_QID_CIR_RATE [72].RATE[16:0]	17
0xBB02DA28	PON_QID_CIR_RATE [73].RATE[16:0]	17
0xBB02DA2C	PON_QID_CIR_RATE [74].RATE[16:0]	17
0xBB02DA30	PON_QID_CIR_RATE [75].RATE[16:0]	17
0xBB02DA34	PON_QID_CIR_RATE [76].RATE[16:0]	17
0xBB02DA38	PON_QID_CIR_RATE [77].RATE[16:0]	17
0xBB02DA3C	PON_QID_CIR_RATE [78].RATE[16:0]	17
0xBB02DA40	PON_QID_CIR_RATE [79].RATE[16:0]	17
0xBB02DA44	PON_QID_CIR_RATE [80].RATE[16:0]	17
0xBB02DA48	PON_QID_CIR_RATE [81].RATE[16:0]	17
0xBB02DA4C	PON_QID_CIR_RATE [82].RATE[16:0]	17
0xBB02DA50	PON_QID_CIR_RATE [83].RATE[16:0]	17
0xBB02DA54	PON_QID_CIR_RATE [84].RATE[16:0]	17
0xBB02DA58	PON_QID_CIR_RATE [85].RATE[16:0]	17
0xBB02DA5C	PON_QID_CIR_RATE [86].RATE[16:0]	17
0xBB02DA60	PON_QID_CIR_RATE [87].RATE[16:0]	17
0xBB02DA64	PON_QID_CIR_RATE [88].RATE[16:0]	17
0xBB02DA68	PON_QID_CIR_RATE [89].RATE[16:0]	17
0xBB02DA6C	PON_QID_CIR_RATE [90].RATE[16:0]	17
0xBB02DA70	PON_QID_CIR_RATE [91].RATE[16:0]	17
0xBB02DA74	PON_QID_CIR_RATE [92].RATE[16:0]	17
0xBB02DA78	PON_QID_CIR_RATE [93].RATE[16:0]	17
0xBB02DA7C	PON_QID_CIR_RATE [94].RATE[16:0]	17
0xBB02DA80	PON_QID_CIR_RATE [95].RATE[16:0]	17
0xBB02DA84	PON_QID_CIR_RATE [96].RATE[16:0]	17

Address	Register	Len
0xBB02DA88	PON_QID_CIR_RATE [97].RATE[16:0]	17
0xBB02DA8C	PON_QID_CIR_RATE [98].RATE[16:0]	17
0xBB02DA90	PON_QID_CIR_RATE [99].RATE[16:0]	17
0xBB02DA94	PON_QID_CIR_RATE [100].RATE[16:0]	17
0xBB02DA98	PON_QID_CIR_RATE [101].RATE[16:0]	17
0xBB02DA9C	PON_QID_CIR_RATE [102].RATE[16:0]	17
0xBB02DAA0	PON_QID_CIR_RATE [103].RATE[16:0]	17
0xBB02DAA4	PON_QID_CIR_RATE [104].RATE[16:0]	17
0xBB02DAA8	PON_QID_CIR_RATE [105].RATE[16:0]	17
0xBB02DAAC	PON_QID_CIR_RATE [106].RATE[16:0]	17
0xBB02DAB0	PON_QID_CIR_RATE [107].RATE[16:0]	17
0xBB02DAB4	PON_QID_CIR_RATE [108].RATE[16:0]	17
0xBB02DAB8	PON_QID_CIR_RATE [109].RATE[16:0]	17
0xBB02DABC	PON_QID_CIR_RATE [110].RATE[16:0]	17
0xBB02DAC0	PON_QID_CIR_RATE [111].RATE[16:0]	17
0xBB02DAC4	PON_QID_CIR_RATE [112].RATE[16:0]	17
0xBB02DAC8	PON_QID_CIR_RATE [113].RATE[16:0]	17
0xBB02DACC	PON_QID_CIR_RATE [114].RATE[16:0]	17
0xBB02DAD0	PON_QID_CIR_RATE [115].RATE[16:0]	17
0xBB02DAD4	PON_QID_CIR_RATE [116].RATE[16:0]	17
0xBB02DAD8	PON_QID_CIR_RATE [117].RATE[16:0]	17
0xBB02DADC	PON_QID_CIR_RATE [118].RATE[16:0]	17
0xBB02DAE0	PON_QID_CIR_RATE [119].RATE[16:0]	17
0xBB02DAE4	PON_QID_CIR_RATE [120].RATE[16:0]	17
0xBB02DAE8	PON_QID_CIR_RATE [121].RATE[16:0]	17
0xBB02DAEC	PON_QID_CIR_RATE [122].RATE[16:0]	17
0xBB02DAF0	PON_QID_CIR_RATE [123].RATE[16:0]	17
0xBB02DAF4	PON_QID_CIR_RATE [124].RATE[16:0]	17
0xBB02DAF8	PON_QID_CIR_RATE [125].RATE[16:0]	17
0xBB02DAFC	PON_QID_CIR_RATE [126].RATE[16:0]	17
0xBB02DB00	PON_QID_CIR_RATE [127].RATE[16:0]	17
0xBB02DB04	PON_QID_PIR_RATE [0].RATE[16:0]	17
0xBB02DB08	PON_QID_PIR_RATE [1].RATE[16:0]	17
0xBB02DB0C	PON_QID_PIR_RATE [2].RATE[16:0]	17
0xBB02DB10	PON_QID_PIR_RATE [3].RATE[16:0]	17
0xBB02DB14	PON_QID_PIR_RATE [4].RATE[16:0]	17
0xBB02DB18	PON_QID_PIR_RATE [5].RATE[16:0]	17
0xBB02DB1C	PON_QID_PIR_RATE [6].RATE[16:0]	17
0xBB02DB20	PON_QID_PIR_RATE [7].RATE[16:0]	17
0xBB02DB24	PON_QID_PIR_RATE [8].RATE[16:0]	17
0xBB02DB28	PON_QID_PIR_RATE [9].RATE[16:0]	17
0xBB02DB2C	PON_QID_PIR_RATE [10].RATE[16:0]	17
0xBB02DB30	PON_QID_PIR_RATE [11].RATE[16:0]	17
0xBB02DB34	PON_QID_PIR_RATE [12].RATE[16:0]	17
0xBB02DB38	PON_QID_PIR_RATE [13].RATE[16:0]	17
0xBB02DB3C	PON_QID_PIR_RATE [14].RATE[16:0]	17

Address	Register	Len
0xBB02DB40	PON_QID_PIR_RATE [15].RATE[16:0]	17
0xBB02DB44	PON_QID_PIR_RATE [16].RATE[16:0]	17
0xBB02DB48	PON_QID_PIR_RATE [17].RATE[16:0]	17
0xBB02DB4C	PON_QID_PIR_RATE [18].RATE[16:0]	17
0xBB02DB50	PON_QID_PIR_RATE [19].RATE[16:0]	17
0xBB02DB54	PON_QID_PIR_RATE [20].RATE[16:0]	17
0xBB02DB58	PON_QID_PIR_RATE [21].RATE[16:0]	17
0xBB02DB5C	PON_QID_PIR_RATE [22].RATE[16:0]	17
0xBB02DB60	PON_QID_PIR_RATE [23].RATE[16:0]	17
0xBB02DB64	PON_QID_PIR_RATE [24].RATE[16:0]	17
0xBB02DB68	PON_QID_PIR_RATE [25].RATE[16:0]	17
0xBB02DB6C	PON_QID_PIR_RATE [26].RATE[16:0]	17
0xBB02DB70	PON_QID_PIR_RATE [27].RATE[16:0]	17
0xBB02DB74	PON_QID_PIR_RATE [28].RATE[16:0]	17
0xBB02DB78	PON_QID_PIR_RATE [29].RATE[16:0]	17
0xBB02DB7C	PON_QID_PIR_RATE [30].RATE[16:0]	17
0xBB02DB80	PON_QID_PIR_RATE [31].RATE[16:0]	17
0xBB02DB84	PON_QID_PIR_RATE [32].RATE[16:0]	17
0xBB02DB88	PON_QID_PIR_RATE [33].RATE[16:0]	17
0xBB02DB8C	PON_QID_PIR_RATE [34].RATE[16:0]	17
0xBB02DB90	PON_QID_PIR_RATE [35].RATE[16:0]	17
0xBB02DB94	PON_QID_PIR_RATE [36].RATE[16:0]	17
0xBB02DB98	PON_QID_PIR_RATE [37].RATE[16:0]	17
0xBB02DB9C	PON_QID_PIR_RATE [38].RATE[16:0]	17
0xBB02DBA0	PON_QID_PIR_RATE [39].RATE[16:0]	17
0xBB02DBA4	PON_QID_PIR_RATE [40].RATE[16:0]	17
0xBB02DBA8	PON_QID_PIR_RATE [41].RATE[16:0]	17
0xBB02DBAC	PON_QID_PIR_RATE [42].RATE[16:0]	17
0xBB02DBB0	PON_QID_PIR_RATE [43].RATE[16:0]	17
0xBB02DBB4	PON_QID_PIR_RATE [44].RATE[16:0]	17
0xBB02DBB8	PON_QID_PIR_RATE [45].RATE[16:0]	17
0xBB02DBBC	PON_QID_PIR_RATE [46].RATE[16:0]	17
0xBB02DBC0	PON_QID_PIR_RATE [47].RATE[16:0]	17
0xBB02DBC4	PON_QID_PIR_RATE [48].RATE[16:0]	17
0xBB02DBC8	PON_QID_PIR_RATE [49].RATE[16:0]	17
0xBB02DBCC	PON_QID_PIR_RATE [50].RATE[16:0]	17
0xBB02DBD0	PON_QID_PIR_RATE [51].RATE[16:0]	17
0xBB02DBD4	PON_QID_PIR_RATE [52].RATE[16:0]	17
0xBB02DBD8	PON_QID_PIR_RATE [53].RATE[16:0]	17
0xBB02DBDC	PON_QID_PIR_RATE [54].RATE[16:0]	17
0xBB02DBE0	PON_QID_PIR_RATE [55].RATE[16:0]	17
0xBB02DBE4	PON_QID_PIR_RATE [56].RATE[16:0]	17
0xBB02DBE8	PON_QID_PIR_RATE [57].RATE[16:0]	17
0xBB02DBEC	PON_QID_PIR_RATE [58].RATE[16:0]	17
0xBB02DBF0	PON_QID_PIR_RATE [59].RATE[16:0]	17
0xBB02DBF4	PON_QID_PIR_RATE [60].RATE[16:0]	17

Address	Register	Len
0xBB02DBF8	PON_QID_PIR_RATE [61].RATE[16:0]	17
0xBB02DBFC	PON_QID_PIR_RATE [62].RATE[16:0]	17
0xBB02DC00	PON_QID_PIR_RATE [63].RATE[16:0]	17
0xBB02DC04	PON_QID_PIR_RATE [64].RATE[16:0]	17
0xBB02DC08	PON_QID_PIR_RATE [65].RATE[16:0]	17
0xBB02DC0C	PON_QID_PIR_RATE [66].RATE[16:0]	17
0xBB02DC10	PON_QID_PIR_RATE [67].RATE[16:0]	17
0xBB02DC14	PON_QID_PIR_RATE [68].RATE[16:0]	17
0xBB02DC18	PON_QID_PIR_RATE [69].RATE[16:0]	17
0xBB02DC1C	PON_QID_PIR_RATE [70].RATE[16:0]	17
0xBB02DC20	PON_QID_PIR_RATE [71].RATE[16:0]	17
0xBB02DC24	PON_QID_PIR_RATE [72].RATE[16:0]	17
0xBB02DC28	PON_QID_PIR_RATE [73].RATE[16:0]	17
0xBB02DC2C	PON_QID_PIR_RATE [74].RATE[16:0]	17
0xBB02DC30	PON_QID_PIR_RATE [75].RATE[16:0]	17
0xBB02DC34	PON_QID_PIR_RATE [76].RATE[16:0]	17
0xBB02DC38	PON_QID_PIR_RATE [77].RATE[16:0]	17
0xBB02DC3C	PON_QID_PIR_RATE [78].RATE[16:0]	17
0xBB02DC40	PON_QID_PIR_RATE [79].RATE[16:0]	17
0xBB02DC44	PON_QID_PIR_RATE [80].RATE[16:0]	17
0xBB02DC48	PON_QID_PIR_RATE [81].RATE[16:0]	17
0xBB02DC4C	PON_QID_PIR_RATE [82].RATE[16:0]	17
0xBB02DC50	PON_QID_PIR_RATE [83].RATE[16:0]	17
0xBB02DC54	PON_QID_PIR_RATE [84].RATE[16:0]	17
0xBB02DC58	PON_QID_PIR_RATE [85].RATE[16:0]	17
0xBB02DC5C	PON_QID_PIR_RATE [86].RATE[16:0]	17
0xBB02DC60	PON_QID_PIR_RATE [87].RATE[16:0]	17
0xBB02DC64	PON_QID_PIR_RATE [88].RATE[16:0]	17
0xBB02DC68	PON_QID_PIR_RATE [89].RATE[16:0]	17
0xBB02DC6C	PON_QID_PIR_RATE [90].RATE[16:0]	17
0xBB02DC70	PON_QID_PIR_RATE [91].RATE[16:0]	17
0xBB02DC74	PON_QID_PIR_RATE [92].RATE[16:0]	17
0xBB02DC78	PON_QID_PIR_RATE [93].RATE[16:0]	17
0xBB02DC7C	PON_QID_PIR_RATE [94].RATE[16:0]	17
0xBB02DC80	PON_QID_PIR_RATE [95].RATE[16:0]	17
0xBB02DC84	PON_QID_PIR_RATE [96].RATE[16:0]	17
0xBB02DC88	PON_QID_PIR_RATE [97].RATE[16:0]	17
0xBB02DC8C	PON_QID_PIR_RATE [98].RATE[16:0]	17
0xBB02DC90	PON_QID_PIR_RATE [99].RATE[16:0]	17
0xBB02DC94	PON_QID_PIR_RATE [100].RATE[16:0]	17
0xBB02DC98	PON_QID_PIR_RATE [101].RATE[16:0]	17
0xBB02DC9C	PON_QID_PIR_RATE [102].RATE[16:0]	17
0xBB02DCA0	PON_QID_PIR_RATE [103].RATE[16:0]	17
0xBB02DCA4	PON_QID_PIR_RATE [104].RATE[16:0]	17
0xBB02DCA8	PON_QID_PIR_RATE [105].RATE[16:0]	17
0xBB02DCAC	PON_QID_PIR_RATE [106].RATE[16:0]	17

Address	Register	Len
0xBB02DCB0	PON_QID_PIR_RATE [107].RATE[16:0]	17
0xBB02DCB4	PON_QID_PIR_RATE [108].RATE[16:0]	17
0xBB02DCB8	PON_QID_PIR_RATE [109].RATE[16:0]	17
0xBB02DCBC	PON_QID_PIR_RATE [110].RATE[16:0]	17
0xBB02DCC0	PON_QID_PIR_RATE [111].RATE[16:0]	17
0xBB02DCC4	PON_QID_PIR_RATE [112].RATE[16:0]	17
0xBB02DCC8	PON_QID_PIR_RATE [113].RATE[16:0]	17
0xBB02DCCC	PON_QID_PIR_RATE [114].RATE[16:0]	17
0xBB02DCD0	PON_QID_PIR_RATE [115].RATE[16:0]	17
0xBB02DCD4	PON_QID_PIR_RATE [116].RATE[16:0]	17
0xBB02DCD8	PON_QID_PIR_RATE [117].RATE[16:0]	17
0xBB02DCDC	PON_QID_PIR_RATE [118].RATE[16:0]	17
0xBB02DCE0	PON_QID_PIR_RATE [119].RATE[16:0]	17
0xBB02DCE4	PON_QID_PIR_RATE [120].RATE[16:0]	17
0xBB02DCE8	PON_QID_PIR_RATE [121].RATE[16:0]	17
0xBB02DCEC	PON_QID_PIR_RATE [122].RATE[16:0]	17
0xBB02DCF0	PON_QID_PIR_RATE [123].RATE[16:0]	17
0xBB02DCF4	PON_QID_PIR_RATE [124].RATE[16:0]	17
0xBB02DCF8	PON_QID_PIR_RATE [125].RATE[16:0]	17
0xBB02DCFC	PON_QID_PIR_RATE [126].RATE[16:0]	17
0xBB02DD00	PON_QID_PIR_RATE [127].RATE[16:0]	17
0xBB02DD04	PON_SCH_QMAP [0].MAPPING_TBL[31:0]	32
0xBB02DD08	PON_SCH_QMAP [1].MAPPING_TBL[31:0]	32
0xBB02DD0C	PON_SCH_QMAP [2].MAPPING_TBL[31:0]	32
0xBB02DD10	PON_SCH_QMAP [3].MAPPING_TBL[31:0]	32
0xBB02DD14	PON_SCH_QMAP [4].MAPPING_TBL[31:0]	32
0xBB02DD18	PON_SCH_QMAP [5].MAPPING_TBL[31:0]	32
0xBB02DD1C	PON_SCH_QMAP [6].MAPPING_TBL[31:0]	32
0xBB02DD20	PON_SCH_QMAP [7].MAPPING_TBL[31:0]	32
0xBB02DD24	PON_SCH_QMAP [8].MAPPING_TBL[31:0]	32
0xBB02DD28	PON_SCH_QMAP [9].MAPPING_TBL[31:0]	32
0xBB02DD2C	PON_SCH_QMAP [10].MAPPING_TBL[31:0]	32
0xBB02DD30	PON_SCH_QMAP [11].MAPPING_TBL[31:0]	32
0xBB02DD34	PON_SCH_QMAP [12].MAPPING_TBL[31:0]	32
0xBB02DD38	PON_SCH_QMAP [13].MAPPING_TBL[31:0]	32
0xBB02DD3C	PON_SCH_QMAP [14].MAPPING_TBL[31:0]	32
0xBB02DD40	PON_SCH_QMAP [15].MAPPING_TBL[31:0]	32
0xBB02DD44	PON_SCH_QMAP [16].MAPPING_TBL[31:0]	32
0xBB02DD48	PON_SCH_QMAP [17].MAPPING_TBL[31:0]	32
0xBB02DD4C	PON_SCH_QMAP [18].MAPPING_TBL[31:0]	32
0xBB02DD50	PON_SCH_QMAP [19].MAPPING_TBL[31:0]	32
0xBB02DD54	PON_SCH_QMAP [20].MAPPING_TBL[31:0]	32
0xBB02DD58	PON_SCH_QMAP [21].MAPPING_TBL[31:0]	32
0xBB02DD5C	PON_SCH_QMAP [22].MAPPING_TBL[31:0]	32
0xBB02DD60	PON_SCH_QMAP [23].MAPPING_TBL[31:0]	32
0xBB02DD64	PON_SCH_QMAP [24].MAPPING_TBL[31:0]	32



Address	Register	Len
0xBB02DD68	PON_SCH_QMAP [25].MAPPING_TBL[31:0]	32
0xBB02DD6C	PON_SCH_QMAP [26].MAPPING_TBL[31:0]	32
0xBB02DD70	PON_SCH_QMAP [27].MAPPING_TBL[31:0]	32
0xBB02DD74	PON_SCH_QMAP [28].MAPPING_TBL[31:0]	32
0xBB02DD78	PON_SCH_QMAP [29].MAPPING_TBL[31:0]	32
0xBB02DD7C	PON_SCH_QMAP [30].MAPPING_TBL[31:0]	32
0xBB02DD80	PON_SCH_QMAP [31].MAPPING_TBL[31:0]	32
0xBB02DD84	PON_WFQ_WEIGHT [0].WEIGHT[9:0]	10
0xBB02DD84	PON_WFQ_WEIGHT [1].WEIGHT[19:10]	10
0xBB02DD84	PON_WFQ_WEIGHT [2].WEIGHT[29:20]	10
0xBB02DD88	PON_WFQ_WEIGHT [3].WEIGHT[9:0]	10
0xBB02DD88	PON_WFQ_WEIGHT [4].WEIGHT[19:10]	10
0xBB02DD88	PON_WFQ_WEIGHT [5].WEIGHT[29:20]	10
0xBB02DD8C	PON_WFQ_WEIGHT [6].WEIGHT[9:0]	10
0xBB02DD8C	PON_WFQ_WEIGHT [7].WEIGHT[19:10]	10
0xBB02DD8C	PON_WFQ_WEIGHT [8].WEIGHT[29:20]	10
0xBB02DD90	PON_WFQ_WEIGHT [9].WEIGHT[9:0]	10
0xBB02DD90	PON_WFQ_WEIGHT [10].WEIGHT[19:10]	10
0xBB02DD90	PON_WFQ_WEIGHT [11].WEIGHT[29:20]	10
0xBB02DD94	PON_WFQ_WEIGHT [12].WEIGHT[9:0]	10
0xBB02DD94	PON_WFQ_WEIGHT [13].WEIGHT[19:10]	10
0xBB02DD94	PON_WFQ_WEIGHT [14].WEIGHT[29:20]	10
0xBB02DD98	PON_WFQ_WEIGHT [15].WEIGHT[9:0]	10
0xBB02DD98	PON_WFQ_WEIGHT [16].WEIGHT[19:10]	10
0xBB02DD98	PON_WFQ_WEIGHT [17].WEIGHT[29:20]	10
0xBB02DD9C	PON_WFQ_WEIGHT [18].WEIGHT[9:0]	10
0xBB02DD9C	PON_WFQ_WEIGHT [19].WEIGHT[19:10]	10
0xBB02DD9C	PON_WFQ_WEIGHT [20].WEIGHT[29:20]	10
0xBB02DDA0	PON_WFQ_WEIGHT [21].WEIGHT[9:0]	10
0xBB02DDA0	PON_WFQ_WEIGHT [22].WEIGHT[19:10]	10
0xBB02DDA0	PON_WFQ_WEIGHT [23].WEIGHT[29:20]	10
0xBB02DDA4	PON_WFQ_WEIGHT [24].WEIGHT[9:0]	10
0xBB02DDA4	PON_WFQ_WEIGHT [25].WEIGHT[19:10]	10
0xBB02DDA4	PON_WFQ_WEIGHT [26].WEIGHT[29:20]	10
0xBB02DDA8	PON_WFQ_WEIGHT [27].WEIGHT[9:0]	10
0xBB02DDA8	PON_WFQ_WEIGHT [28].WEIGHT[19:10]	10
0xBB02DDA8	PON_WFQ_WEIGHT [29].WEIGHT[29:20]	10
0xBB02DDAC	PON_WFQ_WEIGHT [30].WEIGHT[9:0]	10
0xBB02DDAC	PON_WFQ_WEIGHT [31].WEIGHT[19:10]	10
0xBB02DDAC	PON_WFQ_WEIGHT [32].WEIGHT[29:20]	10
0xBB02DDB0	PON_WFQ_WEIGHT [33].WEIGHT[9:0]	10
0xBB02DDB0	PON_WFQ_WEIGHT [34].WEIGHT[19:10]	10
0xBB02DDB0	PON_WFQ_WEIGHT [35].WEIGHT[29:20]	10
0xBB02DDB4	PON_WFQ_WEIGHT [36].WEIGHT[9:0]	10
0xBB02DDB4	PON_WFQ_WEIGHT [37].WEIGHT[19:10]	10
0xBB02DDB4	PON_WFQ_WEIGHT [38].WEIGHT[29:20]	10



Address	Register	Len
0xBB02DDB8	PON_WFQ_WEIGHT [39].WEIGHT[9:0]	10
0xBB02DDB8	PON_WFQ_WEIGHT [40].WEIGHT[19:10]	10
0xBB02DDB8	PON_WFQ_WEIGHT [41].WEIGHT[29:20]	10
0xBB02DDBC	PON_WFQ_WEIGHT [42].WEIGHT[9:0]	10
0xBB02DDBC	PON_WFQ_WEIGHT [43].WEIGHT[19:10]	10
0xBB02DDBC	PON_WFQ_WEIGHT [44].WEIGHT[29:20]	10
0xBB02DDC0	PON_WFQ_WEIGHT [45].WEIGHT[9:0]	10
0xBB02DDC0	PON_WFQ_WEIGHT [46].WEIGHT[19:10]	10
0xBB02DDC0	PON_WFQ_WEIGHT [47].WEIGHT[29:20]	10
0xBB02DDC4	PON_WFQ_WEIGHT [48].WEIGHT[9:0]	10
0xBB02DDC4	PON_WFQ_WEIGHT [49].WEIGHT[19:10]	10
0xBB02DDC4	PON_WFQ_WEIGHT [50].WEIGHT[29:20]	10
0xBB02DDC8	PON_WFQ_WEIGHT [51].WEIGHT[9:0]	10
0xBB02DDC8	PON_WFQ_WEIGHT [52].WEIGHT[19:10]	10
0xBB02DDC8	PON_WFQ_WEIGHT [53].WEIGHT[29:20]	10
0xBB02DDCC	PON_WFQ_WEIGHT [54].WEIGHT[9:0]	10
0xBB02DDCC	PON_WFQ_WEIGHT [55].WEIGHT[19:10]	10
0xBB02DDCC	PON_WFQ_WEIGHT [56].WEIGHT[29:20]	10
0xBB02DDD0	PON_WFQ_WEIGHT [57].WEIGHT[9:0]	10
0xBB02DDD0	PON_WFQ_WEIGHT [58].WEIGHT[19:10]	10
0xBB02DDD0	PON_WFQ_WEIGHT [59].WEIGHT[29:20]	10
0xBB02DDD4	PON_WFQ_WEIGHT [60].WEIGHT[9:0]	10
0xBB02DDD4	PON_WFQ_WEIGHT [61].WEIGHT[19:10]	10
0xBB02DDD4	PON_WFQ_WEIGHT [62].WEIGHT[29:20]	10
0xBB02DDD8	PON_WFQ_WEIGHT [63].WEIGHT[9:0]	10
0xBB02DDD8	PON_WFQ_WEIGHT [64].WEIGHT[19:10]	10
0xBB02DDD8	PON_WFQ_WEIGHT [65].WEIGHT[29:20]	10
0xBB02DDDC	PON_WFQ_WEIGHT [66].WEIGHT[9:0]	10
0xBB02DDDC	PON_WFQ_WEIGHT [67].WEIGHT[19:10]	10
0xBB02DDDC	PON_WFQ_WEIGHT [68].WEIGHT[29:20]	10
0xBB02DDE0	PON_WFQ_WEIGHT [69].WEIGHT[9:0]	10
0xBB02DDE0	PON_WFQ_WEIGHT [70].WEIGHT[19:10]	10
0xBB02DDE0	PON_WFQ_WEIGHT [71].WEIGHT[29:20]	10
0xBB02DDE4	PON_WFQ_WEIGHT [72].WEIGHT[9:0]	10
0xBB02DDE4	PON_WFQ_WEIGHT [73].WEIGHT[19:10]	10
0xBB02DDE4	PON_WFQ_WEIGHT [74].WEIGHT[29:20]	10
0xBB02DDE8	PON_WFQ_WEIGHT [75].WEIGHT[9:0]	10
0xBB02DDE8	PON_WFQ_WEIGHT [76].WEIGHT[19:10]	10
0xBB02DDE8	PON_WFQ_WEIGHT [77].WEIGHT[29:20]	10
0xBB02DDEC	PON_WFQ_WEIGHT [78].WEIGHT[9:0]	10
0xBB02DDEC	PON_WFQ_WEIGHT [79].WEIGHT[19:10]	10
0xBB02DDEC	PON_WFQ_WEIGHT [80].WEIGHT[29:20]	10
0xBB02DDF0	PON_WFQ_WEIGHT [81].WEIGHT[9:0]	10
0xBB02DDF0	PON_WFQ_WEIGHT [82].WEIGHT[19:10]	10
0xBB02DDF0	PON_WFQ_WEIGHT [83].WEIGHT[29:20]	10
0xBB02DDF4	PON_WFQ_WEIGHT [84].WEIGHT[9:0]	10

Address	Register	Len
0xBB02DDF4	PON_WFQ_WEIGHT [85].WEIGHT[19:10]	10
0xBB02DDF4	PON_WFQ_WEIGHT [86].WEIGHT[29:20]	10
0xBB02DDF8	PON_WFQ_WEIGHT [87].WEIGHT[9:0]	10
0xBB02DDF8	PON_WFQ_WEIGHT [88].WEIGHT[19:10]	10
0xBB02DDF8	PON_WFQ_WEIGHT [89].WEIGHT[29:20]	10
0xBB02DDFC	PON_WFQ_WEIGHT [90].WEIGHT[9:0]	10
0xBB02DDFC	PON_WFQ_WEIGHT [91].WEIGHT[19:10]	10
0xBB02DDFC	PON_WFQ_WEIGHT [92].WEIGHT[29:20]	10
0xBB02DE00	PON_WFQ_WEIGHT [93].WEIGHT[9:0]	10
0xBB02DE00	PON_WFQ_WEIGHT [94].WEIGHT[19:10]	10
0xBB02DE00	PON_WFQ_WEIGHT [95].WEIGHT[29:20]	10
0xBB02DE04	PON_WFQ_WEIGHT [96].WEIGHT[9:0]	10
0xBB02DE04	PON_WFQ_WEIGHT [97].WEIGHT[19:10]	10
0xBB02DE04	PON_WFQ_WEIGHT [98].WEIGHT[29:20]	10
0xBB02DE08	PON_WFQ_WEIGHT [99].WEIGHT[9:0]	10
0xBB02DE08	PON_WFQ_WEIGHT [100].WEIGHT[19:10]	10
0xBB02DE08	PON_WFQ_WEIGHT [101].WEIGHT[29:20]	10
0xBB02DE0C	PON_WFQ_WEIGHT [102].WEIGHT[9:0]	10
0xBB02DE0C	PON_WFQ_WEIGHT [103].WEIGHT[19:10]	10
0xBB02DE0C	PON_WFQ_WEIGHT [104].WEIGHT[29:20]	10
0xBB02DE10	PON_WFQ_WEIGHT [105].WEIGHT[9:0]	10
0xBB02DE10	PON_WFQ_WEIGHT [106].WEIGHT[19:10]	10
0xBB02DE10	PON_WFQ_WEIGHT [107].WEIGHT[29:20]	10
0xBB02DE14	PON_WFQ_WEIGHT [108].WEIGHT[9:0]	10
0xBB02DE14	PON_WFQ_WEIGHT [109].WEIGHT[19:10]	10
0xBB02DE14	PON_WFQ_WEIGHT [110].WEIGHT[29:20]	10
0xBB02DE18	PON_WFQ_WEIGHT [111].WEIGHT[9:0]	10
0xBB02DE18	PON_WFQ_WEIGHT [112].WEIGHT[19:10]	10
0xBB02DE18	PON_WFQ_WEIGHT [113].WEIGHT[29:20]	10
0xBB02DE1C	PON_WFQ_WEIGHT [114].WEIGHT[9:0]	10
0xBB02DE1C	PON_WFQ_WEIGHT [115].WEIGHT[19:10]	10
0xBB02DE1C	PON_WFQ_WEIGHT [116].WEIGHT[29:20]	10
0xBB02DE20	PON_WFQ_WEIGHT [117].WEIGHT[9:0]	10
0xBB02DE20	PON_WFQ_WEIGHT [118].WEIGHT[19:10]	10
0xBB02DE20	PON_WFQ_WEIGHT [119].WEIGHT[29:20]	10
0xBB02DE24	PON_WFQ_WEIGHT [120].WEIGHT[9:0]	10
0xBB02DE24	PON_WFQ_WEIGHT [121].WEIGHT[19:10]	10
0xBB02DE24	PON_WFQ_WEIGHT [122].WEIGHT[29:20]	10
0xBB02DE28	PON_WFQ_WEIGHT [123].WEIGHT[9:0]	10
0xBB02DE28	PON_WFQ_WEIGHT [124].WEIGHT[19:10]	10
0xBB02DE28	PON_WFQ_WEIGHT [125].WEIGHT[29:20]	10
0xBB02DE2C	PON_WFQ_WEIGHT [126].WEIGHT[9:0]	10
0xBB02DE2C	PON_WFQ_WEIGHT [127].WEIGHT[19:10]	10
0xBB02DE30	PON_WFQ_TYPE [0].QUEUE_TYPE[0:0]	1
0xBB02DE30	PON_WFQ_TYPE [1].QUEUE_TYPE[1:1]	1
0xBB02DE30	PON_WFQ_TYPE [2].QUEUE_TYPE[2:2]	1

Address	Register	Len
0xBB02DE30	PON_WFQ_TYPE [3].QUEUE_TYPE[3:3]	1
0xBB02DE30	PON_WFQ_TYPE [4].QUEUE_TYPE[4:4]	1
0xBB02DE30	PON_WFQ_TYPE [5].QUEUE_TYPE[5:5]	1
0xBB02DE30	PON_WFQ_TYPE [6].QUEUE_TYPE[6:6]	1
0xBB02DE30	PON_WFQ_TYPE [7].QUEUE_TYPE[7:7]	1
0xBB02DE30	PON_WFQ_TYPE [8].QUEUE_TYPE[8:8]	1
0xBB02DE30	PON_WFQ_TYPE [9].QUEUE_TYPE[9:9]	1
0xBB02DE30	PON_WFQ_TYPE [10].QUEUE_TYPE[10:10]	1
0xBB02DE30	PON_WFQ_TYPE [11].QUEUE_TYPE[11:11]	1
0xBB02DE30	PON_WFQ_TYPE [12].QUEUE_TYPE[12:12]	1
0xBB02DE30	PON_WFQ_TYPE [13].QUEUE_TYPE[13:13]	1
0xBB02DE30	PON_WFQ_TYPE [14].QUEUE_TYPE[14:14]	1
0xBB02DE30	PON_WFQ_TYPE [15].QUEUE_TYPE[15:15]	1
0xBB02DE30	PON_WFQ_TYPE [16].QUEUE_TYPE[16:16]	1
0xBB02DE30	PON_WFQ_TYPE [17].QUEUE_TYPE[17:17]	1
0xBB02DE30	PON_WFQ_TYPE [18].QUEUE_TYPE[18:18]	1
0xBB02DE30	PON_WFQ_TYPE [19].QUEUE_TYPE[19:19]	1
0xBB02DE30	PON_WFQ_TYPE [20].QUEUE_TYPE[20:20]	1
0xBB02DE30	PON_WFQ_TYPE [21].QUEUE_TYPE[21:21]	1
0xBB02DE30	PON_WFQ_TYPE [22].QUEUE_TYPE[22:22]	1
0xBB02DE30	PON_WFQ_TYPE [23].QUEUE_TYPE[23:23]	1
0xBB02DE30	PON_WFQ_TYPE [24].QUEUE_TYPE[24:24]	1
0xBB02DE30	PON_WFQ_TYPE [25].QUEUE_TYPE[25:25]	1
0xBB02DE30	PON_WFQ_TYPE [26].QUEUE_TYPE[26:26]	1
0xBB02DE30	PON_WFQ_TYPE [27].QUEUE_TYPE[27:27]	1
0xBB02DE30	PON_WFQ_TYPE [28].QUEUE_TYPE[28:28]	1
0xBB02DE30	PON_WFQ_TYPE [29].QUEUE_TYPE[29:29]	1
0xBB02DE30	PON_WFQ_TYPE [30].QUEUE_TYPE[30:30]	1
0xBB02DE30	PON_WFQ_TYPE [31].QUEUE_TYPE[31:31]	1
0xBB02DE34	PON_WFQ_TYPE [32].QUEUE_TYPE[0:0]	1
0xBB02DE34	PON_WFQ_TYPE [33].QUEUE_TYPE[1:1]	1
0xBB02DE34	PON_WFQ_TYPE [34].QUEUE_TYPE[2:2]	1
0xBB02DE34	PON_WFQ_TYPE [35].QUEUE_TYPE[3:3]	1
0xBB02DE34	PON_WFQ_TYPE [36].QUEUE_TYPE[4:4]	1
0xBB02DE34	PON_WFQ_TYPE [37].QUEUE_TYPE[5:5]	1
0xBB02DE34	PON_WFQ_TYPE [38].QUEUE_TYPE[6:6]	1
0xBB02DE34	PON_WFQ_TYPE [39].QUEUE_TYPE[7:7]	1
0xBB02DE34	PON_WFQ_TYPE [40].QUEUE_TYPE[8:8]	1
0xBB02DE34	PON_WFQ_TYPE [41].QUEUE_TYPE[9:9]	1
0xBB02DE34	PON_WFQ_TYPE [42].QUEUE_TYPE[10:10]	1
0xBB02DE34	PON_WFQ_TYPE [43].QUEUE_TYPE[11:11]	1
0xBB02DE34	PON_WFQ_TYPE [44].QUEUE_TYPE[12:12]	1
0xBB02DE34	PON_WFQ_TYPE [45].QUEUE_TYPE[13:13]	1
0xBB02DE34	PON_WFQ_TYPE [46].QUEUE_TYPE[14:14]	1
0xBB02DE34	PON_WFQ_TYPE [47].QUEUE_TYPE[15:15]	1
0xBB02DE34	PON_WFQ_TYPE [48].QUEUE_TYPE[16:16]	1

Address	Register	Len
0xBB02DE34	PON_WFQ_TYPE [49].QUEUE_TYPE[17:17]	1
0xBB02DE34	PON_WFQ_TYPE [50].QUEUE_TYPE[18:18]	1
0xBB02DE34	PON_WFQ_TYPE [51].QUEUE_TYPE[19:19]	1
0xBB02DE34	PON_WFQ_TYPE [52].QUEUE_TYPE[20:20]	1
0xBB02DE34	PON_WFQ_TYPE [53].QUEUE_TYPE[21:21]	1
0xBB02DE34	PON_WFQ_TYPE [54].QUEUE_TYPE[22:22]	1
0xBB02DE34	PON_WFQ_TYPE [55].QUEUE_TYPE[23:23]	1
0xBB02DE34	PON_WFQ_TYPE [56].QUEUE_TYPE[24:24]	1
0xBB02DE34	PON_WFQ_TYPE [57].QUEUE_TYPE[25:25]	1
0xBB02DE34	PON_WFQ_TYPE [58].QUEUE_TYPE[26:26]	1
0xBB02DE34	PON_WFQ_TYPE [59].QUEUE_TYPE[27:27]	1
0xBB02DE34	PON_WFQ_TYPE [60].QUEUE_TYPE[28:28]	1
0xBB02DE34	PON_WFQ_TYPE [61].QUEUE_TYPE[29:29]	1
0xBB02DE34	PON_WFQ_TYPE [62].QUEUE_TYPE[30:30]	1
0xBB02DE34	PON_WFQ_TYPE [63].QUEUE_TYPE[31:31]	1
0xBB02DE38	PON_WFQ_TYPE [64].QUEUE_TYPE[0:0]	1
0xBB02DE38	PON_WFQ_TYPE [65].QUEUE_TYPE[1:1]	1
0xBB02DE38	PON_WFQ_TYPE [66].QUEUE_TYPE[2:2]	1
0xBB02DE38	PON_WFQ_TYPE [67].QUEUE_TYPE[3:3]	1
0xBB02DE38	PON_WFQ_TYPE [68].QUEUE_TYPE[4:4]	1
0xBB02DE38	PON_WFQ_TYPE [69].QUEUE_TYPE[5:5]	1
0xBB02DE38	PON_WFQ_TYPE [70].QUEUE_TYPE[6:6]	1
0xBB02DE38	PON_WFQ_TYPE [71].QUEUE_TYPE[7:7]	1
0xBB02DE38	PON_WFQ_TYPE [72].QUEUE_TYPE[8:8]	1
0xBB02DE38	PON_WFQ_TYPE [73].QUEUE_TYPE[9:9]	1
0xBB02DE38	PON_WFQ_TYPE [74].QUEUE_TYPE[10:10]	1
0xBB02DE38	PON_WFQ_TYPE [75].QUEUE_TYPE[11:11]	1
0xBB02DE38	PON_WFQ_TYPE [76].QUEUE_TYPE[12:12]	1
0xBB02DE38	PON_WFQ_TYPE [77].QUEUE_TYPE[13:13]	1
0xBB02DE38	PON_WFQ_TYPE [78].QUEUE_TYPE[14:14]	1
0xBB02DE38	PON_WFQ_TYPE [79].QUEUE_TYPE[15:15]	1
0xBB02DE38	PON_WFQ_TYPE [80].QUEUE_TYPE[16:16]	1
0xBB02DE38	PON_WFQ_TYPE [81].QUEUE_TYPE[17:17]	1
0xBB02DE38	PON_WFQ_TYPE [82].QUEUE_TYPE[18:18]	1
0xBB02DE38	PON_WFQ_TYPE [83].QUEUE_TYPE[19:19]	1
0xBB02DE38	PON_WFQ_TYPE [84].QUEUE_TYPE[20:20]	1
0xBB02DE38	PON_WFQ_TYPE [85].QUEUE_TYPE[21:21]	1
0xBB02DE38	PON_WFQ_TYPE [86].QUEUE_TYPE[22:22]	1
0xBB02DE38	PON_WFQ_TYPE [87].QUEUE_TYPE[23:23]	1
0xBB02DE38	PON_WFQ_TYPE [88].QUEUE_TYPE[24:24]	1
0xBB02DE38	PON_WFQ_TYPE [89].QUEUE_TYPE[25:25]	1
0xBB02DE38	PON_WFQ_TYPE [90].QUEUE_TYPE[26:26]	1
0xBB02DE38	PON_WFQ_TYPE [91].QUEUE_TYPE[27:27]	1
0xBB02DE38	PON_WFQ_TYPE [92].QUEUE_TYPE[28:28]	1
0xBB02DE38	PON_WFQ_TYPE [93].QUEUE_TYPE[29:29]	1
0xBB02DE38	PON_WFQ_TYPE [94].QUEUE_TYPE[30:30]	1

Address	Register	Len
0xBB02DE38	PON_WFQ_TYPE [95].QUEUE_TYPE[31:31]	1
0xBB02DE3C	PON_WFQ_TYPE [96].QUEUE_TYPE[0:0]	1
0xBB02DE3C	PON_WFQ_TYPE [97].QUEUE_TYPE[1:1]	1
0xBB02DE3C	PON_WFQ_TYPE [98].QUEUE_TYPE[2:2]	1
0xBB02DE3C	PON_WFQ_TYPE [99].QUEUE_TYPE[3:3]	1
0xBB02DE3C	PON_WFQ_TYPE [100].QUEUE_TYPE[4:4]	1
0xBB02DE3C	PON_WFQ_TYPE [101].QUEUE_TYPE[5:5]	1
0xBB02DE3C	PON_WFQ_TYPE [102].QUEUE_TYPE[6:6]	1
0xBB02DE3C	PON_WFQ_TYPE [103].QUEUE_TYPE[7:7]	1
0xBB02DE3C	PON_WFQ_TYPE [104].QUEUE_TYPE[8:8]	1
0xBB02DE3C	PON_WFQ_TYPE [105].QUEUE_TYPE[9:9]	1
0xBB02DE3C	PON_WFQ_TYPE [106].QUEUE_TYPE[10:10]	1
0xBB02DE3C	PON_WFQ_TYPE [107].QUEUE_TYPE[11:11]	1
0xBB02DE3C	PON_WFQ_TYPE [108].QUEUE_TYPE[12:12]	1
0xBB02DE3C	PON_WFQ_TYPE [109].QUEUE_TYPE[13:13]	1
0xBB02DE3C	PON_WFQ_TYPE [110].QUEUE_TYPE[14:14]	1
0xBB02DE3C	PON_WFQ_TYPE [111].QUEUE_TYPE[15:15]	1
0xBB02DE3C	PON_WFQ_TYPE [112].QUEUE_TYPE[16:16]	1
0xBB02DE3C	PON_WFQ_TYPE [113].QUEUE_TYPE[17:17]	1
0xBB02DE3C	PON_WFQ_TYPE [114].QUEUE_TYPE[18:18]	1
0xBB02DE3C	PON_WFQ_TYPE [115].QUEUE_TYPE[19:19]	1
0xBB02DE3C	PON_WFQ_TYPE [116].QUEUE_TYPE[20:20]	1
0xBB02DE3C	PON_WFQ_TYPE [117].QUEUE_TYPE[21:21]	1
0xBB02DE3C	PON_WFQ_TYPE [118].QUEUE_TYPE[22:22]	1
0xBB02DE3C	PON_WFQ_TYPE [119].QUEUE_TYPE[23:23]	1
0xBB02DE3C	PON_WFQ_TYPE [120].QUEUE_TYPE[24:24]	1
0xBB02DE3C	PON_WFQ_TYPE [121].QUEUE_TYPE[25:25]	1
0xBB02DE3C	PON_WFQ_TYPE [122].QUEUE_TYPE[26:26]	1
0xBB02DE3C	PON_WFQ_TYPE [123].QUEUE_TYPE[27:27]	1
0xBB02DE3C	PON_WFQ_TYPE [124].QUEUE_TYPE[28:28]	1
0xBB02DE3C	PON_WFQ_TYPE [125].QUEUE_TYPE[29:29]	1
0xBB02DE3C	PON_WFQ_TYPE [126].QUEUE_TYPE[30:30]	1
0xBB02DE3C	PON_WFQ_TYPE [127].QUEUE_TYPE[31:31]	1
0xBB02DE40	PON_TCONT_EN [0].TCONT_EN[0:0]	1
0xBB02DE40	PON_TCONT_EN [1].TCONT_EN[1:1]	1
0xBB02DE40	PON_TCONT_EN [2].TCONT_EN[2:2]	1
0xBB02DE40	PON_TCONT_EN [3].TCONT_EN[3:3]	1
0xBB02DE40	PON_TCONT_EN [4].TCONT_EN[4:4]	1
0xBB02DE40	PON_TCONT_EN [5].TCONT_EN[5:5]	1
0xBB02DE40	PON_TCONT_EN [6].TCONT_EN[6:6]	1
0xBB02DE40	PON_TCONT_EN [7].TCONT_EN[7:7]	1
0xBB02DE40	PON_TCONT_EN [8].TCONT_EN[8:8]	1
0xBB02DE40	PON_TCONT_EN [9].TCONT_EN[9:9]	1
0xBB02DE40	PON_TCONT_EN [10].TCONT_EN[10:10]	1
0xBB02DE40	PON_TCONT_EN [11].TCONT_EN[11:11]	1
0xBB02DE40	PON_TCONT_EN [12].TCONT_EN[12:12]	1

Address	Register	Len
0xBB02DE40	PON_TCONT_EN [13].TCONT_EN[13:13]	1
0xBB02DE40	PON_TCONT_EN [14].TCONT_EN[14:14]	1
0xBB02DE40	PON_TCONT_EN [15].TCONT_EN[15:15]	1
0xBB02DE40	PON_TCONT_EN [16].TCONT_EN[16:16]	1
0xBB02DE40	PON_TCONT_EN [17].TCONT_EN[17:17]	1
0xBB02DE40	PON_TCONT_EN [18].TCONT_EN[18:18]	1
0xBB02DE40	PON_TCONT_EN [19].TCONT_EN[19:19]	1
0xBB02DE40	PON_TCONT_EN [20].TCONT_EN[20:20]	1
0xBB02DE40	PON_TCONT_EN [21].TCONT_EN[21:21]	1
0xBB02DE40	PON_TCONT_EN [22].TCONT_EN[22:22]	1
0xBB02DE40	PON_TCONT_EN [23].TCONT_EN[23:23]	1
0xBB02DE40	PON_TCONT_EN [24].TCONT_EN[24:24]	1
0xBB02DE40	PON_TCONT_EN [25].TCONT_EN[25:25]	1
0xBB02DE40	PON_TCONT_EN [26].TCONT_EN[26:26]	1
0xBB02DE40	PON_TCONT_EN [27].TCONT_EN[27:27]	1
0xBB02DE40	PON_TCONT_EN [28].TCONT_EN[28:28]	1
0xBB02DE40	PON_TCONT_EN [29].TCONT_EN[29:29]	1
0xBB02DE40	PON_TCONT_EN [30].TCONT_EN[30:30]	1
0xBB02DE40	PON_TCONT_EN [31].TCONT_EN[31:31]	1
0xBB02DE44	PON_OLT_BW_MTR_FULL.RESERVED[31:18]	14
0xBB02DE44	PON_OLT_BW_MTR_FULL.OLT_BW_MTR_FULL[17:0]	18
0xBB02DE48	PON_WFQ_IFG_CTRL.RESERVED[31:1]	31
0xBB02DE48	PON_WFQ_IFG_CTRL.PON_WFQ_IFG[0:0]	1
0xBB02DE4C	RGF_VER_EGR_SCH.REGFILE_VER[31:0]	32
0xBB02DE50	RSVD_EGR_SCH [0].RSVD_MEM[31:0]	32
0xBB02DE54	RSVD_EGR_SCH [1].RSVD_MEM[31:0]	32
0xBB02DE58	RSVD_EGR_SCH [2].RSVD_MEM[31:0]	32
0xBB02DE5C	RSVD_EGR_SCH [3].RSVD_MEM[31:0]	32
0xBB02DE60	RSVD_EGR_SCH [4].RSVD_MEM[31:0]	32
0xBB02DE64	RSVD_EGR_SCH [5].RSVD_MEM[31:0]	32
0xBB02DE68	RSVD_EGR_SCH [6].RSVD_MEM[31:0]	32
0xBB02DE6C	RSVD_EGR_SCH [7].RSVD_MEM[31:0]	32
0xBB02DE70	RSVD_EGR_SCH [8].RSVD_MEM[31:0]	32
0xBB02DE74	RSVD_EGR_SCH [9].RSVD_MEM[31:0]	32
0xBB02DE78	RSVD_EGR_SCH [10].RSVD_MEM[31:0]	32
0xBB02DE7C	RSVD_EGR_SCH [11].RSVD_MEM[31:0]	32
0xBB02DE80	RSVD_EGR_SCH [12].RSVD_MEM[31:0]	32
0xBB02DE84	RSVD_EGR_SCH [13].RSVD_MEM[31:0]	32
0xBB02DE88	RSVD_EGR_SCH [14].RSVD_MEM[31:0]	32
0xBB02DE8C	RSVD_EGR_SCH [15].RSVD_MEM[31:0]	32
0xBB02DE90	BYTE_TOKEN_METER.RESERVED[31:8]	24
0xBB02DE90	BYTE_TOKEN_METER.BYTES_PERTKN_BWMTR[7:0]	8
0xBB031000	BIST_CFG19.STS_BIST_DONE[31:0]	32
0xBB031004	BIST_CFG18.COND0_BISR_OUT_0[31:0]	32
0xBB031008	BIST_CFG17.COND0_BISR_OUT_1[31:0]	32
0xBB03100C	BIST_CFG16.RESERVED[31:6]	26

Address	Register	Len
0xBB03100C	BIST_CFG16.COND0_BISR_OUT_2[5:0]	6
0xBB031010	BIST_CFG15.COND1_BISR_OUT_0[31:0]	32
0xBB031014	BIST_CFG14.COND1_BISR_OUT_1[31:0]	32
0xBB031018	BIST_CFG13.STS_DRF_START_PAUSE[31:0]	32
0xBB03101C	BIST_CFG12.RESERVED[31:8]	24
0xBB03101C	BIST_CFG12.STS_BIST_NOFAIL[7:7]	1
0xBB03101C	BIST_CFG12.COND1_BISR_OUT_2[6:1]	6
0xBB03101C	BIST_CFG12.STS_DRF_BIST_NOFAIL[0:0]	1
0xBB031020	BIST_CFG9.STS_DRF_BIST_FAIL_1[31:0]	32
0xBB031024	BIST_CFG8.STS_DRF_BIST_FAIL_0[31:0]	32
0xBB031028	BIST_CFG7.STS_DRF_BIST_DONE[31:0]	32
0xBB03102C	BIST_CFG4.STS_BIST_FAIL_1[31:0]	32
0xBB031030	BIST_CFG3.STS_BIST_FAIL_0[31:0]	32
0xBB031034	BIST_CFG2.RESERVED[31:14]	18
0xBB031034	BIST_CFG2.DRF_TCAMSEL[13:13]	1
0xBB031034	BIST_CFG2.STS_BISR_REPAIRED[12:10]	3
0xBB031034	BIST_CFG2.COND1_DRF_BIST_NOFAIL[9:9]	1
0xBB031034	BIST_CFG2.COND0_DRF_BIST_NOFAIL[8:8]	1
0xBB031034	BIST_CFG2.COND1_BIST_NOFAIL[7:7]	1
0xBB031034	BIST_CFG2.COND0_BIST_NOFAIL[6:6]	1
0xBB031034	BIST_CFG2.COND1_BISR_REPAIRED[5:3]	3
0xBB031034	BIST_CFG2.COND0_BISR_REPAIRED[2:0]	3
0xBB031038	BIST_CFG1.CFG_DRF_BIST_MODE[31:0]	32
0xBB03103C	BIST_CFG0.CFG_BIST_MODE[31:0]	32
0xBB031040	DIAG_MODE.RESERVED[31:6]	26
0xBB031040	DIAG_MODE.DIAGNOSIS_MODE[5:0]	6
0xBB031044	DFR_TEST_RESUME.RESERVED[31:1]	31
0xBB031044	DFR_TEST_RESUME.DRF_TEST_RESUME[0:0]	1
0xBB031048	RGF_VER_BIST_CTRL.REGFILE_VER[31:0]	32
0xBB03104C	RSVD_BIST_CTRL [0].RSVD_MEM[31:0]	32
0xBB031050	RSVD_BIST_CTRL [1].RSVD_MEM[31:0]	32
0xBB031054	RSVD_BIST_CTRL [2].RSVD_MEM[31:0]	32
0xBB031058	RSVD_BIST_CTRL [3].RSVD_MEM[31:0]	32
0xBB03105C	RSVD_BIST_CTRL [4].RSVD_MEM[31:0]	32
0xBB031060	RSVD_BIST_CTRL [5].RSVD_MEM[31:0]	32
0xBB031064	RSVD_BIST_CTRL [6].RSVD_MEM[31:0]	32
0xBB031068	RSVD_BIST_CTRL [7].RSVD_MEM[31:0]	32
0xBB03106C	RSVD_BIST_CTRL [8].RSVD_MEM[31:0]	32
0xBB031070	RSVD_BIST_CTRL [9].RSVD_MEM[31:0]	32
0xBB031074	RSVD_BIST_CTRL [10].RSVD_MEM[31:0]	32
0xBB031078	RSVD_BIST_CTRL [11].RSVD_MEM[31:0]	32
0xBB03107C	RSVD_BIST_CTRL [12].RSVD_MEM[31:0]	32
0xBB031080	RSVD_BIST_CTRL [13].RSVD_MEM[31:0]	32
0xBB031084	RSVD_BIST_CTRL [14].RSVD_MEM[31:0]	32
0xBB031088	RSVD_BIST_CTRL [15].RSVD_MEM[31:0]	32
0xBB032000	STAT_PORT_TX_MIB [0].tx_etherStatsMulticastPkts[31:0]	32



Address	Register	Len
0xBB032004	STAT_PORT_TX_MIB [0].tx_etherStatsBroadcastPkts[31:0]	32
0xBB032008	STAT_PORT_TX_MIB [0].tx_etherStatsUndersizePkts[31:0]	32
0xBB03200C	STAT_PORT_TX_MIB [0].tx_etherStatsOversizePkts[31:0]	32
0xBB032010	STAT_PORT_TX_MIB [0].tx_etherStatsPkts64Octets[31:0]	32
0xBB032014	STAT_PORT_TX_MIB [0].tx_etherStatsPkts65to127Octets[31:0]	32
0xBB032018	STAT_PORT_TX_MIB [0].tx_etherStatsPkts128to255Octets[31:0]	32
0xBB03201C	STAT_PORT_TX_MIB [0].tx_etherStatsPkts256to511Octets[31:0]	32
0xBB032020	STAT_PORT_TX_MIB [0].tx_etherStatsPkts512to1023Octets[31:0]	32
0xBB032024	STAT_PORT_TX_MIB [0].tx_etherStatsPkts1024to1518Octets[31:0]	32
0xBB032028	STAT_PORT_TX_MIB [0].ifOutOctets_L[31:0]	32
0xBB03202C	STAT_PORT_TX_MIB [0].ifOutOctets_H[31:0]	32
0xBB032030	STAT_PORT_TX_MIB [0].dot3StatsSingleCollisionFrames[31:0]	32
0xBB032034	STAT_PORT_TX_MIB [0].dot3StatsMultipleCollisionFrames[31:0]	32
0xBB032038	STAT_PORT_TX_MIB [0].dot3StatsDeferredTransmissions[31:0]	32
0xBB03203C	STAT_PORT_TX_MIB [0].dot3StatsLateCollisions[31:0]	32
0xBB032040	STAT_PORT_TX_MIB [0].etherStatsCollisions[31:0]	32
0xBB032044	STAT_PORT_TX_MIB [0].dot3StatsExcessiveCollisions[31:0]	32
0xBB032048	STAT_PORT_TX_MIB [0].dot3OutPauseFrames[31:0]	32
0xBB03204C	STAT_PORT_TX_MIB [0].ifOutDiscards[31:0]	32
0xBB032050	STAT_PORT_TX_MIB [0].tx_etherStatsPkts1519toMaxOctets[31:0]	32
0xBB032054	STAT_PORT_TX_MIB [0].RESERVED[31:0]	32
0xBB032058	STAT_PORT_TX_MIB [0].dot1dTpPortInDiscards[31:0]	32
0xBB03205C	STAT_PORT_TX_MIB [0].ifOutUcastPkts[31:0]	32
0xBB032060	STAT_PORT_TX_MIB [0].ifOutMulticastPkts[31:0]	32
0xBB032064	STAT_PORT_TX_MIB [0].ifOutBroadcastPkts[31:0]	32
0xBB032068	STAT_PORT_TX_MIB [0].RESERVED[31:0]	32
0xBB03206C	STAT_PORT_TX_MIB [0].RESERVED[31:0]	32
0xBB032070	STAT_PORT_TX_MIB [0].RESERVED[31:0]	32
0xBB032074	STAT_PORT_TX_MIB [0].RESERVED[31:0]	32
0xBB032078	STAT_PORT_TX_MIB [0].RESERVED[31:0]	32
0xBB03207C	STAT_PORT_TX_MIB [0].RESERVED[31:0]	32
0xBB032080	STAT_PORT_TX_MIB [1].tx_etherStatsMulticastPkts[31:0]	32
0xBB032084	STAT_PORT_TX_MIB [1].tx_etherStatsBroadcastPkts[31:0]	32
0xBB032088	STAT_PORT_TX_MIB [1].tx_etherStatsUndersizePkts[31:0]	32
0xBB03208C	STAT_PORT_TX_MIB [1].tx_etherStatsOversizePkts[31:0]	32
0xBB032090	STAT_PORT_TX_MIB [1].tx_etherStatsPkts64Octets[31:0]	32
0xBB032094	STAT_PORT_TX_MIB [1].tx_etherStatsPkts65to127Octets[31:0]	32
0xBB032098	STAT_PORT_TX_MIB [1].tx_etherStatsPkts128to255Octets[31:0]	32
0xBB03209C	STAT_PORT_TX_MIB [1].tx_etherStatsPkts256to511Octets[31:0]	32
0xBB0320A0	STAT_PORT_TX_MIB [1].tx_etherStatsPkts512to1023Octets[31:0]	32
0xBB0320A4	STAT_PORT_TX_MIB [1].tx_etherStatsPkts1024to1518Octets[31:0]	32
0xBB0320A8	STAT_PORT_TX_MIB [1].ifOutOctets_L[31:0]	32
0xBB0320AC	STAT_PORT_TX_MIB [1].ifOutOctets_H[31:0]	32
0xBB0320B0	STAT_PORT_TX_MIB [1].dot3StatsSingleCollisionFrames[31:0]	32
0xBB0320B4	STAT_PORT_TX_MIB [1].dot3StatsMultipleCollisionFrames[31:0]	32
0xBB0320B8	STAT_PORT_TX_MIB [1].dot3StatsDeferredTransmissions[31:0]	32



Address	Register	Len
0xBB0320BC	STAT_PORT_TX_MIB [1].dot3StatsLateCollisions[31:0]	32
0xBB0320C0	STAT_PORT_TX_MIB [1].etherStatsCollisions[31:0]	32
0xBB0320C4	STAT_PORT_TX_MIB [1].dot3StatsExcessiveCollisions[31:0]	32
0xBB0320C8	STAT_PORT_TX_MIB [1].dot3OutPauseFrames[31:0]	32
0xBB0320CC	STAT_PORT_TX_MIB [1].ifOutDiscards[31:0]	32
0xBB0320D0	STAT_PORT_TX_MIB [1].tx_etherStatsPkts1519toMaxOctets[31:0]	32
0xBB0320D4	STAT_PORT_TX_MIB [1].RESERVED[31:0]	32
0xBB0320D8	STAT_PORT_TX_MIB [1].dot1dTpPortInDiscards[31:0]	32
0xBB0320DC	STAT_PORT_TX_MIB [1].ifOutUcastPkts[31:0]	32
0xBB0320E0	STAT_PORT_TX_MIB [1].ifOutMulticastPkts[31:0]	32
0xBB0320E4	STAT_PORT_TX_MIB [1].ifOutBroadcastPkts[31:0]	32
0xBB0320E8	STAT_PORT_TX_MIB [1].RESERVED[31:0]	32
0xBB0320EC	STAT_PORT_TX_MIB [1].RESERVED[31:0]	32
0xBB0320F0	STAT_PORT_TX_MIB [1].RESERVED[31:0]	32
0xBB0320F4	STAT_PORT_TX_MIB [1].RESERVED[31:0]	32
0xBB0320F8	STAT_PORT_TX_MIB [1].RESERVED[31:0]	32
0xBB0320FC	STAT_PORT_TX_MIB [1].RESERVED[31:0]	32
0xBB032100	STAT_PORT_TX_MIB [2].tx_etherStatsMulticastPkts[31:0]	32
0xBB032104	STAT_PORT_TX_MIB [2].tx_etherStatsBroadcastPkts[31:0]	32
0xBB032108	STAT_PORT_TX_MIB [2].tx_etherStatsUndersizePkts[31:0]	32
0xBB03210C	STAT_PORT_TX_MIB [2].tx_etherStatsOversizePkts[31:0]	32
0xBB032110	STAT_PORT_TX_MIB [2].tx_etherStatsPkts64Octets[31:0]	32
0xBB032114	STAT_PORT_TX_MIB [2].tx_etherStatsPkts65to127Octets[31:0]	32
0xBB032118	STAT_PORT_TX_MIB [2].tx_etherStatsPkts128to255Octets[31:0]	32
0xBB03211C	STAT_PORT_TX_MIB [2].tx_etherStatsPkts256to511Octets[31:0]	32
0xBB032120	STAT_PORT_TX_MIB [2].tx_etherStatsPkts512to1023Octets[31:0]	32
0xBB032124	STAT_PORT_TX_MIB [2].tx_etherStatsPkts1024to1518Octets[31:0]	32
0xBB032128	STAT_PORT_TX_MIB [2].ifOutOctets_L[31:0]	32
0xBB03212C	STAT_PORT_TX_MIB [2].ifOutOctets_H[31:0]	32
0xBB032130	STAT_PORT_TX_MIB [2].dot3StatsSingleCollisionFrames[31:0]	32
0xBB032134	STAT_PORT_TX_MIB [2].dot3StatsMultipleCollisionFrames[31:0]	32
0xBB032138	STAT_PORT_TX_MIB [2].dot3StatsDeferredTransmissions[31:0]	32
0xBB03213C	STAT_PORT_TX_MIB [2].dot3StatsLateCollisions[31:0]	32
0xBB032140	STAT_PORT_TX_MIB [2].etherStatsCollisions[31:0]	32
0xBB032144	STAT_PORT_TX_MIB [2].dot3StatsExcessiveCollisions[31:0]	32
0xBB032148	STAT_PORT_TX_MIB [2].dot3OutPauseFrames[31:0]	32
0xBB03214C	STAT_PORT_TX_MIB [2].ifOutDiscards[31:0]	32
0xBB032150	STAT_PORT_TX_MIB [2].tx_etherStatsPkts1519toMaxOctets[31:0]	32
0xBB032154	STAT_PORT_TX_MIB [2].RESERVED[31:0]	32
0xBB032158	STAT_PORT_TX_MIB [2].dot1dTpPortInDiscards[31:0]	32
0xBB03215C	STAT_PORT_TX_MIB [2].ifOutUcastPkts[31:0]	32
0xBB032160	STAT_PORT_TX_MIB [2].ifOutMulticastPkts[31:0]	32
0xBB032164	STAT_PORT_TX_MIB [2].ifOutBroadcastPkts[31:0]	32
0xBB032168	STAT_PORT_TX_MIB [2].RESERVED[31:0]	32
0xBB03216C	STAT_PORT_TX_MIB [2].RESERVED[31:0]	32
0xBB032170	STAT_PORT_TX_MIB [2].RESERVED[31:0]	32

Address	Register	Len
0xBB032174	STAT_PORT_TX_MIB [2].RESERVED[31:0]	32
0xBB032178	STAT_PORT_TX_MIB [2].RESERVED[31:0]	32
0xBB03217C	STAT_PORT_TX_MIB [2].RESERVED[31:0]	32
0xBB032180	STAT_PORT_TX_MIB [3].tx_etherStatsMulticastPkts[31:0]	32
0xBB032184	STAT_PORT_TX_MIB [3].tx_etherStatsBroadcastPkts[31:0]	32
0xBB032188	STAT_PORT_TX_MIB [3].tx_etherStatsUndersizePkts[31:0]	32
0xBB03218C	STAT_PORT_TX_MIB [3].tx_etherStatsOversizePkts[31:0]	32
0xBB032190	STAT_PORT_TX_MIB [3].tx_etherStatsPkts64Octets[31:0]	32
0xBB032194	STAT_PORT_TX_MIB [3].tx_etherStatsPkts65to127Octets[31:0]	32
0xBB032198	STAT_PORT_TX_MIB [3].tx_etherStatsPkts128to255Octets[31:0]	32
0xBB03219C	STAT_PORT_TX_MIB [3].tx_etherStatsPkts256to511Octets[31:0]	32
0xBB0321A0	STAT_PORT_TX_MIB [3].tx_etherStatsPkts512to1023Octets[31:0]	32
0xBB0321A4	STAT_PORT_TX_MIB [3].tx_etherStatsPkts1024to1518Octets[31:0]	32
0xBB0321A8	STAT_PORT_TX_MIB [3].ifOutOctets_L[31:0]	32
0xBB0321AC	STAT_PORT_TX_MIB [3].ifOutOctets_H[31:0]	32
0xBB0321B0	STAT_PORT_TX_MIB [3].dot3StatsSingleCollisionFrames[31:0]	32
0xBB0321B4	STAT_PORT_TX_MIB [3].dot3StatsMultipleCollisionFrames[31:0]	32
0xBB0321B8	STAT_PORT_TX_MIB [3].dot3StatsDeferredTransmissions[31:0]	32
0xBB0321BC	STAT_PORT_TX_MIB [3].dot3StatsLateCollisions[31:0]	32
0xBB0321C0	STAT_PORT_TX_MIB [3].etherStatsCollisions[31:0]	32
0xBB0321C4	STAT_PORT_TX_MIB [3].dot3StatsExcessiveCollisions[31:0]	32
0xBB0321C8	STAT_PORT_TX_MIB [3].dot3OutPauseFrames[31:0]	32
0xBB0321CC	STAT_PORT_TX_MIB [3].ifOutDiscards[31:0]	32
0xBB0321D0	STAT_PORT_TX_MIB [3].tx_etherStatsPkts1519toMaxOctets[31:0]	32
0xBB0321D4	STAT_PORT_TX_MIB [3].RESERVED[31:0]	32
0xBB0321D8	STAT_PORT_TX_MIB [3].dot1dTpPortInDiscards[31:0]	32
0xBB0321DC	STAT_PORT_TX_MIB [3].ifOutUcastPkts[31:0]	32
0xBB0321E0	STAT_PORT_TX_MIB [3].ifOutMulticastPkts[31:0]	32
0xBB0321E4	STAT_PORT_TX_MIB [3].ifOutBroadcastPkts[31:0]	32
0xBB0321E8	STAT_PORT_TX_MIB [3].RESERVED[31:0]	32
0xBB0321EC	STAT_PORT_TX_MIB [3].RESERVED[31:0]	32
0xBB0321F0	STAT_PORT_TX_MIB [3].RESERVED[31:0]	32
0xBB0321F4	STAT_PORT_TX_MIB [3].RESERVED[31:0]	32
0xBB0321F8	STAT_PORT_TX_MIB [3].RESERVED[31:0]	32
0xBB0321FC	STAT_PORT_TX_MIB [3].RESERVED[31:0]	32
0xBB032200	STAT_PORT_TX_MIB [4].tx_etherStatsMulticastPkts[31:0]	32
0xBB032204	STAT_PORT_TX_MIB [4].tx_etherStatsBroadcastPkts[31:0]	32
0xBB032208	STAT_PORT_TX_MIB [4].tx_etherStatsUndersizePkts[31:0]	32
0xBB03220C	STAT_PORT_TX_MIB [4].tx_etherStatsOversizePkts[31:0]	32
0xBB032210	STAT_PORT_TX_MIB [4].tx_etherStatsPkts64Octets[31:0]	32
0xBB032214	STAT_PORT_TX_MIB [4].tx_etherStatsPkts65to127Octets[31:0]	32
0xBB032218	STAT_PORT_TX_MIB [4].tx_etherStatsPkts128to255Octets[31:0]	32
0xBB03221C	STAT_PORT_TX_MIB [4].tx_etherStatsPkts256to511Octets[31:0]	32
0xBB032220	STAT_PORT_TX_MIB [4].tx_etherStatsPkts512to1023Octets[31:0]	32
0xBB032224	STAT_PORT_TX_MIB [4].tx_etherStatsPkts1024to1518Octets[31:0]	32
0xBB032228	STAT_PORT_TX_MIB [4].ifOutOctets_L[31:0]	32

Address	Register	Len
0xBB03222C	STAT_PORT_TX_MIB [4].ifOutOctets_H[31:0]	32
0xBB032230	STAT_PORT_TX_MIB [4].dot3StatsSingleCollisionFrames[31:0]	32
0xBB032234	STAT_PORT_TX_MIB [4].dot3StatsMultipleCollisionFrames[31:0]	32
0xBB032238	STAT_PORT_TX_MIB [4].dot3StatsDeferredTransmissions[31:0]	32
0xBB03223C	STAT_PORT_TX_MIB [4].dot3StatsLateCollisions[31:0]	32
0xBB032240	STAT_PORT_TX_MIB [4].etherStatsCollisions[31:0]	32
0xBB032244	STAT_PORT_TX_MIB [4].dot3StatsExcessiveCollisions[31:0]	32
0xBB032248	STAT_PORT_TX_MIB [4].dot3OutPauseFrames[31:0]	32
0xBB03224C	STAT_PORT_TX_MIB [4].ifOutDiscards[31:0]	32
0xBB032250	STAT_PORT_TX_MIB [4].tx_etherStatsPkts1519toMaxOctets[31:0]	32
0xBB032254	STAT_PORT_TX_MIB [4].RESERVED[31:0]	32
0xBB032258	STAT_PORT_TX_MIB [4].dot1dTpPortInDiscards[31:0]	32
0xBB03225C	STAT_PORT_TX_MIB [4].ifOutUcastPkts[31:0]	32
0xBB032260	STAT_PORT_TX_MIB [4].ifOutMulticastPkts[31:0]	32
0xBB032264	STAT_PORT_TX_MIB [4].ifOutBroadcastPkts[31:0]	32
0xBB032268	STAT_PORT_TX_MIB [4].RESERVED[31:0]	32
0xBB03226C	STAT_PORT_TX_MIB [4].RESERVED[31:0]	32
0xBB032270	STAT_PORT_TX_MIB [4].RESERVED[31:0]	32
0xBB032274	STAT_PORT_TX_MIB [4].RESERVED[31:0]	32
0xBB032278	STAT_PORT_TX_MIB [4].RESERVED[31:0]	32
0xBB03227C	STAT_PORT_TX_MIB [4].RESERVED[31:0]	32
0xBB032280	STAT_PORT_TX_MIB [5].tx_etherStatsMulticastPkts[31:0]	32
0xBB032284	STAT_PORT_TX_MIB [5].tx_etherStatsBroadcastPkts[31:0]	32
0xBB032288	STAT_PORT_TX_MIB [5].tx_etherStatsUndersizePkts[31:0]	32
0xBB03228C	STAT_PORT_TX_MIB [5].tx_etherStatsOversizePkts[31:0]	32
0xBB032290	STAT_PORT_TX_MIB [5].tx_etherStatsPkts64Octets[31:0]	32
0xBB032294	STAT_PORT_TX_MIB [5].tx_etherStatsPkts65to127Octets[31:0]	32
0xBB032298	STAT_PORT_TX_MIB [5].tx_etherStatsPkts128to255Octets[31:0]	32
0xBB03229C	STAT_PORT_TX_MIB [5].tx_etherStatsPkts256to511Octets[31:0]	32
0xBB0322A0	STAT_PORT_TX_MIB [5].tx_etherStatsPkts512to1023Octets[31:0]	32
0xBB0322A4	STAT_PORT_TX_MIB [5].tx_etherStatsPkts1024to1518Octets[31:0]	32
0xBB0322A8	STAT_PORT_TX_MIB [5].ifOutOctets_L[31:0]	32
0xBB0322AC	STAT_PORT_TX_MIB [5].ifOutOctets_H[31:0]	32
0xBB0322B0	STAT_PORT_TX_MIB [5].dot3StatsSingleCollisionFrames[31:0]	32
0xBB0322B4	STAT_PORT_TX_MIB [5].dot3StatsMultipleCollisionFrames[31:0]	32
0xBB0322B8	STAT_PORT_TX_MIB [5].dot3StatsDeferredTransmissions[31:0]	32
0xBB0322BC	STAT_PORT_TX_MIB [5].dot3StatsLateCollisions[31:0]	32
0xBB0322C0	STAT_PORT_TX_MIB [5].etherStatsCollisions[31:0]	32
0xBB0322C4	STAT_PORT_TX_MIB [5].dot3StatsExcessiveCollisions[31:0]	32
0xBB0322C8	STAT_PORT_TX_MIB [5].dot3OutPauseFrames[31:0]	32
0xBB0322CC	STAT_PORT_TX_MIB [5].ifOutDiscards[31:0]	32
0xBB0322D0	STAT_PORT_TX_MIB [5].tx_etherStatsPkts1519toMaxOctets[31:0]	32
0xBB0322D4	STAT_PORT_TX_MIB [5].RESERVED[31:0]	32
0xBB0322D8	STAT_PORT_TX_MIB [5].dot1dTpPortInDiscards[31:0]	32
0xBB0322DC	STAT_PORT_TX_MIB [5].ifOutUcastPkts[31:0]	32
0xBB0322E0	STAT_PORT_TX_MIB [5].ifOutMulticastPkts[31:0]	32

Address	Register	Len
0xBB0322E4	STAT_PORT_TX_MIB [5].ifOutBroadcastPkts[31:0]	32
0xBB0322E8	STAT_PORT_TX_MIB [5].RESERVED[31:0]	32
0xBB0322EC	STAT_PORT_TX_MIB [5].RESERVED[31:0]	32
0xBB0322F0	STAT_PORT_TX_MIB [5].RESERVED[31:0]	32
0xBB0322F4	STAT_PORT_TX_MIB [5].RESERVED[31:0]	32
0xBB0322F8	STAT_PORT_TX_MIB [5].RESERVED[31:0]	32
0xBB0322FC	STAT_PORT_TX_MIB [5].RESERVED[31:0]	32
0xBB032300	STAT_PORT_TX_MIB [6].tx_etherStatsMulticastPkts[31:0]	32
0xBB032304	STAT_PORT_TX_MIB [6].tx_etherStatsBroadcastPkts[31:0]	32
0xBB032308	STAT_PORT_TX_MIB [6].tx_etherStatsUndersizePkts[31:0]	32
0xBB03230C	STAT_PORT_TX_MIB [6].tx_etherStatsOversizePkts[31:0]	32
0xBB032310	STAT_PORT_TX_MIB [6].tx_etherStatsPkts64Octets[31:0]	32
0xBB032314	STAT_PORT_TX_MIB [6].tx_etherStatsPkts65to127Octets[31:0]	32
0xBB032318	STAT_PORT_TX_MIB [6].tx_etherStatsPkts128to255Octets[31:0]	32
0xBB03231C	STAT_PORT_TX_MIB [6].tx_etherStatsPkts256to511Octets[31:0]	32
0xBB032320	STAT_PORT_TX_MIB [6].tx_etherStatsPkts512to1023Octets[31:0]	32
0xBB032324	STAT_PORT_TX_MIB [6].tx_etherStatsPkts1024to1518Octets[31:0]	32
0xBB032328	STAT_PORT_TX_MIB [6].ifOutOctets_L[31:0]	32
0xBB03232C	STAT_PORT_TX_MIB [6].ifOutOctets_H[31:0]	32
0xBB032330	STAT_PORT_TX_MIB [6].dot3StatsSingleCollisionFrames[31:0]	32
0xBB032334	STAT_PORT_TX_MIB [6].dot3StatsMultipleCollisionFrames[31:0]	32
0xBB032338	STAT_PORT_TX_MIB [6].dot3StatsDeferredTransmissions[31:0]	32
0xBB03233C	STAT_PORT_TX_MIB [6].dot3StatsLateCollisions[31:0]	32
0xBB032340	STAT_PORT_TX_MIB [6].etherStatsCollisions[31:0]	32
0xBB032344	STAT_PORT_TX_MIB [6].dot3StatsExcessiveCollisions[31:0]	32
0xBB032348	STAT_PORT_TX_MIB [6].dot3OutPauseFrames[31:0]	32
0xBB03234C	STAT_PORT_TX_MIB [6].ifOutDiscards[31:0]	32
0xBB032350	STAT_PORT_TX_MIB [6].tx_etherStatsPkts1519toMaxOctets[31:0]	32
0xBB032354	STAT_PORT_TX_MIB [6].RESERVED[31:0]	32
0xBB032358	STAT_PORT_TX_MIB [6].dot1dTpPortInDiscards[31:0]	32
0xBB03235C	STAT_PORT_TX_MIB [6].ifOutUcastPkts[31:0]	32
0xBB032360	STAT_PORT_TX_MIB [6].ifOutMulticastPkts[31:0]	32
0xBB032364	STAT_PORT_TX_MIB [6].ifOutBroadcastPkts[31:0]	32
0xBB032368	STAT_PORT_TX_MIB [6].RESERVED[31:0]	32
0xBB03236C	STAT_PORT_TX_MIB [6].RESERVED[31:0]	32
0xBB032370	STAT_PORT_TX_MIB [6].RESERVED[31:0]	32
0xBB032374	STAT_PORT_TX_MIB [6].RESERVED[31:0]	32
0xBB032378	STAT_PORT_TX_MIB [6].RESERVED[31:0]	32
0xBB03237C	STAT_PORT_TX_MIB [6].RESERVED[31:0]	32
0xBB032400	STAT_PORT_RX_MIB [0].ifInOctets_L[31:0]	32
0xBB032404	STAT_PORT_RX_MIB [0].ifInOctets_H[31:0]	32
0xBB032408	STAT_PORT_RX_MIB [0].etherStatsCRCAlignErrors[31:0]	32
0xBB03240C	STAT_PORT_RX_MIB [0].dot3StatsSymbolErrors[31:0]	32
0xBB032410	STAT_PORT_RX_MIB [0].dot3InPauseFrames[31:0]	32
0xBB032414	STAT_PORT_RX_MIB [0].dot3ControlInUnknownOpCodes[31:0]	32
0xBB032418	STAT_PORT_RX_MIB [0].etherStatsFragments[31:0]	32

Address	Register	Len
0xBB03241C	STAT_PORT_RX_MIB [0].etherStatsJabbers[31:0]	32
0xBB032420	STAT_PORT_RX_MIB [0].ifInUcastPkts[31:0]	32
0xBB032424	STAT_PORT_RX_MIB [0].etherStatsDropEvents[31:0]	32
0xBB032428	STAT_PORT_RX_MIB [0].ifInMulticastPkts[31:0]	32
0xBB03242C	STAT_PORT_RX_MIB [0].ifInBroadcastPkts[31:0]	32
0xBB032430	STAT_PORT_RX_MIB [0].rx_etherStatsPkts1519toMaxOctets[31:0]	32
0xBB032434	STAT_PORT_RX_MIB [0].rx_etherStatsUndersizeddropPkts[31:0]	32
0xBB032438	STAT_PORT_RX_MIB [0].rx_etherStatsUndersizePkts[31:0]	32
0xBB03243C	STAT_PORT_RX_MIB [0].rx_etherStatsOversizePkts[31:0]	32
0xBB032440	STAT_PORT_RX_MIB [0].rx_etherStatsPkts64Octets[31:0]	32
0xBB032444	STAT_PORT_RX_MIB [0].rx_etherStatsPkts65to127Octets[31:0]	32
0xBB032448	STAT_PORT_RX_MIB [0].rx_etherStatsPkts128to255Octets[31:0]	32
0xBB03244C	STAT_PORT_RX_MIB [0].rx_etherStatsPkts256to511Octets[31:0]	32
0xBB032450	STAT_PORT_RX_MIB [0].rx_etherStatsPkts512to1023Octets[31:0]	32
0xBB032454	STAT_PORT_RX_MIB [0].rx_etherStatsPkts1024to1518Octets[31:0]	32
0xBB032458	STAT_PORT_RX_MIB [0].RESERVED[31:0]	32
0xBB03245C	STAT_PORT_RX_MIB [0].RESERVED[31:0]	32
0xBB032460	STAT_PORT_RX_MIB [0].RESERVED[31:0]	32
0xBB032464	STAT_PORT_RX_MIB [0].RESERVED[31:0]	32
0xBB032468	STAT_PORT_RX_MIB [0].RESERVED[31:0]	32
0xBB03246C	STAT_PORT_RX_MIB [0].RESERVED[31:0]	32
0xBB032470	STAT_PORT_RX_MIB [0].RESERVED[31:0]	32
0xBB032474	STAT_PORT_RX_MIB [0].RESERVED[31:0]	32
0xBB032478	STAT_PORT_RX_MIB [0].RESERVED[31:0]	32
0xBB03247C	STAT_PORT_RX_MIB [0].RESERVED[31:0]	32
0xBB032480	STAT_PORT_RX_MIB [1].ifInOctets_L[31:0]	32
0xBB032484	STAT_PORT_RX_MIB [1].ifInOctets_H[31:0]	32
0xBB032488	STAT_PORT_RX_MIB [1].etherStatsCRCAlignErrors[31:0]	32
0xBB03248C	STAT_PORT_RX_MIB [1].dot3StatsSymbolErrors[31:0]	32
0xBB032490	STAT_PORT_RX_MIB [1].dot3InPauseFrames[31:0]	32
0xBB032494	STAT_PORT_RX_MIB [1].dot3ControlInUnknownOpCodes[31:0]	32
0xBB032498	STAT_PORT_RX_MIB [1].etherStatsFragments[31:0]	32
0xBB03249C	STAT_PORT_RX_MIB [1].etherStatsJabbers[31:0]	32
0xBB0324A0	STAT_PORT_RX_MIB [1].ifInUcastPkts[31:0]	32
0xBB0324A4	STAT_PORT_RX_MIB [1].etherStatsDropEvents[31:0]	32
0xBB0324A8	STAT_PORT_RX_MIB [1].ifInMulticastPkts[31:0]	32
0xBB0324AC	STAT_PORT_RX_MIB [1].ifInBroadcastPkts[31:0]	32
0xBB0324B0	STAT_PORT_RX_MIB [1].rx_etherStatsPkts1519toMaxOctets[31:0]	32
0xBB0324B4	STAT_PORT_RX_MIB [1].rx_etherStatsUndersizeddropPkts[31:0]	32
0xBB0324B8	STAT_PORT_RX_MIB [1].rx_etherStatsUndersizePkts[31:0]	32
0xBB0324BC	STAT_PORT_RX_MIB [1].rx_etherStatsOversizePkts[31:0]	32
0xBB0324C0	STAT_PORT_RX_MIB [1].rx_etherStatsPkts64Octets[31:0]	32
0xBB0324C4	STAT_PORT_RX_MIB [1].rx_etherStatsPkts65to127Octets[31:0]	32
0xBB0324C8	STAT_PORT_RX_MIB [1].rx_etherStatsPkts128to255Octets[31:0]	32
0xBB0324CC	STAT_PORT_RX_MIB [1].rx_etherStatsPkts256to511Octets[31:0]	32
0xBB0324D0	STAT_PORT_RX_MIB [1].rx_etherStatsPkts512to1023Octets[31:0]	32

Address	Register	Len
0xBB0324D4	STAT_PORT_RX_MIB [1].rx_etherStatsPkts1024to1518Octets[31:0]	32
0xBB0324D8	STAT_PORT_RX_MIB [1].RESERVED[31:0]	32
0xBB0324DC	STAT_PORT_RX_MIB [1].RESERVED[31:0]	32
0xBB0324E0	STAT_PORT_RX_MIB [1].RESERVED[31:0]	32
0xBB0324E4	STAT_PORT_RX_MIB [1].RESERVED[31:0]	32
0xBB0324E8	STAT_PORT_RX_MIB [1].RESERVED[31:0]	32
0xBB0324EC	STAT_PORT_RX_MIB [1].RESERVED[31:0]	32
0xBB0324F0	STAT_PORT_RX_MIB [1].RESERVED[31:0]	32
0xBB0324F4	STAT_PORT_RX_MIB [1].RESERVED[31:0]	32
0xBB0324F8	STAT_PORT_RX_MIB [1].RESERVED[31:0]	32
0xBB0324FC	STAT_PORT_RX_MIB [1].RESERVED[31:0]	32
0xBB032500	STAT_PORT_RX_MIB [2].ifInOctets_L[31:0]	32
0xBB032504	STAT_PORT_RX_MIB [2].ifInOctets_H[31:0]	32
0xBB032508	STAT_PORT_RX_MIB [2].etherStatsCRCAlignErrors[31:0]	32
0xBB03250C	STAT_PORT_RX_MIB [2].dot3StatsSymbolErrors[31:0]	32
0xBB032510	STAT_PORT_RX_MIB [2].dot3InPauseFrames[31:0]	32
0xBB032514	STAT_PORT_RX_MIB [2].dot3ControlInUnknownOpCodes[31:0]	32
0xBB032518	STAT_PORT_RX_MIB [2].etherStatsFragments[31:0]	32
0xBB03251C	STAT_PORT_RX_MIB [2].etherStatsJabbers[31:0]	32
0xBB032520	STAT_PORT_RX_MIB [2].ifInUcastPkts[31:0]	32
0xBB032524	STAT_PORT_RX_MIB [2].etherStatsDropEvents[31:0]	32
0xBB032528	STAT_PORT_RX_MIB [2].ifInMulticastPkts[31:0]	32
0xBB03252C	STAT_PORT_RX_MIB [2].ifInBroadcastPkts[31:0]	32
0xBB032530	STAT_PORT_RX_MIB [2].rx_etherStatsPkts1519toMaxOctets[31:0]	32
0xBB032534	STAT_PORT_RX_MIB [2].rx_etherStatsUndersizeddropPkts[31:0]	32
0xBB032538	STAT_PORT_RX_MIB [2].rx_etherStatsUndersizePkts[31:0]	32
0xBB03253C	STAT_PORT_RX_MIB [2].rx_etherStatsOversizePkts[31:0]	32
0xBB032540	STAT_PORT_RX_MIB [2].rx_etherStatsPkts64Octets[31:0]	32
0xBB032544	STAT_PORT_RX_MIB [2].rx_etherStatsPkts65to127Octets[31:0]	32
0xBB032548	STAT_PORT_RX_MIB [2].rx_etherStatsPkts128to255Octets[31:0]	32
0xBB03254C	STAT_PORT_RX_MIB [2].rx_etherStatsPkts256to511Octets[31:0]	32
0xBB032550	STAT_PORT_RX_MIB [2].rx_etherStatsPkts512to1023Octets[31:0]	32
0xBB032554	STAT_PORT_RX_MIB [2].rx_etherStatsPkts1024to1518Octets[31:0]	32
0xBB032558	STAT_PORT_RX_MIB [2].RESERVED[31:0]	32
0xBB03255C	STAT_PORT_RX_MIB [2].RESERVED[31:0]	32
0xBB032560	STAT_PORT_RX_MIB [2].RESERVED[31:0]	32
0xBB032564	STAT_PORT_RX_MIB [2].RESERVED[31:0]	32
0xBB032568	STAT_PORT_RX_MIB [2].RESERVED[31:0]	32
0xBB03256C	STAT_PORT_RX_MIB [2].RESERVED[31:0]	32
0xBB032570	STAT_PORT_RX_MIB [2].RESERVED[31:0]	32
0xBB032574	STAT_PORT_RX_MIB [2].RESERVED[31:0]	32
0xBB032578	STAT_PORT_RX_MIB [2].RESERVED[31:0]	32
0xBB03257C	STAT_PORT_RX_MIB [2].RESERVED[31:0]	32
0xBB032580	STAT_PORT_RX_MIB [3].ifInOctets_L[31:0]	32
0xBB032584	STAT_PORT_RX_MIB [3].ifInOctets_H[31:0]	32
0xBB032588	STAT_PORT_RX_MIB [3].etherStatsCRCAlignErrors[31:0]	32



Address	Register	Len
0xBB03258C	STAT_PORT_RX_MIB [3].dot3StatsSymbolErrors[31:0]	32
0xBB032590	STAT_PORT_RX_MIB [3].dot3InPauseFrames[31:0]	32
0xBB032594	STAT_PORT_RX_MIB [3].dot3ControlInUnknownOpCodes[31:0]	32
0xBB032598	STAT_PORT_RX_MIB [3].etherStatsFragments[31:0]	32
0xBB03259C	STAT_PORT_RX_MIB [3].etherStatsJabbers[31:0]	32
0xBB0325A0	STAT_PORT_RX_MIB [3].ifInUcastPkts[31:0]	32
0xBB0325A4	STAT_PORT_RX_MIB [3].etherStatsDropEvents[31:0]	32
0xBB0325A8	STAT_PORT_RX_MIB [3].ifInMulticastPkts[31:0]	32
0xBB0325AC	STAT_PORT_RX_MIB [3].ifInBroadcastPkts[31:0]	32
0xBB0325B0	STAT_PORT_RX_MIB [3].rx_etherStatsPkts1519toMaxOctets[31:0]	32
0xBB0325B4	STAT_PORT_RX_MIB [3].rx_etherStatsUndersizeddropPkts[31:0]	32
0xBB0325B8	STAT_PORT_RX_MIB [3].rx_etherStatsUndersizePkts[31:0]	32
0xBB0325BC	STAT_PORT_RX_MIB [3].rx_etherStatsOversizePkts[31:0]	32
0xBB0325C0	STAT_PORT_RX_MIB [3].rx_etherStatsPkts64Octets[31:0]	32
0xBB0325C4	STAT_PORT_RX_MIB [3].rx_etherStatsPkts65to127Octets[31:0]	32
0xBB0325C8	STAT_PORT_RX_MIB [3].rx_etherStatsPkts128to255Octets[31:0]	32
0xBB0325CC	STAT_PORT_RX_MIB [3].rx_etherStatsPkts256to511Octets[31:0]	32
0xBB0325D0	STAT_PORT_RX_MIB [3].rx_etherStatsPkts512to1023Octets[31:0]	32
0xBB0325D4	STAT_PORT_RX_MIB [3].rx_etherStatsPkts1024to1518Octets[31:0]	32
0xBB0325D8	STAT_PORT_RX_MIB [3].RESERVED[31:0]	32
0xBB0325DC	STAT_PORT_RX_MIB [3].RESERVED[31:0]	32
0xBB0325E0	STAT_PORT_RX_MIB [3].RESERVED[31:0]	32
0xBB0325E4	STAT_PORT_RX_MIB [3].RESERVED[31:0]	32
0xBB0325E8	STAT_PORT_RX_MIB [3].RESERVED[31:0]	32
0xBB0325EC	STAT_PORT_RX_MIB [3].RESERVED[31:0]	32
0xBB0325F0	STAT_PORT_RX_MIB [3].RESERVED[31:0]	32
0xBB0325F4	STAT_PORT_RX_MIB [3].RESERVED[31:0]	32
0xBB0325F8	STAT_PORT_RX_MIB [3].RESERVED[31:0]	32
0xBB0325FC	STAT_PORT_RX_MIB [3].RESERVED[31:0]	32
0xBB032600	STAT_PORT_RX_MIB [4].ifInOctets_L[31:0]	32
0xBB032604	STAT_PORT_RX_MIB [4].ifInOctets_H[31:0]	32
0xBB032608	STAT_PORT_RX_MIB [4].etherStatsCRCAlignErrors[31:0]	32
0xBB03260C	STAT_PORT_RX_MIB [4].dot3StatsSymbolErrors[31:0]	32
0xBB032610	STAT_PORT_RX_MIB [4].dot3InPauseFrames[31:0]	32
0xBB032614	STAT_PORT_RX_MIB [4].dot3ControlInUnknownOpCodes[31:0]	32
0xBB032618	STAT_PORT_RX_MIB [4].etherStatsFragments[31:0]	32
0xBB03261C	STAT_PORT_RX_MIB [4].etherStatsJabbers[31:0]	32
0xBB032620	STAT_PORT_RX_MIB [4].ifInUcastPkts[31:0]	32
0xBB032624	STAT_PORT_RX_MIB [4].etherStatsDropEvents[31:0]	32
0xBB032628	STAT_PORT_RX_MIB [4].ifInMulticastPkts[31:0]	32
0xBB03262C	STAT_PORT_RX_MIB [4].ifInBroadcastPkts[31:0]	32
0xBB032630	STAT_PORT_RX_MIB [4].rx_etherStatsPkts1519toMaxOctets[31:0]	32
0xBB032634	STAT_PORT_RX_MIB [4].rx_etherStatsUndersizeddropPkts[31:0]	32
0xBB032638	STAT_PORT_RX_MIB [4].rx_etherStatsUndersizePkts[31:0]	32
0xBB03263C	STAT_PORT_RX_MIB [4].rx_etherStatsOversizePkts[31:0]	32
0xBB032640	STAT_PORT_RX_MIB [4].rx_etherStatsPkts64Octets[31:0]	32

Address	Register	Len
0xBB032644	STAT_PORT_RX_MIB [4].rx_etherStatsPkts65to127Octets[31:0]	32
0xBB032648	STAT_PORT_RX_MIB [4].rx_etherStatsPkts128to255Octets[31:0]	32
0xBB03264C	STAT_PORT_RX_MIB [4].rx_etherStatsPkts256to511Octets[31:0]	32
0xBB032650	STAT_PORT_RX_MIB [4].rx_etherStatsPkts512to1023Octets[31:0]	32
0xBB032654	STAT_PORT_RX_MIB [4].rx_etherStatsPkts1024to1518Octets[31:0]	32
0xBB032658	STAT_PORT_RX_MIB [4].RESERVED[31:0]	32
0xBB03265C	STAT_PORT_RX_MIB [4].RESERVED[31:0]	32
0xBB032660	STAT_PORT_RX_MIB [4].RESERVED[31:0]	32
0xBB032664	STAT_PORT_RX_MIB [4].RESERVED[31:0]	32
0xBB032668	STAT_PORT_RX_MIB [4].RESERVED[31:0]	32
0xBB03266C	STAT_PORT_RX_MIB [4].RESERVED[31:0]	32
0xBB032670	STAT_PORT_RX_MIB [4].RESERVED[31:0]	32
0xBB032674	STAT_PORT_RX_MIB [4].RESERVED[31:0]	32
0xBB032678	STAT_PORT_RX_MIB [4].RESERVED[31:0]	32
0xBB03267C	STAT_PORT_RX_MIB [4].RESERVED[31:0]	32
0xBB032680	STAT_PORT_RX_MIB [5].ifInOctets_L[31:0]	32
0xBB032684	STAT_PORT_RX_MIB [5].ifInOctets_H[31:0]	32
0xBB032688	STAT_PORT_RX_MIB [5].etherStatsCRCAlignErrors[31:0]	32
0xBB03268C	STAT_PORT_RX_MIB [5].dot3StatsSymbolErrors[31:0]	32
0xBB032690	STAT_PORT_RX_MIB [5].dot3InPauseFrames[31:0]	32
0xBB032694	STAT_PORT_RX_MIB [5].dot3ControlInUnknownOpCodes[31:0]	32
0xBB032698	STAT_PORT_RX_MIB [5].etherStatsFragments[31:0]	32
0xBB03269C	STAT_PORT_RX_MIB [5].etherStatsJabbers[31:0]	32
0xBB0326A0	STAT_PORT_RX_MIB [5].ifInUcastPkts[31:0]	32
0xBB0326A4	STAT_PORT_RX_MIB [5].etherStatsDropEvents[31:0]	32
0xBB0326A8	STAT_PORT_RX_MIB [5].ifInMulticastPkts[31:0]	32
0xBB0326AC	STAT_PORT_RX_MIB [5].ifInBroadcastPkts[31:0]	32
0xBB0326B0	STAT_PORT_RX_MIB [5].rx_etherStatsPkts1519toMaxOctets[31:0]	32
0xBB0326B4	STAT_PORT_RX_MIB [5].rx_etherStatsUndersizeddropPkts[31:0]	32
0xBB0326B8	STAT_PORT_RX_MIB [5].rx_etherStatsUndersizePkts[31:0]	32
0xBB0326BC	STAT_PORT_RX_MIB [5].rx_etherStatsOversizePkts[31:0]	32
0xBB0326C0	STAT_PORT_RX_MIB [5].rx_etherStatsPkts64Octets[31:0]	32
0xBB0326C4	STAT_PORT_RX_MIB [5].rx_etherStatsPkts65to127Octets[31:0]	32
0xBB0326C8	STAT_PORT_RX_MIB [5].rx_etherStatsPkts128to255Octets[31:0]	32
0xBB0326CC	STAT_PORT_RX_MIB [5].rx_etherStatsPkts256to511Octets[31:0]	32
0xBB0326D0	STAT_PORT_RX_MIB [5].rx_etherStatsPkts512to1023Octets[31:0]	32
0xBB0326D4	STAT_PORT_RX_MIB [5].rx_etherStatsPkts1024to1518Octets[31:0]	32
0xBB0326D8	STAT_PORT_RX_MIB [5].RESERVED[31:0]	32
0xBB0326DC	STAT_PORT_RX_MIB [5].RESERVED[31:0]	32
0xBB0326E0	STAT_PORT_RX_MIB [5].RESERVED[31:0]	32
0xBB0326E4	STAT_PORT_RX_MIB [5].RESERVED[31:0]	32
0xBB0326E8	STAT_PORT_RX_MIB [5].RESERVED[31:0]	32
0xBB0326EC	STAT_PORT_RX_MIB [5].RESERVED[31:0]	32
0xBB0326F0	STAT_PORT_RX_MIB [5].RESERVED[31:0]	32
0xBB0326F4	STAT_PORT_RX_MIB [5].RESERVED[31:0]	32
0xBB0326F8	STAT_PORT_RX_MIB [5].RESERVED[31:0]	32



Address	Register	Len
0xBB0326FC	STAT_PORT_RX_MIB [5].RESERVED[31:0]	32
0xBB032700	STAT_PORT_RX_MIB [6].ifInOctets_L[31:0]	32
0xBB032704	STAT_PORT_RX_MIB [6].ifInOctets_H[31:0]	32
0xBB032708	STAT_PORT_RX_MIB [6].etherStatsCRCAlignErrors[31:0]	32
0xBB03270C	STAT_PORT_RX_MIB [6].dot3StatsSymbolErrors[31:0]	32
0xBB032710	STAT_PORT_RX_MIB [6].dot3InPauseFrames[31:0]	32
0xBB032714	STAT_PORT_RX_MIB [6].dot3ControlInUnknownOpCodes[31:0]	32
0xBB032718	STAT_PORT_RX_MIB [6].etherStatsFragments[31:0]	32
0xBB03271C	STAT_PORT_RX_MIB [6].etherStatsJabbers[31:0]	32
0xBB032720	STAT_PORT_RX_MIB [6].ifInUcastPkts[31:0]	32
0xBB032724	STAT_PORT_RX_MIB [6].etherStatsDropEvents[31:0]	32
0xBB032728	STAT_PORT_RX_MIB [6].ifInMulticastPkts[31:0]	32
0xBB03272C	STAT_PORT_RX_MIB [6].ifInBroadcastPkts[31:0]	32
0xBB032730	STAT_PORT_RX_MIB [6].rx_etherStatsPkts1519toMaxOctets[31:0]	32
0xBB032734	STAT_PORT_RX_MIB [6].rx_etherStatsUndersizeddropPkts[31:0]	32
0xBB032738	STAT_PORT_RX_MIB [6].rx_etherStatsUndersizePkts[31:0]	32
0xBB03273C	STAT_PORT_RX_MIB [6].rx_etherStatsOversizePkts[31:0]	32
0xBB032740	STAT_PORT_RX_MIB [6].rx_etherStatsPkts64Octets[31:0]	32
0xBB032744	STAT_PORT_RX_MIB [6].rx_etherStatsPkts65to127Octets[31:0]	32
0xBB032748	STAT_PORT_RX_MIB [6].rx_etherStatsPkts128to255Octets[31:0]	32
0xBB03274C	STAT_PORT_RX_MIB [6].rx_etherStatsPkts256to511Octets[31:0]	32
0xBB032750	STAT_PORT_RX_MIB [6].rx_etherStatsPkts512to1023Octets[31:0]	32
0xBB032754	STAT_PORT_RX_MIB [6].rx_etherStatsPkts1024to1518Octets[31:0]	32
0xBB032758	STAT_PORT_RX_MIB [6].RESERVED[31:0]	32
0xBB03275C	STAT_PORT_RX_MIB [6].RESERVED[31:0]	32
0xBB032760	STAT_PORT_RX_MIB [6].RESERVED[31:0]	32
0xBB032764	STAT_PORT_RX_MIB [6].RESERVED[31:0]	32
0xBB032768	STAT_PORT_RX_MIB [6].RESERVED[31:0]	32
0xBB03276C	STAT_PORT_RX_MIB [6].RESERVED[31:0]	32
0xBB032770	STAT_PORT_RX_MIB [6].RESERVED[31:0]	32
0xBB032774	STAT_PORT_RX_MIB [6].RESERVED[31:0]	32
0xBB032778	STAT_PORT_RX_MIB [6].RESERVED[31:0]	32
0xBB03277C	STAT_PORT_RX_MIB [6].RESERVED[31:0]	32
0xBB032800	STAT_PORT_OAM_MIB [0].OutOampduPkts[31:0]	32
0xBB032804	STAT_PORT_OAM_MIB [0].InOampduPkts[31:0]	32
0xBB032808	STAT_PORT_OAM_MIB [1].OutOampduPkts[31:0]	32
0xBB03280C	STAT_PORT_OAM_MIB [1].InOampduPkts[31:0]	32
0xBB032810	STAT_PORT_OAM_MIB [2].OutOampduPkts[31:0]	32
0xBB032814	STAT_PORT_OAM_MIB [2].InOampduPkts[31:0]	32
0xBB032818	STAT_PORT_OAM_MIB [3].OutOampduPkts[31:0]	32
0xBB03281C	STAT_PORT_OAM_MIB [3].InOampduPkts[31:0]	32
0xBB032820	STAT_PORT_OAM_MIB [4].OutOampduPkts[31:0]	32
0xBB032824	STAT_PORT_OAM_MIB [4].InOampduPkts[31:0]	32
0xBB032828	STAT_PORT_OAM_MIB [5].OutOampduPkts[31:0]	32
0xBB03282C	STAT_PORT_OAM_MIB [5].InOampduPkts[31:0]	32
0xBB032830	STAT_PORT_OAM_MIB [6].OutOampduPkts[31:0]	32

Address	Register	Len
0xBB032834	STAT_PORT_OAM_MIB [6].InOampduPkts[31:0]	32
0xBB032840	STAT_BRIDGE_DOT1DTPLEARNEDENTRYDISCARDS.dot1dTpLearnedEntryDiscards[31:0]	32
0xBB032880	STAT_ACL_CNT [0].loggingcounter[31:0]	32
0xBB032884	STAT_ACL_CNT [1].loggingcounter[31:0]	32
0xBB032888	STAT_ACL_CNT [2].loggingcounter[31:0]	32
0xBB03288C	STAT_ACL_CNT [3].loggingcounter[31:0]	32
0xBB032890	STAT_ACL_CNT [4].loggingcounter[31:0]	32
0xBB032894	STAT_ACL_CNT [5].loggingcounter[31:0]	32
0xBB032898	STAT_ACL_CNT [6].loggingcounter[31:0]	32
0xBB03289C	STAT_ACL_CNT [7].loggingcounter[31:0]	32
0xBB0328A0	STAT_ACL_CNT [8].loggingcounter[31:0]	32
0xBB0328A4	STAT_ACL_CNT [9].loggingcounter[31:0]	32
0xBB0328A8	STAT_ACL_CNT [10].loggingcounter[31:0]	32
0xBB0328AC	STAT_ACL_CNT [11].loggingcounter[31:0]	32
0xBB0328B0	STAT_ACL_CNT [12].loggingcounter[31:0]	32
0xBB0328B4	STAT_ACL_CNT [13].loggingcounter[31:0]	32
0xBB0328B8	STAT_ACL_CNT [14].loggingcounter[31:0]	32
0xBB0328BC	STAT_ACL_CNT [15].loggingcounter[31:0]	32
0xBB0328C0	STAT_ACL_CNT [16].loggingcounter[31:0]	32
0xBB0328C4	STAT_ACL_CNT [17].loggingcounter[31:0]	32
0xBB0328C8	STAT_ACL_CNT [18].loggingcounter[31:0]	32
0xBB0328CC	STAT_ACL_CNT [19].loggingcounter[31:0]	32
0xBB0328D0	STAT_ACL_CNT [20].loggingcounter[31:0]	32
0xBB0328D4	STAT_ACL_CNT [21].loggingcounter[31:0]	32
0xBB0328D8	STAT_ACL_CNT [22].loggingcounter[31:0]	32
0xBB0328DC	STAT_ACL_CNT [23].loggingcounter[31:0]	32
0xBB0328E0	STAT_ACL_CNT [24].loggingcounter[31:0]	32
0xBB0328E4	STAT_ACL_CNT [25].loggingcounter[31:0]	32
0xBB0328E8	STAT_ACL_CNT [26].loggingcounter[31:0]	32
0xBB0328EC	STAT_ACL_CNT [27].loggingcounter[31:0]	32
0xBB0328F0	STAT_ACL_CNT [28].loggingcounter[31:0]	32
0xBB0328F4	STAT_ACL_CNT [29].loggingcounter[31:0]	32
0xBB0328F8	STAT_ACL_CNT [30].loggingcounter[31:0]	32
0xBB0328FC	STAT_ACL_CNT [31].loggingcounter[31:0]	32
0xBB032900	OMCI_DROP_PKT_CNT.omciDropPktCnt[31:0]	32
0xBB032904	OMCI_TX_PKT_CNT.omciTxPktCnt[31:0]	32
0xBB032908	OMCI_RX_PKT_CNT.omciRxPktCnt[31:0]	32
0xBB03290C	OMCI_TX_BYTE_CNT.omciTxByteCnt[31:0]	32
0xBB032910	OMCI_RX_BYTE_CNT.omciRxByteCnt[31:0]	32
0xBB032914	OMCI_CRC_ERROR_PKT_CNT.omciCRCErrorPktCnt[31:0]	32
0xBB032918	DOT3_Q_TX_FRAMES [0].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB03291C	DOT3_Q_TX_FRAMES [1].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032920	DOT3_Q_TX_FRAMES [2].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032924	DOT3_Q_TX_FRAMES [3].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032928	DOT3_Q_TX_FRAMES [4].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB03292C	DOT3_Q_TX_FRAMES [5].dot3ExtPkgStatTxFramesQueue[31:0]	32

Address	Register	Len
0xBB032930	DOT3_Q_TX_FRAMES [6].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032934	DOT3_Q_TX_FRAMES [7].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032938	DOT3_Q_TX_FRAMES [8].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB03293C	DOT3_Q_TX_FRAMES [9].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032940	DOT3_Q_TX_FRAMES [10].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032944	DOT3_Q_TX_FRAMES [11].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032948	DOT3_Q_TX_FRAMES [12].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB03294C	DOT3_Q_TX_FRAMES [13].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032950	DOT3_Q_TX_FRAMES [14].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032954	DOT3_Q_TX_FRAMES [15].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032958	DOT3_Q_TX_FRAMES [16].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB03295C	DOT3_Q_TX_FRAMES [17].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032960	DOT3_Q_TX_FRAMES [18].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032964	DOT3_Q_TX_FRAMES [19].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032968	DOT3_Q_TX_FRAMES [20].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB03296C	DOT3_Q_TX_FRAMES [21].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032970	DOT3_Q_TX_FRAMES [22].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032974	DOT3_Q_TX_FRAMES [23].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032978	DOT3_Q_TX_FRAMES [24].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB03297C	DOT3_Q_TX_FRAMES [25].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032980	DOT3_Q_TX_FRAMES [26].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032984	DOT3_Q_TX_FRAMES [27].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032988	DOT3_Q_TX_FRAMES [28].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB03298C	DOT3_Q_TX_FRAMES [29].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032990	DOT3_Q_TX_FRAMES [30].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032994	DOT3_Q_TX_FRAMES [31].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032998	DOT3_Q_TX_FRAMES [32].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB03299C	DOT3_Q_TX_FRAMES [33].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB0329A0	DOT3_Q_TX_FRAMES [34].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB0329A4	DOT3_Q_TX_FRAMES [35].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB0329A8	DOT3_Q_TX_FRAMES [36].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB0329AC	DOT3_Q_TX_FRAMES [37].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB0329B0	DOT3_Q_TX_FRAMES [38].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB0329B4	DOT3_Q_TX_FRAMES [39].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB0329B8	DOT3_Q_TX_FRAMES [40].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB0329BC	DOT3_Q_TX_FRAMES [41].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB0329C0	DOT3_Q_TX_FRAMES [42].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB0329C4	DOT3_Q_TX_FRAMES [43].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB0329C8	DOT3_Q_TX_FRAMES [44].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB0329CC	DOT3_Q_TX_FRAMES [45].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB0329D0	DOT3_Q_TX_FRAMES [46].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB0329D4	DOT3_Q_TX_FRAMES [47].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB0329D8	DOT3_Q_TX_FRAMES [48].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB0329DC	DOT3_Q_TX_FRAMES [49].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB0329E0	DOT3_Q_TX_FRAMES [50].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB0329E4	DOT3_Q_TX_FRAMES [51].dot3ExtPkgStatTxFramesQueue[31:0]	32

Address	Register	Len
0xBB0329E8	DOT3_Q_TX_FRAMES [52].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB0329EC	DOT3_Q_TX_FRAMES [53].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB0329F0	DOT3_Q_TX_FRAMES [54].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB0329F4	DOT3_Q_TX_FRAMES [55].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB0329F8	DOT3_Q_TX_FRAMES [56].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB0329FC	DOT3_Q_TX_FRAMES [57].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A00	DOT3_Q_TX_FRAMES [58].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A04	DOT3_Q_TX_FRAMES [59].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A08	DOT3_Q_TX_FRAMES [60].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A0C	DOT3_Q_TX_FRAMES [61].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A10	DOT3_Q_TX_FRAMES [62].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A14	DOT3_Q_TX_FRAMES [63].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A18	DOT3_Q_TX_FRAMES [64].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A1C	DOT3_Q_TX_FRAMES [65].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A20	DOT3_Q_TX_FRAMES [66].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A24	DOT3_Q_TX_FRAMES [67].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A28	DOT3_Q_TX_FRAMES [68].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A2C	DOT3_Q_TX_FRAMES [69].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A30	DOT3_Q_TX_FRAMES [70].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A34	DOT3_Q_TX_FRAMES [71].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A38	DOT3_Q_TX_FRAMES [72].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A3C	DOT3_Q_TX_FRAMES [73].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A40	DOT3_Q_TX_FRAMES [74].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A44	DOT3_Q_TX_FRAMES [75].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A48	DOT3_Q_TX_FRAMES [76].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A4C	DOT3_Q_TX_FRAMES [77].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A50	DOT3_Q_TX_FRAMES [78].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A54	DOT3_Q_TX_FRAMES [79].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A58	DOT3_Q_TX_FRAMES [80].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A5C	DOT3_Q_TX_FRAMES [81].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A60	DOT3_Q_TX_FRAMES [82].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A64	DOT3_Q_TX_FRAMES [83].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A68	DOT3_Q_TX_FRAMES [84].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A6C	DOT3_Q_TX_FRAMES [85].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A70	DOT3_Q_TX_FRAMES [86].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A74	DOT3_Q_TX_FRAMES [87].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A78	DOT3_Q_TX_FRAMES [88].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A7C	DOT3_Q_TX_FRAMES [89].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A80	DOT3_Q_TX_FRAMES [90].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A84	DOT3_Q_TX_FRAMES [91].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A88	DOT3_Q_TX_FRAMES [92].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A8C	DOT3_Q_TX_FRAMES [93].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A90	DOT3_Q_TX_FRAMES [94].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A94	DOT3_Q_TX_FRAMES [95].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A98	DOT3_Q_TX_FRAMES [96].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032A9C	DOT3_Q_TX_FRAMES [97].dot3ExtPkgStatTxFramesQueue[31:0]	32

Address	Register	Len
0xBB032AA0	DOT3_Q_TX_FRAMES [98].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032AA4	DOT3_Q_TX_FRAMES [99].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032AA8	DOT3_Q_TX_FRAMES [100].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032AAC	DOT3_Q_TX_FRAMES [101].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032AB0	DOT3_Q_TX_FRAMES [102].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032AB4	DOT3_Q_TX_FRAMES [103].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032AB8	DOT3_Q_TX_FRAMES [104].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032ABC	DOT3_Q_TX_FRAMES [105].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032AC0	DOT3_Q_TX_FRAMES [106].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032AC4	DOT3_Q_TX_FRAMES [107].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032AC8	DOT3_Q_TX_FRAMES [108].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032ACC	DOT3_Q_TX_FRAMES [109].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032AD0	DOT3_Q_TX_FRAMES [110].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032AD4	DOT3_Q_TX_FRAMES [111].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032AD8	DOT3_Q_TX_FRAMES [112].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032ADC	DOT3_Q_TX_FRAMES [113].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032AE0	DOT3_Q_TX_FRAMES [114].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032AE4	DOT3_Q_TX_FRAMES [115].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032AE8	DOT3_Q_TX_FRAMES [116].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032AEC	DOT3_Q_TX_FRAMES [117].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032AF0	DOT3_Q_TX_FRAMES [118].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032AF4	DOT3_Q_TX_FRAMES [119].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032AF8	DOT3_Q_TX_FRAMES [120].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032AFC	DOT3_Q_TX_FRAMES [121].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032B00	DOT3_Q_TX_FRAMES [122].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032B04	DOT3_Q_TX_FRAMES [123].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032B08	DOT3_Q_TX_FRAMES [124].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032B0C	DOT3_Q_TX_FRAMES [125].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032B10	DOT3_Q_TX_FRAMES [126].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032B14	DOT3_Q_TX_FRAMES [127].dot3ExtPkgStatTxFramesQueue[31:0]	32
0xBB032B18	DOT3_MPCP_RX_DISC.dot3MpcpRxDiscoveryGate[31:0]	32
0xBB032B1C	DOT3_EPON_FEC_CORRECTED_BLOCKS.dot3EponFecCorrectedBlocks[31:0]	32
0xBB032B20	DOT3_EPON_FEC_UNCORRECTED_BLOCKS.dot3EponFecUncorrectableBlocks[31:0]	32
0xBB032B24	DOT3_EPON_FEC_CODING_VIO.FecPCSCodingViolation[31:0]	32
0xBB032B28	DOT3_NOT_BROADCAST_BIT_NOT_ONU_LLID.NotBroadcastBitNotOnuLlid[31:0]	32
0xBB032B2C	DOT3_BROADCAST_BIT_PLUS_ONU_LLID.BroadcastBitPlusOnuLlid[31:0]	32
0xBB032B30	DOT3_BROADCAST_NOT_ONUID.BroadcastBitNotOnuLlid[31:0]	32
0xBB032B34	DOT3_CRC8_ERRORS.CRC8Errors[31:0]	32
0xBB032B38	DOT3_LLID_RX_BROADCAST_DROP_FRAMES.dot3LLIDRxBroadcastFramesDrop[31:0]	32
0xBB032B3C	DOT3_MPCP_TX_REPORT [0].dot3MpcpTxReport[31:0]	32
0xBB032B40	DOT3_MPCP_TX_REPORT [1].dot3MpcpTxReport[31:0]	32
0xBB032B44	DOT3_MPCP_TX_REPORT [2].dot3MpcpTxReport[31:0]	32
0xBB032B48	DOT3_MPCP_TX_REPORT [3].dot3MpcpTxReport[31:0]	32
0xBB032B4C	DOT3_MPCP_TX_REPORT [4].dot3MpcpTxReport[31:0]	32
0xBB032B50	DOT3_MPCP_TX_REPORT [5].dot3MpcpTxReport[31:0]	32
0xBB032B54	DOT3_MPCP_TX_REPORT [6].dot3MpcpTxReport[31:0]	32



Address	Register	Len
0xBB032B58	DOT3_MPCP_TX_REPORT [7].dot3MpcpTxReport[31:0]	32
0xBB032B5C	DOT3_MPCP_EX_GATE [0].dot3MpcpRxGate[31:0]	32
0xBB032B60	DOT3_MPCP_EX_GATE [1].dot3MpcpRxGate[31:0]	32
0xBB032B64	DOT3_MPCP_EX_GATE [2].dot3MpcpRxGate[31:0]	32
0xBB032B68	DOT3_MPCP_EX_GATE [3].dot3MpcpRxGate[31:0]	32
0xBB032B6C	DOT3_MPCP_EX_GATE [4].dot3MpcpRxGate[31:0]	32
0xBB032B70	DOT3_MPCP_EX_GATE [5].dot3MpcpRxGate[31:0]	32
0xBB032B74	DOT3_MPCP_EX_GATE [6].dot3MpcpRxGate[31:0]	32
0xBB032B78	DOT3_MPCP_EX_GATE [7].dot3MpcpRxGate[31:0]	32
0xBB032B7C	DOT3_ONUID_NOT_BROADCAST [0].OnuLLIDNotBroadcast[31:0]	32
0xBB032B80	DOT3_ONUID_NOT_BROADCAST [1].OnuLLIDNotBroadcast[31:0]	32
0xBB032B84	DOT3_ONUID_NOT_BROADCAST [2].OnuLLIDNotBroadcast[31:0]	32
0xBB032B88	DOT3_ONUID_NOT_BROADCAST [3].OnuLLIDNotBroadcast[31:0]	32
0xBB032B8C	DOT3_ONUID_NOT_BROADCAST [4].OnuLLIDNotBroadcast[31:0]	32
0xBB032B90	DOT3_ONUID_NOT_BROADCAST [5].OnuLLIDNotBroadcast[31:0]	32
0xBB032B94	DOT3_ONUID_NOT_BROADCAST [6].OnuLLIDNotBroadcast[31:0]	32
0xBB032B98	DOT3_ONUID_NOT_BROADCAST [7].OnuLLIDNotBroadcast[31:0]	32
0xBB032B9C	STAT_DOT3_LLIDRXFRAMESDROP [0].dot3LLIDRxFramesDrop[31:0]	32
0xBB032BA0	STAT_DOT3_LLIDRXFRAMESDROP [1].dot3LLIDRxFramesDrop[31:0]	32
0xBB032BA4	STAT_DOT3_LLIDRXFRAMESDROP [2].dot3LLIDRxFramesDrop[31:0]	32
0xBB032BA8	STAT_DOT3_LLIDRXFRAMESDROP [3].dot3LLIDRxFramesDrop[31:0]	32
0xBB032BAC	STAT_DOT3_LLIDRXFRAMESDROP [4].dot3LLIDRxFramesDrop[31:0]	32
0xBB032BB0	STAT_DOT3_LLIDRXFRAMESDROP [5].dot3LLIDRxFramesDrop[31:0]	32
0xBB032BB4	STAT_DOT3_LLIDRXFRAMESDROP [6].dot3LLIDRxFramesDrop[31:0]	32
0xBB032BB8	STAT_DOT3_LLIDRXFRAMESDROP [7].dot3LLIDRxFramesDrop[31:0]	32
0xBB032BBC	DOT3_MPCP_TX_REG_REQ.dot3MpcpTxRegRequest[31:0]	32
0xBB034000	STAT_CTRL.RESERVED[31:13]	19
0xBB034000	STAT_CTRL.SYNC_STATUS[12:12]	1
0xBB034000	STAT_CTRL.LATCH_TIMER[11:4]	8
0xBB034000	STAT_CTRL.TX_CNT_CTAG[3:3]	1
0xBB034000	STAT_CTRL.RX_CNT_CTAG[2:2]	1
0xBB034000	STAT_CTRL.SYNC_MODE[1:1]	1
0xBB034000	STAT_CTRL.CNTING_MODE[0:0]	1
0xBB034004	STAT_ACL_CNT_MODE [0].MODE[0:0]	1
0xBB034004	STAT_ACL_CNT_MODE [1].MODE[1:1]	1
0xBB034004	STAT_ACL_CNT_MODE [2].MODE[2:2]	1
0xBB034004	STAT_ACL_CNT_MODE [3].MODE[3:3]	1
0xBB034004	STAT_ACL_CNT_MODE [4].MODE[4:4]	1
0xBB034004	STAT_ACL_CNT_MODE [5].MODE[5:5]	1
0xBB034004	STAT_ACL_CNT_MODE [6].MODE[6:6]	1
0xBB034004	STAT_ACL_CNT_MODE [7].MODE[7:7]	1
0xBB034004	STAT_ACL_CNT_MODE [8].MODE[8:8]	1
0xBB034004	STAT_ACL_CNT_MODE [9].MODE[9:9]	1
0xBB034004	STAT_ACL_CNT_MODE [10].MODE[10:10]	1
0xBB034004	STAT_ACL_CNT_MODE [11].MODE[11:11]	1
0xBB034004	STAT_ACL_CNT_MODE [12].MODE[12:12]	1

Address	Register	Len
0xBB034004	STAT_ACL_CNT_MODE [13].MODE[13:13]	1
0xBB034004	STAT_ACL_CNT_MODE [14].MODE[14:14]	1
0xBB034004	STAT_ACL_CNT_MODE [15].MODE[15:15]	1
0xBB034008	STAT_ACL_CNT_TYPE [0].TYPE[0:0]	1
0xBB034008	STAT_ACL_CNT_TYPE [1].TYPE[1:1]	1
0xBB034008	STAT_ACL_CNT_TYPE [2].TYPE[2:2]	1
0xBB034008	STAT_ACL_CNT_TYPE [3].TYPE[3:3]	1
0xBB034008	STAT_ACL_CNT_TYPE [4].TYPE[4:4]	1
0xBB034008	STAT_ACL_CNT_TYPE [5].TYPE[5:5]	1
0xBB034008	STAT_ACL_CNT_TYPE [6].TYPE[6:6]	1
0xBB034008	STAT_ACL_CNT_TYPE [7].TYPE[7:7]	1
0xBB034008	STAT_ACL_CNT_TYPE [8].TYPE[8:8]	1
0xBB034008	STAT_ACL_CNT_TYPE [9].TYPE[9:9]	1
0xBB034008	STAT_ACL_CNT_TYPE [10].TYPE[10:10]	1
0xBB034008	STAT_ACL_CNT_TYPE [11].TYPE[11:11]	1
0xBB034008	STAT_ACL_CNT_TYPE [12].TYPE[12:12]	1
0xBB034008	STAT_ACL_CNT_TYPE [13].TYPE[13:13]	1
0xBB034008	STAT_ACL_CNT_TYPE [14].TYPE[14:14]	1
0xBB034008	STAT_ACL_CNT_TYPE [15].TYPE[15:15]	1
0xBB03400C	STAT_ACL_CNT_RST [0].EN[0:0]	1
0xBB03400C	STAT_ACL_CNT_RST [1].EN[1:1]	1
0xBB03400C	STAT_ACL_CNT_RST [2].EN[2:2]	1
0xBB03400C	STAT_ACL_CNT_RST [3].EN[3:3]	1
0xBB03400C	STAT_ACL_CNT_RST [4].EN[4:4]	1
0xBB03400C	STAT_ACL_CNT_RST [5].EN[5:5]	1
0xBB03400C	STAT_ACL_CNT_RST [6].EN[6:6]	1
0xBB03400C	STAT_ACL_CNT_RST [7].EN[7:7]	1
0xBB03400C	STAT_ACL_CNT_RST [8].EN[8:8]	1
0xBB03400C	STAT_ACL_CNT_RST [9].EN[9:9]	1
0xBB03400C	STAT_ACL_CNT_RST [10].EN[10:10]	1
0xBB03400C	STAT_ACL_CNT_RST [11].EN[11:11]	1
0xBB03400C	STAT_ACL_CNT_RST [12].EN[12:12]	1
0xBB03400C	STAT_ACL_CNT_RST [13].EN[13:13]	1
0xBB03400C	STAT_ACL_CNT_RST [14].EN[14:14]	1
0xBB03400C	STAT_ACL_CNT_RST [15].EN[15:15]	1
0xBB03400C	STAT_ACL_CNT_RST [16].EN[16:16]	1
0xBB03400C	STAT_ACL_CNT_RST [17].EN[17:17]	1
0xBB03400C	STAT_ACL_CNT_RST [18].EN[18:18]	1
0xBB03400C	STAT_ACL_CNT_RST [19].EN[19:19]	1
0xBB03400C	STAT_ACL_CNT_RST [20].EN[20:20]	1
0xBB03400C	STAT_ACL_CNT_RST [21].EN[21:21]	1
0xBB03400C	STAT_ACL_CNT_RST [22].EN[22:22]	1
0xBB03400C	STAT_ACL_CNT_RST [23].EN[23:23]	1
0xBB03400C	STAT_ACL_CNT_RST [24].EN[24:24]	1
0xBB03400C	STAT_ACL_CNT_RST [25].EN[25:25]	1
0xBB03400C	STAT_ACL_CNT_RST [26].EN[26:26]	1

Address	Register	Len
0xBB03400C	STAT_ACL_CNT_RST [27].EN[27:27]	1
0xBB03400C	STAT_ACL_CNT_RST [28].EN[28:28]	1
0xBB03400C	STAT_ACL_CNT_RST [29].EN[29:29]	1
0xBB03400C	STAT_ACL_CNT_RST [30].EN[30:30]	1
0xBB03400C	STAT_ACL_CNT_RST [31].EN[31:31]	1
0xBB034010	STAT_PORT_RST [0].RST_PORT_MIB[0:0]	1
0xBB034010	STAT_PORT_RST [1].RST_PORT_MIB[1:1]	1
0xBB034010	STAT_PORT_RST [2].RST_PORT_MIB[2:2]	1
0xBB034010	STAT_PORT_RST [3].RST_PORT_MIB[3:3]	1
0xBB034010	STAT_PORT_RST [4].RST_PORT_MIB[4:4]	1
0xBB034010	STAT_PORT_RST [5].RST_PORT_MIB[5:5]	1
0xBB034010	STAT_PORT_RST [6].RST_PORT_MIB[6:6]	1
0xBB034014	STAT_RST.RESERVED[31:4]	28
0xBB034014	STAT_RST.RST_STAT[3:3]	1
0xBB034014	STAT_RST.RST_MIB_VAL[2:2]	1
0xBB034014	STAT_RST.RESERVED[1:1]	1
0xBB034014	STAT_RST.RST_GLOBAL_MIB[0:0]	1
0xBB034018	EPON_STAT_RST.RESERVED[31:7]	25
0xBB034018	EPON_STAT_RST.BUSY_STAT[6:6]	1
0xBB034018	EPON_STAT_RST.RST_CMD[5:5]	1
0xBB034018	EPON_STAT_RST.RST_LLID_IDX[4:2]	3
0xBB034018	EPON_STAT_RST.RST_LLID[1:1]	1
0xBB034018	EPON_STAT_RST.RST_ALL_MIB[0:0]	1
0xBB03401C	RGF_VER_MIB_CTRL.REGFILE_VER[31:0]	32
0xBB034020	RSVD_MIB_CTRL [0].RSVD_MEM[31:0]	32
0xBB034024	RSVD_MIB_CTRL [1].RSVD_MEM[31:0]	32
0xBB034028	RSVD_MIB_CTRL [2].RSVD_MEM[31:0]	32
0xBB03402C	RSVD_MIB_CTRL [3].RSVD_MEM[31:0]	32
0xBB034030	RSVD_MIB_CTRL [4].RSVD_MEM[31:0]	32
0xBB034034	RSVD_MIB_CTRL [5].RSVD_MEM[31:0]	32
0xBB034038	RSVD_MIB_CTRL [6].RSVD_MEM[31:0]	32
0xBB03403C	RSVD_MIB_CTRL [7].RSVD_MEM[31:0]	32
0xBB034040	RSVD_MIB_CTRL [8].RSVD_MEM[31:0]	32
0xBB034044	RSVD_MIB_CTRL [9].RSVD_MEM[31:0]	32
0xBB034048	RSVD_MIB_CTRL [10].RSVD_MEM[31:0]	32
0xBB03404C	RSVD_MIB_CTRL [11].RSVD_MEM[31:0]	32
0xBB034050	RSVD_MIB_CTRL [12].RSVD_MEM[31:0]	32
0xBB034054	RSVD_MIB_CTRL [13].RSVD_MEM[31:0]	32
0xBB034058	RSVD_MIB_CTRL [14].RSVD_MEM[31:0]	32
0xBB03405C	RSVD_MIB_CTRL [15].RSVD_MEM[31:0]	32
0xBB036000	EPON_FEC_CONFIG.RESERVED[31:16]	16
0xBB036000	EPON_FEC_CONFIG.BYPASS_FEC[15:15]	1
0xBB036000	EPON_FEC_CONFIG.DVSE_TPAR[14:14]	1
0xBB036000	EPON_FEC_CONFIG.DVS_TPAR[13:11]	3
0xBB036000	EPON_FEC_CONFIG.DVSE_DAT[10:10]	1
0xBB036000	EPON_FEC_CONFIG.DVS_DAT[9:7]	3



Address	Register	Len
0xBB036000	EPON_FEC_CONFIG.DVSE_RPAR[6:6]	1
0xBB036000	EPON_FEC_CONFIG.DVS_RPAR[5:3]	3
0xBB036000	EPON_FEC_CONFIG.FEC_RECOVER[2:2]	1
0xBB036000	EPON_FEC_CONFIG.FEC_US_EN[1:1]	1
0xBB036000	EPON_FEC_CONFIG.FEC_DS_EN[0:0]	1
0xBB036004	EPON_ASIC_TIMING_ADJUST1.RESERVED[31:24]	8
0xBB036004	EPON_ASIC_TIMING_ADJUST1.RPT_TMG[23:16]	8
0xBB036004	EPON_ASIC_TIMING_ADJUST1.REG_TMG[15:8]	8
0xBB036004	EPON_ASIC_TIMING_ADJUST1.QU_TMG[7:0]	8
0xBB036008	EPON_ASIC_TIMING_ADJUST2.RESERVED[31:25]	7
0xBB036008	EPON_ASIC_TIMING_ADJUST2.LSR_OFF_SHIFT[24:20]	5
0xBB036008	EPON_ASIC_TIMING_ADJUST2.LSR_ON_SHIFT[19:15]	5
0xBB036008	EPON_ASIC_TIMING_ADJUST2.ADJ_BC[14:0]	15
0xBB03600C	EPON_RGSTR1.RESERVED[31:20]	12
0xBB03600C	EPON_RGSTR1.HW_REGISTRATION[19:19]	1
0xBB03600C	EPON_RGSTR1.REG_LLID_IDX[18:16]	3
0xBB03600C	EPON_RGSTR1.REGISTER_MAC1[15:0]	16
0xBB036010	EPON_RGSTR2.REGISTER_MAC0[31:0]	32
0xBB036014	EPON_RGSTR3.RESERVED[31:9]	23
0xBB036014	EPON_RGSTR3.REG_PENDDING_GRANT[8:1]	8
0xBB036014	EPON_RGSTR3.REGISTER_REQUEST[0:0]	1
0xBB036018	EPON_DEBUG1.RESERVED[31:13]	19
0xBB036018	EPON_DEBUG1.MODE0_INVALID_HDL[12:12]	1
0xBB036018	EPON_DEBUG1.MODE1_INVALID_HDL[11:11]	1
0xBB036018	EPON_DEBUG1.INV_OE_CONTROL[10:10]	1
0xBB036018	EPON_DEBUG1.DBG_SEL[9:0]	10
0xBB03601C	EPON_DEBUG2.RESERVED[31:29]	3
0xBB03601C	EPON_DEBUG2.PR_B_GN[28:24]	5
0xBB03601C	EPON_DEBUG2.PR_B_EPMC[23:0]	24
0xBB036020	EPON_TIMER_CONFIG1.RESERVED[31:7]	25
0xBB036020	EPON_TIMER_CONFIG1.MPCP_TIMEOUT_VALUE[6:0]	7
0xBB036024	EPON_INTR.RESERVED[31:6]	26
0xBB036024	EPON_INTR.REG_LLID_TX_IMR[5:5]	1
0xBB036024	EPON_INTR.TIME_DRIFT_IMR[4:4]	1
0xBB036024	EPON_INTR.MPCP_TIMEOUT_IMR[3:3]	1
0xBB036024	EPON_INTR.REG_LLID_TX_IMS[2:2]	1
0xBB036024	EPON_INTR.TIME_DRIFT_IMS[1:1]	1
0xBB036024	EPON_INTR.MPCP_TIMEOUT_IMS[0:0]	1
0xBB036028	SYNC_TIME.NORMAL_SYNC_TIME[31:16]	16
0xBB036028	SYNC_TIME.DISC_SYNC_TIME[15:0]	16
0xBB03602C	LASER_ON_OFF_TIME.RESERVED[31:12]	20
0xBB03602C	LASER_ON_OFF_TIME.LASER_ON_TIME[11:6]	6
0xBB03602C	LASER_ON_OFF_TIME.LASER_OFF_TIME[5:0]	6
0xBB036030	MIN_GRANT_START.GRANT_STRAT_MIN[31:0]	32
0xBB036034	MAX_GRANT_START.GRANT_STRAT_MAX[31:0]	32
0xBB036038	EPON_TIME_CTRL.RESERVED[31:18]	14

Address	Register	Len
0xBB036038	EPON_TIME_CTRL.QUARD_THRESHOLD[17:16]	2
0xBB036038	EPON_TIME_CTRL.RTT_ADJ[15:0]	16
0xBB03603C	EP_MISC.RESERVED[31:6]	26
0xBB03603C	EP_MISC.SRT_GN[5:5]	1
0xBB03603C	EP_MISC.STOP_LOCAL_TIME[4:4]	1
0xBB03603C	EP_MISC.FEC_ENABLE[3:3]	1
0xBB03603C	EP_MISC.ALWAYS_SVY[2:2]	1
0xBB03603C	EP_MISC.POWER_SAVING_EN[1:1]	1
0xBB03603C	EP_MISC.POWER_SAVING_MODE[0:0]	1
0xBB036040	LLID_TABLE [0].RESERVED[31:23]	9
0xBB036040	LLID_TABLE [0].REPORT_TIMEOUT[22:22]	1
0xBB036040	LLID_TABLE [0].REPORT_TIMER[21:16]	6
0xBB036040	LLID_TABLE [0].VALID[15:15]	1
0xBB036040	LLID_TABLE [0].LLID[14:0]	15
0xBB036044	LLID_TABLE [1].RESERVED[31:23]	9
0xBB036044	LLID_TABLE [1].REPORT_TIMEOUT[22:22]	1
0xBB036044	LLID_TABLE [1].REPORT_TIMER[21:16]	6
0xBB036044	LLID_TABLE [1].VALID[15:15]	1
0xBB036044	LLID_TABLE [1].LLID[14:0]	15
0xBB036048	LLID_TABLE [2].RESERVED[31:23]	9
0xBB036048	LLID_TABLE [2].REPORT_TIMEOUT[22:22]	1
0xBB036048	LLID_TABLE [2].REPORT_TIMER[21:16]	6
0xBB036048	LLID_TABLE [2].VALID[15:15]	1
0xBB036048	LLID_TABLE [2].LLID[14:0]	15
0xBB03604C	LLID_TABLE [3].RESERVED[31:23]	9
0xBB03604C	LLID_TABLE [3].REPORT_TIMEOUT[22:22]	1
0xBB03604C	LLID_TABLE [3].REPORT_TIMER[21:16]	6
0xBB03604C	LLID_TABLE [3].VALID[15:15]	1
0xBB03604C	LLID_TABLE [3].LLID[14:0]	15
0xBB036050	LLID_TABLE [4].RESERVED[31:23]	9
0xBB036050	LLID_TABLE [4].REPORT_TIMEOUT[22:22]	1
0xBB036050	LLID_TABLE [4].REPORT_TIMER[21:16]	6
0xBB036050	LLID_TABLE [4].VALID[15:15]	1
0xBB036050	LLID_TABLE [4].LLID[14:0]	15
0xBB036054	LLID_TABLE [5].RESERVED[31:23]	9
0xBB036054	LLID_TABLE [5].REPORT_TIMEOUT[22:22]	1
0xBB036054	LLID_TABLE [5].REPORT_TIMER[21:16]	6
0xBB036054	LLID_TABLE [5].VALID[15:15]	1
0xBB036054	LLID_TABLE [5].LLID[14:0]	15
0xBB036058	LLID_TABLE [6].RESERVED[31:23]	9
0xBB036058	LLID_TABLE [6].REPORT_TIMEOUT[22:22]	1
0xBB036058	LLID_TABLE [6].REPORT_TIMER[21:16]	6
0xBB036058	LLID_TABLE [6].VALID[15:15]	1
0xBB036058	LLID_TABLE [6].LLID[14:0]	15
0xBB03605C	LLID_TABLE [7].RESERVED[31:23]	9
0xBB03605C	LLID_TABLE [7].REPORT_TIMEOUT[22:22]	1

Address	Register	Len
0xBB03605C	LLID_TABLE [7].REPORT_TIMER[21:16]	6
0xBB03605C	LLID_TABLE [7].VALID[15:15]	1
0xBB03605C	LLID_TABLE [7].LLID[14:0]	15
0xBB036060	EPON_MPCP_CTR.RESERVED[31:3]	29
0xBB036060	EPON_MPCP_CTR.OTHER_HANDLE[2:2]	1
0xBB036060	EPON_MPCP_CTR.GATE_HANDLE[1:1]	1
0xBB036060	EPON_MPCP_CTR.INVALID_LEN_HANDLE[0:0]	1
0xBB036064	EPON_GRANT_LIST0 [0].GRANT_START[31:0]	32
0xBB036068	EPON_GRANT_LIST0 [1].GRANT_START[31:0]	32
0xBB03606C	EPON_GRANT_LIST0 [2].GRANT_START[31:0]	32
0xBB036070	EPON_GRANT_LIST0 [3].GRANT_START[31:0]	32
0xBB036074	EPON_GRANT_LIST0 [4].GRANT_START[31:0]	32
0xBB036078	EPON_GRANT_LIST0 [5].GRANT_START[31:0]	32
0xBB03607C	EPON_GRANT_LIST0 [6].GRANT_START[31:0]	32
0xBB036080	EPON_GRANT_LIST0 [7].GRANT_START[31:0]	32
0xBB036084	EPON_GRANT_LIST0 [8].GRANT_START[31:0]	32
0xBB036088	EPON_GRANT_LIST0 [9].GRANT_START[31:0]	32
0xBB03608C	EPON_GRANT_LIST0 [10].GRANT_START[31:0]	32
0xBB036090	EPON_GRANT_LIST0 [11].GRANT_START[31:0]	32
0xBB036094	EPON_GRANT_LIST0 [12].GRANT_START[31:0]	32
0xBB036098	EPON_GRANT_LIST0 [13].GRANT_START[31:0]	32
0xBB03609C	EPON_GRANT_LIST0 [14].GRANT_START[31:0]	32
0xBB0360A0	EPON_GRANT_LIST0 [15].GRANT_START[31:0]	32
0xBB0360A4	EPON_GRANT_LIST0 [16].GRANT_START[31:0]	32
0xBB0360A8	EPON_GRANT_LIST0 [17].GRANT_START[31:0]	32
0xBB0360AC	EPON_GRANT_LIST0 [18].GRANT_START[31:0]	32
0xBB0360B0	EPON_GRANT_LIST0 [19].GRANT_START[31:0]	32
0xBB0360B4	EPON_GRANT_LIST0 [20].GRANT_START[31:0]	32
0xBB0360B8	EPON_GRANT_LIST0 [21].GRANT_START[31:0]	32
0xBB0360BC	EPON_GRANT_LIST0 [22].GRANT_START[31:0]	32
0xBB0360C0	EPON_GRANT_LIST0 [23].GRANT_START[31:0]	32
0xBB0360C4	EPON_GRANT_LIST0 [24].GRANT_START[31:0]	32
0xBB0360C8	EPON_GRANT_LIST0 [25].GRANT_START[31:0]	32
0xBB0360CC	EPON_GRANT_LIST0 [26].GRANT_START[31:0]	32
0xBB0360D0	EPON_GRANT_LIST0 [27].GRANT_START[31:0]	32
0xBB0360D4	EPON_GRANT_LIST0 [28].GRANT_START[31:0]	32
0xBB0360D8	EPON_GRANT_LIST0 [29].GRANT_START[31:0]	32
0xBB0360DC	EPON_GRANT_LIST0 [30].GRANT_START[31:0]	32
0xBB0360E0	EPON_GRANT_LIST0 [31].GRANT_START[31:0]	32
0xBB0360E4	EPON_GRANT_LIST1 [0].GRANT_END[31:0]	32
0xBB0360E8	EPON_GRANT_LIST1 [1].GRANT_END[31:0]	32
0xBB0360EC	EPON_GRANT_LIST1 [2].GRANT_END[31:0]	32
0xBB0360F0	EPON_GRANT_LIST1 [3].GRANT_END[31:0]	32
0xBB0360F4	EPON_GRANT_LIST1 [4].GRANT_END[31:0]	32
0xBB0360F8	EPON_GRANT_LIST1 [5].GRANT_END[31:0]	32
0xBB0360FC	EPON_GRANT_LIST1 [6].GRANT_END[31:0]	32

Address	Register	Len
0xBB036100	EPON_GRANT_LIST1 [7].GRANT_END[31:0]	32
0xBB036104	EPON_GRANT_LIST1 [8].GRANT_END[31:0]	32
0xBB036108	EPON_GRANT_LIST1 [9].GRANT_END[31:0]	32
0xBB03610C	EPON_GRANT_LIST1 [10].GRANT_END[31:0]	32
0xBB036110	EPON_GRANT_LIST1 [11].GRANT_END[31:0]	32
0xBB036114	EPON_GRANT_LIST1 [12].GRANT_END[31:0]	32
0xBB036118	EPON_GRANT_LIST1 [13].GRANT_END[31:0]	32
0xBB03611C	EPON_GRANT_LIST1 [14].GRANT_END[31:0]	32
0xBB036120	EPON_GRANT_LIST1 [15].GRANT_END[31:0]	32
0xBB036124	EPON_GRANT_LIST1 [16].GRANT_END[31:0]	32
0xBB036128	EPON_GRANT_LIST1 [17].GRANT_END[31:0]	32
0xBB03612C	EPON_GRANT_LIST1 [18].GRANT_END[31:0]	32
0xBB036130	EPON_GRANT_LIST1 [19].GRANT_END[31:0]	32
0xBB036134	EPON_GRANT_LIST1 [20].GRANT_END[31:0]	32
0xBB036138	EPON_GRANT_LIST1 [21].GRANT_END[31:0]	32
0xBB03613C	EPON_GRANT_LIST1 [22].GRANT_END[31:0]	32
0xBB036140	EPON_GRANT_LIST1 [23].GRANT_END[31:0]	32
0xBB036144	EPON_GRANT_LIST1 [24].GRANT_END[31:0]	32
0xBB036148	EPON_GRANT_LIST1 [25].GRANT_END[31:0]	32
0xBB03614C	EPON_GRANT_LIST1 [26].GRANT_END[31:0]	32
0xBB036150	EPON_GRANT_LIST1 [27].GRANT_END[31:0]	32
0xBB036154	EPON_GRANT_LIST1 [28].GRANT_END[31:0]	32
0xBB036158	EPON_GRANT_LIST1 [29].GRANT_END[31:0]	32
0xBB03615C	EPON_GRANT_LIST1 [30].GRANT_END[31:0]	32
0xBB036160	EPON_GRANT_LIST1 [31].GRANT_END[31:0]	32
0xBB036164	EPON_GRANT_LIST2 [0].RESERVED[31:5]	27
0xBB036164	EPON_GRANT_LIST2 [0].FORCE_REPORT[4:4]	1
0xBB036164	EPON_GRANT_LIST2 [0].DISC[3:3]	1
0xBB036164	EPON_GRANT_LIST2 [0].LLID_IDX[2:0]	3
0xBB036168	EPON_GRANT_LIST2 [1].RESERVED[31:5]	27
0xBB036168	EPON_GRANT_LIST2 [1].FORCE_REPORT[4:4]	1
0xBB036168	EPON_GRANT_LIST2 [1].DISC[3:3]	1
0xBB036168	EPON_GRANT_LIST2 [1].LLID_IDX[2:0]	3
0xBB03616C	EPON_GRANT_LIST2 [2].RESERVED[31:5]	27
0xBB03616C	EPON_GRANT_LIST2 [2].FORCE_REPORT[4:4]	1
0xBB03616C	EPON_GRANT_LIST2 [2].DISC[3:3]	1
0xBB03616C	EPON_GRANT_LIST2 [2].LLID_IDX[2:0]	3
0xBB036170	EPON_GRANT_LIST2 [3].RESERVED[31:5]	27
0xBB036170	EPON_GRANT_LIST2 [3].FORCE_REPORT[4:4]	1
0xBB036170	EPON_GRANT_LIST2 [3].DISC[3:3]	1
0xBB036170	EPON_GRANT_LIST2 [3].LLID_IDX[2:0]	3
0xBB036174	EPON_GRANT_LIST2 [4].RESERVED[31:5]	27
0xBB036174	EPON_GRANT_LIST2 [4].FORCE_REPORT[4:4]	1
0xBB036174	EPON_GRANT_LIST2 [4].DISC[3:3]	1
0xBB036174	EPON_GRANT_LIST2 [4].LLID_IDX[2:0]	3
0xBB036178	EPON_GRANT_LIST2 [5].RESERVED[31:5]	27

Address	Register	Len
0xBB036178	EPON_GRANT_LIST2 [5].FORCE_REPORT[4:4]	1
0xBB036178	EPON_GRANT_LIST2 [5].DISC[3:3]	1
0xBB036178	EPON_GRANT_LIST2 [5].LLID_IDX[2:0]	3
0xBB03617C	EPON_GRANT_LIST2 [6].RESERVED[31:5]	27
0xBB03617C	EPON_GRANT_LIST2 [6].FORCE_REPORT[4:4]	1
0xBB03617C	EPON_GRANT_LIST2 [6].DISC[3:3]	1
0xBB03617C	EPON_GRANT_LIST2 [6].LLID_IDX[2:0]	3
0xBB036180	EPON_GRANT_LIST2 [7].RESERVED[31:5]	27
0xBB036180	EPON_GRANT_LIST2 [7].FORCE_REPORT[4:4]	1
0xBB036180	EPON_GRANT_LIST2 [7].DISC[3:3]	1
0xBB036180	EPON_GRANT_LIST2 [7].LLID_IDX[2:0]	3
0xBB036184	EPON_GRANT_LIST2 [8].RESERVED[31:5]	27
0xBB036184	EPON_GRANT_LIST2 [8].FORCE_REPORT[4:4]	1
0xBB036184	EPON_GRANT_LIST2 [8].DISC[3:3]	1
0xBB036184	EPON_GRANT_LIST2 [8].LLID_IDX[2:0]	3
0xBB036188	EPON_GRANT_LIST2 [9].RESERVED[31:5]	27
0xBB036188	EPON_GRANT_LIST2 [9].FORCE_REPORT[4:4]	1
0xBB036188	EPON_GRANT_LIST2 [9].DISC[3:3]	1
0xBB036188	EPON_GRANT_LIST2 [9].LLID_IDX[2:0]	3
0xBB03618C	EPON_GRANT_LIST2 [10].RESERVED[31:5]	27
0xBB03618C	EPON_GRANT_LIST2 [10].FORCE_REPORT[4:4]	1
0xBB03618C	EPON_GRANT_LIST2 [10].DISC[3:3]	1
0xBB03618C	EPON_GRANT_LIST2 [10].LLID_IDX[2:0]	3
0xBB036190	EPON_GRANT_LIST2 [11].RESERVED[31:5]	27
0xBB036190	EPON_GRANT_LIST2 [11].FORCE_REPORT[4:4]	1
0xBB036190	EPON_GRANT_LIST2 [11].DISC[3:3]	1
0xBB036190	EPON_GRANT_LIST2 [11].LLID_IDX[2:0]	3
0xBB036194	EPON_GRANT_LIST2 [12].RESERVED[31:5]	27
0xBB036194	EPON_GRANT_LIST2 [12].FORCE_REPORT[4:4]	1
0xBB036194	EPON_GRANT_LIST2 [12].DISC[3:3]	1
0xBB036194	EPON_GRANT_LIST2 [12].LLID_IDX[2:0]	3
0xBB036198	EPON_GRANT_LIST2 [13].RESERVED[31:5]	27
0xBB036198	EPON_GRANT_LIST2 [13].FORCE_REPORT[4:4]	1
0xBB036198	EPON_GRANT_LIST2 [13].DISC[3:3]	1
0xBB036198	EPON_GRANT_LIST2 [13].LLID_IDX[2:0]	3
0xBB03619C	EPON_GRANT_LIST2 [14].RESERVED[31:5]	27
0xBB03619C	EPON_GRANT_LIST2 [14].FORCE_REPORT[4:4]	1
0xBB03619C	EPON_GRANT_LIST2 [14].DISC[3:3]	1
0xBB03619C	EPON_GRANT_LIST2 [14].LLID_IDX[2:0]	3
0xBB0361A0	EPON_GRANT_LIST2 [15].RESERVED[31:5]	27
0xBB0361A0	EPON_GRANT_LIST2 [15].FORCE_REPORT[4:4]	1
0xBB0361A0	EPON_GRANT_LIST2 [15].DISC[3:3]	1
0xBB0361A0	EPON_GRANT_LIST2 [15].LLID_IDX[2:0]	3
0xBB0361A4	EPON_GRANT_LIST2 [16].RESERVED[31:5]	27
0xBB0361A4	EPON_GRANT_LIST2 [16].FORCE_REPORT[4:4]	1
0xBB0361A4	EPON_GRANT_LIST2 [16].DISC[3:3]	1

Address	Register	Len
0xBB0361A4	EPON_GRANT_LIST2 [16].LLID_IDX[2:0]	3
0xBB0361A8	EPON_GRANT_LIST2 [17].RESERVED[31:5]	27
0xBB0361A8	EPON_GRANT_LIST2 [17].FORCE_REPORT[4:4]	1
0xBB0361A8	EPON_GRANT_LIST2 [17].DISC[3:3]	1
0xBB0361A8	EPON_GRANT_LIST2 [17].LLID_IDX[2:0]	3
0xBB0361AC	EPON_GRANT_LIST2 [18].RESERVED[31:5]	27
0xBB0361AC	EPON_GRANT_LIST2 [18].FORCE_REPORT[4:4]	1
0xBB0361AC	EPON_GRANT_LIST2 [18].DISC[3:3]	1
0xBB0361AC	EPON_GRANT_LIST2 [18].LLID_IDX[2:0]	3
0xBB0361B0	EPON_GRANT_LIST2 [19].RESERVED[31:5]	27
0xBB0361B0	EPON_GRANT_LIST2 [19].FORCE_REPORT[4:4]	1
0xBB0361B0	EPON_GRANT_LIST2 [19].DISC[3:3]	1
0xBB0361B0	EPON_GRANT_LIST2 [19].LLID_IDX[2:0]	3
0xBB0361B4	EPON_GRANT_LIST2 [20].RESERVED[31:5]	27
0xBB0361B4	EPON_GRANT_LIST2 [20].FORCE_REPORT[4:4]	1
0xBB0361B4	EPON_GRANT_LIST2 [20].DISC[3:3]	1
0xBB0361B4	EPON_GRANT_LIST2 [20].LLID_IDX[2:0]	3
0xBB0361B8	EPON_GRANT_LIST2 [21].RESERVED[31:5]	27
0xBB0361B8	EPON_GRANT_LIST2 [21].FORCE_REPORT[4:4]	1
0xBB0361B8	EPON_GRANT_LIST2 [21].DISC[3:3]	1
0xBB0361B8	EPON_GRANT_LIST2 [21].LLID_IDX[2:0]	3
0xBB0361BC	EPON_GRANT_LIST2 [22].RESERVED[31:5]	27
0xBB0361BC	EPON_GRANT_LIST2 [22].FORCE_REPORT[4:4]	1
0xBB0361BC	EPON_GRANT_LIST2 [22].DISC[3:3]	1
0xBB0361BC	EPON_GRANT_LIST2 [22].LLID_IDX[2:0]	3
0xBB0361C0	EPON_GRANT_LIST2 [23].RESERVED[31:5]	27
0xBB0361C0	EPON_GRANT_LIST2 [23].FORCE_REPORT[4:4]	1
0xBB0361C0	EPON_GRANT_LIST2 [23].DISC[3:3]	1
0xBB0361C0	EPON_GRANT_LIST2 [23].LLID_IDX[2:0]	3
0xBB0361C4	EPON_GRANT_LIST2 [24].RESERVED[31:5]	27
0xBB0361C4	EPON_GRANT_LIST2 [24].FORCE_REPORT[4:4]	1
0xBB0361C4	EPON_GRANT_LIST2 [24].DISC[3:3]	1
0xBB0361C4	EPON_GRANT_LIST2 [24].LLID_IDX[2:0]	3
0xBB0361C8	EPON_GRANT_LIST2 [25].RESERVED[31:5]	27
0xBB0361C8	EPON_GRANT_LIST2 [25].FORCE_REPORT[4:4]	1
0xBB0361C8	EPON_GRANT_LIST2 [25].DISC[3:3]	1
0xBB0361C8	EPON_GRANT_LIST2 [25].LLID_IDX[2:0]	3
0xBB0361CC	EPON_GRANT_LIST2 [26].RESERVED[31:5]	27
0xBB0361CC	EPON_GRANT_LIST2 [26].FORCE_REPORT[4:4]	1
0xBB0361CC	EPON_GRANT_LIST2 [26].DISC[3:3]	1
0xBB0361CC	EPON_GRANT_LIST2 [26].LLID_IDX[2:0]	3
0xBB0361D0	EPON_GRANT_LIST2 [27].RESERVED[31:5]	27
0xBB0361D0	EPON_GRANT_LIST2 [27].FORCE_REPORT[4:4]	1
0xBB0361D0	EPON_GRANT_LIST2 [27].DISC[3:3]	1
0xBB0361D0	EPON_GRANT_LIST2 [27].LLID_IDX[2:0]	3
0xBB0361D4	EPON_GRANT_LIST2 [28].RESERVED[31:5]	27

Address	Register	Len
0xBB0361D4	EPON_GRANT_LIST2 [28].FORCE_REPORT[4:4]	1
0xBB0361D4	EPON_GRANT_LIST2 [28].DISC[3:3]	1
0xBB0361D4	EPON_GRANT_LIST2 [28].LLID_IDX[2:0]	3
0xBB0361D8	EPON_GRANT_LIST2 [29].RESERVED[31:5]	27
0xBB0361D8	EPON_GRANT_LIST2 [29].FORCE_REPORT[4:4]	1
0xBB0361D8	EPON_GRANT_LIST2 [29].DISC[3:3]	1
0xBB0361D8	EPON_GRANT_LIST2 [29].LLID_IDX[2:0]	3
0xBB0361DC	EPON_GRANT_LIST2 [30].RESERVED[31:5]	27
0xBB0361DC	EPON_GRANT_LIST2 [30].FORCE_REPORT[4:4]	1
0xBB0361DC	EPON_GRANT_LIST2 [30].DISC[3:3]	1
0xBB0361DC	EPON_GRANT_LIST2 [30].LLID_IDX[2:0]	3
0xBB0361E0	EPON_GRANT_LIST2 [31].RESERVED[31:5]	27
0xBB0361E0	EPON_GRANT_LIST2 [31].FORCE_REPORT[4:4]	1
0xBB0361E0	EPON_GRANT_LIST2 [31].DISC[3:3]	1
0xBB0361E0	EPON_GRANT_LIST2 [31].LLID_IDX[2:0]	3
0xBB0361E4	EPON_TX_CTRL.RESERVED[31:3]	29
0xBB0361E4	EPON_TX_CTRL.LLID_IDX[2:0]	3
0xBB0361E8	RGF_VER_EPON_CTRL.REGFILE_VER[31:0]	32
0xBB0361EC	RSVD_EPON_CTRL [0].RSVD_MEM[31:0]	32
0xBB0361F0	RSVD_EPON_CTRL [1].RSVD_MEM[31:0]	32
0xBB0361F4	RSVD_EPON_CTRL [2].RSVD_MEM[31:0]	32
0xBB0361F8	RSVD_EPON_CTRL [3].RSVD_MEM[31:0]	32
0xBB0361FC	RSVD_EPON_CTRL [4].RSVD_MEM[31:0]	32
0xBB036200	RSVD_EPON_CTRL [5].RSVD_MEM[31:0]	32
0xBB036204	RSVD_EPON_CTRL [6].RSVD_MEM[31:0]	32
0xBB036208	RSVD_EPON_CTRL [7].RSVD_MEM[31:0]	32
0xBB03620C	RSVD_EPON_CTRL [8].RSVD_MEM[31:0]	32
0xBB036210	RSVD_EPON_CTRL [9].RSVD_MEM[31:0]	32
0xBB036214	RSVD_EPON_CTRL [10].RSVD_MEM[31:0]	32
0xBB036218	RSVD_EPON_CTRL [11].RSVD_MEM[31:0]	32
0xBB03621C	RSVD_EPON_CTRL [12].RSVD_MEM[31:0]	32
0xBB036220	RSVD_EPON_CTRL [13].RSVD_MEM[31:0]	32
0xBB036224	RSVD_EPON_CTRL [14].RSVD_MEM[31:0]	32
0xBB036228	RSVD_EPON_CTRL [15].RSVD_MEM[31:0]	32
0xBB03622C	EPON_DECRYPT_CFG.RESERVED[31:2]	30
0xBB03622C	EPON_DECRYPT_CFG.EPON_DECRYPT[1:0]	2
0xBB036230	EPON_DECRYPT_KEY0 [0].EPON_DECRYPT_KEY0[23:0]	24
0xBB036234	EPON_DECRYPT_KEY0 [1].EPON_DECRYPT_KEY0[23:0]	24
0xBB036238	EPON_DECRYPT_KEY0 [2].EPON_DECRYPT_KEY0[23:0]	24
0xBB03623C	EPON_DECRYPT_KEY0 [3].EPON_DECRYPT_KEY0[23:0]	24
0xBB036240	EPON_DECRYPT_KEY0 [4].EPON_DECRYPT_KEY0[23:0]	24
0xBB036244	EPON_DECRYPT_KEY0 [5].EPON_DECRYPT_KEY0[23:0]	24
0xBB036248	EPON_DECRYPT_KEY0 [6].EPON_DECRYPT_KEY0[23:0]	24
0xBB03624C	EPON_DECRYPT_KEY0 [7].EPON_DECRYPT_KEY0[23:0]	24
0xBB036250	EPON_DECRYPT_KEY1 [0].EPON_DECRYPT_KEY1[23:0]	24
0xBB036254	EPON_DECRYPT_KEY1 [1].EPON_DECRYPT_KEY1[23:0]	24



Address	Register	Len
0xBB036258	EPON_DECRYPT_KEY1 [2].EPON_DECRYPT_KEY1[23:0]	24
0xBB03625C	EPON_DECRYPT_KEY1 [3].EPON_DECRYPT_KEY1[23:0]	24
0xBB036260	EPON_DECRYPT_KEY1 [4].EPON_DECRYPT_KEY1[23:0]	24
0xBB036264	EPON_DECRYPT_KEY1 [5].EPON_DECRYPT_KEY1[23:0]	24
0xBB036268	EPON_DECRYPT_KEY1 [6].EPON_DECRYPT_KEY1[23:0]	24
0xBB03626C	EPON_DECRYPT_KEY1 [7].EPON_DECRYPT_KEY1[23:0]	24
0xBB036270	EPON_MISC_CFG.RESERVED[31:2]	30
0xBB036270	EPON_MISC_CFG.GMII_RXER_EN[1:1]	1
0xBB036270	EPON_MISC_CFG.PRB_LST_GN[0:0]	1
0xBB700000	GPON_INT_DLT.RESERVED[31:16]	16
0xBB700000	GPON_INT_DLT.GPON_IRQ[15:15]	1
0xBB700000	GPON_INT_DLT.RESERVED[14:0]	15
0xBB70000C	GPON_RESET.RESERVED[31:9]	23
0xBB70000C	GPON_RESET.RST_DONE[8:8]	1
0xBB70000C	GPON_RESET.RESERVED[7:1]	7
0xBB70000C	GPON_RESET.SOFT_RST[0:0]	1
0xBB700010	GPON_VERSION.VER_ID[31:0]	32
0xBB700014	GPON_TEST.TEST_REG[31:0]	32
0xBB700020	GPON_AES_BYPASS.RESERVED[31:1]	31
0xBB700020	GPON_AES_BYPASS.M_BYPASS_AES_MOD[0:0]	1
0xBB700040	GPON_INTR_MASK.RESERVED[31:11]	21
0xBB700040	GPON_INTR_MASK.GEM_US_M[10:10]	1
0xBB700040	GPON_INTR_MASK.RESERVED[9:9]	1
0xBB700040	GPON_INTR_MASK.GTC_US_M[8:8]	1
0xBB700040	GPON_INTR_MASK.RESERVED[7:5]	3
0xBB700040	GPON_INTR_MASK.GEM_DS_M[4:4]	1
0xBB700040	GPON_INTR_MASK.AES_DECRYPT_M[3:3]	1
0xBB700040	GPON_INTR_MASK.GTC_DS_CAP_M[2:2]	1
0xBB700040	GPON_INTR_MASK.GTC_DS_M[1:1]	1
0xBB700040	GPON_INTR_MASK.RESERVED[0:0]	1
0xBB700044	GPON_INTR_STS.RESERVED[31:11]	21
0xBB700044	GPON_INTR_STS.GEM_US_INTR[10:10]	1
0xBB700044	GPON_INTR_STS.RESERVED[9:9]	1
0xBB700044	GPON_INTR_STS.GTC_US_INTR[8:8]	1
0xBB700044	GPON_INTR_STS.RESERVED[7:5]	3
0xBB700044	GPON_INTR_STS.GEM_DS_INTR[4:4]	1
0xBB700044	GPON_INTR_STS.AES_DECRYPT_INTR[3:3]	1
0xBB700044	GPON_INTR_STS.GTC_DS_CAP_INTR[2:2]	1
0xBB700044	GPON_INTR_STS.GTC_DS_INTR[1:1]	1
0xBB700044	GPON_INTR_STS.RESERVED[0:0]	1
0xBB701000	GPON_GTC_DS_INTR_DLT.RESERVED[31:16]	16
0xBB701000	GPON_GTC_DS_INTR_DLT.GTC_DS_INTR[15:15]	1
0xBB701000	GPON_GTC_DS_INTR_DLT.RESERVED[14:11]	4
0xBB701000	GPON_GTC_DS_INTR_DLT.PLM_BUF_REQ[10:10]	1
0xBB701000	GPON_GTC_DS_INTR_DLT.RNG_REQ_HIS[9:9]	1
0xBB701000	GPON_GTC_DS_INTR_DLT.SN_REQ_HIS[8:8]	1



Address	Register	Len
0xBB701000	GPON_GTC_DS_INTR_DLT.RESERVED[7:4]	4
0xBB701000	GPON_GTC_DS_INTR_DLT.LOM_DLT[3:3]	1
0xBB701000	GPON_GTC_DS_INTR_DLT.DS_FEC_STA_DLT[2:2]	1
0xBB701000	GPON_GTC_DS_INTR_DLT.LOF_DLT[1:1]	1
0xBB701000	GPON_GTC_DS_INTR_DLT.LOS_DLT[0:0]	1
0xBB701004	GPON_GTC_DS_INTR_MASK.RESERVED[31:11]	21
0xBB701004	GPON_GTC_DS_INTR_MASK.PLM_BUF_M[10:10]	1
0xBB701004	GPON_GTC_DS_INTR_MASK.RNG_REQ_M[9:9]	1
0xBB701004	GPON_GTC_DS_INTR_MASK.SN_REQ_M[8:8]	1
0xBB701004	GPON_GTC_DS_INTR_MASK.RESERVED[7:4]	4
0xBB701004	GPON_GTC_DS_INTR_MASK.LOM_M[3:3]	1
0xBB701004	GPON_GTC_DS_INTR_MASK.DS_FEC_STA_M[2:2]	1
0xBB701004	GPON_GTC_DS_INTR_MASK.LOF_M[1:1]	1
0xBB701004	GPON_GTC_DS_INTR_MASK.LOS_M[0:0]	1
0xBB701008	GPON_GTC_DS_INTR_STS.RESERVED[31:4]	28
0xBB701008	GPON_GTC_DS_INTR_STS.LOM[3:3]	1
0xBB701008	GPON_GTC_DS_INTR_STS.DS_FEC_STS[2:2]	1
0xBB701008	GPON_GTC_DS_INTR_STS.LOF[1:1]	1
0xBB701008	GPON_GTC_DS_INTR_STS.LOS[0:0]	1
0xBB701010	GPON_GTC_DS_ONU_ID_STATUS.RESERVED[31:16]	16
0xBB701010	GPON_GTC_DS_ONU_ID_STATUS.ONU_ID[15:8]	8
0xBB701010	GPON_GTC_DS_ONU_ID_STATUS.RESERVED[7:4]	4
0xBB701010	GPON_GTC_DS_ONU_ID_STATUS.ONU_STATE[3:0]	4
0xBB701014	GPON_GTC_DS_CFG.RESERVED[31:11]	21
0xBB701014	GPON_GTC_DS_CFG.BWM_FILT_ONUID[10:10]	1
0xBB701014	GPON_GTC_DS_CFG.CHK_BWM_CRC[9:9]	1
0xBB701014	GPON_GTC_DS_CFG.PLEND_STRICT_MODE[8:8]	1
0xBB701014	GPON_GTC_DS_CFG.EXTRA_SN_TX[7:6]	2
0xBB701014	GPON_GTC_DS_CFG.RESERVED[5:5]	1
0xBB701014	GPON_GTC_DS_CFG.FEC_CORRECT_DIS[4:4]	1
0xBB701014	GPON_GTC_DS_CFG.FEC_DET_THRSH[3:1]	3
0xBB701014	GPON_GTC_DS_CFG.DESCRAM_DIS[0:0]	1
0xBB70101C	GPON_GTC_DS_PLOAM_CFG.RESERVED[31:11]	21
0xBB70101C	GPON_GTC_DS_PLOAM_CFG.PLM_DROP_CRCE[10:10]	1
0xBB70101C	GPON_GTC_DS_PLOAM_CFG.PLM_BC_ACC_EN[9:9]	1
0xBB70101C	GPON_GTC_DS_PLOAM_CFG.PLM_DS_ONUID_FLT_EN[8:8]	1
0xBB70101C	GPON_GTC_DS_PLOAM_CFG.PLM_DS_NOMSG_ID[7:0]	8
0xBB701040	GPON_GTC_DS_LOS_CFG_STS.RESERVED[31:11]	21
0xBB701040	GPON_GTC_DS_LOS_CFG_STS.CDR_LOS_SIG[10:10]	1
0xBB701040	GPON_GTC_DS_LOS_CFG_STS.RESERVED[9:9]	1
0xBB701040	GPON_GTC_DS_LOS_CFG_STS.OPTIC_LOS_SIG[8:8]	1
0xBB701040	GPON_GTC_DS_LOS_CFG_STS.RESERVED[7:5]	3
0xBB701040	GPON_GTC_DS_LOS_CFG_STS.LOS_FILTER_EN[4:4]	1
0xBB701040	GPON_GTC_DS_LOS_CFG_STS.CDR_LOS_POLAR[3:3]	1
0xBB701040	GPON_GTC_DS_LOS_CFG_STS.CDR_LOS_EN[2:2]	1
0xBB701040	GPON_GTC_DS_LOS_CFG_STS.OPTIC_LOS_POLAR[1:1]	1

Address	Register	Len
0xBB701040	GPON_GTC_DS_LOS_CFG_STS.OPTIC_LOS_EN[0:0]	1
0xBB701048	GPON_GTC_DS_SUPERFRAME_CNT.RESERVED[31:30]	2
0xBB701048	GPON_GTC_DS_SUPERFRAME_CNT.SF_CNTR[29:0]	30
0xBB701080	GPON_GTC_DS_PLOAM_IND.RESERVED[31:6]	26
0xBB701080	GPON_GTC_DS_PLOAM_IND.PLM_BUF_EMPTY[5:5]	1
0xBB701080	GPON_GTC_DS_PLOAM_IND.PLM_BUF_FULL[4:4]	1
0xBB701080	GPON_GTC_DS_PLOAM_IND.RESERVED[3:1]	3
0xBB701080	GPON_GTC_DS_PLOAM_IND.PLM_DEQ[0:0]	1
0xBB7010A0	GPON_GTC_DS_PLOAM_MSG [0].RESERVED[31:16]	16
0xBB7010A0	GPON_GTC_DS_PLOAM_MSG [0].PLOAM_RDATA[15:0]	16
0xBB7010A4	GPON_GTC_DS_PLOAM_MSG [1].RESERVED[31:16]	16
0xBB7010A4	GPON_GTC_DS_PLOAM_MSG [1].PLOAM_RDATA[15:0]	16
0xBB7010A8	GPON_GTC_DS_PLOAM_MSG [2].RESERVED[31:16]	16
0xBB7010A8	GPON_GTC_DS_PLOAM_MSG [2].PLOAM_RDATA[15:0]	16
0xBB7010AC	GPON_GTC_DS_PLOAM_MSG [3].RESERVED[31:16]	16
0xBB7010AC	GPON_GTC_DS_PLOAM_MSG [3].PLOAM_RDATA[15:0]	16
0xBB7010B0	GPON_GTC_DS_PLOAM_MSG [4].RESERVED[31:16]	16
0xBB7010B0	GPON_GTC_DS_PLOAM_MSG [4].PLOAM_RDATA[15:0]	16
0xBB7010B4	GPON_GTC_DS_PLOAM_MSG [5].RESERVED[31:16]	16
0xBB7010B4	GPON_GTC_DS_PLOAM_MSG [5].PLOAM_RDATA[15:0]	16
0xBB7010B8	GPON_GTC_DS_PLOAM_MSG [6].RESERVED[31:16]	16
0xBB7010B8	GPON_GTC_DS_PLOAM_MSG [6].PLOAM_RDATA[15:0]	16
0xBB7010BC	GPON_GTC_DS_PLOAM_MSG [7].RESERVED[31:16]	16
0xBB7010BC	GPON_GTC_DS_PLOAM_MSG [7].PLOAM_RDATA[15:0]	16
0xBB7010C0	GPON_GTC_DS_ALLOC_IND.RESERVED[31:16]	16
0xBB7010C0	GPON_GTC_DS_ALLOC_IND.ALLOCID_OP_REQ[15:15]	1
0xBB7010C0	GPON_GTC_DS_ALLOC_IND.ALLOCID_OP_COMPL[14:14]	1
0xBB7010C0	GPON_GTC_DS_ALLOC_IND.ALLOCID_OP_HIT[13:13]	1
0xBB7010C0	GPON_GTC_DS_ALLOC_IND.RESERVED[12:10]	3
0xBB7010C0	GPON_GTC_DS_ALLOC_IND.ALLOCID_OP_MODE[9:8]	2
0xBB7010C0	GPON_GTC_DS_ALLOC_IND.RESERVED[7:5]	3
0xBB7010C0	GPON_GTC_DS_ALLOC_IND.ALLOCID_OP_IDX[4:0]	5
0xBB7010C4	GPON_GTC_DS_ALLOC_WR.RESERVED[31:12]	20
0xBB7010C4	GPON_GTC_DS_ALLOC_WR.ALLOCID_OP_WDATA[11:0]	12
0xBB7010CC	GPON_GTC_DS_ALLOC_RD.RESERVED[31:12]	20
0xBB7010CC	GPON_GTC_DS_ALLOC_RD.ALLOCID_OP_RDATA[11:0]	12
0xBB701100	GPON_GTC_DS_PORT_IND.RESERVED[31:16]	16
0xBB701100	GPON_GTC_DS_PORT_IND.PORTID_OP_REQ[15:15]	1
0xBB701100	GPON_GTC_DS_PORT_IND.PORTID_OP_COMPL[14:14]	1
0xBB701100	GPON_GTC_DS_PORT_IND.PORTID_OP_HIT[13:13]	1
0xBB701100	GPON_GTC_DS_PORT_IND.RESERVED[12:10]	3
0xBB701100	GPON_GTC_DS_PORT_IND.PORTID_OP_MODE[9:8]	2
0xBB701100	GPON_GTC_DS_PORT_IND.RESERVED[7:7]	1
0xBB701100	GPON_GTC_DS_PORT_IND.PORTID_OP_IDX[6:0]	7
0xBB701104	GPON_GTC_DS_PORT_WR.RESERVED[31:12]	20
0xBB701104	GPON_GTC_DS_PORT_WR.PORTID_OP_WDATA[11:0]	12

Address	Register	Len
0xBB70110C	GPON_GTC_DS_PORT_RD.RESERVED[31:12]	20
0xBB70110C	GPON_GTC_DS_PORT_RD.PORTID_OP_RDATA[11:0]	12
0xBB701140	GPON_GTC_DS_PORT_CNTR_IND.RESERVED[31:16]	16
0xBB701140	GPON_GTC_DS_PORT_CNTR_IND.GEM_CNTR_R_ACK[15:15]	1
0xBB701140	GPON_GTC_DS_PORT_CNTR_IND.RESERVED[14:9]	6
0xBB701140	GPON_GTC_DS_PORT_CNTR_IND.GEM_CNTR_RSEL[8:8]	1
0xBB701140	GPON_GTC_DS_PORT_CNTR_IND.RESERVED[7:7]	1
0xBB701140	GPON_GTC_DS_PORT_CNTR_IND.GEM_CNTR_IDX[6:0]	7
0xBB701144	GPON_GTC_DS_PORT_CNTR_STAT.GEM_CNTR[31:0]	32
0xBB701184	GPON_GTC_DS_MISC_CNTR_BIP_ERR_BLK.CNTR_DS_BIP_ERR_BLOCK[31:0]	32
0xBB701188	GPON_GTC_DS_MISC_CNTR_BIP_ERR_BIT.CNTR_DS_BIP_ERR_BITS[31:0]	32
0xBB70118C	GPON_GTC_DS_MISC_CNTR_FEC_CORRECT_BIT.CNTR_FEC_CORRECTED_BITS[31:0]	32
0xBB701190	GPON_GTC_DS_MISC_CNTR_FEC_CORRECT_BYTE.CNTR_FEC_CORRECTED_BYTES[31:0]	32
0xBB701194	GPON_GTC_DS_MISC_CNTR_FEC_CORRECT_CW.CNTR_FEC_CORRECTED_CW[31:0]	32
0xBB701198	GPON_GTC_DS_MISC_CNTR_FEC_UNCOR_CW.CNTR_FEC_UNCORRECTABLE_CW[31:0]	32
0xBB70119C	GPON_GTC_DS_MISC_CNTR_LOM.CNTR_PLEND_FAIL[31:16]	16
0xBB70119C	GPON_GTC_DS_MISC_CNTR_LOM.CNTR_SUPERFRAME_LOS[15:0]	16
0xBB7011A0	GPON_GTC_DS_MISC_CNTR_PLOAM_ACPT.CNTR_PLOAMD_ACCEPTED[31:0]	32
0xBB7011A4	GPON_GTC_DS_MISC_CNTR_PLOAM_FAIL.CNTR_PLOAMD_OVERFLOW[31:16]	16
0xBB7011A4	GPON_GTC_DS_MISC_CNTR_PLOAM_FAIL.CNTR_PLOAMD_CRC_ERR[15:0]	16
0xBB7011A8	GPON_GTC_DS_MISC_CNTR_BWM_FAIL.CNTR_BWMAP_OVERFLOW[31:16]	16
0xBB7011A8	GPON_GTC_DS_MISC_CNTR_BWM_FAIL.CNTR_BWMAP_CRC_ERR[15:0]	16
0xBB7011AC	GPON_GTC_DS_MISC_CNTR_BWM_INV.CNTR_BWMAP_INV1[31:16]	16
0xBB7011AC	GPON_GTC_DS_MISC_CNTR_BWM_INV.CNTR_BWMAP_INV0[15:0]	16
0xBB7011B0	GPON_GTC_DS_MISC_CNTR_ACTIVE.CNTR_RANGING_REQ[31:16]	16
0xBB7011B0	GPON_GTC_DS_MISC_CNTR_ACTIVE.CNTR_SN_REQ[15:0]	16
0xBB7011B4	GPON_GTC_DS_MISC_CNTR_BWM_ACPT.CNTR_BWMAP_ACCEPTED[31:0]	32
0xBB7011B8	GPON_GTC_DS_MISC_CNTR_GEM_LOS.CNTR_GEM_LOS[31:0]	32
0xBB7011BC	GPON_GTC_DS_MISC_CNTR_HEC_CORRECT.CNTR_HEC_CORRECTED[31:0]	32
0xBB7011C0	GPON_GTC_DS_MISC_CNTR_GEM_IDLE.CNTR_GEM_IDLE[31:0]	32
0xBB7011C4	GPON_GTC_DS_MISC_CNTR_GEM_FAIL.CNTR_PORTID_MMATCH[31:16]	16
0xBB7011C4	GPON_GTC_DS_MISC_CNTR_GEM_FAIL.CNTR_GEM_LEN_MISM[15:0]	16
0xBB7011C8	GPON_GTC_DS_MISC_CNTR_GEM_NON_IDLE.CNTR_RX_GEM_NON_IDLE[31:0]	32
0xBB7011CC	GPON_GTC_DS_MISC_CNTR_PLEN_CORRECT.CNTR_PLEND_CORRECTIONS[31:0]	32
0xBB701204	GPON_GTC_DS_OMCI_PTI.RESERVED[31:7]	25
0xBB701204	GPON_GTC_DS_OMCI_PTI.OMCI_PTI_MASK[6:4]	3
0xBB701204	GPON_GTC_DS_OMCI_PTI.RESERVED[3:3]	1
0xBB701204	GPON_GTC_DS_OMCI_PTI.OMCI_END_PTI[2:0]	3
0xBB701208	GPON_GTC_DS_ETH_PTI.RESERVED[31:7]	25
0xBB701208	GPON_GTC_DS_ETH_PTI.ETH_PTI_MASK[6:4]	3
0xBB701208	GPON_GTC_DS_ETH_PTI.RESERVED[3:3]	1
0xBB701208	GPON_GTC_DS_ETH_PTI.ETH_END_PTI[2:0]	3
0xBB701400	GPON_GTC_DS_TRAFFIC_CFG [0].RESERVED[31:5]	27
0xBB701400	GPON_GTC_DS_TRAFFIC_CFG [0].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701404	GPON_GTC_DS_TRAFFIC_CFG [1].RESERVED[31:5]	27
0xBB701404	GPON_GTC_DS_TRAFFIC_CFG [1].TRAFFIC_TYPE_CFG[4:0]	5

Address	Register	Len
0xBB701408	GPON_GTC_DS_TRAFFIC_CFG [2].RESERVED[31:5]	27
0xBB701408	GPON_GTC_DS_TRAFFIC_CFG [2].TRAFFIC_TYPE_CFG[4:0]	5
0xBB70140C	GPON_GTC_DS_TRAFFIC_CFG [3].RESERVED[31:5]	27
0xBB70140C	GPON_GTC_DS_TRAFFIC_CFG [3].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701410	GPON_GTC_DS_TRAFFIC_CFG [4].RESERVED[31:5]	27
0xBB701410	GPON_GTC_DS_TRAFFIC_CFG [4].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701414	GPON_GTC_DS_TRAFFIC_CFG [5].RESERVED[31:5]	27
0xBB701414	GPON_GTC_DS_TRAFFIC_CFG [5].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701418	GPON_GTC_DS_TRAFFIC_CFG [6].RESERVED[31:5]	27
0xBB701418	GPON_GTC_DS_TRAFFIC_CFG [6].TRAFFIC_TYPE_CFG[4:0]	5
0xBB70141C	GPON_GTC_DS_TRAFFIC_CFG [7].RESERVED[31:5]	27
0xBB70141C	GPON_GTC_DS_TRAFFIC_CFG [7].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701420	GPON_GTC_DS_TRAFFIC_CFG [8].RESERVED[31:5]	27
0xBB701420	GPON_GTC_DS_TRAFFIC_CFG [8].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701424	GPON_GTC_DS_TRAFFIC_CFG [9].RESERVED[31:5]	27
0xBB701424	GPON_GTC_DS_TRAFFIC_CFG [9].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701428	GPON_GTC_DS_TRAFFIC_CFG [10].RESERVED[31:5]	27
0xBB701428	GPON_GTC_DS_TRAFFIC_CFG [10].TRAFFIC_TYPE_CFG[4:0]	5
0xBB70142C	GPON_GTC_DS_TRAFFIC_CFG [11].RESERVED[31:5]	27
0xBB70142C	GPON_GTC_DS_TRAFFIC_CFG [11].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701430	GPON_GTC_DS_TRAFFIC_CFG [12].RESERVED[31:5]	27
0xBB701430	GPON_GTC_DS_TRAFFIC_CFG [12].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701434	GPON_GTC_DS_TRAFFIC_CFG [13].RESERVED[31:5]	27
0xBB701434	GPON_GTC_DS_TRAFFIC_CFG [13].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701438	GPON_GTC_DS_TRAFFIC_CFG [14].RESERVED[31:5]	27
0xBB701438	GPON_GTC_DS_TRAFFIC_CFG [14].TRAFFIC_TYPE_CFG[4:0]	5
0xBB70143C	GPON_GTC_DS_TRAFFIC_CFG [15].RESERVED[31:5]	27
0xBB70143C	GPON_GTC_DS_TRAFFIC_CFG [15].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701440	GPON_GTC_DS_TRAFFIC_CFG [16].RESERVED[31:5]	27
0xBB701440	GPON_GTC_DS_TRAFFIC_CFG [16].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701444	GPON_GTC_DS_TRAFFIC_CFG [17].RESERVED[31:5]	27
0xBB701444	GPON_GTC_DS_TRAFFIC_CFG [17].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701448	GPON_GTC_DS_TRAFFIC_CFG [18].RESERVED[31:5]	27
0xBB701448	GPON_GTC_DS_TRAFFIC_CFG [18].TRAFFIC_TYPE_CFG[4:0]	5
0xBB70144C	GPON_GTC_DS_TRAFFIC_CFG [19].RESERVED[31:5]	27
0xBB70144C	GPON_GTC_DS_TRAFFIC_CFG [19].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701450	GPON_GTC_DS_TRAFFIC_CFG [20].RESERVED[31:5]	27
0xBB701450	GPON_GTC_DS_TRAFFIC_CFG [20].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701454	GPON_GTC_DS_TRAFFIC_CFG [21].RESERVED[31:5]	27
0xBB701454	GPON_GTC_DS_TRAFFIC_CFG [21].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701458	GPON_GTC_DS_TRAFFIC_CFG [22].RESERVED[31:5]	27
0xBB701458	GPON_GTC_DS_TRAFFIC_CFG [22].TRAFFIC_TYPE_CFG[4:0]	5
0xBB70145C	GPON_GTC_DS_TRAFFIC_CFG [23].RESERVED[31:5]	27
0xBB70145C	GPON_GTC_DS_TRAFFIC_CFG [23].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701460	GPON_GTC_DS_TRAFFIC_CFG [24].RESERVED[31:5]	27
0xBB701460	GPON_GTC_DS_TRAFFIC_CFG [24].TRAFFIC_TYPE_CFG[4:0]	5

Address	Register	Len
0xBB701464	GPON_GTC_DS_TRAFFIC_CFG [25].RESERVED[31:5]	27
0xBB701464	GPON_GTC_DS_TRAFFIC_CFG [25].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701468	GPON_GTC_DS_TRAFFIC_CFG [26].RESERVED[31:5]	27
0xBB701468	GPON_GTC_DS_TRAFFIC_CFG [26].TRAFFIC_TYPE_CFG[4:0]	5
0xBB70146C	GPON_GTC_DS_TRAFFIC_CFG [27].RESERVED[31:5]	27
0xBB70146C	GPON_GTC_DS_TRAFFIC_CFG [27].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701470	GPON_GTC_DS_TRAFFIC_CFG [28].RESERVED[31:5]	27
0xBB701470	GPON_GTC_DS_TRAFFIC_CFG [28].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701474	GPON_GTC_DS_TRAFFIC_CFG [29].RESERVED[31:5]	27
0xBB701474	GPON_GTC_DS_TRAFFIC_CFG [29].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701478	GPON_GTC_DS_TRAFFIC_CFG [30].RESERVED[31:5]	27
0xBB701478	GPON_GTC_DS_TRAFFIC_CFG [30].TRAFFIC_TYPE_CFG[4:0]	5
0xBB70147C	GPON_GTC_DS_TRAFFIC_CFG [31].RESERVED[31:5]	27
0xBB70147C	GPON_GTC_DS_TRAFFIC_CFG [31].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701480	GPON_GTC_DS_TRAFFIC_CFG [32].RESERVED[31:5]	27
0xBB701480	GPON_GTC_DS_TRAFFIC_CFG [32].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701484	GPON_GTC_DS_TRAFFIC_CFG [33].RESERVED[31:5]	27
0xBB701484	GPON_GTC_DS_TRAFFIC_CFG [33].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701488	GPON_GTC_DS_TRAFFIC_CFG [34].RESERVED[31:5]	27
0xBB701488	GPON_GTC_DS_TRAFFIC_CFG [34].TRAFFIC_TYPE_CFG[4:0]	5
0xBB70148C	GPON_GTC_DS_TRAFFIC_CFG [35].RESERVED[31:5]	27
0xBB70148C	GPON_GTC_DS_TRAFFIC_CFG [35].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701490	GPON_GTC_DS_TRAFFIC_CFG [36].RESERVED[31:5]	27
0xBB701490	GPON_GTC_DS_TRAFFIC_CFG [36].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701494	GPON_GTC_DS_TRAFFIC_CFG [37].RESERVED[31:5]	27
0xBB701494	GPON_GTC_DS_TRAFFIC_CFG [37].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701498	GPON_GTC_DS_TRAFFIC_CFG [38].RESERVED[31:5]	27
0xBB701498	GPON_GTC_DS_TRAFFIC_CFG [38].TRAFFIC_TYPE_CFG[4:0]	5
0xBB70149C	GPON_GTC_DS_TRAFFIC_CFG [39].RESERVED[31:5]	27
0xBB70149C	GPON_GTC_DS_TRAFFIC_CFG [39].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7014A0	GPON_GTC_DS_TRAFFIC_CFG [40].RESERVED[31:5]	27
0xBB7014A0	GPON_GTC_DS_TRAFFIC_CFG [40].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7014A4	GPON_GTC_DS_TRAFFIC_CFG [41].RESERVED[31:5]	27
0xBB7014A4	GPON_GTC_DS_TRAFFIC_CFG [41].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7014A8	GPON_GTC_DS_TRAFFIC_CFG [42].RESERVED[31:5]	27
0xBB7014A8	GPON_GTC_DS_TRAFFIC_CFG [42].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7014AC	GPON_GTC_DS_TRAFFIC_CFG [43].RESERVED[31:5]	27
0xBB7014AC	GPON_GTC_DS_TRAFFIC_CFG [43].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7014B0	GPON_GTC_DS_TRAFFIC_CFG [44].RESERVED[31:5]	27
0xBB7014B0	GPON_GTC_DS_TRAFFIC_CFG [44].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7014B4	GPON_GTC_DS_TRAFFIC_CFG [45].RESERVED[31:5]	27
0xBB7014B4	GPON_GTC_DS_TRAFFIC_CFG [45].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7014B8	GPON_GTC_DS_TRAFFIC_CFG [46].RESERVED[31:5]	27
0xBB7014B8	GPON_GTC_DS_TRAFFIC_CFG [46].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7014BC	GPON_GTC_DS_TRAFFIC_CFG [47].RESERVED[31:5]	27
0xBB7014BC	GPON_GTC_DS_TRAFFIC_CFG [47].TRAFFIC_TYPE_CFG[4:0]	5

Address	Register	Len
0xBB7014C0	GPON_GTC_DS_TRAFFIC_CFG [48].RESERVED[31:5]	27
0xBB7014C0	GPON_GTC_DS_TRAFFIC_CFG [48].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7014C4	GPON_GTC_DS_TRAFFIC_CFG [49].RESERVED[31:5]	27
0xBB7014C4	GPON_GTC_DS_TRAFFIC_CFG [49].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7014C8	GPON_GTC_DS_TRAFFIC_CFG [50].RESERVED[31:5]	27
0xBB7014C8	GPON_GTC_DS_TRAFFIC_CFG [50].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7014CC	GPON_GTC_DS_TRAFFIC_CFG [51].RESERVED[31:5]	27
0xBB7014CC	GPON_GTC_DS_TRAFFIC_CFG [51].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7014D0	GPON_GTC_DS_TRAFFIC_CFG [52].RESERVED[31:5]	27
0xBB7014D0	GPON_GTC_DS_TRAFFIC_CFG [52].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7014D4	GPON_GTC_DS_TRAFFIC_CFG [53].RESERVED[31:5]	27
0xBB7014D4	GPON_GTC_DS_TRAFFIC_CFG [53].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7014D8	GPON_GTC_DS_TRAFFIC_CFG [54].RESERVED[31:5]	27
0xBB7014D8	GPON_GTC_DS_TRAFFIC_CFG [54].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7014DC	GPON_GTC_DS_TRAFFIC_CFG [55].RESERVED[31:5]	27
0xBB7014DC	GPON_GTC_DS_TRAFFIC_CFG [55].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7014E0	GPON_GTC_DS_TRAFFIC_CFG [56].RESERVED[31:5]	27
0xBB7014E0	GPON_GTC_DS_TRAFFIC_CFG [56].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7014E4	GPON_GTC_DS_TRAFFIC_CFG [57].RESERVED[31:5]	27
0xBB7014E4	GPON_GTC_DS_TRAFFIC_CFG [57].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7014E8	GPON_GTC_DS_TRAFFIC_CFG [58].RESERVED[31:5]	27
0xBB7014E8	GPON_GTC_DS_TRAFFIC_CFG [58].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7014EC	GPON_GTC_DS_TRAFFIC_CFG [59].RESERVED[31:5]	27
0xBB7014EC	GPON_GTC_DS_TRAFFIC_CFG [59].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7014F0	GPON_GTC_DS_TRAFFIC_CFG [60].RESERVED[31:5]	27
0xBB7014F0	GPON_GTC_DS_TRAFFIC_CFG [60].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7014F4	GPON_GTC_DS_TRAFFIC_CFG [61].RESERVED[31:5]	27
0xBB7014F4	GPON_GTC_DS_TRAFFIC_CFG [61].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7014F8	GPON_GTC_DS_TRAFFIC_CFG [62].RESERVED[31:5]	27
0xBB7014F8	GPON_GTC_DS_TRAFFIC_CFG [62].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7014FC	GPON_GTC_DS_TRAFFIC_CFG [63].RESERVED[31:5]	27
0xBB7014FC	GPON_GTC_DS_TRAFFIC_CFG [63].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701500	GPON_GTC_DS_TRAFFIC_CFG [64].RESERVED[31:5]	27
0xBB701500	GPON_GTC_DS_TRAFFIC_CFG [64].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701504	GPON_GTC_DS_TRAFFIC_CFG [65].RESERVED[31:5]	27
0xBB701504	GPON_GTC_DS_TRAFFIC_CFG [65].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701508	GPON_GTC_DS_TRAFFIC_CFG [66].RESERVED[31:5]	27
0xBB701508	GPON_GTC_DS_TRAFFIC_CFG [66].TRAFFIC_TYPE_CFG[4:0]	5
0xBB70150C	GPON_GTC_DS_TRAFFIC_CFG [67].RESERVED[31:5]	27
0xBB70150C	GPON_GTC_DS_TRAFFIC_CFG [67].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701510	GPON_GTC_DS_TRAFFIC_CFG [68].RESERVED[31:5]	27
0xBB701510	GPON_GTC_DS_TRAFFIC_CFG [68].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701514	GPON_GTC_DS_TRAFFIC_CFG [69].RESERVED[31:5]	27
0xBB701514	GPON_GTC_DS_TRAFFIC_CFG [69].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701518	GPON_GTC_DS_TRAFFIC_CFG [70].RESERVED[31:5]	27
0xBB701518	GPON_GTC_DS_TRAFFIC_CFG [70].TRAFFIC_TYPE_CFG[4:0]	5



Address	Register	Len
0xBB70151C	GPON_GTC_DS_TRAFFIC_CFG [71].RESERVED[31:5]	27
0xBB70151C	GPON_GTC_DS_TRAFFIC_CFG [71].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701520	GPON_GTC_DS_TRAFFIC_CFG [72].RESERVED[31:5]	27
0xBB701520	GPON_GTC_DS_TRAFFIC_CFG [72].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701524	GPON_GTC_DS_TRAFFIC_CFG [73].RESERVED[31:5]	27
0xBB701524	GPON_GTC_DS_TRAFFIC_CFG [73].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701528	GPON_GTC_DS_TRAFFIC_CFG [74].RESERVED[31:5]	27
0xBB701528	GPON_GTC_DS_TRAFFIC_CFG [74].TRAFFIC_TYPE_CFG[4:0]	5
0xBB70152C	GPON_GTC_DS_TRAFFIC_CFG [75].RESERVED[31:5]	27
0xBB70152C	GPON_GTC_DS_TRAFFIC_CFG [75].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701530	GPON_GTC_DS_TRAFFIC_CFG [76].RESERVED[31:5]	27
0xBB701530	GPON_GTC_DS_TRAFFIC_CFG [76].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701534	GPON_GTC_DS_TRAFFIC_CFG [77].RESERVED[31:5]	27
0xBB701534	GPON_GTC_DS_TRAFFIC_CFG [77].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701538	GPON_GTC_DS_TRAFFIC_CFG [78].RESERVED[31:5]	27
0xBB701538	GPON_GTC_DS_TRAFFIC_CFG [78].TRAFFIC_TYPE_CFG[4:0]	5
0xBB70153C	GPON_GTC_DS_TRAFFIC_CFG [79].RESERVED[31:5]	27
0xBB70153C	GPON_GTC_DS_TRAFFIC_CFG [79].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701540	GPON_GTC_DS_TRAFFIC_CFG [80].RESERVED[31:5]	27
0xBB701540	GPON_GTC_DS_TRAFFIC_CFG [80].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701544	GPON_GTC_DS_TRAFFIC_CFG [81].RESERVED[31:5]	27
0xBB701544	GPON_GTC_DS_TRAFFIC_CFG [81].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701548	GPON_GTC_DS_TRAFFIC_CFG [82].RESERVED[31:5]	27
0xBB701548	GPON_GTC_DS_TRAFFIC_CFG [82].TRAFFIC_TYPE_CFG[4:0]	5
0xBB70154C	GPON_GTC_DS_TRAFFIC_CFG [83].RESERVED[31:5]	27
0xBB70154C	GPON_GTC_DS_TRAFFIC_CFG [83].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701550	GPON_GTC_DS_TRAFFIC_CFG [84].RESERVED[31:5]	27
0xBB701550	GPON_GTC_DS_TRAFFIC_CFG [84].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701554	GPON_GTC_DS_TRAFFIC_CFG [85].RESERVED[31:5]	27
0xBB701554	GPON_GTC_DS_TRAFFIC_CFG [85].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701558	GPON_GTC_DS_TRAFFIC_CFG [86].RESERVED[31:5]	27
0xBB701558	GPON_GTC_DS_TRAFFIC_CFG [86].TRAFFIC_TYPE_CFG[4:0]	5
0xBB70155C	GPON_GTC_DS_TRAFFIC_CFG [87].RESERVED[31:5]	27
0xBB70155C	GPON_GTC_DS_TRAFFIC_CFG [87].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701560	GPON_GTC_DS_TRAFFIC_CFG [88].RESERVED[31:5]	27
0xBB701560	GPON_GTC_DS_TRAFFIC_CFG [88].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701564	GPON_GTC_DS_TRAFFIC_CFG [89].RESERVED[31:5]	27
0xBB701564	GPON_GTC_DS_TRAFFIC_CFG [89].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701568	GPON_GTC_DS_TRAFFIC_CFG [90].RESERVED[31:5]	27
0xBB701568	GPON_GTC_DS_TRAFFIC_CFG [90].TRAFFIC_TYPE_CFG[4:0]	5
0xBB70156C	GPON_GTC_DS_TRAFFIC_CFG [91].RESERVED[31:5]	27
0xBB70156C	GPON_GTC_DS_TRAFFIC_CFG [91].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701570	GPON_GTC_DS_TRAFFIC_CFG [92].RESERVED[31:5]	27
0xBB701570	GPON_GTC_DS_TRAFFIC_CFG [92].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701574	GPON_GTC_DS_TRAFFIC_CFG [93].RESERVED[31:5]	27
0xBB701574	GPON_GTC_DS_TRAFFIC_CFG [93].TRAFFIC_TYPE_CFG[4:0]	5

Address	Register	Len
0xBB701578	GPON_GTC_DS_TRAFFIC_CFG [94].RESERVED[31:5]	27
0xBB701578	GPON_GTC_DS_TRAFFIC_CFG [94].TRAFFIC_TYPE_CFG[4:0]	5
0xBB70157C	GPON_GTC_DS_TRAFFIC_CFG [95].RESERVED[31:5]	27
0xBB70157C	GPON_GTC_DS_TRAFFIC_CFG [95].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701580	GPON_GTC_DS_TRAFFIC_CFG [96].RESERVED[31:5]	27
0xBB701580	GPON_GTC_DS_TRAFFIC_CFG [96].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701584	GPON_GTC_DS_TRAFFIC_CFG [97].RESERVED[31:5]	27
0xBB701584	GPON_GTC_DS_TRAFFIC_CFG [97].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701588	GPON_GTC_DS_TRAFFIC_CFG [98].RESERVED[31:5]	27
0xBB701588	GPON_GTC_DS_TRAFFIC_CFG [98].TRAFFIC_TYPE_CFG[4:0]	5
0xBB70158C	GPON_GTC_DS_TRAFFIC_CFG [99].RESERVED[31:5]	27
0xBB70158C	GPON_GTC_DS_TRAFFIC_CFG [99].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701590	GPON_GTC_DS_TRAFFIC_CFG [100].RESERVED[31:5]	27
0xBB701590	GPON_GTC_DS_TRAFFIC_CFG [100].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701594	GPON_GTC_DS_TRAFFIC_CFG [101].RESERVED[31:5]	27
0xBB701594	GPON_GTC_DS_TRAFFIC_CFG [101].TRAFFIC_TYPE_CFG[4:0]	5
0xBB701598	GPON_GTC_DS_TRAFFIC_CFG [102].RESERVED[31:5]	27
0xBB701598	GPON_GTC_DS_TRAFFIC_CFG [102].TRAFFIC_TYPE_CFG[4:0]	5
0xBB70159C	GPON_GTC_DS_TRAFFIC_CFG [103].RESERVED[31:5]	27
0xBB70159C	GPON_GTC_DS_TRAFFIC_CFG [103].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7015A0	GPON_GTC_DS_TRAFFIC_CFG [104].RESERVED[31:5]	27
0xBB7015A0	GPON_GTC_DS_TRAFFIC_CFG [104].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7015A4	GPON_GTC_DS_TRAFFIC_CFG [105].RESERVED[31:5]	27
0xBB7015A4	GPON_GTC_DS_TRAFFIC_CFG [105].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7015A8	GPON_GTC_DS_TRAFFIC_CFG [106].RESERVED[31:5]	27
0xBB7015A8	GPON_GTC_DS_TRAFFIC_CFG [106].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7015AC	GPON_GTC_DS_TRAFFIC_CFG [107].RESERVED[31:5]	27
0xBB7015AC	GPON_GTC_DS_TRAFFIC_CFG [107].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7015B0	GPON_GTC_DS_TRAFFIC_CFG [108].RESERVED[31:5]	27
0xBB7015B0	GPON_GTC_DS_TRAFFIC_CFG [108].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7015B4	GPON_GTC_DS_TRAFFIC_CFG [109].RESERVED[31:5]	27
0xBB7015B4	GPON_GTC_DS_TRAFFIC_CFG [109].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7015B8	GPON_GTC_DS_TRAFFIC_CFG [110].RESERVED[31:5]	27
0xBB7015B8	GPON_GTC_DS_TRAFFIC_CFG [110].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7015BC	GPON_GTC_DS_TRAFFIC_CFG [111].RESERVED[31:5]	27
0xBB7015BC	GPON_GTC_DS_TRAFFIC_CFG [111].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7015C0	GPON_GTC_DS_TRAFFIC_CFG [112].RESERVED[31:5]	27
0xBB7015C0	GPON_GTC_DS_TRAFFIC_CFG [112].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7015C4	GPON_GTC_DS_TRAFFIC_CFG [113].RESERVED[31:5]	27
0xBB7015C4	GPON_GTC_DS_TRAFFIC_CFG [113].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7015C8	GPON_GTC_DS_TRAFFIC_CFG [114].RESERVED[31:5]	27
0xBB7015C8	GPON_GTC_DS_TRAFFIC_CFG [114].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7015CC	GPON_GTC_DS_TRAFFIC_CFG [115].RESERVED[31:5]	27
0xBB7015CC	GPON_GTC_DS_TRAFFIC_CFG [115].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7015D0	GPON_GTC_DS_TRAFFIC_CFG [116].RESERVED[31:5]	27
0xBB7015D0	GPON_GTC_DS_TRAFFIC_CFG [116].TRAFFIC_TYPE_CFG[4:0]	5



Address	Register	Len
0xBB7015D4	GPON_GTC_DS_TRAFFIC_CFG [117].RESERVED[31:5]	27
0xBB7015D4	GPON_GTC_DS_TRAFFIC_CFG [117].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7015D8	GPON_GTC_DS_TRAFFIC_CFG [118].RESERVED[31:5]	27
0xBB7015D8	GPON_GTC_DS_TRAFFIC_CFG [118].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7015DC	GPON_GTC_DS_TRAFFIC_CFG [119].RESERVED[31:5]	27
0xBB7015DC	GPON_GTC_DS_TRAFFIC_CFG [119].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7015E0	GPON_GTC_DS_TRAFFIC_CFG [120].RESERVED[31:5]	27
0xBB7015E0	GPON_GTC_DS_TRAFFIC_CFG [120].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7015E4	GPON_GTC_DS_TRAFFIC_CFG [121].RESERVED[31:5]	27
0xBB7015E4	GPON_GTC_DS_TRAFFIC_CFG [121].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7015E8	GPON_GTC_DS_TRAFFIC_CFG [122].RESERVED[31:5]	27
0xBB7015E8	GPON_GTC_DS_TRAFFIC_CFG [122].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7015EC	GPON_GTC_DS_TRAFFIC_CFG [123].RESERVED[31:5]	27
0xBB7015EC	GPON_GTC_DS_TRAFFIC_CFG [123].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7015F0	GPON_GTC_DS_TRAFFIC_CFG [124].RESERVED[31:5]	27
0xBB7015F0	GPON_GTC_DS_TRAFFIC_CFG [124].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7015F4	GPON_GTC_DS_TRAFFIC_CFG [125].RESERVED[31:5]	27
0xBB7015F4	GPON_GTC_DS_TRAFFIC_CFG [125].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7015F8	GPON_GTC_DS_TRAFFIC_CFG [126].RESERVED[31:5]	27
0xBB7015F8	GPON_GTC_DS_TRAFFIC_CFG [126].TRAFFIC_TYPE_CFG[4:0]	5
0xBB7015FC	GPON_GTC_DS_TRAFFIC_CFG [127].RESERVED[31:5]	27
0xBB7015FC	GPON_GTC_DS_TRAFFIC_CFG [127].TRAFFIC_TYPE_CFG[4:0]	5
0xBB70200C	GPON_BWMAP_CTRL.RESERVED[31:16]	16
0xBB70200C	GPON_BWMAP_CTRL.CAP_EN[15:15]	1
0xBB70200C	GPON_BWMAP_CTRL.CAP_CLR[14:14]	1
0xBB70200C	GPON_BWMAP_CTRL.RESERVED[13:8]	6
0xBB70200C	GPON_BWMAP_CTRL.CAP_FRAME_NUM[7:0]	8
0xBB702010	GPON_BWMAP_STS.RESERVED[31:9]	23
0xBB702010	GPON_BWMAP_STS.CAP_OVERFL[8:8]	1
0xBB702010	GPON_BWMAP_STS.RESERVED[7:0]	8
0xBB702400	GPON_BWMAP_DATA [0].RESERVED[31:16]	16
0xBB702400	GPON_BWMAP_DATA [0].CAP_DATA[15:0]	16
0xBB702404	GPON_BWMAP_DATA [1].RESERVED[31:16]	16
0xBB702404	GPON_BWMAP_DATA [1].CAP_DATA[15:0]	16
0xBB702408	GPON_BWMAP_DATA [2].RESERVED[31:16]	16
0xBB702408	GPON_BWMAP_DATA [2].CAP_DATA[15:0]	16
0xBB70240C	GPON_BWMAP_DATA [3].RESERVED[31:16]	16
0xBB70240C	GPON_BWMAP_DATA [3].CAP_DATA[15:0]	16
0xBB702410	GPON_BWMAP_DATA [4].RESERVED[31:16]	16
0xBB702410	GPON_BWMAP_DATA [4].CAP_DATA[15:0]	16
0xBB702414	GPON_BWMAP_DATA [5].RESERVED[31:16]	16
0xBB702414	GPON_BWMAP_DATA [5].CAP_DATA[15:0]	16
0xBB702418	GPON_BWMAP_DATA [6].RESERVED[31:16]	16
0xBB702418	GPON_BWMAP_DATA [6].CAP_DATA[15:0]	16
0xBB70241C	GPON_BWMAP_DATA [7].RESERVED[31:16]	16
0xBB70241C	GPON_BWMAP_DATA [7].CAP_DATA[15:0]	16

Address	Register	Len
0xBB702420	GPON_BWMAP_DATA [8].RESERVED[31:16]	16
0xBB702420	GPON_BWMAP_DATA [8].CAP_DATA[15:0]	16
0xBB702424	GPON_BWMAP_DATA [9].RESERVED[31:16]	16
0xBB702424	GPON_BWMAP_DATA [9].CAP_DATA[15:0]	16
0xBB702428	GPON_BWMAP_DATA [10].RESERVED[31:16]	16
0xBB702428	GPON_BWMAP_DATA [10].CAP_DATA[15:0]	16
0xBB70242C	GPON_BWMAP_DATA [11].RESERVED[31:16]	16
0xBB70242C	GPON_BWMAP_DATA [11].CAP_DATA[15:0]	16
0xBB702430	GPON_BWMAP_DATA [12].RESERVED[31:16]	16
0xBB702430	GPON_BWMAP_DATA [12].CAP_DATA[15:0]	16
0xBB702434	GPON_BWMAP_DATA [13].RESERVED[31:16]	16
0xBB702434	GPON_BWMAP_DATA [13].CAP_DATA[15:0]	16
0xBB702438	GPON_BWMAP_DATA [14].RESERVED[31:16]	16
0xBB702438	GPON_BWMAP_DATA [14].CAP_DATA[15:0]	16
0xBB70243C	GPON_BWMAP_DATA [15].RESERVED[31:16]	16
0xBB70243C	GPON_BWMAP_DATA [15].CAP_DATA[15:0]	16
0xBB702440	GPON_BWMAP_DATA [16].RESERVED[31:16]	16
0xBB702440	GPON_BWMAP_DATA [16].CAP_DATA[15:0]	16
0xBB702444	GPON_BWMAP_DATA [17].RESERVED[31:16]	16
0xBB702444	GPON_BWMAP_DATA [17].CAP_DATA[15:0]	16
0xBB702448	GPON_BWMAP_DATA [18].RESERVED[31:16]	16
0xBB702448	GPON_BWMAP_DATA [18].CAP_DATA[15:0]	16
0xBB70244C	GPON_BWMAP_DATA [19].RESERVED[31:16]	16
0xBB70244C	GPON_BWMAP_DATA [19].CAP_DATA[15:0]	16
0xBB702450	GPON_BWMAP_DATA [20].RESERVED[31:16]	16
0xBB702450	GPON_BWMAP_DATA [20].CAP_DATA[15:0]	16
0xBB702454	GPON_BWMAP_DATA [21].RESERVED[31:16]	16
0xBB702454	GPON_BWMAP_DATA [21].CAP_DATA[15:0]	16
0xBB702458	GPON_BWMAP_DATA [22].RESERVED[31:16]	16
0xBB702458	GPON_BWMAP_DATA [22].CAP_DATA[15:0]	16
0xBB70245C	GPON_BWMAP_DATA [23].RESERVED[31:16]	16
0xBB70245C	GPON_BWMAP_DATA [23].CAP_DATA[15:0]	16
0xBB702460	GPON_BWMAP_DATA [24].RESERVED[31:16]	16
0xBB702460	GPON_BWMAP_DATA [24].CAP_DATA[15:0]	16
0xBB702464	GPON_BWMAP_DATA [25].RESERVED[31:16]	16
0xBB702464	GPON_BWMAP_DATA [25].CAP_DATA[15:0]	16
0xBB702468	GPON_BWMAP_DATA [26].RESERVED[31:16]	16
0xBB702468	GPON_BWMAP_DATA [26].CAP_DATA[15:0]	16
0xBB70246C	GPON_BWMAP_DATA [27].RESERVED[31:16]	16
0xBB70246C	GPON_BWMAP_DATA [27].CAP_DATA[15:0]	16
0xBB702470	GPON_BWMAP_DATA [28].RESERVED[31:16]	16
0xBB702470	GPON_BWMAP_DATA [28].CAP_DATA[15:0]	16
0xBB702474	GPON_BWMAP_DATA [29].RESERVED[31:16]	16
0xBB702474	GPON_BWMAP_DATA [29].CAP_DATA[15:0]	16
0xBB702478	GPON_BWMAP_DATA [30].RESERVED[31:16]	16
0xBB702478	GPON_BWMAP_DATA [30].CAP_DATA[15:0]	16

Address	Register	Len
0xBB70247C	GPON_BWMAP_DATA [31].RESERVED[31:16]	16
0xBB70247C	GPON_BWMAP_DATA [31].CAP_DATA[15:0]	16
0xBB702480	GPON_BWMAP_DATA [32].RESERVED[31:16]	16
0xBB702480	GPON_BWMAP_DATA [32].CAP_DATA[15:0]	16
0xBB702484	GPON_BWMAP_DATA [33].RESERVED[31:16]	16
0xBB702484	GPON_BWMAP_DATA [33].CAP_DATA[15:0]	16
0xBB702488	GPON_BWMAP_DATA [34].RESERVED[31:16]	16
0xBB702488	GPON_BWMAP_DATA [34].CAP_DATA[15:0]	16
0xBB70248C	GPON_BWMAP_DATA [35].RESERVED[31:16]	16
0xBB70248C	GPON_BWMAP_DATA [35].CAP_DATA[15:0]	16
0xBB702490	GPON_BWMAP_DATA [36].RESERVED[31:16]	16
0xBB702490	GPON_BWMAP_DATA [36].CAP_DATA[15:0]	16
0xBB702494	GPON_BWMAP_DATA [37].RESERVED[31:16]	16
0xBB702494	GPON_BWMAP_DATA [37].CAP_DATA[15:0]	16
0xBB702498	GPON_BWMAP_DATA [38].RESERVED[31:16]	16
0xBB702498	GPON_BWMAP_DATA [38].CAP_DATA[15:0]	16
0xBB70249C	GPON_BWMAP_DATA [39].RESERVED[31:16]	16
0xBB70249C	GPON_BWMAP_DATA [39].CAP_DATA[15:0]	16
0xBB7024A0	GPON_BWMAP_DATA [40].RESERVED[31:16]	16
0xBB7024A0	GPON_BWMAP_DATA [40].CAP_DATA[15:0]	16
0xBB7024A4	GPON_BWMAP_DATA [41].RESERVED[31:16]	16
0xBB7024A4	GPON_BWMAP_DATA [41].CAP_DATA[15:0]	16
0xBB7024A8	GPON_BWMAP_DATA [42].RESERVED[31:16]	16
0xBB7024A8	GPON_BWMAP_DATA [42].CAP_DATA[15:0]	16
0xBB7024AC	GPON_BWMAP_DATA [43].RESERVED[31:16]	16
0xBB7024AC	GPON_BWMAP_DATA [43].CAP_DATA[15:0]	16
0xBB7024B0	GPON_BWMAP_DATA [44].RESERVED[31:16]	16
0xBB7024B0	GPON_BWMAP_DATA [44].CAP_DATA[15:0]	16
0xBB7024B4	GPON_BWMAP_DATA [45].RESERVED[31:16]	16
0xBB7024B4	GPON_BWMAP_DATA [45].CAP_DATA[15:0]	16
0xBB7024B8	GPON_BWMAP_DATA [46].RESERVED[31:16]	16
0xBB7024B8	GPON_BWMAP_DATA [46].CAP_DATA[15:0]	16
0xBB7024BC	GPON_BWMAP_DATA [47].RESERVED[31:16]	16
0xBB7024BC	GPON_BWMAP_DATA [47].CAP_DATA[15:0]	16
0xBB7024C0	GPON_BWMAP_DATA [48].RESERVED[31:16]	16
0xBB7024C0	GPON_BWMAP_DATA [48].CAP_DATA[15:0]	16
0xBB7024C4	GPON_BWMAP_DATA [49].RESERVED[31:16]	16
0xBB7024C4	GPON_BWMAP_DATA [49].CAP_DATA[15:0]	16
0xBB7024C8	GPON_BWMAP_DATA [50].RESERVED[31:16]	16
0xBB7024C8	GPON_BWMAP_DATA [50].CAP_DATA[15:0]	16
0xBB7024CC	GPON_BWMAP_DATA [51].RESERVED[31:16]	16
0xBB7024CC	GPON_BWMAP_DATA [51].CAP_DATA[15:0]	16
0xBB7024D0	GPON_BWMAP_DATA [52].RESERVED[31:16]	16
0xBB7024D0	GPON_BWMAP_DATA [52].CAP_DATA[15:0]	16
0xBB7024D4	GPON_BWMAP_DATA [53].RESERVED[31:16]	16
0xBB7024D4	GPON_BWMAP_DATA [53].CAP_DATA[15:0]	16

Address	Register	Len
0xBB7024D8	GPON_BWMAP_DATA [54].RESERVED[31:16]	16
0xBB7024D8	GPON_BWMAP_DATA [54].CAP_DATA[15:0]	16
0xBB7024DC	GPON_BWMAP_DATA [55].RESERVED[31:16]	16
0xBB7024DC	GPON_BWMAP_DATA [55].CAP_DATA[15:0]	16
0xBB7024E0	GPON_BWMAP_DATA [56].RESERVED[31:16]	16
0xBB7024E0	GPON_BWMAP_DATA [56].CAP_DATA[15:0]	16
0xBB7024E4	GPON_BWMAP_DATA [57].RESERVED[31:16]	16
0xBB7024E4	GPON_BWMAP_DATA [57].CAP_DATA[15:0]	16
0xBB7024E8	GPON_BWMAP_DATA [58].RESERVED[31:16]	16
0xBB7024E8	GPON_BWMAP_DATA [58].CAP_DATA[15:0]	16
0xBB7024EC	GPON_BWMAP_DATA [59].RESERVED[31:16]	16
0xBB7024EC	GPON_BWMAP_DATA [59].CAP_DATA[15:0]	16
0xBB7024F0	GPON_BWMAP_DATA [60].RESERVED[31:16]	16
0xBB7024F0	GPON_BWMAP_DATA [60].CAP_DATA[15:0]	16
0xBB7024F4	GPON_BWMAP_DATA [61].RESERVED[31:16]	16
0xBB7024F4	GPON_BWMAP_DATA [61].CAP_DATA[15:0]	16
0xBB7024F8	GPON_BWMAP_DATA [62].RESERVED[31:16]	16
0xBB7024F8	GPON_BWMAP_DATA [62].CAP_DATA[15:0]	16
0xBB7024FC	GPON_BWMAP_DATA [63].RESERVED[31:16]	16
0xBB7024FC	GPON_BWMAP_DATA [63].CAP_DATA[15:0]	16
0xBB702500	GPON_BWMAP_DATA [64].RESERVED[31:16]	16
0xBB702500	GPON_BWMAP_DATA [64].CAP_DATA[15:0]	16
0xBB702504	GPON_BWMAP_DATA [65].RESERVED[31:16]	16
0xBB702504	GPON_BWMAP_DATA [65].CAP_DATA[15:0]	16
0xBB702508	GPON_BWMAP_DATA [66].RESERVED[31:16]	16
0xBB702508	GPON_BWMAP_DATA [66].CAP_DATA[15:0]	16
0xBB70250C	GPON_BWMAP_DATA [67].RESERVED[31:16]	16
0xBB70250C	GPON_BWMAP_DATA [67].CAP_DATA[15:0]	16
0xBB702510	GPON_BWMAP_DATA [68].RESERVED[31:16]	16
0xBB702510	GPON_BWMAP_DATA [68].CAP_DATA[15:0]	16
0xBB702514	GPON_BWMAP_DATA [69].RESERVED[31:16]	16
0xBB702514	GPON_BWMAP_DATA [69].CAP_DATA[15:0]	16
0xBB702518	GPON_BWMAP_DATA [70].RESERVED[31:16]	16
0xBB702518	GPON_BWMAP_DATA [70].CAP_DATA[15:0]	16
0xBB70251C	GPON_BWMAP_DATA [71].RESERVED[31:16]	16
0xBB70251C	GPON_BWMAP_DATA [71].CAP_DATA[15:0]	16
0xBB702520	GPON_BWMAP_DATA [72].RESERVED[31:16]	16
0xBB702520	GPON_BWMAP_DATA [72].CAP_DATA[15:0]	16
0xBB702524	GPON_BWMAP_DATA [73].RESERVED[31:16]	16
0xBB702524	GPON_BWMAP_DATA [73].CAP_DATA[15:0]	16
0xBB702528	GPON_BWMAP_DATA [74].RESERVED[31:16]	16
0xBB702528	GPON_BWMAP_DATA [74].CAP_DATA[15:0]	16
0xBB70252C	GPON_BWMAP_DATA [75].RESERVED[31:16]	16
0xBB70252C	GPON_BWMAP_DATA [75].CAP_DATA[15:0]	16
0xBB702530	GPON_BWMAP_DATA [76].RESERVED[31:16]	16
0xBB702530	GPON_BWMAP_DATA [76].CAP_DATA[15:0]	16

Address	Register	Len
0xBB702534	GPON_BWMAP_DATA [77].RESERVED[31:16]	16
0xBB702534	GPON_BWMAP_DATA [77].CAP_DATA[15:0]	16
0xBB702538	GPON_BWMAP_DATA [78].RESERVED[31:16]	16
0xBB702538	GPON_BWMAP_DATA [78].CAP_DATA[15:0]	16
0xBB70253C	GPON_BWMAP_DATA [79].RESERVED[31:16]	16
0xBB70253C	GPON_BWMAP_DATA [79].CAP_DATA[15:0]	16
0xBB702540	GPON_BWMAP_DATA [80].RESERVED[31:16]	16
0xBB702540	GPON_BWMAP_DATA [80].CAP_DATA[15:0]	16
0xBB702544	GPON_BWMAP_DATA [81].RESERVED[31:16]	16
0xBB702544	GPON_BWMAP_DATA [81].CAP_DATA[15:0]	16
0xBB702548	GPON_BWMAP_DATA [82].RESERVED[31:16]	16
0xBB702548	GPON_BWMAP_DATA [82].CAP_DATA[15:0]	16
0xBB70254C	GPON_BWMAP_DATA [83].RESERVED[31:16]	16
0xBB70254C	GPON_BWMAP_DATA [83].CAP_DATA[15:0]	16
0xBB702550	GPON_BWMAP_DATA [84].RESERVED[31:16]	16
0xBB702550	GPON_BWMAP_DATA [84].CAP_DATA[15:0]	16
0xBB702554	GPON_BWMAP_DATA [85].RESERVED[31:16]	16
0xBB702554	GPON_BWMAP_DATA [85].CAP_DATA[15:0]	16
0xBB702558	GPON_BWMAP_DATA [86].RESERVED[31:16]	16
0xBB702558	GPON_BWMAP_DATA [86].CAP_DATA[15:0]	16
0xBB70255C	GPON_BWMAP_DATA [87].RESERVED[31:16]	16
0xBB70255C	GPON_BWMAP_DATA [87].CAP_DATA[15:0]	16
0xBB702560	GPON_BWMAP_DATA [88].RESERVED[31:16]	16
0xBB702560	GPON_BWMAP_DATA [88].CAP_DATA[15:0]	16
0xBB702564	GPON_BWMAP_DATA [89].RESERVED[31:16]	16
0xBB702564	GPON_BWMAP_DATA [89].CAP_DATA[15:0]	16
0xBB702568	GPON_BWMAP_DATA [90].RESERVED[31:16]	16
0xBB702568	GPON_BWMAP_DATA [90].CAP_DATA[15:0]	16
0xBB70256C	GPON_BWMAP_DATA [91].RESERVED[31:16]	16
0xBB70256C	GPON_BWMAP_DATA [91].CAP_DATA[15:0]	16
0xBB702570	GPON_BWMAP_DATA [92].RESERVED[31:16]	16
0xBB702570	GPON_BWMAP_DATA [92].CAP_DATA[15:0]	16
0xBB702574	GPON_BWMAP_DATA [93].RESERVED[31:16]	16
0xBB702574	GPON_BWMAP_DATA [93].CAP_DATA[15:0]	16
0xBB702578	GPON_BWMAP_DATA [94].RESERVED[31:16]	16
0xBB702578	GPON_BWMAP_DATA [94].CAP_DATA[15:0]	16
0xBB70257C	GPON_BWMAP_DATA [95].RESERVED[31:16]	16
0xBB70257C	GPON_BWMAP_DATA [95].CAP_DATA[15:0]	16
0xBB702580	GPON_BWMAP_DATA [96].RESERVED[31:16]	16
0xBB702580	GPON_BWMAP_DATA [96].CAP_DATA[15:0]	16
0xBB702584	GPON_BWMAP_DATA [97].RESERVED[31:16]	16
0xBB702584	GPON_BWMAP_DATA [97].CAP_DATA[15:0]	16
0xBB702588	GPON_BWMAP_DATA [98].RESERVED[31:16]	16
0xBB702588	GPON_BWMAP_DATA [98].CAP_DATA[15:0]	16
0xBB70258C	GPON_BWMAP_DATA [99].RESERVED[31:16]	16
0xBB70258C	GPON_BWMAP_DATA [99].CAP_DATA[15:0]	16

Address	Register	Len
0xBB702590	GPON_BWMAP_DATA [100].RESERVED[31:16]	16
0xBB702590	GPON_BWMAP_DATA [100].CAP_DATA[15:0]	16
0xBB702594	GPON_BWMAP_DATA [101].RESERVED[31:16]	16
0xBB702594	GPON_BWMAP_DATA [101].CAP_DATA[15:0]	16
0xBB702598	GPON_BWMAP_DATA [102].RESERVED[31:16]	16
0xBB702598	GPON_BWMAP_DATA [102].CAP_DATA[15:0]	16
0xBB70259C	GPON_BWMAP_DATA [103].RESERVED[31:16]	16
0xBB70259C	GPON_BWMAP_DATA [103].CAP_DATA[15:0]	16
0xBB7025A0	GPON_BWMAP_DATA [104].RESERVED[31:16]	16
0xBB7025A0	GPON_BWMAP_DATA [104].CAP_DATA[15:0]	16
0xBB7025A4	GPON_BWMAP_DATA [105].RESERVED[31:16]	16
0xBB7025A4	GPON_BWMAP_DATA [105].CAP_DATA[15:0]	16
0xBB7025A8	GPON_BWMAP_DATA [106].RESERVED[31:16]	16
0xBB7025A8	GPON_BWMAP_DATA [106].CAP_DATA[15:0]	16
0xBB7025AC	GPON_BWMAP_DATA [107].RESERVED[31:16]	16
0xBB7025AC	GPON_BWMAP_DATA [107].CAP_DATA[15:0]	16
0xBB7025B0	GPON_BWMAP_DATA [108].RESERVED[31:16]	16
0xBB7025B0	GPON_BWMAP_DATA [108].CAP_DATA[15:0]	16
0xBB7025B4	GPON_BWMAP_DATA [109].RESERVED[31:16]	16
0xBB7025B4	GPON_BWMAP_DATA [109].CAP_DATA[15:0]	16
0xBB7025B8	GPON_BWMAP_DATA [110].RESERVED[31:16]	16
0xBB7025B8	GPON_BWMAP_DATA [110].CAP_DATA[15:0]	16
0xBB7025BC	GPON_BWMAP_DATA [111].RESERVED[31:16]	16
0xBB7025BC	GPON_BWMAP_DATA [111].CAP_DATA[15:0]	16
0xBB7025C0	GPON_BWMAP_DATA [112].RESERVED[31:16]	16
0xBB7025C0	GPON_BWMAP_DATA [112].CAP_DATA[15:0]	16
0xBB7025C4	GPON_BWMAP_DATA [113].RESERVED[31:16]	16
0xBB7025C4	GPON_BWMAP_DATA [113].CAP_DATA[15:0]	16
0xBB7025C8	GPON_BWMAP_DATA [114].RESERVED[31:16]	16
0xBB7025C8	GPON_BWMAP_DATA [114].CAP_DATA[15:0]	16
0xBB7025CC	GPON_BWMAP_DATA [115].RESERVED[31:16]	16
0xBB7025CC	GPON_BWMAP_DATA [115].CAP_DATA[15:0]	16
0xBB7025D0	GPON_BWMAP_DATA [116].RESERVED[31:16]	16
0xBB7025D0	GPON_BWMAP_DATA [116].CAP_DATA[15:0]	16
0xBB7025D4	GPON_BWMAP_DATA [117].RESERVED[31:16]	16
0xBB7025D4	GPON_BWMAP_DATA [117].CAP_DATA[15:0]	16
0xBB7025D8	GPON_BWMAP_DATA [118].RESERVED[31:16]	16
0xBB7025D8	GPON_BWMAP_DATA [118].CAP_DATA[15:0]	16
0xBB7025DC	GPON_BWMAP_DATA [119].RESERVED[31:16]	16
0xBB7025DC	GPON_BWMAP_DATA [119].CAP_DATA[15:0]	16
0xBB7025E0	GPON_BWMAP_DATA [120].RESERVED[31:16]	16
0xBB7025E0	GPON_BWMAP_DATA [120].CAP_DATA[15:0]	16
0xBB7025E4	GPON_BWMAP_DATA [121].RESERVED[31:16]	16
0xBB7025E4	GPON_BWMAP_DATA [121].CAP_DATA[15:0]	16
0xBB7025E8	GPON_BWMAP_DATA [122].RESERVED[31:16]	16
0xBB7025E8	GPON_BWMAP_DATA [122].CAP_DATA[15:0]	16



Address	Register	Len
0xBB7025EC	GPON_BWMAP_DATA [123].RESERVED[31:16]	16
0xBB7025EC	GPON_BWMAP_DATA [123].CAP_DATA[15:0]	16
0xBB7025F0	GPON_BWMAP_DATA [124].RESERVED[31:16]	16
0xBB7025F0	GPON_BWMAP_DATA [124].CAP_DATA[15:0]	16
0xBB7025F4	GPON_BWMAP_DATA [125].RESERVED[31:16]	16
0xBB7025F4	GPON_BWMAP_DATA [125].CAP_DATA[15:0]	16
0xBB7025F8	GPON_BWMAP_DATA [126].RESERVED[31:16]	16
0xBB7025F8	GPON_BWMAP_DATA [126].CAP_DATA[15:0]	16
0xBB7025FC	GPON_BWMAP_DATA [127].RESERVED[31:16]	16
0xBB7025FC	GPON_BWMAP_DATA [127].CAP_DATA[15:0]	16
0xBB702600	GPON_BWMAP_DATA [128].RESERVED[31:16]	16
0xBB702600	GPON_BWMAP_DATA [128].CAP_DATA[15:0]	16
0xBB702604	GPON_BWMAP_DATA [129].RESERVED[31:16]	16
0xBB702604	GPON_BWMAP_DATA [129].CAP_DATA[15:0]	16
0xBB702608	GPON_BWMAP_DATA [130].RESERVED[31:16]	16
0xBB702608	GPON_BWMAP_DATA [130].CAP_DATA[15:0]	16
0xBB70260C	GPON_BWMAP_DATA [131].RESERVED[31:16]	16
0xBB70260C	GPON_BWMAP_DATA [131].CAP_DATA[15:0]	16
0xBB702610	GPON_BWMAP_DATA [132].RESERVED[31:16]	16
0xBB702610	GPON_BWMAP_DATA [132].CAP_DATA[15:0]	16
0xBB702614	GPON_BWMAP_DATA [133].RESERVED[31:16]	16
0xBB702614	GPON_BWMAP_DATA [133].CAP_DATA[15:0]	16
0xBB702618	GPON_BWMAP_DATA [134].RESERVED[31:16]	16
0xBB702618	GPON_BWMAP_DATA [134].CAP_DATA[15:0]	16
0xBB70261C	GPON_BWMAP_DATA [135].RESERVED[31:16]	16
0xBB70261C	GPON_BWMAP_DATA [135].CAP_DATA[15:0]	16
0xBB702620	GPON_BWMAP_DATA [136].RESERVED[31:16]	16
0xBB702620	GPON_BWMAP_DATA [136].CAP_DATA[15:0]	16
0xBB702624	GPON_BWMAP_DATA [137].RESERVED[31:16]	16
0xBB702624	GPON_BWMAP_DATA [137].CAP_DATA[15:0]	16
0xBB702628	GPON_BWMAP_DATA [138].RESERVED[31:16]	16
0xBB702628	GPON_BWMAP_DATA [138].CAP_DATA[15:0]	16
0xBB70262C	GPON_BWMAP_DATA [139].RESERVED[31:16]	16
0xBB70262C	GPON_BWMAP_DATA [139].CAP_DATA[15:0]	16
0xBB702630	GPON_BWMAP_DATA [140].RESERVED[31:16]	16
0xBB702630	GPON_BWMAP_DATA [140].CAP_DATA[15:0]	16
0xBB702634	GPON_BWMAP_DATA [141].RESERVED[31:16]	16
0xBB702634	GPON_BWMAP_DATA [141].CAP_DATA[15:0]	16
0xBB702638	GPON_BWMAP_DATA [142].RESERVED[31:16]	16
0xBB702638	GPON_BWMAP_DATA [142].CAP_DATA[15:0]	16
0xBB70263C	GPON_BWMAP_DATA [143].RESERVED[31:16]	16
0xBB70263C	GPON_BWMAP_DATA [143].CAP_DATA[15:0]	16
0xBB702640	GPON_BWMAP_DATA [144].RESERVED[31:16]	16
0xBB702640	GPON_BWMAP_DATA [144].CAP_DATA[15:0]	16
0xBB702644	GPON_BWMAP_DATA [145].RESERVED[31:16]	16
0xBB702644	GPON_BWMAP_DATA [145].CAP_DATA[15:0]	16

Address	Register	Len
0xBB702648	GPON_BWMAP_DATA [146].RESERVED[31:16]	16
0xBB702648	GPON_BWMAP_DATA [146].CAP_DATA[15:0]	16
0xBB70264C	GPON_BWMAP_DATA [147].RESERVED[31:16]	16
0xBB70264C	GPON_BWMAP_DATA [147].CAP_DATA[15:0]	16
0xBB702650	GPON_BWMAP_DATA [148].RESERVED[31:16]	16
0xBB702650	GPON_BWMAP_DATA [148].CAP_DATA[15:0]	16
0xBB702654	GPON_BWMAP_DATA [149].RESERVED[31:16]	16
0xBB702654	GPON_BWMAP_DATA [149].CAP_DATA[15:0]	16
0xBB702658	GPON_BWMAP_DATA [150].RESERVED[31:16]	16
0xBB702658	GPON_BWMAP_DATA [150].CAP_DATA[15:0]	16
0xBB70265C	GPON_BWMAP_DATA [151].RESERVED[31:16]	16
0xBB70265C	GPON_BWMAP_DATA [151].CAP_DATA[15:0]	16
0xBB702660	GPON_BWMAP_DATA [152].RESERVED[31:16]	16
0xBB702660	GPON_BWMAP_DATA [152].CAP_DATA[15:0]	16
0xBB702664	GPON_BWMAP_DATA [153].RESERVED[31:16]	16
0xBB702664	GPON_BWMAP_DATA [153].CAP_DATA[15:0]	16
0xBB702668	GPON_BWMAP_DATA [154].RESERVED[31:16]	16
0xBB702668	GPON_BWMAP_DATA [154].CAP_DATA[15:0]	16
0xBB70266C	GPON_BWMAP_DATA [155].RESERVED[31:16]	16
0xBB70266C	GPON_BWMAP_DATA [155].CAP_DATA[15:0]	16
0xBB702670	GPON_BWMAP_DATA [156].RESERVED[31:16]	16
0xBB702670	GPON_BWMAP_DATA [156].CAP_DATA[15:0]	16
0xBB702674	GPON_BWMAP_DATA [157].RESERVED[31:16]	16
0xBB702674	GPON_BWMAP_DATA [157].CAP_DATA[15:0]	16
0xBB702678	GPON_BWMAP_DATA [158].RESERVED[31:16]	16
0xBB702678	GPON_BWMAP_DATA [158].CAP_DATA[15:0]	16
0xBB70267C	GPON_BWMAP_DATA [159].RESERVED[31:16]	16
0xBB70267C	GPON_BWMAP_DATA [159].CAP_DATA[15:0]	16
0xBB702680	GPON_BWMAP_DATA [160].RESERVED[31:16]	16
0xBB702680	GPON_BWMAP_DATA [160].CAP_DATA[15:0]	16
0xBB702684	GPON_BWMAP_DATA [161].RESERVED[31:16]	16
0xBB702684	GPON_BWMAP_DATA [161].CAP_DATA[15:0]	16
0xBB702688	GPON_BWMAP_DATA [162].RESERVED[31:16]	16
0xBB702688	GPON_BWMAP_DATA [162].CAP_DATA[15:0]	16
0xBB70268C	GPON_BWMAP_DATA [163].RESERVED[31:16]	16
0xBB70268C	GPON_BWMAP_DATA [163].CAP_DATA[15:0]	16
0xBB702690	GPON_BWMAP_DATA [164].RESERVED[31:16]	16
0xBB702690	GPON_BWMAP_DATA [164].CAP_DATA[15:0]	16
0xBB702694	GPON_BWMAP_DATA [165].RESERVED[31:16]	16
0xBB702694	GPON_BWMAP_DATA [165].CAP_DATA[15:0]	16
0xBB702698	GPON_BWMAP_DATA [166].RESERVED[31:16]	16
0xBB702698	GPON_BWMAP_DATA [166].CAP_DATA[15:0]	16
0xBB70269C	GPON_BWMAP_DATA [167].RESERVED[31:16]	16
0xBB70269C	GPON_BWMAP_DATA [167].CAP_DATA[15:0]	16
0xBB7026A0	GPON_BWMAP_DATA [168].RESERVED[31:16]	16
0xBB7026A0	GPON_BWMAP_DATA [168].CAP_DATA[15:0]	16



Address	Register	Len
0xBB7026A4	GPON_BWMAP_DATA [169].RESERVED[31:16]	16
0xBB7026A4	GPON_BWMAP_DATA [169].CAP_DATA[15:0]	16
0xBB7026A8	GPON_BWMAP_DATA [170].RESERVED[31:16]	16
0xBB7026A8	GPON_BWMAP_DATA [170].CAP_DATA[15:0]	16
0xBB7026AC	GPON_BWMAP_DATA [171].RESERVED[31:16]	16
0xBB7026AC	GPON_BWMAP_DATA [171].CAP_DATA[15:0]	16
0xBB7026B0	GPON_BWMAP_DATA [172].RESERVED[31:16]	16
0xBB7026B0	GPON_BWMAP_DATA [172].CAP_DATA[15:0]	16
0xBB7026B4	GPON_BWMAP_DATA [173].RESERVED[31:16]	16
0xBB7026B4	GPON_BWMAP_DATA [173].CAP_DATA[15:0]	16
0xBB7026B8	GPON_BWMAP_DATA [174].RESERVED[31:16]	16
0xBB7026B8	GPON_BWMAP_DATA [174].CAP_DATA[15:0]	16
0xBB7026BC	GPON_BWMAP_DATA [175].RESERVED[31:16]	16
0xBB7026BC	GPON_BWMAP_DATA [175].CAP_DATA[15:0]	16
0xBB7026C0	GPON_BWMAP_DATA [176].RESERVED[31:16]	16
0xBB7026C0	GPON_BWMAP_DATA [176].CAP_DATA[15:0]	16
0xBB7026C4	GPON_BWMAP_DATA [177].RESERVED[31:16]	16
0xBB7026C4	GPON_BWMAP_DATA [177].CAP_DATA[15:0]	16
0xBB7026C8	GPON_BWMAP_DATA [178].RESERVED[31:16]	16
0xBB7026C8	GPON_BWMAP_DATA [178].CAP_DATA[15:0]	16
0xBB7026CC	GPON_BWMAP_DATA [179].RESERVED[31:16]	16
0xBB7026CC	GPON_BWMAP_DATA [179].CAP_DATA[15:0]	16
0xBB7026D0	GPON_BWMAP_DATA [180].RESERVED[31:16]	16
0xBB7026D0	GPON_BWMAP_DATA [180].CAP_DATA[15:0]	16
0xBB7026D4	GPON_BWMAP_DATA [181].RESERVED[31:16]	16
0xBB7026D4	GPON_BWMAP_DATA [181].CAP_DATA[15:0]	16
0xBB7026D8	GPON_BWMAP_DATA [182].RESERVED[31:16]	16
0xBB7026D8	GPON_BWMAP_DATA [182].CAP_DATA[15:0]	16
0xBB7026DC	GPON_BWMAP_DATA [183].RESERVED[31:16]	16
0xBB7026DC	GPON_BWMAP_DATA [183].CAP_DATA[15:0]	16
0xBB7026E0	GPON_BWMAP_DATA [184].RESERVED[31:16]	16
0xBB7026E0	GPON_BWMAP_DATA [184].CAP_DATA[15:0]	16
0xBB7026E4	GPON_BWMAP_DATA [185].RESERVED[31:16]	16
0xBB7026E4	GPON_BWMAP_DATA [185].CAP_DATA[15:0]	16
0xBB7026E8	GPON_BWMAP_DATA [186].RESERVED[31:16]	16
0xBB7026E8	GPON_BWMAP_DATA [186].CAP_DATA[15:0]	16
0xBB7026EC	GPON_BWMAP_DATA [187].RESERVED[31:16]	16
0xBB7026EC	GPON_BWMAP_DATA [187].CAP_DATA[15:0]	16
0xBB7026F0	GPON_BWMAP_DATA [188].RESERVED[31:16]	16
0xBB7026F0	GPON_BWMAP_DATA [188].CAP_DATA[15:0]	16
0xBB7026F4	GPON_BWMAP_DATA [189].RESERVED[31:16]	16
0xBB7026F4	GPON_BWMAP_DATA [189].CAP_DATA[15:0]	16
0xBB7026F8	GPON_BWMAP_DATA [190].RESERVED[31:16]	16
0xBB7026F8	GPON_BWMAP_DATA [190].CAP_DATA[15:0]	16
0xBB7026FC	GPON_BWMAP_DATA [191].RESERVED[31:16]	16
0xBB7026FC	GPON_BWMAP_DATA [191].CAP_DATA[15:0]	16

Address	Register	Len
0xBB702700	GPON_BWMAP_DATA [192].RESERVED[31:16]	16
0xBB702700	GPON_BWMAP_DATA [192].CAP_DATA[15:0]	16
0xBB702704	GPON_BWMAP_DATA [193].RESERVED[31:16]	16
0xBB702704	GPON_BWMAP_DATA [193].CAP_DATA[15:0]	16
0xBB702708	GPON_BWMAP_DATA [194].RESERVED[31:16]	16
0xBB702708	GPON_BWMAP_DATA [194].CAP_DATA[15:0]	16
0xBB70270C	GPON_BWMAP_DATA [195].RESERVED[31:16]	16
0xBB70270C	GPON_BWMAP_DATA [195].CAP_DATA[15:0]	16
0xBB702710	GPON_BWMAP_DATA [196].RESERVED[31:16]	16
0xBB702710	GPON_BWMAP_DATA [196].CAP_DATA[15:0]	16
0xBB702714	GPON_BWMAP_DATA [197].RESERVED[31:16]	16
0xBB702714	GPON_BWMAP_DATA [197].CAP_DATA[15:0]	16
0xBB702718	GPON_BWMAP_DATA [198].RESERVED[31:16]	16
0xBB702718	GPON_BWMAP_DATA [198].CAP_DATA[15:0]	16
0xBB70271C	GPON_BWMAP_DATA [199].RESERVED[31:16]	16
0xBB70271C	GPON_BWMAP_DATA [199].CAP_DATA[15:0]	16
0xBB702720	GPON_BWMAP_DATA [200].RESERVED[31:16]	16
0xBB702720	GPON_BWMAP_DATA [200].CAP_DATA[15:0]	16
0xBB702724	GPON_BWMAP_DATA [201].RESERVED[31:16]	16
0xBB702724	GPON_BWMAP_DATA [201].CAP_DATA[15:0]	16
0xBB702728	GPON_BWMAP_DATA [202].RESERVED[31:16]	16
0xBB702728	GPON_BWMAP_DATA [202].CAP_DATA[15:0]	16
0xBB70272C	GPON_BWMAP_DATA [203].RESERVED[31:16]	16
0xBB70272C	GPON_BWMAP_DATA [203].CAP_DATA[15:0]	16
0xBB702730	GPON_BWMAP_DATA [204].RESERVED[31:16]	16
0xBB702730	GPON_BWMAP_DATA [204].CAP_DATA[15:0]	16
0xBB702734	GPON_BWMAP_DATA [205].RESERVED[31:16]	16
0xBB702734	GPON_BWMAP_DATA [205].CAP_DATA[15:0]	16
0xBB702738	GPON_BWMAP_DATA [206].RESERVED[31:16]	16
0xBB702738	GPON_BWMAP_DATA [206].CAP_DATA[15:0]	16
0xBB70273C	GPON_BWMAP_DATA [207].RESERVED[31:16]	16
0xBB70273C	GPON_BWMAP_DATA [207].CAP_DATA[15:0]	16
0xBB702740	GPON_BWMAP_DATA [208].RESERVED[31:16]	16
0xBB702740	GPON_BWMAP_DATA [208].CAP_DATA[15:0]	16
0xBB702744	GPON_BWMAP_DATA [209].RESERVED[31:16]	16
0xBB702744	GPON_BWMAP_DATA [209].CAP_DATA[15:0]	16
0xBB702748	GPON_BWMAP_DATA [210].RESERVED[31:16]	16
0xBB702748	GPON_BWMAP_DATA [210].CAP_DATA[15:0]	16
0xBB70274C	GPON_BWMAP_DATA [211].RESERVED[31:16]	16
0xBB70274C	GPON_BWMAP_DATA [211].CAP_DATA[15:0]	16
0xBB702750	GPON_BWMAP_DATA [212].RESERVED[31:16]	16
0xBB702750	GPON_BWMAP_DATA [212].CAP_DATA[15:0]	16
0xBB702754	GPON_BWMAP_DATA [213].RESERVED[31:16]	16
0xBB702754	GPON_BWMAP_DATA [213].CAP_DATA[15:0]	16
0xBB702758	GPON_BWMAP_DATA [214].RESERVED[31:16]	16
0xBB702758	GPON_BWMAP_DATA [214].CAP_DATA[15:0]	16

Address	Register	Len
0xBB70275C	GPON_BWMAP_DATA [215].RESERVED[31:16]	16
0xBB70275C	GPON_BWMAP_DATA [215].CAP_DATA[15:0]	16
0xBB702760	GPON_BWMAP_DATA [216].RESERVED[31:16]	16
0xBB702760	GPON_BWMAP_DATA [216].CAP_DATA[15:0]	16
0xBB702764	GPON_BWMAP_DATA [217].RESERVED[31:16]	16
0xBB702764	GPON_BWMAP_DATA [217].CAP_DATA[15:0]	16
0xBB702768	GPON_BWMAP_DATA [218].RESERVED[31:16]	16
0xBB702768	GPON_BWMAP_DATA [218].CAP_DATA[15:0]	16
0xBB70276C	GPON_BWMAP_DATA [219].RESERVED[31:16]	16
0xBB70276C	GPON_BWMAP_DATA [219].CAP_DATA[15:0]	16
0xBB702770	GPON_BWMAP_DATA [220].RESERVED[31:16]	16
0xBB702770	GPON_BWMAP_DATA [220].CAP_DATA[15:0]	16
0xBB702774	GPON_BWMAP_DATA [221].RESERVED[31:16]	16
0xBB702774	GPON_BWMAP_DATA [221].CAP_DATA[15:0]	16
0xBB702778	GPON_BWMAP_DATA [222].RESERVED[31:16]	16
0xBB702778	GPON_BWMAP_DATA [222].CAP_DATA[15:0]	16
0xBB70277C	GPON_BWMAP_DATA [223].RESERVED[31:16]	16
0xBB70277C	GPON_BWMAP_DATA [223].CAP_DATA[15:0]	16
0xBB702780	GPON_BWMAP_DATA [224].RESERVED[31:16]	16
0xBB702780	GPON_BWMAP_DATA [224].CAP_DATA[15:0]	16
0xBB702784	GPON_BWMAP_DATA [225].RESERVED[31:16]	16
0xBB702784	GPON_BWMAP_DATA [225].CAP_DATA[15:0]	16
0xBB702788	GPON_BWMAP_DATA [226].RESERVED[31:16]	16
0xBB702788	GPON_BWMAP_DATA [226].CAP_DATA[15:0]	16
0xBB70278C	GPON_BWMAP_DATA [227].RESERVED[31:16]	16
0xBB70278C	GPON_BWMAP_DATA [227].CAP_DATA[15:0]	16
0xBB702790	GPON_BWMAP_DATA [228].RESERVED[31:16]	16
0xBB702790	GPON_BWMAP_DATA [228].CAP_DATA[15:0]	16
0xBB702794	GPON_BWMAP_DATA [229].RESERVED[31:16]	16
0xBB702794	GPON_BWMAP_DATA [229].CAP_DATA[15:0]	16
0xBB702798	GPON_BWMAP_DATA [230].RESERVED[31:16]	16
0xBB702798	GPON_BWMAP_DATA [230].CAP_DATA[15:0]	16
0xBB70279C	GPON_BWMAP_DATA [231].RESERVED[31:16]	16
0xBB70279C	GPON_BWMAP_DATA [231].CAP_DATA[15:0]	16
0xBB7027A0	GPON_BWMAP_DATA [232].RESERVED[31:16]	16
0xBB7027A0	GPON_BWMAP_DATA [232].CAP_DATA[15:0]	16
0xBB7027A4	GPON_BWMAP_DATA [233].RESERVED[31:16]	16
0xBB7027A4	GPON_BWMAP_DATA [233].CAP_DATA[15:0]	16
0xBB7027A8	GPON_BWMAP_DATA [234].RESERVED[31:16]	16
0xBB7027A8	GPON_BWMAP_DATA [234].CAP_DATA[15:0]	16
0xBB7027AC	GPON_BWMAP_DATA [235].RESERVED[31:16]	16
0xBB7027AC	GPON_BWMAP_DATA [235].CAP_DATA[15:0]	16
0xBB7027B0	GPON_BWMAP_DATA [236].RESERVED[31:16]	16
0xBB7027B0	GPON_BWMAP_DATA [236].CAP_DATA[15:0]	16
0xBB7027B4	GPON_BWMAP_DATA [237].RESERVED[31:16]	16
0xBB7027B4	GPON_BWMAP_DATA [237].CAP_DATA[15:0]	16

Address	Register	Len
0xBB7027B8	GPON_BWMAP_DATA [238].RESERVED[31:16]	16
0xBB7027B8	GPON_BWMAP_DATA [238].CAP_DATA[15:0]	16
0xBB7027BC	GPON_BWMAP_DATA [239].RESERVED[31:16]	16
0xBB7027BC	GPON_BWMAP_DATA [239].CAP_DATA[15:0]	16
0xBB7027C0	GPON_BWMAP_DATA [240].RESERVED[31:16]	16
0xBB7027C0	GPON_BWMAP_DATA [240].CAP_DATA[15:0]	16
0xBB7027C4	GPON_BWMAP_DATA [241].RESERVED[31:16]	16
0xBB7027C4	GPON_BWMAP_DATA [241].CAP_DATA[15:0]	16
0xBB7027C8	GPON_BWMAP_DATA [242].RESERVED[31:16]	16
0xBB7027C8	GPON_BWMAP_DATA [242].CAP_DATA[15:0]	16
0xBB7027CC	GPON_BWMAP_DATA [243].RESERVED[31:16]	16
0xBB7027CC	GPON_BWMAP_DATA [243].CAP_DATA[15:0]	16
0xBB7027D0	GPON_BWMAP_DATA [244].RESERVED[31:16]	16
0xBB7027D0	GPON_BWMAP_DATA [244].CAP_DATA[15:0]	16
0xBB7027D4	GPON_BWMAP_DATA [245].RESERVED[31:16]	16
0xBB7027D4	GPON_BWMAP_DATA [245].CAP_DATA[15:0]	16
0xBB7027D8	GPON_BWMAP_DATA [246].RESERVED[31:16]	16
0xBB7027D8	GPON_BWMAP_DATA [246].CAP_DATA[15:0]	16
0xBB7027DC	GPON_BWMAP_DATA [247].RESERVED[31:16]	16
0xBB7027DC	GPON_BWMAP_DATA [247].CAP_DATA[15:0]	16
0xBB7027E0	GPON_BWMAP_DATA [248].RESERVED[31:16]	16
0xBB7027E0	GPON_BWMAP_DATA [248].CAP_DATA[15:0]	16
0xBB7027E4	GPON_BWMAP_DATA [249].RESERVED[31:16]	16
0xBB7027E4	GPON_BWMAP_DATA [249].CAP_DATA[15:0]	16
0xBB7027E8	GPON_BWMAP_DATA [250].RESERVED[31:16]	16
0xBB7027E8	GPON_BWMAP_DATA [250].CAP_DATA[15:0]	16
0xBB7027EC	GPON_BWMAP_DATA [251].RESERVED[31:16]	16
0xBB7027EC	GPON_BWMAP_DATA [251].CAP_DATA[15:0]	16
0xBB7027F0	GPON_BWMAP_DATA [252].RESERVED[31:16]	16
0xBB7027F0	GPON_BWMAP_DATA [252].CAP_DATA[15:0]	16
0xBB7027F4	GPON_BWMAP_DATA [253].RESERVED[31:16]	16
0xBB7027F4	GPON_BWMAP_DATA [253].CAP_DATA[15:0]	16
0xBB7027F8	GPON_BWMAP_DATA [254].RESERVED[31:16]	16
0xBB7027F8	GPON_BWMAP_DATA [254].CAP_DATA[15:0]	16
0xBB7027FC	GPON_BWMAP_DATA [255].RESERVED[31:16]	16
0xBB7027FC	GPON_BWMAP_DATA [255].CAP_DATA[15:0]	16
0xBB703000	GPON_AES_INTR_DLT.RESERVED[31:16]	16
0xBB703000	GPON_AES_INTR_DLT.AES_DECRYPT_INTR[15:15]	1
0xBB703000	GPON_AES_INTR_DLT.RESERVED[14:2]	13
0xBB703000	GPON_AES_INTR_DLT.INFO_FIFO_OVERFL_DLT[1:1]	1
0xBB703000	GPON_AES_INTR_DLT.DATA_FIFO_OVERFL_DLT[0:0]	1
0xBB703004	GPON_AES_INTR_MASK.RESERVED[31:2]	30
0xBB703004	GPON_AES_INTR_MASK.INFO_FIFO_OVERFL_M[1:1]	1
0xBB703004	GPON_AES_INTR_MASK.DATA_FIFO_OVERFL_M[0:0]	1
0xBB703008	GPON_AES_INTR_STS.RESERVED[31:2]	30
0xBB703008	GPON_AES_INTR_STS.INFO_FIFO_OVERFL[1:1]	1

Address	Register	Len
0xBB703008	GPON_AES_INTR_STS.DATA_FIFO_OVERFL[0:0]	1
0xBB703010	GPON_AES_KEY_SWITCH_REQ.RESERVED[31:16]	16
0xBB703010	GPON_AES_KEY_SWITCH_REQ.KEY_CFG_REQ[15:15]	1
0xBB703010	GPON_AES_KEY_SWITCH_REQ.CFG_ACTIVE_KEY[14:14]	1
0xBB703010	GPON_AES_KEY_SWITCH_REQ.RESERVED[13:0]	14
0xBB703014	GPON_AES_KEY_SWITCH_TIME.RESERVED[31:30]	2
0xBB703014	GPON_AES_KEY_SWITCH_TIME.SWITCH_SUPERFRAME[29:0]	30
0xBB703020	GPON_AES_KEY_WORD_IND.RESERVED[31:16]	16
0xBB703020	GPON_AES_KEY_WORD_IND.KEY_WR_REQ[15:15]	1
0xBB703020	GPON_AES_KEY_WORD_IND.KEY_WR_COMPL[14:14]	1
0xBB703020	GPON_AES_KEY_WORD_IND.RESERVED[13:8]	6
0xBB703020	GPON_AES_KEY_WORD_IND.KEY_USE_IND[7:7]	1
0xBB703020	GPON_AES_KEY_WORD_IND.RESERVED[6:3]	4
0xBB703020	GPON_AES_KEY_WORD_IND.KEY_WORD_IDX[2:0]	3
0xBB703024	GPON_AES_WORD_DATA.RESERVED[31:16]	16
0xBB703024	GPON_AES_WORD_DATA.KEY_DATA[15:0]	16
0xBB704040	GPON_GEM_DS_RX_CNTR_IND.RESERVED[31:16]	16
0xBB704040	GPON_GEM_DS_RX_CNTR_IND.ETH_PKT_RX_R_ACK[15:15]	1
0xBB704040	GPON_GEM_DS_RX_CNTR_IND.RESERVED[14:7]	8
0xBB704040	GPON_GEM_DS_RX_CNTR_IND.ETH_PKT_RX_IDX[6:0]	7
0xBB704044	GPON_GEM_DS_RX_CNTR_STAT.ETH_PKT_RX[31:0]	32
0xBB70404C	GPON_GEM_DS_FWD_CNTR_IND.RESERVED[31:16]	16
0xBB70404C	GPON_GEM_DS_FWD_CNTR_IND.ETH_PKT_FWD_R_ACK[15:15]	1
0xBB70404C	GPON_GEM_DS_FWD_CNTR_IND.RESERVED[14:7]	8
0xBB70404C	GPON_GEM_DS_FWD_CNTR_IND.ETH_PKT_FWD_IDX[6:0]	7
0xBB704050	GPON_GEM_DS_FWD_CNTR_STAT.ETH_PKT_FWD[31:0]	32
0xBB704064	GPON_GEM_DS_MISC_IND.RESERVED[31:4]	28
0xBB704064	GPON_GEM_DS_MISC_IND.MISC_CNTR_IDX[3:0]	4
0xBB704068	GPON_GEM_DS_MISC_CNTR_STAT.MISC_CNTR[31:0]	32
0xBB704080	GPON_GEM_DS_MC_CFG.RESERVED[31:11]	21
0xBB704080	GPON_GEM_DS_MC_CFG.IPV6_MC_FORCE_PASS[10:10]	1
0xBB704080	GPON_GEM_DS_MC_CFG.IPV6_MC_FORCE_DROP[9:9]	1
0xBB704080	GPON_GEM_DS_MC_CFG.RESERVED[8:7]	2
0xBB704080	GPON_GEM_DS_MC_CFG.BROADCAST_PASS[6:6]	1
0xBB704080	GPON_GEM_DS_MC_CFG.RESERVED[5:5]	1
0xBB704080	GPON_GEM_DS_MC_CFG.NON_MULTICAST_PASS[4:4]	1
0xBB704080	GPON_GEM_DS_MC_CFG.FCS_CHK_EN[3:3]	1
0xBB704080	GPON_GEM_DS_MC_CFG.IPV4_MC_FORCE_PASS[2:2]	1
0xBB704080	GPON_GEM_DS_MC_CFG.IPV4_MC_FORCE_DROP[1:1]	1
0xBB704080	GPON_GEM_DS_MC_CFG.MC_EXCL_MODE[0:0]	1
0xBB704084	GPON_GEM_DS_MC_IND.RESERVED[31:16]	16
0xBB704084	GPON_GEM_DS_MC_IND.MC_ITEM_OP_REQ[15:15]	1
0xBB704084	GPON_GEM_DS_MC_IND.MC_ITEM_OP_COMPL[14:14]	1
0xBB704084	GPON_GEM_DS_MC_IND.MC_ITEM_OP_HIT[13:13]	1
0xBB704084	GPON_GEM_DS_MC_IND.RESERVED[12:10]	3
0xBB704084	GPON_GEM_DS_MC_IND.MC_ITEM_OP_MODE[9:8]	2

Address	Register	Len
0xBB704084	GPON_GEM_DS_MC_IND.MC_ITEM_OP_IDX[7:0]	8
0xBB704088	GPON_GEM_DS_MC_WR.MC_ITEM_OP_WDATA[31:0]	32
0xBB704090	GPON_GEM_DS_MC_RD.MC_ITEM_OP_RDATA[31:0]	32
0xBB704098	GPON_GEM_DS_FRM_TIMEOUT.RESERVED[31:9]	23
0xBB704098	GPON_GEM_DS_FRM_TIMEOUT.OMCI_TR_MODE[8:8]	1
0xBB704098	GPON_GEM_DS_FRM_TIMEOUT.RESERVED[7:5]	3
0xBB704098	GPON_GEM_DS_FRM_TIMEOUT.ASSM_TIMEOUT_FRM[4:0]	5
0xBB70409C	GPON_GEM_DS_MC_ADDR_PTN_IPV4.RESERVED[31:24]	8
0xBB70409C	GPON_GEM_DS_MC_ADDR_PTN_IPV4.IPV4_MC_MAC_PREFIX[23:0]	24
0xBB7040A0	GPON_GEM_DS_MC_ADDR_PTN_IPV6.RESERVED[31:16]	16
0xBB7040A0	GPON_GEM_DS_MC_ADDR_PTN_IPV6.IPV6_MC_MAC_PREFIX[15:0]	16
0xBB705000	GPON_GTC_US_INTR_DLT.RESERVED[31:16]	16
0xBB705000	GPON_GTC_US_INTR_DLT.GTC_US_INTR[15:15]	1
0xBB705000	GPON_GTC_US_INTR_DLT.RESERVED[14:10]	5
0xBB705000	GPON_GTC_US_INTR_DLT.OPTIC_SD_MISM_DLT[9:9]	1
0xBB705000	GPON_GTC_US_INTR_DLT.OPTIC_SD_TOOLONG_DLT[8:8]	1
0xBB705000	GPON_GTC_US_INTR_DLT.PLM_NRM_EMPTY_DLT[7:7]	1
0xBB705000	GPON_GTC_US_INTR_DLT.RESERVED[6:6]	1
0xBB705000	GPON_GTC_US_INTR_DLT.PLM_URG_EMPTY_DLT[5:5]	1
0xBB705000	GPON_GTC_US_INTR_DLT.RESERVED[4:3]	2
0xBB705000	GPON_GTC_US_INTR_DLT.US_FEC_STS_DLT[2:2]	1
0xBB705000	GPON_GTC_US_INTR_DLT.RESERVED[1:1]	1
0xBB705000	GPON_GTC_US_INTR_DLT.DG_MSG_TX_DLT[0:0]	1
0xBB705004	GPON_GTC_US_INTR_MASK.RESERVED[31:10]	22
0xBB705004	GPON_GTC_US_INTR_MASK.OPTIC_SD_MISM_M[9:9]	1
0xBB705004	GPON_GTC_US_INTR_MASK.OPTIC_SD_TOOLONG_M[8:8]	1
0xBB705004	GPON_GTC_US_INTR_MASK.PLM_NRM_EMPTY_M[7:7]	1
0xBB705004	GPON_GTC_US_INTR_MASK.RESERVED[6:6]	1
0xBB705004	GPON_GTC_US_INTR_MASK.PLM_URG_EMPTY_M[5:5]	1
0xBB705004	GPON_GTC_US_INTR_MASK.RESERVED[4:3]	2
0xBB705004	GPON_GTC_US_INTR_MASK.US_FEC_STS_M[2:2]	1
0xBB705004	GPON_GTC_US_INTR_MASK.RESERVED[1:1]	1
0xBB705004	GPON_GTC_US_INTR_MASK.DG_MSG_TX_M[0:0]	1
0xBB705008	GPON_GTC_US_INTR_STS.RESERVED[31:3]	29
0xBB705008	GPON_GTC_US_INTR_STS.US_FEC_STS[2:2]	1
0xBB705008	GPON_GTC_US_INTR_STS.RESERVED[1:0]	2
0xBB705010	GPON_GTC_US_ONU_ID.RESERVED[31:16]	16
0xBB705010	GPON_GTC_US_ONU_ID.ONU_ID[15:8]	8
0xBB705010	GPON_GTC_US_ONU_ID.RESERVED[7:0]	8
0xBB705014	GPON_GTC_US_CFG.RESERVED[31:16]	16
0xBB705014	GPON_GTC_US_CFG.FS_LON[15:15]	1
0xBB705014	GPON_GTC_US_CFG.FS_LOFF[14:14]	1
0xBB705014	GPON_GTC_US_CFG.RESERVED[13:11]	3
0xBB705014	GPON_GTC_US_CFG.IND_NRM_PLM[10:10]	1
0xBB705014	GPON_GTC_US_CFG.PLM_DIS[9:9]	1
0xBB705014	GPON_GTC_US_CFG.DBRU_DIS[8:8]	1



Address	Register	Len
0xBB705014	GPON_GTC_US_CFG.RESERVED[7:5]	3
0xBB705014	GPON_GTC_US_CFG.ENA_AUTO_DG[4:4]	1
0xBB705014	GPON_GTC_US_CFG.US_BEN_POLAR[3:3]	1
0xBB705014	GPON_GTC_US_CFG.RESERVED[2:1]	2
0xBB705014	GPON_GTC_US_CFG.SCRM_DIS[0:0]	1
0xBB705018	GPON_GTC_US_WRITE_PROTECT.RESERVED[31:16]	16
0xBB705018	GPON_GTC_US_WRITE_PROTECT.RSV_REG_WRITE_PROTECTION[15:0]	16
0xBB705020	GPON_GTC_US_TX_PATTERN_CTL.RESERVED[31:9]	23
0xBB705020	GPON_GTC_US_TX_PATTERN_CTL.TX_PATTERN_MODE_NO_FG[8:8]	1
0xBB705020	GPON_GTC_US_TX_PATTERN_CTL.RESERVED[7:6]	2
0xBB705020	GPON_GTC_US_TX_PATTERN_CTL.TX_PATTERN_MODE_BG[5:4]	2
0xBB705020	GPON_GTC_US_TX_PATTERN_CTL.RESERVED[3:2]	2
0xBB705020	GPON_GTC_US_TX_PATTERN_CTL.TX_PATTERN_MODE_FG[1:0]	2
0xBB705024	GPON_GTC_US_TX_PATTERN_BG.TX_PATTERN_BG[31:0]	32
0xBB705028	GPON_GTC_US_TX_PATTERN_FG.TX_PATTERN_FG[31:0]	32
0xBB705040	GPON_GTC_US_MIN_DELAY.RESERVED[31:16]	16
0xBB705040	GPON_GTC_US_MIN_DELAY.MIN_DELAY1[15:7]	9
0xBB705040	GPON_GTC_US_MIN_DELAY.MIN_DELAY2[6:0]	7
0xBB705044	GPON_GTC_US_EQD.RESERVED[31:27]	5
0xBB705044	GPON_GTC_US_EQD.EQD1_MULTIFRAME[26:24]	3
0xBB705044	GPON_GTC_US_EQD.RESERVED[23:18]	6
0xBB705044	GPON_GTC_US_EQD.EQD1_INFRAME[17:0]	18
0xBB70504C	GPON_GTC_US_LASER.RESERVED[31:14]	18
0xBB70504C	GPON_GTC_US_LASER.LON_TIME[13:8]	6
0xBB70504C	GPON_GTC_US_LASER.RESERVED[7:6]	2
0xBB70504C	GPON_GTC_US_LASER.LOFF_TIME[5:0]	6
0xBB705054	GPON_GTC_US_BOH_CFG.RESERVED[31:12]	20
0xBB705054	GPON_GTC_US_BOH_CFG.BOH_REPEAT[11:8]	4
0xBB705054	GPON_GTC_US_BOH_CFG.BOH_LENGTH[7:0]	8
0xBB705080	GPON_GTC_US_BOH_DATA [0].RESERVED[31:8]	24
0xBB705080	GPON_GTC_US_BOH_DATA [0].BOH_DATA[7:0]	8
0xBB705084	GPON_GTC_US_BOH_DATA [1].RESERVED[31:8]	24
0xBB705084	GPON_GTC_US_BOH_DATA [1].BOH_DATA[7:0]	8
0xBB705088	GPON_GTC_US_BOH_DATA [2].RESERVED[31:8]	24
0xBB705088	GPON_GTC_US_BOH_DATA [2].BOH_DATA[7:0]	8
0xBB70508C	GPON_GTC_US_BOH_DATA [3].RESERVED[31:8]	24
0xBB70508C	GPON_GTC_US_BOH_DATA [3].BOH_DATA[7:0]	8
0xBB705090	GPON_GTC_US_BOH_DATA [4].RESERVED[31:8]	24
0xBB705090	GPON_GTC_US_BOH_DATA [4].BOH_DATA[7:0]	8
0xBB705094	GPON_GTC_US_BOH_DATA [5].RESERVED[31:8]	24
0xBB705094	GPON_GTC_US_BOH_DATA [5].BOH_DATA[7:0]	8
0xBB705098	GPON_GTC_US_BOH_DATA [6].RESERVED[31:8]	24
0xBB705098	GPON_GTC_US_BOH_DATA [6].BOH_DATA[7:0]	8
0xBB70509C	GPON_GTC_US_BOH_DATA [7].RESERVED[31:8]	24
0xBB70509C	GPON_GTC_US_BOH_DATA [7].BOH_DATA[7:0]	8
0xBB7050A0	GPON_GTC_US_BOH_DATA [8].RESERVED[31:8]	24

Address	Register	Len
0xBB7050A0	GPON_GTC_US_BOH_DATA [8].BOH_DATA[7:0]	8
0xBB7050A4	GPON_GTC_US_BOH_DATA [9].RESERVED[31:8]	24
0xBB7050A4	GPON_GTC_US_BOH_DATA [9].BOH_DATA[7:0]	8
0xBB7050A8	GPON_GTC_US_BOH_DATA [10].RESERVED[31:8]	24
0xBB7050A8	GPON_GTC_US_BOH_DATA [10].BOH_DATA[7:0]	8
0xBB7050AC	GPON_GTC_US_BOH_DATA [11].RESERVED[31:8]	24
0xBB7050AC	GPON_GTC_US_BOH_DATA [11].BOH_DATA[7:0]	8
0xBB7050C0	GPON_GTC_US_PLOAM_IND.RESERVED[31:11]	21
0xBB7050C0	GPON_GTC_US_PLOAM_IND.PLM_TYPE[10:8]	3
0xBB7050C0	GPON_GTC_US_PLOAM_IND.PLM_NRM_EMPTY[7:7]	1
0xBB7050C0	GPON_GTC_US_PLOAM_IND.PLM_NRM_FULL[6:6]	1
0xBB7050C0	GPON_GTC_US_PLOAM_IND.PLM_URG_EMPTY[5:5]	1
0xBB7050C0	GPON_GTC_US_PLOAM_IND.PLM_URG_FULL[4:4]	1
0xBB7050C0	GPON_GTC_US_PLOAM_IND.RESERVED[3:1]	3
0xBB7050C0	GPON_GTC_US_PLOAM_IND.PLM_ENQ[0:0]	1
0xBB7050E0	GPON_GTC_US_PLOAM_DATA [0].RESERVED[31:16]	16
0xBB7050E0	GPON_GTC_US_PLOAM_DATA [0].PLM_DATA[15:0]	16
0xBB7050E4	GPON_GTC_US_PLOAM_DATA [1].RESERVED[31:16]	16
0xBB7050E4	GPON_GTC_US_PLOAM_DATA [1].PLM_DATA[15:0]	16
0xBB7050E8	GPON_GTC_US_PLOAM_DATA [2].RESERVED[31:16]	16
0xBB7050E8	GPON_GTC_US_PLOAM_DATA [2].PLM_DATA[15:0]	16
0xBB7050EC	GPON_GTC_US_PLOAM_DATA [3].RESERVED[31:16]	16
0xBB7050EC	GPON_GTC_US_PLOAM_DATA [3].PLM_DATA[15:0]	16
0xBB7050F0	GPON_GTC_US_PLOAM_DATA [4].RESERVED[31:16]	16
0xBB7050F0	GPON_GTC_US_PLOAM_DATA [4].PLM_DATA[15:0]	16
0xBB7050F4	GPON_GTC_US_PLOAM_DATA [5].RESERVED[31:16]	16
0xBB7050F4	GPON_GTC_US_PLOAM_DATA [5].PLM_DATA[15:0]	16
0xBB7050F8	GPON_GTC_US_PLOAM_DATA [6].RESERVED[31:16]	16
0xBB7050F8	GPON_GTC_US_PLOAM_DATA [6].PLM_DATA[15:0]	16
0xBB7050FC	GPON_GTC_US_PLOAM_DATA [7].RESERVED[31:16]	16
0xBB7050FC	GPON_GTC_US_PLOAM_DATA [7].PLM_DATA[15:0]	16
0xBB705100	GPON_GTC_US_PLOAM_CFG.RESERVED[31:5]	27
0xBB705100	GPON_GTC_US_PLOAM_CFG.PLM_FLUSH_BUF[4:4]	1
0xBB705100	GPON_GTC_US_PLOAM_CFG.RESERVED[3:2]	2
0xBB705100	GPON_GTC_US_PLOAM_CFG.PLM_US_CRC_GEN_EN[1:1]	1
0xBB705100	GPON_GTC_US_PLOAM_CFG.PLM_US_ONUID_OVRD_EN[0:0]	1
0xBB705140	GPON_GTC_US_MISC_CNTR_IDX.RESERVED[31:3]	29
0xBB705140	GPON_GTC_US_MISC_CNTR_IDX.MISC_IDX[2:0]	3
0xBB705148	GPON_GTC_US_MISC_CNTR_STAT.MISC_CNTR[31:0]	32
0xBB705180	GPON_GTC_US_RDI.RESERVED[31:1]	31
0xBB705180	GPON_GTC_US_RDI.ONU_RDI[0:0]	1
0xBB705184	GPON_GTC_US_DG.RESERVED[31:9]	23
0xBB705184	GPON_GTC_US_DG.DG_STATUS[8:8]	1
0xBB705184	GPON_GTC_US_DG.DG_MSG_TX_CNT[7:4]	4
0xBB705184	GPON_GTC_US_DG.DG_MSG_TX_CNT_THRESHOLD[3:0]	4
0xBB705188	GPON_GTC_US_OPTIC_SD_TH.RESERVED[31:31]	1



Address	Register	Len
0xBB705188	GPON_GTC_US_OPTIC_SD_TH.OPTIC_SD_MISM_THREH[30:16]	15
0xBB705188	GPON_GTC_US_OPTIC_SD_TH.RESERVED[15:15]	1
0xBB705188	GPON_GTC_US_OPTIC_SD_TH.OPTIC_SD_TOOLONG_THRESH[14:0]	15
0xBB705200	GPON_GTC_US_PROC_MODE.RESERVED[31:2]	30
0xBB705200	GPON_GTC_US_PROC_MODE.OPTIC_AUTO_SUPPRESS_DIS[1:1]	1
0xBB705200	GPON_GTC_US_PROC_MODE.AUTO_PROC_SSTART[0:0]	1
0xBB706000	GPON_GEM_US_INTR_DLT.GEM_US_INTR[31:31]	1
0xBB706000	GPON_GEM_US_INTR_DLT.RESERVED[30:10]	21
0xBB706000	GPON_GEM_US_INTR_DLT.SD_VALID_LONG_DLT[9:9]	1
0xBB706000	GPON_GEM_US_INTR_DLT.SD_DIFF_HUGE_DLT[8:8]	1
0xBB706000	GPON_GEM_US_INTR_DLT.REQUEST_DELAY_DLT[7:7]	1
0xBB706000	GPON_GEM_US_INTR_DLT.BC_LESS6_DLT[6:6]	1
0xBB706000	GPON_GEM_US_INTR_DLT.ERR_PLI_DLT[5:5]	1
0xBB706000	GPON_GEM_US_INTR_DLT.BURST_TM_LARGER_GTC_DLT[4:4]	1
0xBB706000	GPON_GEM_US_INTR_DLT.BANK_TOO_MUCH_AT_END_DLT[3:3]	1
0xBB706000	GPON_GEM_US_INTR_DLT.BANK_REMAIN_AFRD_DLT[2:2]	1
0xBB706000	GPON_GEM_US_INTR_DLT.BANK_OVERFL_DLT[1:1]	1
0xBB706000	GPON_GEM_US_INTR_DLT.BANK_UNDERFL_DLT[0:0]	1
0xBB706004	GPON_GEM_US_INTR_MASK.RESERVED[31:10]	22
0xBB706004	GPON_GEM_US_INTR_MASK.SD_VALID_LONG_M[9:9]	1
0xBB706004	GPON_GEM_US_INTR_MASK.SD_DIFF_HUGE_M[8:8]	1
0xBB706004	GPON_GEM_US_INTR_MASK.REQUEST_DELAY_M[7:7]	1
0xBB706004	GPON_GEM_US_INTR_MASK.BC_LESS6_M[6:6]	1
0xBB706004	GPON_GEM_US_INTR_MASK.ERR_PLI_M[5:5]	1
0xBB706004	GPON_GEM_US_INTR_MASK.BURST_TM_LARGER_GTC_M[4:4]	1
0xBB706004	GPON_GEM_US_INTR_MASK.BANK_TOO_MUCH_AT_END_M[3:3]	1
0xBB706004	GPON_GEM_US_INTR_MASK.BANK_REMAIN_AFRD_M[2:2]	1
0xBB706004	GPON_GEM_US_INTR_MASK.BANK_OVERFL_M[1:1]	1
0xBB706004	GPON_GEM_US_INTR_MASK.BANK_UNDERFL_M[0:0]	1
0xBB706008	GPON_GEM_US_INTR_STS.RESERVED[31:10]	22
0xBB706008	GPON_GEM_US_INTR_STS.SD_VALID_LONG_IND[9:9]	1
0xBB706008	GPON_GEM_US_INTR_STS.SD_DIFF_HUGE_IND[8:8]	1
0xBB706008	GPON_GEM_US_INTR_STS.REQUEST_DELAY_IND[7:7]	1
0xBB706008	GPON_GEM_US_INTR_STS.BC_LESS6_IND[6:6]	1
0xBB706008	GPON_GEM_US_INTR_STS.ERR_PLI_IND[5:5]	1
0xBB706008	GPON_GEM_US_INTR_STS.BURST_TM_LARGER_GTC_IND[4:4]	1
0xBB706008	GPON_GEM_US_INTR_STS.BANK_TOO_INDUCH_AT_END_IND[3:3]	1
0xBB706008	GPON_GEM_US_INTR_STS.BANK_REMAIN_AFRD_IND[2:2]	1
0xBB706008	GPON_GEM_US_INTR_STS.BANK_OVERFL_IND[1:1]	1
0xBB706008	GPON_GEM_US_INTR_STS.BANK_UNDERFL_IND[0:0]	1
0xBB706020	GPON_GEM_US_PTI_CFG.FS_GEM_IDLE[31:31]	1
0xBB706020	GPON_GEM_US_PTI_CFG.RESERVED[30:15]	16
0xBB706020	GPON_GEM_US_PTI_CFG.PTI_VECTOR3[14:12]	3
0xBB706020	GPON_GEM_US_PTI_CFG.RESERVED[11:11]	1
0xBB706020	GPON_GEM_US_PTI_CFG.PTI_VECTOR2[10:8]	3
0xBB706020	GPON_GEM_US_PTI_CFG.RESERVED[7:7]	1

Address	Register	Len
0xBB706020	GPON_GEM_US_PTI_CFG.PTI_VECTOR1[6:4]	3
0xBB706020	GPON_GEM_US_PTI_CFG.RESERVED[3:3]	1
0xBB706020	GPON_GEM_US_PTI_CFG.PTI_VECTOR0[2:0]	3
0xBB706048	GPON_GEM_US_ETH_GEM_RX_CNTR_IDX.RESERVED[31:16]	16
0xBB706048	GPON_GEM_US_ETH_GEM_RX_CNTR_IDX.ETH_GEM_RX_R_ACK[15:15]	1
0xBB706048	GPON_GEM_US_ETH_GEM_RX_CNTR_IDX.RESERVED[14:8]	7
0xBB706048	GPON_GEM_US_ETH_GEM_RX_CNTR_IDX.ETH_GEM_RX_IDX[7:0]	8
0xBB70604C	GPON_GEM_US_ETH_GEM_RX_CNTR_STAT.ETH_GEM_RX_CNTR[31:0]	32
0xBB706054	GPON_GEM_US_PTN_CTRL.RESERVED[31:17]	15
0xBB706054	GPON_GEM_US_PTN_CTRL.DEBUG_BUS_SEL[16:16]	1
0xBB706054	GPON_GEM_US_PTN_CTRL.RESERVED[15:10]	6
0xBB706054	GPON_GEM_US_PTN_CTRL.GEM_PTN_MODE[9:8]	2
0xBB706054	GPON_GEM_US_PTN_CTRL.GEM_PTN_BYTE[7:0]	8
0xBB706400	GPON_GEM_US_PORT_MAP [0].RESERVED[31:12]	20
0xBB706400	GPON_GEM_US_PORT_MAP [0].PORT_CFG_DATA[11:0]	12
0xBB706404	GPON_GEM_US_PORT_MAP [1].RESERVED[31:12]	20
0xBB706404	GPON_GEM_US_PORT_MAP [1].PORT_CFG_DATA[11:0]	12
0xBB706408	GPON_GEM_US_PORT_MAP [2].RESERVED[31:12]	20
0xBB706408	GPON_GEM_US_PORT_MAP [2].PORT_CFG_DATA[11:0]	12
0xBB70640C	GPON_GEM_US_PORT_MAP [3].RESERVED[31:12]	20
0xBB70640C	GPON_GEM_US_PORT_MAP [3].PORT_CFG_DATA[11:0]	12
0xBB706410	GPON_GEM_US_PORT_MAP [4].RESERVED[31:12]	20
0xBB706410	GPON_GEM_US_PORT_MAP [4].PORT_CFG_DATA[11:0]	12
0xBB706414	GPON_GEM_US_PORT_MAP [5].RESERVED[31:12]	20
0xBB706414	GPON_GEM_US_PORT_MAP [5].PORT_CFG_DATA[11:0]	12
0xBB706418	GPON_GEM_US_PORT_MAP [6].RESERVED[31:12]	20
0xBB706418	GPON_GEM_US_PORT_MAP [6].PORT_CFG_DATA[11:0]	12
0xBB70641C	GPON_GEM_US_PORT_MAP [7].RESERVED[31:12]	20
0xBB70641C	GPON_GEM_US_PORT_MAP [7].PORT_CFG_DATA[11:0]	12
0xBB706420	GPON_GEM_US_PORT_MAP [8].RESERVED[31:12]	20
0xBB706420	GPON_GEM_US_PORT_MAP [8].PORT_CFG_DATA[11:0]	12
0xBB706424	GPON_GEM_US_PORT_MAP [9].RESERVED[31:12]	20
0xBB706424	GPON_GEM_US_PORT_MAP [9].PORT_CFG_DATA[11:0]	12
0xBB706428	GPON_GEM_US_PORT_MAP [10].RESERVED[31:12]	20
0xBB706428	GPON_GEM_US_PORT_MAP [10].PORT_CFG_DATA[11:0]	12
0xBB70642C	GPON_GEM_US_PORT_MAP [11].RESERVED[31:12]	20
0xBB70642C	GPON_GEM_US_PORT_MAP [11].PORT_CFG_DATA[11:0]	12
0xBB706430	GPON_GEM_US_PORT_MAP [12].RESERVED[31:12]	20
0xBB706430	GPON_GEM_US_PORT_MAP [12].PORT_CFG_DATA[11:0]	12
0xBB706434	GPON_GEM_US_PORT_MAP [13].RESERVED[31:12]	20
0xBB706434	GPON_GEM_US_PORT_MAP [13].PORT_CFG_DATA[11:0]	12
0xBB706438	GPON_GEM_US_PORT_MAP [14].RESERVED[31:12]	20
0xBB706438	GPON_GEM_US_PORT_MAP [14].PORT_CFG_DATA[11:0]	12
0xBB70643C	GPON_GEM_US_PORT_MAP [15].RESERVED[31:12]	20
0xBB70643C	GPON_GEM_US_PORT_MAP [15].PORT_CFG_DATA[11:0]	12
0xBB706440	GPON_GEM_US_PORT_MAP [16].RESERVED[31:12]	20

Address	Register	Len
0xBB706440	GPON_GEM_US_PORT_MAP [16].PORT_CFG_DATA[11:0]	12
0xBB706444	GPON_GEM_US_PORT_MAP [17].RESERVED[31:12]	20
0xBB706444	GPON_GEM_US_PORT_MAP [17].PORT_CFG_DATA[11:0]	12
0xBB706448	GPON_GEM_US_PORT_MAP [18].RESERVED[31:12]	20
0xBB706448	GPON_GEM_US_PORT_MAP [18].PORT_CFG_DATA[11:0]	12
0xBB70644C	GPON_GEM_US_PORT_MAP [19].RESERVED[31:12]	20
0xBB70644C	GPON_GEM_US_PORT_MAP [19].PORT_CFG_DATA[11:0]	12
0xBB706450	GPON_GEM_US_PORT_MAP [20].RESERVED[31:12]	20
0xBB706450	GPON_GEM_US_PORT_MAP [20].PORT_CFG_DATA[11:0]	12
0xBB706454	GPON_GEM_US_PORT_MAP [21].RESERVED[31:12]	20
0xBB706454	GPON_GEM_US_PORT_MAP [21].PORT_CFG_DATA[11:0]	12
0xBB706458	GPON_GEM_US_PORT_MAP [22].RESERVED[31:12]	20
0xBB706458	GPON_GEM_US_PORT_MAP [22].PORT_CFG_DATA[11:0]	12
0xBB70645C	GPON_GEM_US_PORT_MAP [23].RESERVED[31:12]	20
0xBB70645C	GPON_GEM_US_PORT_MAP [23].PORT_CFG_DATA[11:0]	12
0xBB706460	GPON_GEM_US_PORT_MAP [24].RESERVED[31:12]	20
0xBB706460	GPON_GEM_US_PORT_MAP [24].PORT_CFG_DATA[11:0]	12
0xBB706464	GPON_GEM_US_PORT_MAP [25].RESERVED[31:12]	20
0xBB706464	GPON_GEM_US_PORT_MAP [25].PORT_CFG_DATA[11:0]	12
0xBB706468	GPON_GEM_US_PORT_MAP [26].RESERVED[31:12]	20
0xBB706468	GPON_GEM_US_PORT_MAP [26].PORT_CFG_DATA[11:0]	12
0xBB70646C	GPON_GEM_US_PORT_MAP [27].RESERVED[31:12]	20
0xBB70646C	GPON_GEM_US_PORT_MAP [27].PORT_CFG_DATA[11:0]	12
0xBB706470	GPON_GEM_US_PORT_MAP [28].RESERVED[31:12]	20
0xBB706470	GPON_GEM_US_PORT_MAP [28].PORT_CFG_DATA[11:0]	12
0xBB706474	GPON_GEM_US_PORT_MAP [29].RESERVED[31:12]	20
0xBB706474	GPON_GEM_US_PORT_MAP [29].PORT_CFG_DATA[11:0]	12
0xBB706478	GPON_GEM_US_PORT_MAP [30].RESERVED[31:12]	20
0xBB706478	GPON_GEM_US_PORT_MAP [30].PORT_CFG_DATA[11:0]	12
0xBB70647C	GPON_GEM_US_PORT_MAP [31].RESERVED[31:12]	20
0xBB70647C	GPON_GEM_US_PORT_MAP [31].PORT_CFG_DATA[11:0]	12
0xBB706480	GPON_GEM_US_PORT_MAP [32].RESERVED[31:12]	20
0xBB706480	GPON_GEM_US_PORT_MAP [32].PORT_CFG_DATA[11:0]	12
0xBB706484	GPON_GEM_US_PORT_MAP [33].RESERVED[31:12]	20
0xBB706484	GPON_GEM_US_PORT_MAP [33].PORT_CFG_DATA[11:0]	12
0xBB706488	GPON_GEM_US_PORT_MAP [34].RESERVED[31:12]	20
0xBB706488	GPON_GEM_US_PORT_MAP [34].PORT_CFG_DATA[11:0]	12
0xBB70648C	GPON_GEM_US_PORT_MAP [35].RESERVED[31:12]	20
0xBB70648C	GPON_GEM_US_PORT_MAP [35].PORT_CFG_DATA[11:0]	12
0xBB706490	GPON_GEM_US_PORT_MAP [36].RESERVED[31:12]	20
0xBB706490	GPON_GEM_US_PORT_MAP [36].PORT_CFG_DATA[11:0]	12
0xBB706494	GPON_GEM_US_PORT_MAP [37].RESERVED[31:12]	20
0xBB706494	GPON_GEM_US_PORT_MAP [37].PORT_CFG_DATA[11:0]	12
0xBB706498	GPON_GEM_US_PORT_MAP [38].RESERVED[31:12]	20
0xBB706498	GPON_GEM_US_PORT_MAP [38].PORT_CFG_DATA[11:0]	12
0xBB70649C	GPON_GEM_US_PORT_MAP [39].RESERVED[31:12]	20

Address	Register	Len
0xBB70649C	GPON_GEM_US_PORT_MAP [39].PORT_CFG_DATA[11:0]	12
0xBB7064A0	GPON_GEM_US_PORT_MAP [40].RESERVED[31:12]	20
0xBB7064A0	GPON_GEM_US_PORT_MAP [40].PORT_CFG_DATA[11:0]	12
0xBB7064A4	GPON_GEM_US_PORT_MAP [41].RESERVED[31:12]	20
0xBB7064A4	GPON_GEM_US_PORT_MAP [41].PORT_CFG_DATA[11:0]	12
0xBB7064A8	GPON_GEM_US_PORT_MAP [42].RESERVED[31:12]	20
0xBB7064A8	GPON_GEM_US_PORT_MAP [42].PORT_CFG_DATA[11:0]	12
0xBB7064AC	GPON_GEM_US_PORT_MAP [43].RESERVED[31:12]	20
0xBB7064AC	GPON_GEM_US_PORT_MAP [43].PORT_CFG_DATA[11:0]	12
0xBB7064B0	GPON_GEM_US_PORT_MAP [44].RESERVED[31:12]	20
0xBB7064B0	GPON_GEM_US_PORT_MAP [44].PORT_CFG_DATA[11:0]	12
0xBB7064B4	GPON_GEM_US_PORT_MAP [45].RESERVED[31:12]	20
0xBB7064B4	GPON_GEM_US_PORT_MAP [45].PORT_CFG_DATA[11:0]	12
0xBB7064B8	GPON_GEM_US_PORT_MAP [46].RESERVED[31:12]	20
0xBB7064B8	GPON_GEM_US_PORT_MAP [46].PORT_CFG_DATA[11:0]	12
0xBB7064BC	GPON_GEM_US_PORT_MAP [47].RESERVED[31:12]	20
0xBB7064BC	GPON_GEM_US_PORT_MAP [47].PORT_CFG_DATA[11:0]	12
0xBB7064C0	GPON_GEM_US_PORT_MAP [48].RESERVED[31:12]	20
0xBB7064C0	GPON_GEM_US_PORT_MAP [48].PORT_CFG_DATA[11:0]	12
0xBB7064C4	GPON_GEM_US_PORT_MAP [49].RESERVED[31:12]	20
0xBB7064C4	GPON_GEM_US_PORT_MAP [49].PORT_CFG_DATA[11:0]	12
0xBB7064C8	GPON_GEM_US_PORT_MAP [50].RESERVED[31:12]	20
0xBB7064C8	GPON_GEM_US_PORT_MAP [50].PORT_CFG_DATA[11:0]	12
0xBB7064CC	GPON_GEM_US_PORT_MAP [51].RESERVED[31:12]	20
0xBB7064CC	GPON_GEM_US_PORT_MAP [51].PORT_CFG_DATA[11:0]	12
0xBB7064D0	GPON_GEM_US_PORT_MAP [52].RESERVED[31:12]	20
0xBB7064D0	GPON_GEM_US_PORT_MAP [52].PORT_CFG_DATA[11:0]	12
0xBB7064D4	GPON_GEM_US_PORT_MAP [53].RESERVED[31:12]	20
0xBB7064D4	GPON_GEM_US_PORT_MAP [53].PORT_CFG_DATA[11:0]	12
0xBB7064D8	GPON_GEM_US_PORT_MAP [54].RESERVED[31:12]	20
0xBB7064D8	GPON_GEM_US_PORT_MAP [54].PORT_CFG_DATA[11:0]	12
0xBB7064DC	GPON_GEM_US_PORT_MAP [55].RESERVED[31:12]	20
0xBB7064DC	GPON_GEM_US_PORT_MAP [55].PORT_CFG_DATA[11:0]	12
0xBB7064E0	GPON_GEM_US_PORT_MAP [56].RESERVED[31:12]	20
0xBB7064E0	GPON_GEM_US_PORT_MAP [56].PORT_CFG_DATA[11:0]	12
0xBB7064E4	GPON_GEM_US_PORT_MAP [57].RESERVED[31:12]	20
0xBB7064E4	GPON_GEM_US_PORT_MAP [57].PORT_CFG_DATA[11:0]	12
0xBB7064E8	GPON_GEM_US_PORT_MAP [58].RESERVED[31:12]	20
0xBB7064E8	GPON_GEM_US_PORT_MAP [58].PORT_CFG_DATA[11:0]	12
0xBB7064EC	GPON_GEM_US_PORT_MAP [59].RESERVED[31:12]	20
0xBB7064EC	GPON_GEM_US_PORT_MAP [59].PORT_CFG_DATA[11:0]	12
0xBB7064F0	GPON_GEM_US_PORT_MAP [60].RESERVED[31:12]	20
0xBB7064F0	GPON_GEM_US_PORT_MAP [60].PORT_CFG_DATA[11:0]	12
0xBB7064F4	GPON_GEM_US_PORT_MAP [61].RESERVED[31:12]	20
0xBB7064F4	GPON_GEM_US_PORT_MAP [61].PORT_CFG_DATA[11:0]	12
0xBB7064F8	GPON_GEM_US_PORT_MAP [62].RESERVED[31:12]	20

Address	Register	Len
0xBB7064F8	GPON_GEM_US_PORT_MAP [62].PORT_CFG_DATA[11:0]	12
0xBB7064FC	GPON_GEM_US_PORT_MAP [63].RESERVED[31:12]	20
0xBB7064FC	GPON_GEM_US_PORT_MAP [63].PORT_CFG_DATA[11:0]	12
0xBB706500	GPON_GEM_US_PORT_MAP [64].RESERVED[31:12]	20
0xBB706500	GPON_GEM_US_PORT_MAP [64].PORT_CFG_DATA[11:0]	12
0xBB706504	GPON_GEM_US_PORT_MAP [65].RESERVED[31:12]	20
0xBB706504	GPON_GEM_US_PORT_MAP [65].PORT_CFG_DATA[11:0]	12
0xBB706508	GPON_GEM_US_PORT_MAP [66].RESERVED[31:12]	20
0xBB706508	GPON_GEM_US_PORT_MAP [66].PORT_CFG_DATA[11:0]	12
0xBB70650C	GPON_GEM_US_PORT_MAP [67].RESERVED[31:12]	20
0xBB70650C	GPON_GEM_US_PORT_MAP [67].PORT_CFG_DATA[11:0]	12
0xBB706510	GPON_GEM_US_PORT_MAP [68].RESERVED[31:12]	20
0xBB706510	GPON_GEM_US_PORT_MAP [68].PORT_CFG_DATA[11:0]	12
0xBB706514	GPON_GEM_US_PORT_MAP [69].RESERVED[31:12]	20
0xBB706514	GPON_GEM_US_PORT_MAP [69].PORT_CFG_DATA[11:0]	12
0xBB706518	GPON_GEM_US_PORT_MAP [70].RESERVED[31:12]	20
0xBB706518	GPON_GEM_US_PORT_MAP [70].PORT_CFG_DATA[11:0]	12
0xBB70651C	GPON_GEM_US_PORT_MAP [71].RESERVED[31:12]	20
0xBB70651C	GPON_GEM_US_PORT_MAP [71].PORT_CFG_DATA[11:0]	12
0xBB706520	GPON_GEM_US_PORT_MAP [72].RESERVED[31:12]	20
0xBB706520	GPON_GEM_US_PORT_MAP [72].PORT_CFG_DATA[11:0]	12
0xBB706524	GPON_GEM_US_PORT_MAP [73].RESERVED[31:12]	20
0xBB706524	GPON_GEM_US_PORT_MAP [73].PORT_CFG_DATA[11:0]	12
0xBB706528	GPON_GEM_US_PORT_MAP [74].RESERVED[31:12]	20
0xBB706528	GPON_GEM_US_PORT_MAP [74].PORT_CFG_DATA[11:0]	12
0xBB70652C	GPON_GEM_US_PORT_MAP [75].RESERVED[31:12]	20
0xBB70652C	GPON_GEM_US_PORT_MAP [75].PORT_CFG_DATA[11:0]	12
0xBB706530	GPON_GEM_US_PORT_MAP [76].RESERVED[31:12]	20
0xBB706530	GPON_GEM_US_PORT_MAP [76].PORT_CFG_DATA[11:0]	12
0xBB706534	GPON_GEM_US_PORT_MAP [77].RESERVED[31:12]	20
0xBB706534	GPON_GEM_US_PORT_MAP [77].PORT_CFG_DATA[11:0]	12
0xBB706538	GPON_GEM_US_PORT_MAP [78].RESERVED[31:12]	20
0xBB706538	GPON_GEM_US_PORT_MAP [78].PORT_CFG_DATA[11:0]	12
0xBB70653C	GPON_GEM_US_PORT_MAP [79].RESERVED[31:12]	20
0xBB70653C	GPON_GEM_US_PORT_MAP [79].PORT_CFG_DATA[11:0]	12
0xBB706540	GPON_GEM_US_PORT_MAP [80].RESERVED[31:12]	20
0xBB706540	GPON_GEM_US_PORT_MAP [80].PORT_CFG_DATA[11:0]	12
0xBB706544	GPON_GEM_US_PORT_MAP [81].RESERVED[31:12]	20
0xBB706544	GPON_GEM_US_PORT_MAP [81].PORT_CFG_DATA[11:0]	12
0xBB706548	GPON_GEM_US_PORT_MAP [82].RESERVED[31:12]	20
0xBB706548	GPON_GEM_US_PORT_MAP [82].PORT_CFG_DATA[11:0]	12
0xBB70654C	GPON_GEM_US_PORT_MAP [83].RESERVED[31:12]	20
0xBB70654C	GPON_GEM_US_PORT_MAP [83].PORT_CFG_DATA[11:0]	12
0xBB706550	GPON_GEM_US_PORT_MAP [84].RESERVED[31:12]	20
0xBB706550	GPON_GEM_US_PORT_MAP [84].PORT_CFG_DATA[11:0]	12
0xBB706554	GPON_GEM_US_PORT_MAP [85].RESERVED[31:12]	20



Address	Register	Len
0xBB706554	GPON_GEM_US_PORT_MAP [85].PORT_CFG_DATA[11:0]	12
0xBB706558	GPON_GEM_US_PORT_MAP [86].RESERVED[31:12]	20
0xBB706558	GPON_GEM_US_PORT_MAP [86].PORT_CFG_DATA[11:0]	12
0xBB70655C	GPON_GEM_US_PORT_MAP [87].RESERVED[31:12]	20
0xBB70655C	GPON_GEM_US_PORT_MAP [87].PORT_CFG_DATA[11:0]	12
0xBB706560	GPON_GEM_US_PORT_MAP [88].RESERVED[31:12]	20
0xBB706560	GPON_GEM_US_PORT_MAP [88].PORT_CFG_DATA[11:0]	12
0xBB706564	GPON_GEM_US_PORT_MAP [89].RESERVED[31:12]	20
0xBB706564	GPON_GEM_US_PORT_MAP [89].PORT_CFG_DATA[11:0]	12
0xBB706568	GPON_GEM_US_PORT_MAP [90].RESERVED[31:12]	20
0xBB706568	GPON_GEM_US_PORT_MAP [90].PORT_CFG_DATA[11:0]	12
0xBB70656C	GPON_GEM_US_PORT_MAP [91].RESERVED[31:12]	20
0xBB70656C	GPON_GEM_US_PORT_MAP [91].PORT_CFG_DATA[11:0]	12
0xBB706570	GPON_GEM_US_PORT_MAP [92].RESERVED[31:12]	20
0xBB706570	GPON_GEM_US_PORT_MAP [92].PORT_CFG_DATA[11:0]	12
0xBB706574	GPON_GEM_US_PORT_MAP [93].RESERVED[31:12]	20
0xBB706574	GPON_GEM_US_PORT_MAP [93].PORT_CFG_DATA[11:0]	12
0xBB706578	GPON_GEM_US_PORT_MAP [94].RESERVED[31:12]	20
0xBB706578	GPON_GEM_US_PORT_MAP [94].PORT_CFG_DATA[11:0]	12
0xBB70657C	GPON_GEM_US_PORT_MAP [95].RESERVED[31:12]	20
0xBB70657C	GPON_GEM_US_PORT_MAP [95].PORT_CFG_DATA[11:0]	12
0xBB706580	GPON_GEM_US_PORT_MAP [96].RESERVED[31:12]	20
0xBB706580	GPON_GEM_US_PORT_MAP [96].PORT_CFG_DATA[11:0]	12
0xBB706584	GPON_GEM_US_PORT_MAP [97].RESERVED[31:12]	20
0xBB706584	GPON_GEM_US_PORT_MAP [97].PORT_CFG_DATA[11:0]	12
0xBB706588	GPON_GEM_US_PORT_MAP [98].RESERVED[31:12]	20
0xBB706588	GPON_GEM_US_PORT_MAP [98].PORT_CFG_DATA[11:0]	12
0xBB70658C	GPON_GEM_US_PORT_MAP [99].RESERVED[31:12]	20
0xBB70658C	GPON_GEM_US_PORT_MAP [99].PORT_CFG_DATA[11:0]	12
0xBB706590	GPON_GEM_US_PORT_MAP [100].RESERVED[31:12]	20
0xBB706590	GPON_GEM_US_PORT_MAP [100].PORT_CFG_DATA[11:0]	12
0xBB706594	GPON_GEM_US_PORT_MAP [101].RESERVED[31:12]	20
0xBB706594	GPON_GEM_US_PORT_MAP [101].PORT_CFG_DATA[11:0]	12
0xBB706598	GPON_GEM_US_PORT_MAP [102].RESERVED[31:12]	20
0xBB706598	GPON_GEM_US_PORT_MAP [102].PORT_CFG_DATA[11:0]	12
0xBB70659C	GPON_GEM_US_PORT_MAP [103].RESERVED[31:12]	20
0xBB70659C	GPON_GEM_US_PORT_MAP [103].PORT_CFG_DATA[11:0]	12
0xBB7065A0	GPON_GEM_US_PORT_MAP [104].RESERVED[31:12]	20
0xBB7065A0	GPON_GEM_US_PORT_MAP [104].PORT_CFG_DATA[11:0]	12
0xBB7065A4	GPON_GEM_US_PORT_MAP [105].RESERVED[31:12]	20
0xBB7065A4	GPON_GEM_US_PORT_MAP [105].PORT_CFG_DATA[11:0]	12
0xBB7065A8	GPON_GEM_US_PORT_MAP [106].RESERVED[31:12]	20
0xBB7065A8	GPON_GEM_US_PORT_MAP [106].PORT_CFG_DATA[11:0]	12
0xBB7065AC	GPON_GEM_US_PORT_MAP [107].RESERVED[31:12]	20
0xBB7065AC	GPON_GEM_US_PORT_MAP [107].PORT_CFG_DATA[11:0]	12
0xBB7065B0	GPON_GEM_US_PORT_MAP [108].RESERVED[31:12]	20

Address	Register	Len
0xBB7065B0	GPON_GEM_US_PORT_MAP [108].PORT_CFG_DATA[11:0]	12
0xBB7065B4	GPON_GEM_US_PORT_MAP [109].RESERVED[31:12]	20
0xBB7065B4	GPON_GEM_US_PORT_MAP [109].PORT_CFG_DATA[11:0]	12
0xBB7065B8	GPON_GEM_US_PORT_MAP [110].RESERVED[31:12]	20
0xBB7065B8	GPON_GEM_US_PORT_MAP [110].PORT_CFG_DATA[11:0]	12
0xBB7065BC	GPON_GEM_US_PORT_MAP [111].RESERVED[31:12]	20
0xBB7065BC	GPON_GEM_US_PORT_MAP [111].PORT_CFG_DATA[11:0]	12
0xBB7065C0	GPON_GEM_US_PORT_MAP [112].RESERVED[31:12]	20
0xBB7065C0	GPON_GEM_US_PORT_MAP [112].PORT_CFG_DATA[11:0]	12
0xBB7065C4	GPON_GEM_US_PORT_MAP [113].RESERVED[31:12]	20
0xBB7065C4	GPON_GEM_US_PORT_MAP [113].PORT_CFG_DATA[11:0]	12
0xBB7065C8	GPON_GEM_US_PORT_MAP [114].RESERVED[31:12]	20
0xBB7065C8	GPON_GEM_US_PORT_MAP [114].PORT_CFG_DATA[11:0]	12
0xBB7065CC	GPON_GEM_US_PORT_MAP [115].RESERVED[31:12]	20
0xBB7065CC	GPON_GEM_US_PORT_MAP [115].PORT_CFG_DATA[11:0]	12
0xBB7065D0	GPON_GEM_US_PORT_MAP [116].RESERVED[31:12]	20
0xBB7065D0	GPON_GEM_US_PORT_MAP [116].PORT_CFG_DATA[11:0]	12
0xBB7065D4	GPON_GEM_US_PORT_MAP [117].RESERVED[31:12]	20
0xBB7065D4	GPON_GEM_US_PORT_MAP [117].PORT_CFG_DATA[11:0]	12
0xBB7065D8	GPON_GEM_US_PORT_MAP [118].RESERVED[31:12]	20
0xBB7065D8	GPON_GEM_US_PORT_MAP [118].PORT_CFG_DATA[11:0]	12
0xBB7065DC	GPON_GEM_US_PORT_MAP [119].RESERVED[31:12]	20
0xBB7065DC	GPON_GEM_US_PORT_MAP [119].PORT_CFG_DATA[11:0]	12
0xBB7065E0	GPON_GEM_US_PORT_MAP [120].RESERVED[31:12]	20
0xBB7065E0	GPON_GEM_US_PORT_MAP [120].PORT_CFG_DATA[11:0]	12
0xBB7065E4	GPON_GEM_US_PORT_MAP [121].RESERVED[31:12]	20
0xBB7065E4	GPON_GEM_US_PORT_MAP [121].PORT_CFG_DATA[11:0]	12
0xBB7065E8	GPON_GEM_US_PORT_MAP [122].RESERVED[31:12]	20
0xBB7065E8	GPON_GEM_US_PORT_MAP [122].PORT_CFG_DATA[11:0]	12
0xBB7065EC	GPON_GEM_US_PORT_MAP [123].RESERVED[31:12]	20
0xBB7065EC	GPON_GEM_US_PORT_MAP [123].PORT_CFG_DATA[11:0]	12
0xBB7065F0	GPON_GEM_US_PORT_MAP [124].RESERVED[31:12]	20
0xBB7065F0	GPON_GEM_US_PORT_MAP [124].PORT_CFG_DATA[11:0]	12
0xBB7065F4	GPON_GEM_US_PORT_MAP [125].RESERVED[31:12]	20
0xBB7065F4	GPON_GEM_US_PORT_MAP [125].PORT_CFG_DATA[11:0]	12
0xBB7065F8	GPON_GEM_US_PORT_MAP [126].RESERVED[31:12]	20
0xBB7065F8	GPON_GEM_US_PORT_MAP [126].PORT_CFG_DATA[11:0]	12
0xBB7065FC	GPON_GEM_US_PORT_MAP [127].RESERVED[31:12]	20
0xBB7065FC	GPON_GEM_US_PORT_MAP [127].PORT_CFG_DATA[11:0]	12
0xBB706800	GPON_GEM_US_BYTE_STAT [0].CNTR_LOW32[31:0]	32
0xBB706804	GPON_GEM_US_BYTE_STAT [0].CNTR_HIGH32[31:0]	32
0xBB706808	GPON_GEM_US_BYTE_STAT [1].CNTR_LOW32[31:0]	32
0xBB70680C	GPON_GEM_US_BYTE_STAT [1].CNTR_HIGH32[31:0]	32
0xBB706810	GPON_GEM_US_BYTE_STAT [2].CNTR_LOW32[31:0]	32
0xBB706814	GPON_GEM_US_BYTE_STAT [2].CNTR_HIGH32[31:0]	32
0xBB706818	GPON_GEM_US_BYTE_STAT [3].CNTR_LOW32[31:0]	32

Address	Register	Len
0xBB70681C	GPON_GEM_US_BYTE_STAT [3].CNTR_HIGH32[31:0]	32
0xBB706820	GPON_GEM_US_BYTE_STAT [4].CNTR_LOW32[31:0]	32
0xBB706824	GPON_GEM_US_BYTE_STAT [4].CNTR_HIGH32[31:0]	32
0xBB706828	GPON_GEM_US_BYTE_STAT [5].CNTR_LOW32[31:0]	32
0xBB70682C	GPON_GEM_US_BYTE_STAT [5].CNTR_HIGH32[31:0]	32
0xBB706830	GPON_GEM_US_BYTE_STAT [6].CNTR_LOW32[31:0]	32
0xBB706834	GPON_GEM_US_BYTE_STAT [6].CNTR_HIGH32[31:0]	32
0xBB706838	GPON_GEM_US_BYTE_STAT [7].CNTR_LOW32[31:0]	32
0xBB70683C	GPON_GEM_US_BYTE_STAT [7].CNTR_HIGH32[31:0]	32
0xBB706840	GPON_GEM_US_BYTE_STAT [8].CNTR_LOW32[31:0]	32
0xBB706844	GPON_GEM_US_BYTE_STAT [8].CNTR_HIGH32[31:0]	32
0xBB706848	GPON_GEM_US_BYTE_STAT [9].CNTR_LOW32[31:0]	32
0xBB70684C	GPON_GEM_US_BYTE_STAT [9].CNTR_HIGH32[31:0]	32
0xBB706850	GPON_GEM_US_BYTE_STAT [10].CNTR_LOW32[31:0]	32
0xBB706854	GPON_GEM_US_BYTE_STAT [10].CNTR_HIGH32[31:0]	32
0xBB706858	GPON_GEM_US_BYTE_STAT [11].CNTR_LOW32[31:0]	32
0xBB70685C	GPON_GEM_US_BYTE_STAT [11].CNTR_HIGH32[31:0]	32
0xBB706860	GPON_GEM_US_BYTE_STAT [12].CNTR_LOW32[31:0]	32
0xBB706864	GPON_GEM_US_BYTE_STAT [12].CNTR_HIGH32[31:0]	32
0xBB706868	GPON_GEM_US_BYTE_STAT [13].CNTR_LOW32[31:0]	32
0xBB70686C	GPON_GEM_US_BYTE_STAT [13].CNTR_HIGH32[31:0]	32
0xBB706870	GPON_GEM_US_BYTE_STAT [14].CNTR_LOW32[31:0]	32
0xBB706874	GPON_GEM_US_BYTE_STAT [14].CNTR_HIGH32[31:0]	32
0xBB706878	GPON_GEM_US_BYTE_STAT [15].CNTR_LOW32[31:0]	32
0xBB70687C	GPON_GEM_US_BYTE_STAT [15].CNTR_HIGH32[31:0]	32
0xBB706880	GPON_GEM_US_BYTE_STAT [16].CNTR_LOW32[31:0]	32
0xBB706884	GPON_GEM_US_BYTE_STAT [16].CNTR_HIGH32[31:0]	32
0xBB706888	GPON_GEM_US_BYTE_STAT [17].CNTR_LOW32[31:0]	32
0xBB70688C	GPON_GEM_US_BYTE_STAT [17].CNTR_HIGH32[31:0]	32
0xBB706890	GPON_GEM_US_BYTE_STAT [18].CNTR_LOW32[31:0]	32
0xBB706894	GPON_GEM_US_BYTE_STAT [18].CNTR_HIGH32[31:0]	32
0xBB706898	GPON_GEM_US_BYTE_STAT [19].CNTR_LOW32[31:0]	32
0xBB70689C	GPON_GEM_US_BYTE_STAT [19].CNTR_HIGH32[31:0]	32
0xBB7068A0	GPON_GEM_US_BYTE_STAT [20].CNTR_LOW32[31:0]	32
0xBB7068A4	GPON_GEM_US_BYTE_STAT [20].CNTR_HIGH32[31:0]	32
0xBB7068A8	GPON_GEM_US_BYTE_STAT [21].CNTR_LOW32[31:0]	32
0xBB7068AC	GPON_GEM_US_BYTE_STAT [21].CNTR_HIGH32[31:0]	32
0xBB7068B0	GPON_GEM_US_BYTE_STAT [22].CNTR_LOW32[31:0]	32
0xBB7068B4	GPON_GEM_US_BYTE_STAT [22].CNTR_HIGH32[31:0]	32
0xBB7068B8	GPON_GEM_US_BYTE_STAT [23].CNTR_LOW32[31:0]	32
0xBB7068BC	GPON_GEM_US_BYTE_STAT [23].CNTR_HIGH32[31:0]	32
0xBB7068C0	GPON_GEM_US_BYTE_STAT [24].CNTR_LOW32[31:0]	32
0xBB7068C4	GPON_GEM_US_BYTE_STAT [24].CNTR_HIGH32[31:0]	32
0xBB7068C8	GPON_GEM_US_BYTE_STAT [25].CNTR_LOW32[31:0]	32
0xBB7068CC	GPON_GEM_US_BYTE_STAT [25].CNTR_HIGH32[31:0]	32
0xBB7068D0	GPON_GEM_US_BYTE_STAT [26].CNTR_LOW32[31:0]	32



Address	Register	Len
0xBB7068D4	GPON_GEM_US_BYTE_STAT [26].CNTR_HIGH32[31:0]	32
0xBB7068D8	GPON_GEM_US_BYTE_STAT [27].CNTR_LOW32[31:0]	32
0xBB7068DC	GPON_GEM_US_BYTE_STAT [27].CNTR_HIGH32[31:0]	32
0xBB7068E0	GPON_GEM_US_BYTE_STAT [28].CNTR_LOW32[31:0]	32
0xBB7068E4	GPON_GEM_US_BYTE_STAT [28].CNTR_HIGH32[31:0]	32
0xBB7068E8	GPON_GEM_US_BYTE_STAT [29].CNTR_LOW32[31:0]	32
0xBB7068EC	GPON_GEM_US_BYTE_STAT [29].CNTR_HIGH32[31:0]	32
0xBB7068F0	GPON_GEM_US_BYTE_STAT [30].CNTR_LOW32[31:0]	32
0xBB7068F4	GPON_GEM_US_BYTE_STAT [30].CNTR_HIGH32[31:0]	32
0xBB7068F8	GPON_GEM_US_BYTE_STAT [31].CNTR_LOW32[31:0]	32
0xBB7068FC	GPON_GEM_US_BYTE_STAT [31].CNTR_HIGH32[31:0]	32
0xBB706900	GPON_GEM_US_BYTE_STAT [32].CNTR_LOW32[31:0]	32
0xBB706904	GPON_GEM_US_BYTE_STAT [32].CNTR_HIGH32[31:0]	32
0xBB706908	GPON_GEM_US_BYTE_STAT [33].CNTR_LOW32[31:0]	32
0xBB70690C	GPON_GEM_US_BYTE_STAT [33].CNTR_HIGH32[31:0]	32
0xBB706910	GPON_GEM_US_BYTE_STAT [34].CNTR_LOW32[31:0]	32
0xBB706914	GPON_GEM_US_BYTE_STAT [34].CNTR_HIGH32[31:0]	32
0xBB706918	GPON_GEM_US_BYTE_STAT [35].CNTR_LOW32[31:0]	32
0xBB70691C	GPON_GEM_US_BYTE_STAT [35].CNTR_HIGH32[31:0]	32
0xBB706920	GPON_GEM_US_BYTE_STAT [36].CNTR_LOW32[31:0]	32
0xBB706924	GPON_GEM_US_BYTE_STAT [36].CNTR_HIGH32[31:0]	32
0xBB706928	GPON_GEM_US_BYTE_STAT [37].CNTR_LOW32[31:0]	32
0xBB70692C	GPON_GEM_US_BYTE_STAT [37].CNTR_HIGH32[31:0]	32
0xBB706930	GPON_GEM_US_BYTE_STAT [38].CNTR_LOW32[31:0]	32
0xBB706934	GPON_GEM_US_BYTE_STAT [38].CNTR_HIGH32[31:0]	32
0xBB706938	GPON_GEM_US_BYTE_STAT [39].CNTR_LOW32[31:0]	32
0xBB70693C	GPON_GEM_US_BYTE_STAT [39].CNTR_HIGH32[31:0]	32
0xBB706940	GPON_GEM_US_BYTE_STAT [40].CNTR_LOW32[31:0]	32
0xBB706944	GPON_GEM_US_BYTE_STAT [40].CNTR_HIGH32[31:0]	32
0xBB706948	GPON_GEM_US_BYTE_STAT [41].CNTR_LOW32[31:0]	32
0xBB70694C	GPON_GEM_US_BYTE_STAT [41].CNTR_HIGH32[31:0]	32
0xBB706950	GPON_GEM_US_BYTE_STAT [42].CNTR_LOW32[31:0]	32
0xBB706954	GPON_GEM_US_BYTE_STAT [42].CNTR_HIGH32[31:0]	32
0xBB706958	GPON_GEM_US_BYTE_STAT [43].CNTR_LOW32[31:0]	32
0xBB70695C	GPON_GEM_US_BYTE_STAT [43].CNTR_HIGH32[31:0]	32
0xBB706960	GPON_GEM_US_BYTE_STAT [44].CNTR_LOW32[31:0]	32
0xBB706964	GPON_GEM_US_BYTE_STAT [44].CNTR_HIGH32[31:0]	32
0xBB706968	GPON_GEM_US_BYTE_STAT [45].CNTR_LOW32[31:0]	32
0xBB70696C	GPON_GEM_US_BYTE_STAT [45].CNTR_HIGH32[31:0]	32
0xBB706970	GPON_GEM_US_BYTE_STAT [46].CNTR_LOW32[31:0]	32
0xBB706974	GPON_GEM_US_BYTE_STAT [46].CNTR_HIGH32[31:0]	32
0xBB706978	GPON_GEM_US_BYTE_STAT [47].CNTR_LOW32[31:0]	32
0xBB70697C	GPON_GEM_US_BYTE_STAT [47].CNTR_HIGH32[31:0]	32
0xBB706980	GPON_GEM_US_BYTE_STAT [48].CNTR_LOW32[31:0]	32
0xBB706984	GPON_GEM_US_BYTE_STAT [48].CNTR_HIGH32[31:0]	32
0xBB706988	GPON_GEM_US_BYTE_STAT [49].CNTR_LOW32[31:0]	32

Address	Register	Len
0xBB70698C	GPON_GEM_US_BYTE_STAT [49].CNTR_HIGH32[31:0]	32
0xBB706990	GPON_GEM_US_BYTE_STAT [50].CNTR_LOW32[31:0]	32
0xBB706994	GPON_GEM_US_BYTE_STAT [50].CNTR_HIGH32[31:0]	32
0xBB706998	GPON_GEM_US_BYTE_STAT [51].CNTR_LOW32[31:0]	32
0xBB70699C	GPON_GEM_US_BYTE_STAT [51].CNTR_HIGH32[31:0]	32
0xBB7069A0	GPON_GEM_US_BYTE_STAT [52].CNTR_LOW32[31:0]	32
0xBB7069A4	GPON_GEM_US_BYTE_STAT [52].CNTR_HIGH32[31:0]	32
0xBB7069A8	GPON_GEM_US_BYTE_STAT [53].CNTR_LOW32[31:0]	32
0xBB7069AC	GPON_GEM_US_BYTE_STAT [53].CNTR_HIGH32[31:0]	32
0xBB7069B0	GPON_GEM_US_BYTE_STAT [54].CNTR_LOW32[31:0]	32
0xBB7069B4	GPON_GEM_US_BYTE_STAT [54].CNTR_HIGH32[31:0]	32
0xBB7069B8	GPON_GEM_US_BYTE_STAT [55].CNTR_LOW32[31:0]	32
0xBB7069BC	GPON_GEM_US_BYTE_STAT [55].CNTR_HIGH32[31:0]	32
0xBB7069C0	GPON_GEM_US_BYTE_STAT [56].CNTR_LOW32[31:0]	32
0xBB7069C4	GPON_GEM_US_BYTE_STAT [56].CNTR_HIGH32[31:0]	32
0xBB7069C8	GPON_GEM_US_BYTE_STAT [57].CNTR_LOW32[31:0]	32
0xBB7069CC	GPON_GEM_US_BYTE_STAT [57].CNTR_HIGH32[31:0]	32
0xBB7069D0	GPON_GEM_US_BYTE_STAT [58].CNTR_LOW32[31:0]	32
0xBB7069D4	GPON_GEM_US_BYTE_STAT [58].CNTR_HIGH32[31:0]	32
0xBB7069D8	GPON_GEM_US_BYTE_STAT [59].CNTR_LOW32[31:0]	32
0xBB7069DC	GPON_GEM_US_BYTE_STAT [59].CNTR_HIGH32[31:0]	32
0xBB7069E0	GPON_GEM_US_BYTE_STAT [60].CNTR_LOW32[31:0]	32
0xBB7069E4	GPON_GEM_US_BYTE_STAT [60].CNTR_HIGH32[31:0]	32
0xBB7069E8	GPON_GEM_US_BYTE_STAT [61].CNTR_LOW32[31:0]	32
0xBB7069EC	GPON_GEM_US_BYTE_STAT [61].CNTR_HIGH32[31:0]	32
0xBB7069F0	GPON_GEM_US_BYTE_STAT [62].CNTR_LOW32[31:0]	32
0xBB7069F4	GPON_GEM_US_BYTE_STAT [62].CNTR_HIGH32[31:0]	32
0xBB7069F8	GPON_GEM_US_BYTE_STAT [63].CNTR_LOW32[31:0]	32
0xBB7069FC	GPON_GEM_US_BYTE_STAT [63].CNTR_HIGH32[31:0]	32
0xBB706A00	GPON_GEM_US_BYTE_STAT [64].CNTR_LOW32[31:0]	32
0xBB706A04	GPON_GEM_US_BYTE_STAT [64].CNTR_HIGH32[31:0]	32
0xBB706A08	GPON_GEM_US_BYTE_STAT [65].CNTR_LOW32[31:0]	32
0xBB706A0C	GPON_GEM_US_BYTE_STAT [65].CNTR_HIGH32[31:0]	32
0xBB706A10	GPON_GEM_US_BYTE_STAT [66].CNTR_LOW32[31:0]	32
0xBB706A14	GPON_GEM_US_BYTE_STAT [66].CNTR_HIGH32[31:0]	32
0xBB706A18	GPON_GEM_US_BYTE_STAT [67].CNTR_LOW32[31:0]	32
0xBB706A1C	GPON_GEM_US_BYTE_STAT [67].CNTR_HIGH32[31:0]	32
0xBB706A20	GPON_GEM_US_BYTE_STAT [68].CNTR_LOW32[31:0]	32
0xBB706A24	GPON_GEM_US_BYTE_STAT [68].CNTR_HIGH32[31:0]	32
0xBB706A28	GPON_GEM_US_BYTE_STAT [69].CNTR_LOW32[31:0]	32
0xBB706A2C	GPON_GEM_US_BYTE_STAT [69].CNTR_HIGH32[31:0]	32
0xBB706A30	GPON_GEM_US_BYTE_STAT [70].CNTR_LOW32[31:0]	32
0xBB706A34	GPON_GEM_US_BYTE_STAT [70].CNTR_HIGH32[31:0]	32
0xBB706A38	GPON_GEM_US_BYTE_STAT [71].CNTR_LOW32[31:0]	32
0xBB706A3C	GPON_GEM_US_BYTE_STAT [71].CNTR_HIGH32[31:0]	32
0xBB706A40	GPON_GEM_US_BYTE_STAT [72].CNTR_LOW32[31:0]	32

Address	Register	Len
0xBB706A44	GPON_GEM_US_BYTE_STAT [72].CNTR_HIGH32[31:0]	32
0xBB706A48	GPON_GEM_US_BYTE_STAT [73].CNTR_LOW32[31:0]	32
0xBB706A4C	GPON_GEM_US_BYTE_STAT [73].CNTR_HIGH32[31:0]	32
0xBB706A50	GPON_GEM_US_BYTE_STAT [74].CNTR_LOW32[31:0]	32
0xBB706A54	GPON_GEM_US_BYTE_STAT [74].CNTR_HIGH32[31:0]	32
0xBB706A58	GPON_GEM_US_BYTE_STAT [75].CNTR_LOW32[31:0]	32
0xBB706A5C	GPON_GEM_US_BYTE_STAT [75].CNTR_HIGH32[31:0]	32
0xBB706A60	GPON_GEM_US_BYTE_STAT [76].CNTR_LOW32[31:0]	32
0xBB706A64	GPON_GEM_US_BYTE_STAT [76].CNTR_HIGH32[31:0]	32
0xBB706A68	GPON_GEM_US_BYTE_STAT [77].CNTR_LOW32[31:0]	32
0xBB706A6C	GPON_GEM_US_BYTE_STAT [77].CNTR_HIGH32[31:0]	32
0xBB706A70	GPON_GEM_US_BYTE_STAT [78].CNTR_LOW32[31:0]	32
0xBB706A74	GPON_GEM_US_BYTE_STAT [78].CNTR_HIGH32[31:0]	32
0xBB706A78	GPON_GEM_US_BYTE_STAT [79].CNTR_LOW32[31:0]	32
0xBB706A7C	GPON_GEM_US_BYTE_STAT [79].CNTR_HIGH32[31:0]	32
0xBB706A80	GPON_GEM_US_BYTE_STAT [80].CNTR_LOW32[31:0]	32
0xBB706A84	GPON_GEM_US_BYTE_STAT [80].CNTR_HIGH32[31:0]	32
0xBB706A88	GPON_GEM_US_BYTE_STAT [81].CNTR_LOW32[31:0]	32
0xBB706A8C	GPON_GEM_US_BYTE_STAT [81].CNTR_HIGH32[31:0]	32
0xBB706A90	GPON_GEM_US_BYTE_STAT [82].CNTR_LOW32[31:0]	32
0xBB706A94	GPON_GEM_US_BYTE_STAT [82].CNTR_HIGH32[31:0]	32
0xBB706A98	GPON_GEM_US_BYTE_STAT [83].CNTR_LOW32[31:0]	32
0xBB706A9C	GPON_GEM_US_BYTE_STAT [83].CNTR_HIGH32[31:0]	32
0xBB706AA0	GPON_GEM_US_BYTE_STAT [84].CNTR_LOW32[31:0]	32
0xBB706AA4	GPON_GEM_US_BYTE_STAT [84].CNTR_HIGH32[31:0]	32
0xBB706AA8	GPON_GEM_US_BYTE_STAT [85].CNTR_LOW32[31:0]	32
0xBB706AAC	GPON_GEM_US_BYTE_STAT [85].CNTR_HIGH32[31:0]	32
0xBB706AB0	GPON_GEM_US_BYTE_STAT [86].CNTR_LOW32[31:0]	32
0xBB706AB4	GPON_GEM_US_BYTE_STAT [86].CNTR_HIGH32[31:0]	32
0xBB706AB8	GPON_GEM_US_BYTE_STAT [87].CNTR_LOW32[31:0]	32
0xBB706ABC	GPON_GEM_US_BYTE_STAT [87].CNTR_HIGH32[31:0]	32
0xBB706AC0	GPON_GEM_US_BYTE_STAT [88].CNTR_LOW32[31:0]	32
0xBB706AC4	GPON_GEM_US_BYTE_STAT [88].CNTR_HIGH32[31:0]	32
0xBB706AC8	GPON_GEM_US_BYTE_STAT [89].CNTR_LOW32[31:0]	32
0xBB706ACC	GPON_GEM_US_BYTE_STAT [89].CNTR_HIGH32[31:0]	32
0xBB706AD0	GPON_GEM_US_BYTE_STAT [90].CNTR_LOW32[31:0]	32
0xBB706AD4	GPON_GEM_US_BYTE_STAT [90].CNTR_HIGH32[31:0]	32
0xBB706AD8	GPON_GEM_US_BYTE_STAT [91].CNTR_LOW32[31:0]	32
0xBB706ADC	GPON_GEM_US_BYTE_STAT [91].CNTR_HIGH32[31:0]	32
0xBB706AE0	GPON_GEM_US_BYTE_STAT [92].CNTR_LOW32[31:0]	32
0xBB706AE4	GPON_GEM_US_BYTE_STAT [92].CNTR_HIGH32[31:0]	32
0xBB706AE8	GPON_GEM_US_BYTE_STAT [93].CNTR_LOW32[31:0]	32
0xBB706AEC	GPON_GEM_US_BYTE_STAT [93].CNTR_HIGH32[31:0]	32
0xBB706AF0	GPON_GEM_US_BYTE_STAT [94].CNTR_LOW32[31:0]	32
0xBB706AF4	GPON_GEM_US_BYTE_STAT [94].CNTR_HIGH32[31:0]	32
0xBB706AF8	GPON_GEM_US_BYTE_STAT [95].CNTR_LOW32[31:0]	32

Address	Register	Len
0xBB706AFC	GPON_GEM_US_BYTE_STAT [95].CNTR_HIGH32[31:0]	32
0xBB706B00	GPON_GEM_US_BYTE_STAT [96].CNTR_LOW32[31:0]	32
0xBB706B04	GPON_GEM_US_BYTE_STAT [96].CNTR_HIGH32[31:0]	32
0xBB706B08	GPON_GEM_US_BYTE_STAT [97].CNTR_LOW32[31:0]	32
0xBB706B0C	GPON_GEM_US_BYTE_STAT [97].CNTR_HIGH32[31:0]	32
0xBB706B10	GPON_GEM_US_BYTE_STAT [98].CNTR_LOW32[31:0]	32
0xBB706B14	GPON_GEM_US_BYTE_STAT [98].CNTR_HIGH32[31:0]	32
0xBB706B18	GPON_GEM_US_BYTE_STAT [99].CNTR_LOW32[31:0]	32
0xBB706B1C	GPON_GEM_US_BYTE_STAT [99].CNTR_HIGH32[31:0]	32
0xBB706B20	GPON_GEM_US_BYTE_STAT [100].CNTR_LOW32[31:0]	32
0xBB706B24	GPON_GEM_US_BYTE_STAT [100].CNTR_HIGH32[31:0]	32
0xBB706B28	GPON_GEM_US_BYTE_STAT [101].CNTR_LOW32[31:0]	32
0xBB706B2C	GPON_GEM_US_BYTE_STAT [101].CNTR_HIGH32[31:0]	32
0xBB706B30	GPON_GEM_US_BYTE_STAT [102].CNTR_LOW32[31:0]	32
0xBB706B34	GPON_GEM_US_BYTE_STAT [102].CNTR_HIGH32[31:0]	32
0xBB706B38	GPON_GEM_US_BYTE_STAT [103].CNTR_LOW32[31:0]	32
0xBB706B3C	GPON_GEM_US_BYTE_STAT [103].CNTR_HIGH32[31:0]	32
0xBB706B40	GPON_GEM_US_BYTE_STAT [104].CNTR_LOW32[31:0]	32
0xBB706B44	GPON_GEM_US_BYTE_STAT [104].CNTR_HIGH32[31:0]	32
0xBB706B48	GPON_GEM_US_BYTE_STAT [105].CNTR_LOW32[31:0]	32
0xBB706B4C	GPON_GEM_US_BYTE_STAT [105].CNTR_HIGH32[31:0]	32
0xBB706B50	GPON_GEM_US_BYTE_STAT [106].CNTR_LOW32[31:0]	32
0xBB706B54	GPON_GEM_US_BYTE_STAT [106].CNTR_HIGH32[31:0]	32
0xBB706B58	GPON_GEM_US_BYTE_STAT [107].CNTR_LOW32[31:0]	32
0xBB706B5C	GPON_GEM_US_BYTE_STAT [107].CNTR_HIGH32[31:0]	32
0xBB706B60	GPON_GEM_US_BYTE_STAT [108].CNTR_LOW32[31:0]	32
0xBB706B64	GPON_GEM_US_BYTE_STAT [108].CNTR_HIGH32[31:0]	32
0xBB706B68	GPON_GEM_US_BYTE_STAT [109].CNTR_LOW32[31:0]	32
0xBB706B6C	GPON_GEM_US_BYTE_STAT [109].CNTR_HIGH32[31:0]	32
0xBB706B70	GPON_GEM_US_BYTE_STAT [110].CNTR_LOW32[31:0]	32
0xBB706B74	GPON_GEM_US_BYTE_STAT [110].CNTR_HIGH32[31:0]	32
0xBB706B78	GPON_GEM_US_BYTE_STAT [111].CNTR_LOW32[31:0]	32
0xBB706B7C	GPON_GEM_US_BYTE_STAT [111].CNTR_HIGH32[31:0]	32
0xBB706B80	GPON_GEM_US_BYTE_STAT [112].CNTR_LOW32[31:0]	32
0xBB706B84	GPON_GEM_US_BYTE_STAT [112].CNTR_HIGH32[31:0]	32
0xBB706B88	GPON_GEM_US_BYTE_STAT [113].CNTR_LOW32[31:0]	32
0xBB706B8C	GPON_GEM_US_BYTE_STAT [113].CNTR_HIGH32[31:0]	32
0xBB706B90	GPON_GEM_US_BYTE_STAT [114].CNTR_LOW32[31:0]	32
0xBB706B94	GPON_GEM_US_BYTE_STAT [114].CNTR_HIGH32[31:0]	32
0xBB706B98	GPON_GEM_US_BYTE_STAT [115].CNTR_LOW32[31:0]	32
0xBB706B9C	GPON_GEM_US_BYTE_STAT [115].CNTR_HIGH32[31:0]	32
0xBB706BA0	GPON_GEM_US_BYTE_STAT [116].CNTR_LOW32[31:0]	32
0xBB706BA4	GPON_GEM_US_BYTE_STAT [116].CNTR_HIGH32[31:0]	32
0xBB706BA8	GPON_GEM_US_BYTE_STAT [117].CNTR_LOW32[31:0]	32
0xBB706BAC	GPON_GEM_US_BYTE_STAT [117].CNTR_HIGH32[31:0]	32
0xBB706BB0	GPON_GEM_US_BYTE_STAT [118].CNTR_LOW32[31:0]	32

Address	Register	Len
0xBB706BB4	GPON_GEM_US_BYTE_STAT [118].CNTR_HIGH32[31:0]	32
0xBB706BB8	GPON_GEM_US_BYTE_STAT [119].CNTR_LOW32[31:0]	32
0xBB706BBC	GPON_GEM_US_BYTE_STAT [119].CNTR_HIGH32[31:0]	32
0xBB706BC0	GPON_GEM_US_BYTE_STAT [120].CNTR_LOW32[31:0]	32
0xBB706BC4	GPON_GEM_US_BYTE_STAT [120].CNTR_HIGH32[31:0]	32
0xBB706BC8	GPON_GEM_US_BYTE_STAT [121].CNTR_LOW32[31:0]	32
0xBB706BCC	GPON_GEM_US_BYTE_STAT [121].CNTR_HIGH32[31:0]	32
0xBB706BD0	GPON_GEM_US_BYTE_STAT [122].CNTR_LOW32[31:0]	32
0xBB706BD4	GPON_GEM_US_BYTE_STAT [122].CNTR_HIGH32[31:0]	32
0xBB706BD8	GPON_GEM_US_BYTE_STAT [123].CNTR_LOW32[31:0]	32
0xBB706BDC	GPON_GEM_US_BYTE_STAT [123].CNTR_HIGH32[31:0]	32
0xBB706BE0	GPON_GEM_US_BYTE_STAT [124].CNTR_LOW32[31:0]	32
0xBB706BE4	GPON_GEM_US_BYTE_STAT [124].CNTR_HIGH32[31:0]	32
0xBB706BE8	GPON_GEM_US_BYTE_STAT [125].CNTR_LOW32[31:0]	32
0xBB706BEC	GPON_GEM_US_BYTE_STAT [125].CNTR_HIGH32[31:0]	32
0xBB706BF0	GPON_GEM_US_BYTE_STAT [126].CNTR_LOW32[31:0]	32
0xBB706BF4	GPON_GEM_US_BYTE_STAT [126].CNTR_HIGH32[31:0]	32
0xBB706BF8	GPON_GEM_US_BYTE_STAT [127].CNTR_LOW32[31:0]	32
0xBB706BFC	GPON_GEM_US_BYTE_STAT [127].CNTR_HIGH32[31:0]	32
0xBB706C00	TCONT_IDLE_BYTE_STAT [0].CNTR_LOW32[31:0]	32
0xBB706C04	TCONT_IDLE_BYTE_STAT [0].CNTR_HIGH32[31:0]	32
0xBB706C08	TCONT_IDLE_BYTE_STAT [1].CNTR_LOW32[31:0]	32
0xBB706C0C	TCONT_IDLE_BYTE_STAT [1].CNTR_HIGH32[31:0]	32
0xBB706C10	TCONT_IDLE_BYTE_STAT [2].CNTR_LOW32[31:0]	32
0xBB706C14	TCONT_IDLE_BYTE_STAT [2].CNTR_HIGH32[31:0]	32
0xBB706C18	TCONT_IDLE_BYTE_STAT [3].CNTR_LOW32[31:0]	32
0xBB706C1C	TCONT_IDLE_BYTE_STAT [3].CNTR_HIGH32[31:0]	32
0xBB706C20	TCONT_IDLE_BYTE_STAT [4].CNTR_LOW32[31:0]	32
0xBB706C24	TCONT_IDLE_BYTE_STAT [4].CNTR_HIGH32[31:0]	32
0xBB706C28	TCONT_IDLE_BYTE_STAT [5].CNTR_LOW32[31:0]	32
0xBB706C2C	TCONT_IDLE_BYTE_STAT [5].CNTR_HIGH32[31:0]	32
0xBB706C30	TCONT_IDLE_BYTE_STAT [6].CNTR_LOW32[31:0]	32
0xBB706C34	TCONT_IDLE_BYTE_STAT [6].CNTR_HIGH32[31:0]	32
0xBB706C38	TCONT_IDLE_BYTE_STAT [7].CNTR_LOW32[31:0]	32
0xBB706C3C	TCONT_IDLE_BYTE_STAT [7].CNTR_HIGH32[31:0]	32
0xBB706C40	TCONT_IDLE_BYTE_STAT [8].CNTR_LOW32[31:0]	32
0xBB706C44	TCONT_IDLE_BYTE_STAT [8].CNTR_HIGH32[31:0]	32
0xBB706C48	TCONT_IDLE_BYTE_STAT [9].CNTR_LOW32[31:0]	32
0xBB706C4C	TCONT_IDLE_BYTE_STAT [9].CNTR_HIGH32[31:0]	32
0xBB706C50	TCONT_IDLE_BYTE_STAT [10].CNTR_LOW32[31:0]	32
0xBB706C54	TCONT_IDLE_BYTE_STAT [10].CNTR_HIGH32[31:0]	32
0xBB706C58	TCONT_IDLE_BYTE_STAT [11].CNTR_LOW32[31:0]	32
0xBB706C5C	TCONT_IDLE_BYTE_STAT [11].CNTR_HIGH32[31:0]	32
0xBB706C60	TCONT_IDLE_BYTE_STAT [12].CNTR_LOW32[31:0]	32
0xBB706C64	TCONT_IDLE_BYTE_STAT [12].CNTR_HIGH32[31:0]	32
0xBB706C68	TCONT_IDLE_BYTE_STAT [13].CNTR_LOW32[31:0]	32

Address	Register	Len
0xBB706C6C	TCONT_IDLE_BYTE_STAT [13].CNTR_HIGH32[31:0]	32
0xBB706C70	TCONT_IDLE_BYTE_STAT [14].CNTR_LOW32[31:0]	32
0xBB706C74	TCONT_IDLE_BYTE_STAT [14].CNTR_HIGH32[31:0]	32
0xBB706C78	TCONT_IDLE_BYTE_STAT [15].CNTR_LOW32[31:0]	32
0xBB706C7C	TCONT_IDLE_BYTE_STAT [15].CNTR_HIGH32[31:0]	32
0xBB706C80	TCONT_IDLE_BYTE_STAT [16].CNTR_LOW32[31:0]	32
0xBB706C84	TCONT_IDLE_BYTE_STAT [16].CNTR_HIGH32[31:0]	32
0xBB706C88	TCONT_IDLE_BYTE_STAT [17].CNTR_LOW32[31:0]	32
0xBB706C8C	TCONT_IDLE_BYTE_STAT [17].CNTR_HIGH32[31:0]	32
0xBB706C90	TCONT_IDLE_BYTE_STAT [18].CNTR_LOW32[31:0]	32
0xBB706C94	TCONT_IDLE_BYTE_STAT [18].CNTR_HIGH32[31:0]	32
0xBB706C98	TCONT_IDLE_BYTE_STAT [19].CNTR_LOW32[31:0]	32
0xBB706C9C	TCONT_IDLE_BYTE_STAT [19].CNTR_HIGH32[31:0]	32
0xBB706CA0	TCONT_IDLE_BYTE_STAT [20].CNTR_LOW32[31:0]	32
0xBB706CA4	TCONT_IDLE_BYTE_STAT [20].CNTR_HIGH32[31:0]	32
0xBB706CA8	TCONT_IDLE_BYTE_STAT [21].CNTR_LOW32[31:0]	32
0xBB706CAC	TCONT_IDLE_BYTE_STAT [21].CNTR_HIGH32[31:0]	32
0xBB706CB0	TCONT_IDLE_BYTE_STAT [22].CNTR_LOW32[31:0]	32
0xBB706CB4	TCONT_IDLE_BYTE_STAT [22].CNTR_HIGH32[31:0]	32
0xBB706CB8	TCONT_IDLE_BYTE_STAT [23].CNTR_LOW32[31:0]	32
0xBB706CBC	TCONT_IDLE_BYTE_STAT [23].CNTR_HIGH32[31:0]	32
0xBB706CC0	TCONT_IDLE_BYTE_STAT [24].CNTR_LOW32[31:0]	32
0xBB706CC4	TCONT_IDLE_BYTE_STAT [24].CNTR_HIGH32[31:0]	32
0xBB706CC8	TCONT_IDLE_BYTE_STAT [25].CNTR_LOW32[31:0]	32
0xBB706CCC	TCONT_IDLE_BYTE_STAT [25].CNTR_HIGH32[31:0]	32
0xBB706CD0	TCONT_IDLE_BYTE_STAT [26].CNTR_LOW32[31:0]	32
0xBB706CD4	TCONT_IDLE_BYTE_STAT [26].CNTR_HIGH32[31:0]	32
0xBB706CD8	TCONT_IDLE_BYTE_STAT [27].CNTR_LOW32[31:0]	32
0xBB706CDC	TCONT_IDLE_BYTE_STAT [27].CNTR_HIGH32[31:0]	32
0xBB706CE0	TCONT_IDLE_BYTE_STAT [28].CNTR_LOW32[31:0]	32
0xBB706CE4	TCONT_IDLE_BYTE_STAT [28].CNTR_HIGH32[31:0]	32
0xBB706CE8	TCONT_IDLE_BYTE_STAT [29].CNTR_LOW32[31:0]	32
0xBB706CEC	TCONT_IDLE_BYTE_STAT [29].CNTR_HIGH32[31:0]	32
0xBB706CF0	TCONT_IDLE_BYTE_STAT [30].CNTR_LOW32[31:0]	32
0xBB706CF4	TCONT_IDLE_BYTE_STAT [30].CNTR_HIGH32[31:0]	32
0xBB706CF8	TCONT_IDLE_BYTE_STAT [31].CNTR_LOW32[31:0]	32
0xBB706CFC	TCONT_IDLE_BYTE_STAT [31].CNTR_HIGH32[31:0]	32
0xBB710000	NIC_ID_CRTL0.IDR3[31:24]	8
0xBB710000	NIC_ID_CRTL0.IDR2[23:16]	8
0xBB710000	NIC_ID_CRTL0.IDR1[15:8]	8
0xBB710000	NIC_ID_CRTL0.IDR0[7:0]	8
0xBB710004	NIC_ID_CRTL1.RESERVED[31:16]	16
0xBB710004	NIC_ID_CRTL1.IDR5[15:8]	8
0xBB710004	NIC_ID_CRTL1.IDR4[7:0]	8
0xBB710008	NIC_MC_CRTL0.MAR3[31:24]	8
0xBB710008	NIC_MC_CRTL0.MAR2[23:16]	8



Address	Register	Len
0xBB710008	NIC_MC_CRTL0.MAR1[15:8]	8
0xBB710008	NIC_MC_CRTL0.MAR0[7:0]	8
0xBB71000C	NIC_MC_CRTL1.MAR7[31:24]	8
0xBB71000C	NIC_MC_CRTL1.MAR6[23:16]	8
0xBB71000C	NIC_MC_CRTL1.MAR5[15:8]	8
0xBB71000C	NIC_MC_CRTL1.MAR4[7:0]	8
0xBB710010	NIC_MIB0.RX_OK_CNT[31:16]	16
0xBB710010	NIC_MIB0.TX_OK_CNT[15:0]	16
0xBB710014	NIC_MIB1.RX_ERR_CNT[31:16]	16
0xBB710014	NIC_MIB1.TX_ERR_CNT[15:0]	16
0xBB710018	NIC_MIB2.FAE[31:16]	16
0xBB710018	NIC_MIB2.MISS_PKT[15:0]	16
0xBB71001C	NIC_MIB3.TX_MUL_COL[31:16]	16
0xBB71001C	NIC_MIB3.TX_1_COL[15:0]	16
0xBB710020	NIC_MIB4.RX_OK_BC[31:16]	16
0xBB710020	NIC_MIB4.RX_OK_PHY[15:0]	16
0xBB710024	NIC_MIB5.TX_ABORT[31:16]	16
0xBB710024	NIC_MIB5.RX_OK_MC[15:0]	16
0xBB710028	NIC_MIB6.RSV2A[31:16]	16
0xBB710028	NIC_MIB6.TX_UNDER_RUN[15:0]	16
0xBB710034	NIC_STS.RESERVED[31:3]	29
0xBB710034	NIC_STS.TX_UNDER[2:2]	1
0xBB710034	NIC_STS.RESERVED[1:0]	2
0xBB710038	NIC_COM.RESERVED[31:4]	28
0xBB710038	NIC_COM.RX_JUMBO[3:3]	1
0xBB710038	NIC_COM.RX_VLAN[2:2]	1
0xBB710038	NIC_COM.RX_CHKSUM[1:1]	1
0xBB710038	NIC_COM.RST[0:0]	1
0xBB71003C	NIC_INTR.ISR_RDU6[31:31]	1
0xBB71003C	NIC_INTR.ISR_RDU5[30:30]	1
0xBB71003C	NIC_INTR.ISR_RDU4[29:29]	1
0xBB71003C	NIC_INTR.ISR_RDU3[28:28]	1
0xBB71003C	NIC_INTR.ISR_RDU2[27:27]	1
0xBB71003C	NIC_INTR.ISR_SW_INT[26:26]	1
0xBB71003C	NIC_INTR.ISR_TDU[25:25]	1
0xBB71003C	NIC_INTR.ISR_LINK_CHG[24:24]	1
0xBB71003C	NIC_INTR.ISR_TER[23:23]	1
0xBB71003C	NIC_INTR.ISR_TOK_TI[22:22]	1
0xBB71003C	NIC_INTR.ISR_RDU[21:21]	1
0xBB71003C	NIC_INTR.ISR_RER_OVF[20:20]	1
0xBB71003C	NIC_INTR.RESERVED[19:19]	1
0xBB71003C	NIC_INTR.ISR_RER_RUNT[18:18]	1
0xBB71003C	NIC_INTR.RESERVED[17:17]	1
0xBB71003C	NIC_INTR.ISR_ROK[16:16]	1
0xBB71003C	NIC_INTR.IMR_RDU6[15:15]	1
0xBB71003C	NIC_INTR.IMR_RDU5[14:14]	1

Address	Register	Len
0xBB71003C	NIC_INTR.IMR_RDU4[13:13]	1
0xBB71003C	NIC_INTR.IMR_RDU3[12:12]	1
0xBB71003C	NIC_INTR.IMR_RDU2[11:11]	1
0xBB71003C	NIC_INTR.IMR_SW_INT[10:10]	1
0xBB71003C	NIC_INTR.IMR_TDU[9:9]	1
0xBB71003C	NIC_INTR.IMR_LINK_CHG[8:8]	1
0xBB71003C	NIC_INTR.IMR_TER[7:7]	1
0xBB71003C	NIC_INTR.IMR_TOK_TI[6:6]	1
0xBB71003C	NIC_INTR.IMR_RDU[5:5]	1
0xBB71003C	NIC_INTR.IMR_RER_OVF[4:4]	1
0xBB71003C	NIC_INTR.RESERVED[3:3]	1
0xBB71003C	NIC_INTR.IMR_RER_RUNT[2:2]	1
0xBB71003C	NIC_INTR.RESERVED[1:1]	1
0xBB71003C	NIC_INTR.IMR_ROK[0:0]	1
0xBB710040	NIC_IMR0_CFG.RESERVED[31:29]	3
0xBB710040	NIC_IMR0_CFG.IMR0_TDU5[28:28]	1
0xBB710040	NIC_IMR0_CFG.IMR0_TDU4[27:27]	1
0xBB710040	NIC_IMR0_CFG.IMR0_TDU3[26:26]	1
0xBB710040	NIC_IMR0_CFG.IMR0_TDU2[25:25]	1
0xBB710040	NIC_IMR0_CFG.IMR0_TDU1[24:24]	1
0xBB710040	NIC_IMR0_CFG.RESERVED[23:21]	3
0xBB710040	NIC_IMR0_CFG.IMR0_TOK5[20:20]	1
0xBB710040	NIC_IMR0_CFG.IMR0_TOK4[19:19]	1
0xBB710040	NIC_IMR0_CFG.IMR0_TOK3[18:18]	1
0xBB710040	NIC_IMR0_CFG.IMR0_TOK2[17:17]	1
0xBB710040	NIC_IMR0_CFG.IMR0_TOK1[16:16]	1
0xBB710040	NIC_IMR0_CFG.RESERVED[15:6]	10
0xBB710040	NIC_IMR0_CFG.IMR0_ROK6[5:5]	1
0xBB710040	NIC_IMR0_CFG.IMR0_ROK5[4:4]	1
0xBB710040	NIC_IMR0_CFG.IMR0_ROK4[3:3]	1
0xBB710040	NIC_IMR0_CFG.IMR0_ROK3[2:2]	1
0xBB710040	NIC_IMR0_CFG.IMR0_ROK2[1:1]	1
0xBB710040	NIC_IMR0_CFG.IMR0_ROK1[0:0]	1
0xBB710044	NIC_IMR1_CFG.RESERVED[31:29]	3
0xBB710044	NIC_IMR1_CFG.IMR1_TDU5[28:28]	1
0xBB710044	NIC_IMR1_CFG.IMR1_TDU4[27:27]	1
0xBB710044	NIC_IMR1_CFG.IMR1_TDU3[26:26]	1
0xBB710044	NIC_IMR1_CFG.IMR1_TDU2[25:25]	1
0xBB710044	NIC_IMR1_CFG.IMR0_TDU1[24:24]	1
0xBB710044	NIC_IMR1_CFG.RESERVED[23:21]	3
0xBB710044	NIC_IMR1_CFG.IMR1_TOK5[20:20]	1
0xBB710044	NIC_IMR1_CFG.IMR1_TOK4[19:19]	1
0xBB710044	NIC_IMR1_CFG.IMR1_TOK3[18:18]	1
0xBB710044	NIC_IMR1_CFG.IMR1_TOK2[17:17]	1
0xBB710044	NIC_IMR1_CFG.IMR1_TOK1[16:16]	1
0xBB710044	NIC_IMR1_CFG.RESERVED[15:14]	2



Address	Register	Len
0xBB710044	NIC_IMR1_CFG.IMR1_RDU6[13:13]	1
0xBB710044	NIC_IMR1_CFG.IMR1_RDU5[12:12]	1
0xBB710044	NIC_IMR1_CFG.IMR1_RDU4[11:11]	1
0xBB710044	NIC_IMR1_CFG.IMR1_RDU3[10:10]	1
0xBB710044	NIC_IMR1_CFG.IMR1_RDU2[9:9]	1
0xBB710044	NIC_IMR1_CFG.IMR1_RDU1[8:8]	1
0xBB710044	NIC_IMR1_CFG.RESERVED[7:6]	2
0xBB710044	NIC_IMR1_CFG.IMR1_ROK6[5:5]	1
0xBB710044	NIC_IMR1_CFG.IMR1_ROK5[4:4]	1
0xBB710044	NIC_IMR1_CFG.IMR1_ROK4[3:3]	1
0xBB710044	NIC_IMR1_CFG.IMR1_ROK3[2:2]	1
0xBB710044	NIC_IMR1_CFG.IMR1_ROK2[1:1]	1
0xBB710044	NIC_IMR1_CFG.IMR1_ROK1[0:0]	1
0xBB710048	NIC_ISR1_CFG.RESERVED[31:29]	3
0xBB710048	NIC_ISR1_CFG.ISR1_TDU5[28:28]	1
0xBB710048	NIC_ISR1_CFG.ISR1_TDU4[27:27]	1
0xBB710048	NIC_ISR1_CFG.ISR1_TDU3[26:26]	1
0xBB710048	NIC_ISR1_CFG.ISR1_TDU2[25:25]	1
0xBB710048	NIC_ISR1_CFG.ISR1_TDU1[24:24]	1
0xBB710048	NIC_ISR1_CFG.RESERVED[23:21]	3
0xBB710048	NIC_ISR1_CFG.ISR1_TOK5[20:20]	1
0xBB710048	NIC_ISR1_CFG.ISR1_TOK4[19:19]	1
0xBB710048	NIC_ISR1_CFG.ISR1_TOK3[18:18]	1
0xBB710048	NIC_ISR1_CFG.ISR1_TOK2[17:17]	1
0xBB710048	NIC_ISR1_CFG.ISR1_TOK1[16:16]	1
0xBB710048	NIC_ISR1_CFG.RESERVED[15:6]	10
0xBB710048	NIC_ISR1_CFG.ISR1_ROK6[5:5]	1
0xBB710048	NIC_ISR1_CFG.ISR1_ROK5[4:4]	1
0xBB710048	NIC_ISR1_CFG.ISR1_ROK4[3:3]	1
0xBB710048	NIC_ISR1_CFG.ISR1_ROK3[2:2]	1
0xBB710048	NIC_ISR1_CFG.ISR1_ROK2[1:1]	1
0xBB710048	NIC_ISR1_CFG.ISR1_ROK1[0:0]	1
0xBB71004C	NIC_INT_ROUTE.RESERVED[31:25]	7
0xBB71004C	NIC_INT_ROUTE.TR5_INT_ROUTING[24:24]	1
0xBB71004C	NIC_INT_ROUTE.RESERVED[23:23]	1
0xBB71004C	NIC_INT_ROUTE.TR4_INT_ROUTING[22:22]	1
0xBB71004C	NIC_INT_ROUTE.RESERVED[21:21]	1
0xBB71004C	NIC_INT_ROUTE.TR3_INT_ROUTING[20:20]	1
0xBB71004C	NIC_INT_ROUTE.RESERVED[19:19]	1
0xBB71004C	NIC_INT_ROUTE.TR2_INT_ROUTING[18:18]	1
0xBB71004C	NIC_INT_ROUTE.RESERVED[17:17]	1
0xBB71004C	NIC_INT_ROUTE.TR1_INT_ROUTING[16:16]	1
0xBB71004C	NIC_INT_ROUTE.RESERVED[15:11]	5
0xBB71004C	NIC_INT_ROUTE.RR6_INT_ROUTING[10:10]	1
0xBB71004C	NIC_INT_ROUTE.RESERVED[9:9]	1
0xBB71004C	NIC_INT_ROUTE.RR5_INT_ROUTING[8:8]	1

Address	Register	Len
0xBB71004C	NIC_INT_ROUTE.RESERVED[7:7]	1
0xBB71004C	NIC_INT_ROUTE.RR4_INT_ROUTING[6:6]	1
0xBB71004C	NIC_INT_ROUTE.RESERVED[5:5]	1
0xBB71004C	NIC_INT_ROUTE.RR3_INT_ROUTING[4:4]	1
0xBB71004C	NIC_INT_ROUTE.RESERVED[3:3]	1
0xBB71004C	NIC_INT_ROUTE.RR2_INT_ROUTING[2:2]	1
0xBB71004C	NIC_INT_ROUTE.RESERVED[1:1]	1
0xBB71004C	NIC_INT_ROUTE.RR1_INT_ROUTING[0:0]	1
0xBB710050	NIC_TC.RESERVED[31:13]	19
0xBB710050	NIC_TC.IFG2_0[12:10]	3
0xBB710050	NIC_TC.LBK1_0[9:8]	2
0xBB710050	NIC_TC.RESERVED[7:0]	8
0xBB710054	NIC_RC.RESERVED[31:8]	24
0xBB710054	NIC_RC.HOME_PNA[7:7]	1
0xBB710054	NIC_RC.AFLOW[6:6]	1
0xBB710054	NIC_RC.AER[5:5]	1
0xBB710054	NIC_RC.AR[4:4]	1
0xBB710054	NIC_RC.AB[3:3]	1
0xBB710054	NIC_RC.AM[2:2]	1
0xBB710054	NIC_RC.APM[1:1]	1
0xBB710054	NIC_RC.AAP[0:0]	1
0xBB710058	NIC_CPUTAG.CTEN_RX[31:31]	1
0xBB710058	NIC_CPUTAG.CT_TSIZE[30:27]	4
0xBB710058	NIC_CPUTAG.CT_RSIZE_3_2[26:25]	2
0xBB710058	NIC_CPUTAG.CT_DSLRN[24:24]	1
0xBB710058	NIC_CPUTAG.CT_NORMK[23:23]	1
0xBB710058	NIC_CPUTAG.CT_ASPRI[22:22]	1
0xBB710058	NIC_CPUTAG.CT_SWITCH[21:18]	4
0xBB710058	NIC_CPUTAG.CT_RSIZE_1_0[17:16]	2
0xBB710058	NIC_CPUTAG.CTPM[15:8]	8
0xBB710058	NIC_CPUTAG.CTPV[7:0]	8
0xBB71005C	NIC_CONFIG.EN_INT_ROUTE[31:31]	1
0xBB71005C	NIC_CONFIG.EN_INT_SPLIT[30:30]	1
0xBB71005C	NIC_CONFIG.RFF_SIZE_SEL[29:28]	2
0xBB71005C	NIC_CONFIG.TSO_ID_SEL[27:27]	1
0xBB71005C	NIC_CONFIG.RESERVED[26:0]	27
0xBB710060	NIC_CPUTAG1.RESERVED[31:7]	25
0xBB710060	NIC_CPUTAG1.SPA_DSL[6:4]	3
0xBB710060	NIC_CPUTAG1.RESERVED[3:3]	1
0xBB710060	NIC_CPUTAG1.SPA_PON[2:0]	3
0xBB710068	NIC_MS.FORCE_TRXFCE[31:31]	1
0xBB710068	NIC_MS.RXFCE[30:30]	1
0xBB710068	NIC_MS.TXFCE[29:29]	1
0xBB710068	NIC_MS.SPEED_1000[28:28]	1
0xBB710068	NIC_MS.SPEED_10[27:27]	1
0xBB710068	NIC_MS.LINKB[26:26]	1

Address	Register	Len
0xBB710068	NIC_MS.TXPF[25:25]	1
0xBB710068	NIC_MS.RXPF[24:24]	1
0xBB710068	NIC_MS.SEL_RGMII[23:23]	1
0xBB710068	NIC_MS.FULLDUPREG[22:22]	1
0xBB710068	NIC_MS.NWCOMPLETE[21:21]	1
0xBB710068	NIC_MS.SEL_MII[20:20]	1
0xBB710068	NIC_MS.FORCEDFULLDUP[19:19]	1
0xBB710068	NIC_MS.FORCELINK[18:18]	1
0xBB710068	NIC_MS.FORCE_SPD[17:16]	2
0xBB710068	NIC_MS.SEL_PHYIF_0[15:15]	1
0xBB710068	NIC_MS.RESERVED[14:14]	1
0xBB710068	NIC_MS.PHY_MODE[13:13]	1
0xBB710068	NIC_MS.RGMII_RX_STS[12:12]	1
0xBB710068	NIC_MS.RGMII_TX_STS[11:11]	1
0xBB710068	NIC_MS.FORCE_SPD_MODE[10:10]	1
0xBB710068	NIC_MS.RESERVED[9:0]	10
0xBB71006C	NIC_MIIA.FLAG[31:31]	1
0xBB71006C	NIC_MIIA.PHY_ADDR[30:26]	5
0xBB71006C	NIC_MIIA.RESERVED[25:23]	3
0xBB71006C	NIC_MIIA.DIS_AUTO_POLLING[22:22]	1
0xBB71006C	NIC_MIIA.POLLING_EEE[21:21]	1
0xBB71006C	NIC_MIIA.REG_ADDR_4_0[20:16]	5
0xBB71006C	NIC_MIIA.DATA_15_0[15:0]	16
0xBB710070	NIC_SWINT.RESERVED[31:1]	31
0xBB710070	NIC_SWINT.SWINT[0:0]	1
0xBB710074	NIC_VLAN.STAG_PID[31:16]	16
0xBB710074	NIC_VLAN.TDSC_VLAN_TYPE[15:15]	1
0xBB710074	NIC_VLAN.RESERVED[14:0]	15
0xBB710080	NIC_LED_CR.RESERVED[31:20]	12
0xBB710080	NIC_LED_CR.EEE_EN_LED[19:19]	1
0xBB710080	NIC_LED_CR.CUSTOM_LED[18:18]	1
0xBB710080	NIC_LED_CR.LED_SEL[17:16]	2
0xBB710080	NIC_LED_CR.LED_SEL3[15:12]	4
0xBB710080	NIC_LED_CR.LED_SEL2[11:8]	4
0xBB710080	NIC_LED_CR.LED_SEL1[7:4]	4
0xBB710080	NIC_LED_CR.LED_SEL0[3:0]	4
0xBB720000	NIC_TXFDP1.TXFDP1[31:0]	32
0xBB720004	NIC_TXCDO1.RESERVED[31:12]	20
0xBB720004	NIC_TXCDO1.TXCDO1[11:0]	12
0xBB720010	NIC_TXFDP2.TXFDP2[31:0]	32
0xBB720014	NIC_TXCDO2.RESERVED[31:12]	20
0xBB720014	NIC_TXCDO2.TXCDO2[11:0]	12
0xBB720020	NIC_TXFDP3.TXFDP3[31:0]	32
0xBB720024	NIC_TXCDO3.RESERVED[31:12]	20
0xBB720024	NIC_TXCDO3.TXCDO3[11:0]	12
0xBB720030	NIC_TXFDP4.TXFDP4[31:0]	32

Address	Register	Len
0xBB720034	NIC_TXCDO4.RESERVED[31:12]	20
0xBB720034	NIC_TXCDO4.TXCDO4[11:0]	12
0xBB720040	NIC_TXFDP5.TXFDP5[31:0]	32
0xBB720044	NIC_TXCDO5.RESERVED[31:12]	20
0xBB720044	NIC_TXCDO5.TXCDO5[11:0]	12
0xBB720070	NIC_RRING_ROUTING1.RESERVED[31:31]	1
0xBB720070	NIC_RRING_ROUTING1.PRI_7_ROUTE[30:28]	3
0xBB720070	NIC_RRING_ROUTING1.RESERVED[27:27]	1
0xBB720070	NIC_RRING_ROUTING1.PRI_6_ROUTE[26:24]	3
0xBB720070	NIC_RRING_ROUTING1.RESERVED[23:23]	1
0xBB720070	NIC_RRING_ROUTING1.PRI_5_ROUTE[22:20]	3
0xBB720070	NIC_RRING_ROUTING1.RESERVED[19:19]	1
0xBB720070	NIC_RRING_ROUTING1.PRI_4_ROUTE[18:16]	3
0xBB720070	NIC_RRING_ROUTING1.RESERVED[15:15]	1
0xBB720070	NIC_RRING_ROUTING1.PRI_3_ROUTE[14:12]	3
0xBB720070	NIC_RRING_ROUTING1.RESERVED[11:11]	1
0xBB720070	NIC_RRING_ROUTING1.PRI_2_ROUTE[10:8]	3
0xBB720070	NIC_RRING_ROUTING1.RESERVED[7:7]	1
0xBB720070	NIC_RRING_ROUTING1.PRI_1_ROUTE[6:4]	3
0xBB720070	NIC_RRING_ROUTING1.RESERVED[3:3]	1
0xBB720070	NIC_RRING_ROUTING1.PRI_0_ROUTE[2:0]	3
0xBB720074	NIC_RRING_ROUTING2.RESERVED[31:31]	1
0xBB720074	NIC_RRING_ROUTING2.PRI_7_ROUTE[30:28]	3
0xBB720074	NIC_RRING_ROUTING2.RESERVED[27:27]	1
0xBB720074	NIC_RRING_ROUTING2.PRI_6_ROUTE[26:24]	3
0xBB720074	NIC_RRING_ROUTING2.RESERVED[23:23]	1
0xBB720074	NIC_RRING_ROUTING2.PRI_5_ROUTE[22:20]	3
0xBB720074	NIC_RRING_ROUTING2.RESERVED[19:19]	1
0xBB720074	NIC_RRING_ROUTING2.PRI_4_ROUTE[18:16]	3
0xBB720074	NIC_RRING_ROUTING2.RESERVED[15:15]	1
0xBB720074	NIC_RRING_ROUTING2.PRI_3_ROUTE[14:12]	3
0xBB720074	NIC_RRING_ROUTING2.RESERVED[11:11]	1
0xBB720074	NIC_RRING_ROUTING2.PRI_2_ROUTE[10:8]	3
0xBB720074	NIC_RRING_ROUTING2.RESERVED[7:7]	1
0xBB720074	NIC_RRING_ROUTING2.PRI_1_ROUTE[6:4]	3
0xBB720074	NIC_RRING_ROUTING2.RESERVED[3:3]	1
0xBB720074	NIC_RRING_ROUTING2.PRI_0_ROUTE[2:0]	3
0xBB720078	NIC_RRING_ROUTING3.RESERVED[31:31]	1
0xBB720078	NIC_RRING_ROUTING3.PRI_7_ROUTE[30:28]	3
0xBB720078	NIC_RRING_ROUTING3.RESERVED[27:27]	1
0xBB720078	NIC_RRING_ROUTING3.PRI_6_ROUTE[26:24]	3
0xBB720078	NIC_RRING_ROUTING3.RESERVED[23:23]	1
0xBB720078	NIC_RRING_ROUTING3.PRI_5_ROUTE[22:20]	3
0xBB720078	NIC_RRING_ROUTING3.RESERVED[19:19]	1
0xBB720078	NIC_RRING_ROUTING3.PRI_4_ROUTE[18:16]	3
0xBB720078	NIC_RRING_ROUTING3.RESERVED[15:15]	1

Address	Register	Len
0xBB720078	NIC_RRING_ROUTING3.PRI_3_ROUTE[14:12]	3
0xBB720078	NIC_RRING_ROUTING3.RESERVED[11:11]	1
0xBB720078	NIC_RRING_ROUTING3.PRI_2_ROUTE[10:8]	3
0xBB720078	NIC_RRING_ROUTING3.RESERVED[7:7]	1
0xBB720078	NIC_RRING_ROUTING3.PRI_1_ROUTE[6:4]	3
0xBB720078	NIC_RRING_ROUTING3.RESERVED[3:3]	1
0xBB720078	NIC_RRING_ROUTING3.PRI_0_ROUTE[2:0]	3
0xBB72007C	NIC_RRING_ROUTING4.RESERVED[31:31]	1
0xBB72007C	NIC_RRING_ROUTING4.PRI_7_ROUTE[30:28]	3
0xBB72007C	NIC_RRING_ROUTING4.RESERVED[27:27]	1
0xBB72007C	NIC_RRING_ROUTING4.PRI_6_ROUTE[26:24]	3
0xBB72007C	NIC_RRING_ROUTING4.RESERVED[23:23]	1
0xBB72007C	NIC_RRING_ROUTING4.PRI_5_ROUTE[22:20]	3
0xBB72007C	NIC_RRING_ROUTING4.RESERVED[19:19]	1
0xBB72007C	NIC_RRING_ROUTING4.PRI_4_ROUTE[18:16]	3
0xBB72007C	NIC_RRING_ROUTING4.RESERVED[15:15]	1
0xBB72007C	NIC_RRING_ROUTING4.PRI_3_ROUTE[14:12]	3
0xBB72007C	NIC_RRING_ROUTING4.RESERVED[11:11]	1
0xBB72007C	NIC_RRING_ROUTING4.PRI_2_ROUTE[10:8]	3
0xBB72007C	NIC_RRING_ROUTING4.RESERVED[7:7]	1
0xBB72007C	NIC_RRING_ROUTING4.PRI_1_ROUTE[6:4]	3
0xBB72007C	NIC_RRING_ROUTING4.RESERVED[3:3]	1
0xBB72007C	NIC_RRING_ROUTING4.PRI_0_ROUTE[2:0]	3
0xBB720080	NIC_RRING_ROUTING5.RESERVED[31:31]	1
0xBB720080	NIC_RRING_ROUTING5.PRI_7_ROUTE[30:28]	3
0xBB720080	NIC_RRING_ROUTING5.RESERVED[27:27]	1
0xBB720080	NIC_RRING_ROUTING5.PRI_6_ROUTE[26:24]	3
0xBB720080	NIC_RRING_ROUTING5.RESERVED[23:23]	1
0xBB720080	NIC_RRING_ROUTING5.PRI_5_ROUTE[22:20]	3
0xBB720080	NIC_RRING_ROUTING5.RESERVED[19:19]	1
0xBB720080	NIC_RRING_ROUTING5.PRI_4_ROUTE[18:16]	3
0xBB720080	NIC_RRING_ROUTING5.RESERVED[15:15]	1
0xBB720080	NIC_RRING_ROUTING5.PRI_3_ROUTE[14:12]	3
0xBB720080	NIC_RRING_ROUTING5.RESERVED[11:11]	1
0xBB720080	NIC_RRING_ROUTING5.PRI_2_ROUTE[10:8]	3
0xBB720080	NIC_RRING_ROUTING5.RESERVED[7:7]	1
0xBB720080	NIC_RRING_ROUTING5.PRI_1_ROUTE[6:4]	3
0xBB720080	NIC_RRING_ROUTING5.RESERVED[3:3]	1
0xBB720080	NIC_RRING_ROUTING5.PRI_0_ROUTE[2:0]	3
0xBB720084	NIC_RRING_ROUTING6.RESERVED[31:31]	1
0xBB720084	NIC_RRING_ROUTING6.PRI_7_ROUTE[30:28]	3
0xBB720084	NIC_RRING_ROUTING6.RESERVED[27:27]	1
0xBB720084	NIC_RRING_ROUTING6.PRI_6_ROUTE[26:24]	3
0xBB720084	NIC_RRING_ROUTING6.RESERVED[23:23]	1
0xBB720084	NIC_RRING_ROUTING6.PRI_5_ROUTE[22:20]	3
0xBB720084	NIC_RRING_ROUTING6.RESERVED[19:19]	1

Address	Register	Len
0xBB720084	NIC_RRING_ROUTING6.PRI_4_ROUTE[18:16]	3
0xBB720084	NIC_RRING_ROUTING6.RESERVED[15:15]	1
0xBB720084	NIC_RRING_ROUTING6.PRI_3_ROUTE[14:12]	3
0xBB720084	NIC_RRING_ROUTING6.RESERVED[11:11]	1
0xBB720084	NIC_RRING_ROUTING6.PRI_2_ROUTE[10:8]	3
0xBB720084	NIC_RRING_ROUTING6.RESERVED[7:7]	1
0xBB720084	NIC_RRING_ROUTING6.PRI_1_ROUTE[6:4]	3
0xBB720084	NIC_RRING_ROUTING6.RESERVED[3:3]	1
0xBB720084	NIC_RRING_ROUTING6.PRI_0_ROUTE[2:0]	3
0xBB720088	DUMMY [0].DUMMY[31:0]	32
0xBB72008C	DUMMY [1].DUMMY[31:0]	32
0xBB720090	NIC_RXFDP2.RXFDP[31:0]	32
0xBB720094	NIC_RXCDORINGRS2.RESERVED[31:28]	4
0xBB720094	NIC_RXCDORINGRS2.RXRINGSIZE[27:16]	12
0xBB720094	NIC_RXCDORINGRS2.RESERVED[15:12]	4
0xBB720094	NIC_RXCDORINGRS2.RXCDO[11:0]	12
0xBB720098	NIC_RX_CPU_DESN2.RESERVED[31:12]	20
0xBB720098	NIC_RX_CPU_DESN2.CPU_DES_NUM[11:0]	12
0xBB72009C	NIC_RX_DES_THRES2.RESERVED[31:28]	4
0xBB72009C	NIC_RX_DES_THRES2.DES_ON_TH[27:16]	12
0xBB72009C	NIC_RX_DES_THRES2.RESERVED[15:12]	4
0xBB72009C	NIC_RX_DES_THRES2.DES_OFF_TH[11:0]	12
0xBB7200A0	NIC_RXFDP3.RXFDP[31:0]	32
0xBB7200A4	NIC_RXCDORINGRS3.RESERVED[31:28]	4
0xBB7200A4	NIC_RXCDORINGRS3.RXRINGSIZE[27:16]	12
0xBB7200A4	NIC_RXCDORINGRS3.RESERVED[15:12]	4
0xBB7200A4	NIC_RXCDORINGRS3.RXCDO[11:0]	12
0xBB7200A8	NIC_RX_CPU_DESN3.RESERVED[31:12]	20
0xBB7200A8	NIC_RX_CPU_DESN3.CPU_DES_NO[11:0]	12
0xBB7200AC	NIC_RX_DES_THRES3.RESERVED[31:28]	4
0xBB7200AC	NIC_RX_DES_THRES3.DES_ON_TH[27:16]	12
0xBB7200AC	NIC_RX_DES_THRES3.RESERVED[15:12]	4
0xBB7200AC	NIC_RX_DES_THRES3.DES_OFF_TH[11:0]	12
0xBB7200B0	NIC_RXFDP4.RXFDP4[31:0]	32
0xBB7200B4	NIC_RXCDORINGRS4.RESERVED[31:28]	4
0xBB7200B4	NIC_RXCDORINGRS4.RXRINGSIZE[27:16]	12
0xBB7200B4	NIC_RXCDORINGRS4.RESERVED[15:12]	4
0xBB7200B4	NIC_RXCDORINGRS4.RXCDO[11:0]	12
0xBB7200B8	NIC_RX_CPU_DESN4.RESERVED[31:12]	20
0xBB7200B8	NIC_RX_CPU_DESN4.CPU_DES_NO[11:0]	12
0xBB7200BC	NIC_RX_DES_THRES4.RESERVED[31:28]	4
0xBB7200BC	NIC_RX_DES_THRES4.DES_ON_TH[27:16]	12
0xBB7200BC	NIC_RX_DES_THRES4.RESERVED[15:12]	4
0xBB7200BC	NIC_RX_DES_THRES4.DES_OFF_TH[11:0]	12
0xBB7200C0	NIC_RXFDP5.RXFDP5[31:0]	32
0xBB7200C4	NIC_RXCDORINGRS5.RESERVED[31:28]	4

Address	Register	Len
0xBB7200C4	NIC_RXCDORINGRS5.RXRINGSIZE[27:16]	12
0xBB7200C4	NIC_RXCDORINGRS5.RESERVED[15:12]	4
0xBB7200C4	NIC_RXCDORINGRS5.RXCDO[11:0]	12
0xBB7200C8	NIC_RX_CPU_DESN5.RESERVED[31:12]	20
0xBB7200C8	NIC_RX_CPU_DESN5.CPU_DES_NO[11:0]	12
0xBB7200CC	NIC_RX_DES_THRES5.RESERVED[31:28]	4
0xBB7200CC	NIC_RX_DES_THRES5.DES_ON_TH[27:16]	12
0xBB7200CC	NIC_RX_DES_THRES5.RESERVED[15:12]	4
0xBB7200CC	NIC_RX_DES_THRES5.DES_OFF_TH[11:0]	12
0xBB7200D0	NIC_RXFDP6.RXFDP6[31:0]	32
0xBB7200D4	NIC_RXCDORINGRS6.RESERVED[31:28]	4
0xBB7200D4	NIC_RXCDORINGRS6.RXRINGSIZE[27:16]	12
0xBB7200D4	NIC_RXCDORINGRS6.RESERVED[15:12]	4
0xBB7200D4	NIC_RXCDORINGRS6.RXCDO[11:0]	12
0xBB7200D8	NIC_RX_CPU_DESN6.RESERVED[31:12]	20
0xBB7200D8	NIC_RX_CPU_DESN6.CPU_DES_NO[11:0]	12
0xBB7200DC	NIC_RX_DES_THRES6.RESERVED[31:28]	4
0xBB7200DC	NIC_RX_DES_THRES6.DES_ON_TH[27:16]	12
0xBB7200DC	NIC_RX_DES_THRES6.RESERVED[15:12]	4
0xBB7200DC	NIC_RX_DES_THRES6.DES_OFF_TH[11:0]	12
0xBB7200E0	DUMMY [0].DUMMY[31:0]	32
0xBB7200E4	DUMMY [1].DUMMY[31:0]	32
0xBB7200E8	DUMMY [2].DUMMY[31:0]	32
0xBB7200EC	DUMMY [3].DUMMY[31:0]	32
0xBB7200F0	NIC_RXFDP1.RXFDP1[31:0]	32
0xBB7200F4	NIC_RXCDORINGRS1.RESERVED[31:28]	4
0xBB7200F4	NIC_RXCDORINGRS1.RXRINGSIZE[27:16]	12
0xBB7200F4	NIC_RXCDORINGRS1.RESERVED[15:12]	4
0xBB7200F4	NIC_RXCDORINGRS1.RXCDO[11:0]	12
0xBB7200F8	DUMMY.DUMMY[31:0]	32
0xBB7200FC	NIC_SMSA.SMSA[31:0]	32
0xBB720100	NIC_PROBE_SELECT.RESERVED[31:26]	6
0xBB720100	NIC_PROBE_SELECT.PROB_SEL[25:24]	2
0xBB720100	NIC_PROBE_SELECT.RESERVED[23:9]	15
0xBB720104	NIC_DIAGNOSE1.RESERVED[31:6]	26
0xBB720104	NIC_DIAGNOSE1.RXMRRING[5:3]	3
0xBB720104	NIC_DIAGNOSE1.LSO_STS[2:0]	3
0xBB720108	DUMMY [0].DUMMY[31:0]	32
0xBB72010C	DUMMY [1].DUMMY[31:0]	32
0xBB720110	DUMMY [2].DUMMY[31:0]	32
0xBB720114	DUMMY [3].DUMMY[31:0]	32
0xBB720118	DUMMY [4].DUMMY[31:0]	32
0xBB72011C	DUMMY [5].DUMMY[31:0]	32
0xBB720120	DUMMY [6].DUMMY[31:0]	32
0xBB720124	DUMMY [7].DUMMY[31:0]	32
0xBB720128	DUMMY [8].DUMMY[31:0]	32

Address	Register	Len
0xBB72012C	NIC_RX_PSE1_TXC_OUT_SEL1.RESERVED[31:30]	2
0xBB72012C	NIC_RX_PSE1_TXC_OUT_SEL1.SET_D_TXC[29:29]	1
0xBB72012C	NIC_RX_PSE1_TXC_OUT_SEL1.TXC_OUT_PH_SEL[28:24]	5
0xBB72012C	NIC_RX_PSE1_TXC_OUT_SEL1.RESERVED[23:4]	20
0xBB72012C	NIC_RX_PSE1_TXC_OUT_SEL1.RX_TH_OFF_1[3:0]	4
0xBB720130	NIC_ETNRXCPU1.CPU_DES_NUM_7_0[31:30]	2
0xBB720130	NIC_ETNRXCPU1.DES_ON_TH_7_0[29:29]	1
0xBB720130	NIC_ETNRXCPU1.DES_OFF_TH[28:24]	5
0xBB720134	NIC_ETN_IO_CMD.MAX_DMA_SEL_0[31:31]	1
0xBB720134	NIC_ETN_IO_CMD.SHORT_DES_FMT[30:30]	1
0xBB720134	NIC_ETN_IO_CMD.MAX_DMA_SEL_1[29:29]	1
0xBB720134	NIC_ETN_IO_CMD.EN_EARLY_TX[28:28]	1
0xBB720134	NIC_ETN_IO_CMD.TX_PKT_TMR[27:24]	4
0xBB720134	NIC_ETN_IO_CMD.TX_INT_MITIG_3[23:23]	1
0xBB720134	NIC_ETN_IO_CMD.RX_PKT_TMR_3[22:22]	1
0xBB720134	NIC_ETN_IO_CMD.RX_INT_MITIG_3[21:21]	1
0xBB720134	NIC_ETN_IO_CMD.TSH[20:19]	2
0xBB720134	NIC_ETN_IO_CMD.TX_INT_MITIG_2_0[18:16]	3
0xBB720134	NIC_ETN_IO_CMD.RX_PKT_TMR_2_0[15:13]	3
0xBB720134	NIC_ETN_IO_CMD.RXFTH[12:11]	2
0xBB720134	NIC_ETN_IO_CMD.RX_INT_MITIG_2_0[10:8]	3
0xBB720134	NIC_ETN_IO_CMD.REG_INI_TMR_SEL[7:6]	2
0xBB720134	NIC_ETN_IO_CMD.RE[5:5]	1
0xBB720134	NIC_ETN_IO_CMD.TE[4:4]	1
0xBB720134	NIC_ETN_IO_CMD.TXFN4[3:3]	1
0xBB720134	NIC_ETN_IO_CMD.TXFN3[2:2]	1
0xBB720134	NIC_ETN_IO_CMD.TXFN2[1:1]	1
0xBB720134	NIC_ETN_IO_CMD.TXFN1[0:0]	1
0xBB720138	NIC_ETN_IO_CMD1.RESERVED[31:31]	1
0xBB720138	NIC_ETN_IO_CMD1.DSC_FMT_EXTRA[30:28]	3
0xBB720138	NIC_ETN_IO_CMD1.RESERVED[27:27]	1
0xBB720138	NIC_ETN_IO_CMD1.RXOKINT_MSK_128B[26:26]	1
0xBB720138	NIC_ETN_IO_CMD1.EN_RX_MRING[25:25]	1
0xBB720138	NIC_ETN_IO_CMD1.EN_1GB[24:24]	1
0xBB720138	NIC_ETN_IO_CMD1.RESERVED[23:22]	2
0xBB720138	NIC_ETN_IO_CMD1.RXRING6[21:21]	1
0xBB720138	NIC_ETN_IO_CMD1.RXRING5[20:20]	1
0xBB720138	NIC_ETN_IO_CMD1.RXRING4[19:19]	1
0xBB720138	NIC_ETN_IO_CMD1.RXRING3[18:18]	1
0xBB720138	NIC_ETN_IO_CMD1.RXRING2[17:17]	1
0xBB720138	NIC_ETN_IO_CMD1.RXRING1[16:16]	1
0xBB720138	NIC_ETN_IO_CMD1.TX_HL_PRI_SEL[15:14]	2
0xBB720138	NIC_ETN_IO_CMD1.RESERVED[13:9]	5
0xBB720138	NIC_ETN_IO_CMD1.TX_FN5[8:8]	1
0xBB720138	NIC_ETN_IO_CMD1.RESERVED[7:5]	3
0xBB720138	NIC_ETN_IO_CMD1.TXQ5_H[4:4]	1



Address	Register	Len
0xBB720138	NIC_ETN_IO_CMD1.TXQ4_H[3:3]	1
0xBB720138	NIC_ETN_IO_CMD1.TXQ3_H[2:2]	1
0xBB720138	NIC_ETN_IO_CMD1.TXQ2_H[1:1]	1
0xBB720138	NIC_ETN_IO_CMD1.TXQ1_H[0:0]	1
0xBB72013C	NIC_WOL.RESERVED[31:3]	29
0xBB72013C	NIC_WOL.WOL_PME[2:2]	1
0xBB72013C	NIC_WOL.WOL_STS[1:1]	1
0xBB72013C	NIC_WOL.WOL_CMD[0:0]	1
0xBB800000	NIFP.RESERVED[31:18]	14
0xBB800000	NIFP.INTP5[17:15]	3
0xBB800000	NIFP.INTP4[14:12]	3
0xBB800000	NIFP.INTP3[11:9]	3
0xBB800000	NIFP.INTP2[8:6]	3
0xBB800000	NIFP.INTP1[5:3]	3
0xBB800000	NIFP.INTP0[2:0]	3
0xBB800004	NIFEP.RESERVED[31:15]	17
0xBB800004	NIFEP.INTEXTP4[14:12]	3
0xBB800004	NIFEP.INTEXTP3[11:9]	3
0xBB800004	NIFEP.INTEXTP2[8:6]	3
0xBB800004	NIFEP.INTEXTP1[5:3]	3
0xBB800004	NIFEP.INTEXTP0[2:0]	3
0xBB800008	NIFVCH.RESERVED[31:24]	8
0xBB800008	NIFVCH.VC15[23:21]	3
0xBB800008	NIFVCH.VC14[20:18]	3
0xBB800008	NIFVCH.VC13[17:15]	3
0xBB800008	NIFVCH.VC12[14:12]	3
0xBB800008	NIFVCH.VC11[11:9]	3
0xBB800008	NIFVCH.VC10[8:6]	3
0xBB800008	NIFVCH.VC9[5:3]	3
0xBB800008	NIFVCH.VC8[2:0]	3
0xBB80000C	NIFVCL.RESERVED[31:24]	8
0xBB80000C	NIFVCL.VC7[23:21]	3
0xBB80000C	NIFVCL.VC6[20:18]	3
0xBB80000C	NIFVCL.VC5[17:15]	3
0xBB80000C	NIFVCL.VC4[14:12]	3
0xBB80000C	NIFVCL.VC3[11:9]	3
0xBB80000C	NIFVCL.VC2[8:6]	3
0xBB80000C	NIFVCL.VC1[5:3]	3
0xBB80000C	NIFVCL.VC0[2:0]	3
0xBB800010	SWTCR0.RESERVED[31:26]	6
0xBB800010	SWTCR0.IPMST_CTRL[25:24]	2
0xBB800010	SWTCR0.FRAGMENT2CPU[23:23]	1
0xBB800010	SWTCR0.L4_TRF_HWWRK_SEL[22:22]	1
0xBB800010	SWTCR0.L4_TRF_CHG[21:21]	1
0xBB800010	SWTCR0.L4_TRF_EXEC_CLR[20:19]	2
0xBB800010	SWTCR0.ARP_TRF_HWWRK_SEL[18:18]	1

Address	Register	Len
0xBB800010	SWTCR0.ARP_TRF_CHG[17:17]	1
0xBB800010	SWTCR0.ARP_TRF_EXEC_CLR[16:15]	2
0xBB800010	SWTCR0.L4CHKSERRALLOW[14:14]	1
0xBB800010	SWTCR0.L3CHKSERRALLOW[13:13]	1
0xBB800010	SWTCR0.TTL_1ENABLE[12:12]	1
0xBB800010	SWTCR0.NATMODE[11:10]	2
0xBB800010	SWTCR0.LIMDBC[9:8]	2
0xBB800010	SWTCR0.WANROUTEMODE[7:6]	2
0xBB800010	SWTCR0.RESERVED[5:5]	1
0xBB800010	SWTCR0.ENNATT2LOG[4:4]	1
0xBB800010	SWTCR0.MONSEL[3:0]	4
0xBB800014	PP_AGE.RESERVED[31:8]	24
0xBB800014	PP_AGE.PPPOE_TRF_BMP[7:0]	8
0xBB800018	NB_TRF.NBT3[31:0]	32
0xBB80001C	NB_TRF.NBT2[31:0]	32
0xBB800020	NB_TRF.NBT1[31:0]	32
0xBB800024	NB_TRF.NBT0[31:0]	32
0xBB800028	V6_BD_CTL.RESERVED[31:31]	1
0xBB800028	V6_BD_CTL.PB_EN[30:30]	1
0xBB800028	V6_BD_CTL.RESERVED[29:0]	30
0xBB80002C	BD_TRF.BD_TRF_BMP[31:0]	32
0xBB800030	BD_CFG.WAN_BINDING_UNMATCHED_L2L3[31:30]	2
0xBB800030	BD_CFG.WAN_BINDING_UNMATCHED_L2L34[29:28]	2
0xBB800030	BD_CFG.WAN_BINDING_UNMATCHED_L3L2[27:26]	2
0xBB800030	BD_CFG.WAN_BINDING_UNMATCHED_L3L34[25:25]	1
0xBB800030	BD_CFG.WAN_BINDING_UNMATCHED_L34L2[24:23]	2
0xBB800030	BD_CFG.WAN_BINDING_UNMATCHED_L34L3[22:22]	1
0xBB800030	BD_CFG.WAN_BINDING_UNMATCHED_L3L3[21:21]	1
0xBB800030	BD_CFG.WAN_BINDING_CUSTOMIZED_L2[20:19]	2
0xBB800030	BD_CFG.WAN_BINDING_CUSTOMIZED_L3[18:17]	2
0xBB800030	BD_CFG.WAN_BINDING_CUSTOMIZED_L34[16:15]	2
0xBB800030	BD_CFG.RESERVED[14:0]	15
0xBB800100	NAT_TBL_ACCESS_CTRL.RESERVED[31:26]	6
0xBB800100	NAT_TBL_ACCESS_CTRL.RD_EXE[25:25]	1
0xBB800100	NAT_TBL_ACCESS_CTRL.WR_EXE[24:24]	1
0xBB800100	NAT_TBL_ACCESS_CTRL.RESERVED[23:20]	4
0xBB800100	NAT_TBL_ACCESS_CTRL.TBL_IDX[19:16]	4
0xBB800100	NAT_TBL_ACCESS_CTRL.ENTRY_IDX[15:0]	16
0xBB800104	NAT_TBL_ACCESS_CLR.RESERVED[31:14]	18
0xBB800104	NAT_TBL_ACCESS_CLR.RST_V6RT[13:13]	1
0xBB800104	NAT_TBL_ACCESS_CLR.RST_NB[12:12]	1
0xBB800104	NAT_TBL_ACCESS_CLR.RST_BD[11:11]	1
0xBB800104	NAT_TBL_ACCESS_CLR.RST_WT[10:10]	1
0xBB800104	NAT_TBL_ACCESS_CLR.RST_L3[9:9]	1
0xBB800104	NAT_TBL_ACCESS_CLR.RST_PP[8:8]	1
0xBB800104	NAT_TBL_ACCESS_CLR.RST_NH[7:7]	1

Address	Register	Len
0xBB800104	NAT_TBL_ACCESS_CLR.RST_IF[6:6]	1
0xBB800104	NAT_TBL_ACCESS_CLR.RST_IP[5:5]	1
0xBB800104	NAT_TBL_ACCESS_CLR.RST_ARP[4:4]	1
0xBB800104	NAT_TBL_ACCESS_CLR.RST_NAPTR[3:3]	1
0xBB800104	NAT_TBL_ACCESS_CLR.RST_NAPT[2:2]	1
0xBB800104	NAT_TBL_ACCESS_CLR.RESERVED[1:0]	2
0xBB800108	NAT_TBL_ACCESS_RDDATA.RDDATA4[31:0]	32
0xBB80010C	NAT_TBL_ACCESS_RDDATA.RDDATA3[31:0]	32
0xBB800110	NAT_TBL_ACCESS_RDDATA.RDDATA2[31:0]	32
0xBB800114	NAT_TBL_ACCESS_RDDATA.RDDATA1[31:0]	32
0xBB800118	NAT_TBL_ACCESS_RDDATA.RDDATA0[31:0]	32
0xBB80011C	NAT_TBL_ACCESS_WRDATA.WRDATA4[31:0]	32
0xBB800120	NAT_TBL_ACCESS_WRDATA.WRDATA3[31:0]	32
0xBB800124	NAT_TBL_ACCESS_WRDATA.WRDATA2[31:0]	32
0xBB800128	NAT_TBL_ACCESS_WRDATA.WRDATA1[31:0]	32
0xBB80012C	NAT_TBL_ACCESS_WRDATA.WRDATA0[31:0]	32
0xBB800200	HSBA_CTRL.RESERVED[31:5]	27
0xBB800200	HSBA_CTRL.TST_LOG_MD[4:2]	3
0xBB800200	HSBA_CTRL.HSB_ATV[1:1]	1
0xBB800200	HSBA_CTRL.ALE34_BZ[0:0]	1
0xBB800204	HSB_DESC [0].HSB_DATA[31:0]	32
0xBB800208	HSB_DESC [1].HSB_DATA[31:0]	32
0xBB80020C	HSB_DESC [2].HSB_DATA[31:0]	32
0xBB800210	HSB_DESC [3].HSB_DATA[31:0]	32
0xBB800214	HSB_DESC [4].HSB_DATA[31:0]	32
0xBB800218	HSB_DESC [5].HSB_DATA[31:0]	32
0xBB80021C	HSB_DESC [6].HSB_DATA[31:0]	32
0xBB800220	HSB_DESC [7].HSB_DATA[31:0]	32
0xBB800224	HSB_DESC [8].HSB_DATA[31:0]	32
0xBB800228	HSB_DESC [9].HSB_DATA[31:0]	32
0xBB80022C	HSA_DESC [0].HSA_DATA[31:0]	32
0xBB800230	HSA_DESC [1].HSA_DATA[31:0]	32
0xBB800234	HSA_DESC [2].HSA_DATA[31:0]	32
0xBB800238	HSA_DESC [3].HSA_DATA[31:0]	32
0xBB800300	L4_TRF0 [0].TRF[0:0]	1
0xBB800300	L4_TRF0 [1].TRF[1:1]	1
0xBB800300	L4_TRF0 [2].TRF[2:2]	1
0xBB800300	L4_TRF0 [3].TRF[3:3]	1
0xBB800300	L4_TRF0 [4].TRF[4:4]	1
0xBB800300	L4_TRF0 [5].TRF[5:5]	1
0xBB800300	L4_TRF0 [6].TRF[6:6]	1
0xBB800300	L4_TRF0 [7].TRF[7:7]	1
0xBB800300	L4_TRF0 [8].TRF[8:8]	1
0xBB800300	L4_TRF0 [9].TRF[9:9]	1
0xBB800300	L4_TRF0 [10].TRF[10:10]	1
0xBB800300	L4_TRF0 [11].TRF[11:11]	1

Address	Register	Len
0xBB800300	L4_TRF0 [12].TRF[12:12]	1
0xBB800300	L4_TRF0 [13].TRF[13:13]	1
0xBB800300	L4_TRF0 [14].TRF[14:14]	1
0xBB800300	L4_TRF0 [15].TRF[15:15]	1
0xBB800300	L4_TRF0 [16].TRF[16:16]	1
0xBB800300	L4_TRF0 [17].TRF[17:17]	1
0xBB800300	L4_TRF0 [18].TRF[18:18]	1
0xBB800300	L4_TRF0 [19].TRF[19:19]	1
0xBB800300	L4_TRF0 [20].TRF[20:20]	1
0xBB800300	L4_TRF0 [21].TRF[21:21]	1
0xBB800300	L4_TRF0 [22].TRF[22:22]	1
0xBB800300	L4_TRF0 [23].TRF[23:23]	1
0xBB800300	L4_TRF0 [24].TRF[24:24]	1
0xBB800300	L4_TRF0 [25].TRF[25:25]	1
0xBB800300	L4_TRF0 [26].TRF[26:26]	1
0xBB800300	L4_TRF0 [27].TRF[27:27]	1
0xBB800300	L4_TRF0 [28].TRF[28:28]	1
0xBB800300	L4_TRF0 [29].TRF[29:29]	1
0xBB800300	L4_TRF0 [30].TRF[30:30]	1
0xBB800300	L4_TRF0 [31].TRF[31:31]	1
0xBB800304	L4_TRF0 [32].TRF[0:0]	1
0xBB800304	L4_TRF0 [33].TRF[1:1]	1
0xBB800304	L4_TRF0 [34].TRF[2:2]	1
0xBB800304	L4_TRF0 [35].TRF[3:3]	1
0xBB800304	L4_TRF0 [36].TRF[4:4]	1
0xBB800304	L4_TRF0 [37].TRF[5:5]	1
0xBB800304	L4_TRF0 [38].TRF[6:6]	1
0xBB800304	L4_TRF0 [39].TRF[7:7]	1
0xBB800304	L4_TRF0 [40].TRF[8:8]	1
0xBB800304	L4_TRF0 [41].TRF[9:9]	1
0xBB800304	L4_TRF0 [42].TRF[10:10]	1
0xBB800304	L4_TRF0 [43].TRF[11:11]	1
0xBB800304	L4_TRF0 [44].TRF[12:12]	1
0xBB800304	L4_TRF0 [45].TRF[13:13]	1
0xBB800304	L4_TRF0 [46].TRF[14:14]	1
0xBB800304	L4_TRF0 [47].TRF[15:15]	1
0xBB800304	L4_TRF0 [48].TRF[16:16]	1
0xBB800304	L4_TRF0 [49].TRF[17:17]	1
0xBB800304	L4_TRF0 [50].TRF[18:18]	1
0xBB800304	L4_TRF0 [51].TRF[19:19]	1
0xBB800304	L4_TRF0 [52].TRF[20:20]	1
0xBB800304	L4_TRF0 [53].TRF[21:21]	1
0xBB800304	L4_TRF0 [54].TRF[22:22]	1
0xBB800304	L4_TRF0 [55].TRF[23:23]	1
0xBB800304	L4_TRF0 [56].TRF[24:24]	1
0xBB800304	L4_TRF0 [57].TRF[25:25]	1

Address	Register	Len
0xBB800304	L4_TRF0 [58].TRF[26:26]	1
0xBB800304	L4_TRF0 [59].TRF[27:27]	1
0xBB800304	L4_TRF0 [60].TRF[28:28]	1
0xBB800304	L4_TRF0 [61].TRF[29:29]	1
0xBB800304	L4_TRF0 [62].TRF[30:30]	1
0xBB800304	L4_TRF0 [63].TRF[31:31]	1
0xBB800308	L4_TRF0 [64].TRF[0:0]	1
0xBB800308	L4_TRF0 [65].TRF[1:1]	1
0xBB800308	L4_TRF0 [66].TRF[2:2]	1
0xBB800308	L4_TRF0 [67].TRF[3:3]	1
0xBB800308	L4_TRF0 [68].TRF[4:4]	1
0xBB800308	L4_TRF0 [69].TRF[5:5]	1
0xBB800308	L4_TRF0 [70].TRF[6:6]	1
0xBB800308	L4_TRF0 [71].TRF[7:7]	1
0xBB800308	L4_TRF0 [72].TRF[8:8]	1
0xBB800308	L4_TRF0 [73].TRF[9:9]	1
0xBB800308	L4_TRF0 [74].TRF[10:10]	1
0xBB800308	L4_TRF0 [75].TRF[11:11]	1
0xBB800308	L4_TRF0 [76].TRF[12:12]	1
0xBB800308	L4_TRF0 [77].TRF[13:13]	1
0xBB800308	L4_TRF0 [78].TRF[14:14]	1
0xBB800308	L4_TRF0 [79].TRF[15:15]	1
0xBB800308	L4_TRF0 [80].TRF[16:16]	1
0xBB800308	L4_TRF0 [81].TRF[17:17]	1
0xBB800308	L4_TRF0 [82].TRF[18:18]	1
0xBB800308	L4_TRF0 [83].TRF[19:19]	1
0xBB800308	L4_TRF0 [84].TRF[20:20]	1
0xBB800308	L4_TRF0 [85].TRF[21:21]	1
0xBB800308	L4_TRF0 [86].TRF[22:22]	1
0xBB800308	L4_TRF0 [87].TRF[23:23]	1
0xBB800308	L4_TRF0 [88].TRF[24:24]	1
0xBB800308	L4_TRF0 [89].TRF[25:25]	1
0xBB800308	L4_TRF0 [90].TRF[26:26]	1
0xBB800308	L4_TRF0 [91].TRF[27:27]	1
0xBB800308	L4_TRF0 [92].TRF[28:28]	1
0xBB800308	L4_TRF0 [93].TRF[29:29]	1
0xBB800308	L4_TRF0 [94].TRF[30:30]	1
0xBB800308	L4_TRF0 [95].TRF[31:31]	1
0xBB80030C	L4_TRF0 [96].TRF[0:0]	1
0xBB80030C	L4_TRF0 [97].TRF[1:1]	1
0xBB80030C	L4_TRF0 [98].TRF[2:2]	1
0xBB80030C	L4_TRF0 [99].TRF[3:3]	1
0xBB80030C	L4_TRF0 [100].TRF[4:4]	1
0xBB80030C	L4_TRF0 [101].TRF[5:5]	1
0xBB80030C	L4_TRF0 [102].TRF[6:6]	1
0xBB80030C	L4_TRF0 [103].TRF[7:7]	1

Address	Register	Len
0xBB80030C	L4_TRF0 [104].TRF[8:8]	1
0xBB80030C	L4_TRF0 [105].TRF[9:9]	1
0xBB80030C	L4_TRF0 [106].TRF[10:10]	1
0xBB80030C	L4_TRF0 [107].TRF[11:11]	1
0xBB80030C	L4_TRF0 [108].TRF[12:12]	1
0xBB80030C	L4_TRF0 [109].TRF[13:13]	1
0xBB80030C	L4_TRF0 [110].TRF[14:14]	1
0xBB80030C	L4_TRF0 [111].TRF[15:15]	1
0xBB80030C	L4_TRF0 [112].TRF[16:16]	1
0xBB80030C	L4_TRF0 [113].TRF[17:17]	1
0xBB80030C	L4_TRF0 [114].TRF[18:18]	1
0xBB80030C	L4_TRF0 [115].TRF[19:19]	1
0xBB80030C	L4_TRF0 [116].TRF[20:20]	1
0xBB80030C	L4_TRF0 [117].TRF[21:21]	1
0xBB80030C	L4_TRF0 [118].TRF[22:22]	1
0xBB80030C	L4_TRF0 [119].TRF[23:23]	1
0xBB80030C	L4_TRF0 [120].TRF[24:24]	1
0xBB80030C	L4_TRF0 [121].TRF[25:25]	1
0xBB80030C	L4_TRF0 [122].TRF[26:26]	1
0xBB80030C	L4_TRF0 [123].TRF[27:27]	1
0xBB80030C	L4_TRF0 [124].TRF[28:28]	1
0xBB80030C	L4_TRF0 [125].TRF[29:29]	1
0xBB80030C	L4_TRF0 [126].TRF[30:30]	1
0xBB80030C	L4_TRF0 [127].TRF[31:31]	1
0xBB800310	L4_TRF0 [128].TRF[0:0]	1
0xBB800310	L4_TRF0 [129].TRF[1:1]	1
0xBB800310	L4_TRF0 [130].TRF[2:2]	1
0xBB800310	L4_TRF0 [131].TRF[3:3]	1
0xBB800310	L4_TRF0 [132].TRF[4:4]	1
0xBB800310	L4_TRF0 [133].TRF[5:5]	1
0xBB800310	L4_TRF0 [134].TRF[6:6]	1
0xBB800310	L4_TRF0 [135].TRF[7:7]	1
0xBB800310	L4_TRF0 [136].TRF[8:8]	1
0xBB800310	L4_TRF0 [137].TRF[9:9]	1
0xBB800310	L4_TRF0 [138].TRF[10:10]	1
0xBB800310	L4_TRF0 [139].TRF[11:11]	1
0xBB800310	L4_TRF0 [140].TRF[12:12]	1
0xBB800310	L4_TRF0 [141].TRF[13:13]	1
0xBB800310	L4_TRF0 [142].TRF[14:14]	1
0xBB800310	L4_TRF0 [143].TRF[15:15]	1
0xBB800310	L4_TRF0 [144].TRF[16:16]	1
0xBB800310	L4_TRF0 [145].TRF[17:17]	1
0xBB800310	L4_TRF0 [146].TRF[18:18]	1
0xBB800310	L4_TRF0 [147].TRF[19:19]	1
0xBB800310	L4_TRF0 [148].TRF[20:20]	1
0xBB800310	L4_TRF0 [149].TRF[21:21]	1

Address	Register	Len
0xBB800310	L4_TRF0 [150].TRF[22:22]	1
0xBB800310	L4_TRF0 [151].TRF[23:23]	1
0xBB800310	L4_TRF0 [152].TRF[24:24]	1
0xBB800310	L4_TRF0 [153].TRF[25:25]	1
0xBB800310	L4_TRF0 [154].TRF[26:26]	1
0xBB800310	L4_TRF0 [155].TRF[27:27]	1
0xBB800310	L4_TRF0 [156].TRF[28:28]	1
0xBB800310	L4_TRF0 [157].TRF[29:29]	1
0xBB800310	L4_TRF0 [158].TRF[30:30]	1
0xBB800310	L4_TRF0 [159].TRF[31:31]	1
0xBB800314	L4_TRF0 [160].TRF[0:0]	1
0xBB800314	L4_TRF0 [161].TRF[1:1]	1
0xBB800314	L4_TRF0 [162].TRF[2:2]	1
0xBB800314	L4_TRF0 [163].TRF[3:3]	1
0xBB800314	L4_TRF0 [164].TRF[4:4]	1
0xBB800314	L4_TRF0 [165].TRF[5:5]	1
0xBB800314	L4_TRF0 [166].TRF[6:6]	1
0xBB800314	L4_TRF0 [167].TRF[7:7]	1
0xBB800314	L4_TRF0 [168].TRF[8:8]	1
0xBB800314	L4_TRF0 [169].TRF[9:9]	1
0xBB800314	L4_TRF0 [170].TRF[10:10]	1
0xBB800314	L4_TRF0 [171].TRF[11:11]	1
0xBB800314	L4_TRF0 [172].TRF[12:12]	1
0xBB800314	L4_TRF0 [173].TRF[13:13]	1
0xBB800314	L4_TRF0 [174].TRF[14:14]	1
0xBB800314	L4_TRF0 [175].TRF[15:15]	1
0xBB800314	L4_TRF0 [176].TRF[16:16]	1
0xBB800314	L4_TRF0 [177].TRF[17:17]	1
0xBB800314	L4_TRF0 [178].TRF[18:18]	1
0xBB800314	L4_TRF0 [179].TRF[19:19]	1
0xBB800314	L4_TRF0 [180].TRF[20:20]	1
0xBB800314	L4_TRF0 [181].TRF[21:21]	1
0xBB800314	L4_TRF0 [182].TRF[22:22]	1
0xBB800314	L4_TRF0 [183].TRF[23:23]	1
0xBB800314	L4_TRF0 [184].TRF[24:24]	1
0xBB800314	L4_TRF0 [185].TRF[25:25]	1
0xBB800314	L4_TRF0 [186].TRF[26:26]	1
0xBB800314	L4_TRF0 [187].TRF[27:27]	1
0xBB800314	L4_TRF0 [188].TRF[28:28]	1
0xBB800314	L4_TRF0 [189].TRF[29:29]	1
0xBB800314	L4_TRF0 [190].TRF[30:30]	1
0xBB800314	L4_TRF0 [191].TRF[31:31]	1
0xBB800318	L4_TRF0 [192].TRF[0:0]	1
0xBB800318	L4_TRF0 [193].TRF[1:1]	1
0xBB800318	L4_TRF0 [194].TRF[2:2]	1
0xBB800318	L4_TRF0 [195].TRF[3:3]	1

Address	Register	Len
0xBB800318	L4_TRF0 [196].TRF[4:4]	1
0xBB800318	L4_TRF0 [197].TRF[5:5]	1
0xBB800318	L4_TRF0 [198].TRF[6:6]	1
0xBB800318	L4_TRF0 [199].TRF[7:7]	1
0xBB800318	L4_TRF0 [200].TRF[8:8]	1
0xBB800318	L4_TRF0 [201].TRF[9:9]	1
0xBB800318	L4_TRF0 [202].TRF[10:10]	1
0xBB800318	L4_TRF0 [203].TRF[11:11]	1
0xBB800318	L4_TRF0 [204].TRF[12:12]	1
0xBB800318	L4_TRF0 [205].TRF[13:13]	1
0xBB800318	L4_TRF0 [206].TRF[14:14]	1
0xBB800318	L4_TRF0 [207].TRF[15:15]	1
0xBB800318	L4_TRF0 [208].TRF[16:16]	1
0xBB800318	L4_TRF0 [209].TRF[17:17]	1
0xBB800318	L4_TRF0 [210].TRF[18:18]	1
0xBB800318	L4_TRF0 [211].TRF[19:19]	1
0xBB800318	L4_TRF0 [212].TRF[20:20]	1
0xBB800318	L4_TRF0 [213].TRF[21:21]	1
0xBB800318	L4_TRF0 [214].TRF[22:22]	1
0xBB800318	L4_TRF0 [215].TRF[23:23]	1
0xBB800318	L4_TRF0 [216].TRF[24:24]	1
0xBB800318	L4_TRF0 [217].TRF[25:25]	1
0xBB800318	L4_TRF0 [218].TRF[26:26]	1
0xBB800318	L4_TRF0 [219].TRF[27:27]	1
0xBB800318	L4_TRF0 [220].TRF[28:28]	1
0xBB800318	L4_TRF0 [221].TRF[29:29]	1
0xBB800318	L4_TRF0 [222].TRF[30:30]	1
0xBB800318	L4_TRF0 [223].TRF[31:31]	1
0xBB80031C	L4_TRF0 [224].TRF[0:0]	1
0xBB80031C	L4_TRF0 [225].TRF[1:1]	1
0xBB80031C	L4_TRF0 [226].TRF[2:2]	1
0xBB80031C	L4_TRF0 [227].TRF[3:3]	1
0xBB80031C	L4_TRF0 [228].TRF[4:4]	1
0xBB80031C	L4_TRF0 [229].TRF[5:5]	1
0xBB80031C	L4_TRF0 [230].TRF[6:6]	1
0xBB80031C	L4_TRF0 [231].TRF[7:7]	1
0xBB80031C	L4_TRF0 [232].TRF[8:8]	1
0xBB80031C	L4_TRF0 [233].TRF[9:9]	1
0xBB80031C	L4_TRF0 [234].TRF[10:10]	1
0xBB80031C	L4_TRF0 [235].TRF[11:11]	1
0xBB80031C	L4_TRF0 [236].TRF[12:12]	1
0xBB80031C	L4_TRF0 [237].TRF[13:13]	1
0xBB80031C	L4_TRF0 [238].TRF[14:14]	1
0xBB80031C	L4_TRF0 [239].TRF[15:15]	1
0xBB80031C	L4_TRF0 [240].TRF[16:16]	1
0xBB80031C	L4_TRF0 [241].TRF[17:17]	1



Address	Register	Len
0xBB80031C	L4_TRF0 [242].TRF[18:18]	1
0xBB80031C	L4_TRF0 [243].TRF[19:19]	1
0xBB80031C	L4_TRF0 [244].TRF[20:20]	1
0xBB80031C	L4_TRF0 [245].TRF[21:21]	1
0xBB80031C	L4_TRF0 [246].TRF[22:22]	1
0xBB80031C	L4_TRF0 [247].TRF[23:23]	1
0xBB80031C	L4_TRF0 [248].TRF[24:24]	1
0xBB80031C	L4_TRF0 [249].TRF[25:25]	1
0xBB80031C	L4_TRF0 [250].TRF[26:26]	1
0xBB80031C	L4_TRF0 [251].TRF[27:27]	1
0xBB80031C	L4_TRF0 [252].TRF[28:28]	1
0xBB80031C	L4_TRF0 [253].TRF[29:29]	1
0xBB80031C	L4_TRF0 [254].TRF[30:30]	1
0xBB80031C	L4_TRF0 [255].TRF[31:31]	1
0xBB800320	L4_TRF0 [256].TRF[0:0]	1
0xBB800320	L4_TRF0 [257].TRF[1:1]	1
0xBB800320	L4_TRF0 [258].TRF[2:2]	1
0xBB800320	L4_TRF0 [259].TRF[3:3]	1
0xBB800320	L4_TRF0 [260].TRF[4:4]	1
0xBB800320	L4_TRF0 [261].TRF[5:5]	1
0xBB800320	L4_TRF0 [262].TRF[6:6]	1
0xBB800320	L4_TRF0 [263].TRF[7:7]	1
0xBB800320	L4_TRF0 [264].TRF[8:8]	1
0xBB800320	L4_TRF0 [265].TRF[9:9]	1
0xBB800320	L4_TRF0 [266].TRF[10:10]	1
0xBB800320	L4_TRF0 [267].TRF[11:11]	1
0xBB800320	L4_TRF0 [268].TRF[12:12]	1
0xBB800320	L4_TRF0 [269].TRF[13:13]	1
0xBB800320	L4_TRF0 [270].TRF[14:14]	1
0xBB800320	L4_TRF0 [271].TRF[15:15]	1
0xBB800320	L4_TRF0 [272].TRF[16:16]	1
0xBB800320	L4_TRF0 [273].TRF[17:17]	1
0xBB800320	L4_TRF0 [274].TRF[18:18]	1
0xBB800320	L4_TRF0 [275].TRF[19:19]	1
0xBB800320	L4_TRF0 [276].TRF[20:20]	1
0xBB800320	L4_TRF0 [277].TRF[21:21]	1
0xBB800320	L4_TRF0 [278].TRF[22:22]	1
0xBB800320	L4_TRF0 [279].TRF[23:23]	1
0xBB800320	L4_TRF0 [280].TRF[24:24]	1
0xBB800320	L4_TRF0 [281].TRF[25:25]	1
0xBB800320	L4_TRF0 [282].TRF[26:26]	1
0xBB800320	L4_TRF0 [283].TRF[27:27]	1
0xBB800320	L4_TRF0 [284].TRF[28:28]	1
0xBB800320	L4_TRF0 [285].TRF[29:29]	1
0xBB800320	L4_TRF0 [286].TRF[30:30]	1
0xBB800320	L4_TRF0 [287].TRF[31:31]	1

Address	Register	Len
0xBB800324	L4_TRF0 [288].TRF[0:0]	1
0xBB800324	L4_TRF0 [289].TRF[1:1]	1
0xBB800324	L4_TRF0 [290].TRF[2:2]	1
0xBB800324	L4_TRF0 [291].TRF[3:3]	1
0xBB800324	L4_TRF0 [292].TRF[4:4]	1
0xBB800324	L4_TRF0 [293].TRF[5:5]	1
0xBB800324	L4_TRF0 [294].TRF[6:6]	1
0xBB800324	L4_TRF0 [295].TRF[7:7]	1
0xBB800324	L4_TRF0 [296].TRF[8:8]	1
0xBB800324	L4_TRF0 [297].TRF[9:9]	1
0xBB800324	L4_TRF0 [298].TRF[10:10]	1
0xBB800324	L4_TRF0 [299].TRF[11:11]	1
0xBB800324	L4_TRF0 [300].TRF[12:12]	1
0xBB800324	L4_TRF0 [301].TRF[13:13]	1
0xBB800324	L4_TRF0 [302].TRF[14:14]	1
0xBB800324	L4_TRF0 [303].TRF[15:15]	1
0xBB800324	L4_TRF0 [304].TRF[16:16]	1
0xBB800324	L4_TRF0 [305].TRF[17:17]	1
0xBB800324	L4_TRF0 [306].TRF[18:18]	1
0xBB800324	L4_TRF0 [307].TRF[19:19]	1
0xBB800324	L4_TRF0 [308].TRF[20:20]	1
0xBB800324	L4_TRF0 [309].TRF[21:21]	1
0xBB800324	L4_TRF0 [310].TRF[22:22]	1
0xBB800324	L4_TRF0 [311].TRF[23:23]	1
0xBB800324	L4_TRF0 [312].TRF[24:24]	1
0xBB800324	L4_TRF0 [313].TRF[25:25]	1
0xBB800324	L4_TRF0 [314].TRF[26:26]	1
0xBB800324	L4_TRF0 [315].TRF[27:27]	1
0xBB800324	L4_TRF0 [316].TRF[28:28]	1
0xBB800324	L4_TRF0 [317].TRF[29:29]	1
0xBB800324	L4_TRF0 [318].TRF[30:30]	1
0xBB800324	L4_TRF0 [319].TRF[31:31]	1
0xBB800328	L4_TRF0 [320].TRF[0:0]	1
0xBB800328	L4_TRF0 [321].TRF[1:1]	1
0xBB800328	L4_TRF0 [322].TRF[2:2]	1
0xBB800328	L4_TRF0 [323].TRF[3:3]	1
0xBB800328	L4_TRF0 [324].TRF[4:4]	1
0xBB800328	L4_TRF0 [325].TRF[5:5]	1
0xBB800328	L4_TRF0 [326].TRF[6:6]	1
0xBB800328	L4_TRF0 [327].TRF[7:7]	1
0xBB800328	L4_TRF0 [328].TRF[8:8]	1
0xBB800328	L4_TRF0 [329].TRF[9:9]	1
0xBB800328	L4_TRF0 [330].TRF[10:10]	1
0xBB800328	L4_TRF0 [331].TRF[11:11]	1
0xBB800328	L4_TRF0 [332].TRF[12:12]	1
0xBB800328	L4_TRF0 [333].TRF[13:13]	1

Address	Register	Len
0xBB800328	L4_TRF0 [334].TRF[14:14]	1
0xBB800328	L4_TRF0 [335].TRF[15:15]	1
0xBB800328	L4_TRF0 [336].TRF[16:16]	1
0xBB800328	L4_TRF0 [337].TRF[17:17]	1
0xBB800328	L4_TRF0 [338].TRF[18:18]	1
0xBB800328	L4_TRF0 [339].TRF[19:19]	1
0xBB800328	L4_TRF0 [340].TRF[20:20]	1
0xBB800328	L4_TRF0 [341].TRF[21:21]	1
0xBB800328	L4_TRF0 [342].TRF[22:22]	1
0xBB800328	L4_TRF0 [343].TRF[23:23]	1
0xBB800328	L4_TRF0 [344].TRF[24:24]	1
0xBB800328	L4_TRF0 [345].TRF[25:25]	1
0xBB800328	L4_TRF0 [346].TRF[26:26]	1
0xBB800328	L4_TRF0 [347].TRF[27:27]	1
0xBB800328	L4_TRF0 [348].TRF[28:28]	1
0xBB800328	L4_TRF0 [349].TRF[29:29]	1
0xBB800328	L4_TRF0 [350].TRF[30:30]	1
0xBB800328	L4_TRF0 [351].TRF[31:31]	1
0xBB80032C	L4_TRF0 [352].TRF[0:0]	1
0xBB80032C	L4_TRF0 [353].TRF[1:1]	1
0xBB80032C	L4_TRF0 [354].TRF[2:2]	1
0xBB80032C	L4_TRF0 [355].TRF[3:3]	1
0xBB80032C	L4_TRF0 [356].TRF[4:4]	1
0xBB80032C	L4_TRF0 [357].TRF[5:5]	1
0xBB80032C	L4_TRF0 [358].TRF[6:6]	1
0xBB80032C	L4_TRF0 [359].TRF[7:7]	1
0xBB80032C	L4_TRF0 [360].TRF[8:8]	1
0xBB80032C	L4_TRF0 [361].TRF[9:9]	1
0xBB80032C	L4_TRF0 [362].TRF[10:10]	1
0xBB80032C	L4_TRF0 [363].TRF[11:11]	1
0xBB80032C	L4_TRF0 [364].TRF[12:12]	1
0xBB80032C	L4_TRF0 [365].TRF[13:13]	1
0xBB80032C	L4_TRF0 [366].TRF[14:14]	1
0xBB80032C	L4_TRF0 [367].TRF[15:15]	1
0xBB80032C	L4_TRF0 [368].TRF[16:16]	1
0xBB80032C	L4_TRF0 [369].TRF[17:17]	1
0xBB80032C	L4_TRF0 [370].TRF[18:18]	1
0xBB80032C	L4_TRF0 [371].TRF[19:19]	1
0xBB80032C	L4_TRF0 [372].TRF[20:20]	1
0xBB80032C	L4_TRF0 [373].TRF[21:21]	1
0xBB80032C	L4_TRF0 [374].TRF[22:22]	1
0xBB80032C	L4_TRF0 [375].TRF[23:23]	1
0xBB80032C	L4_TRF0 [376].TRF[24:24]	1
0xBB80032C	L4_TRF0 [377].TRF[25:25]	1
0xBB80032C	L4_TRF0 [378].TRF[26:26]	1
0xBB80032C	L4_TRF0 [379].TRF[27:27]	1

Address	Register	Len
0xBB80032C	L4_TRF0 [380].TRF[28:28]	1
0xBB80032C	L4_TRF0 [381].TRF[29:29]	1
0xBB80032C	L4_TRF0 [382].TRF[30:30]	1
0xBB80032C	L4_TRF0 [383].TRF[31:31]	1
0xBB800330	L4_TRF0 [384].TRF[0:0]	1
0xBB800330	L4_TRF0 [385].TRF[1:1]	1
0xBB800330	L4_TRF0 [386].TRF[2:2]	1
0xBB800330	L4_TRF0 [387].TRF[3:3]	1
0xBB800330	L4_TRF0 [388].TRF[4:4]	1
0xBB800330	L4_TRF0 [389].TRF[5:5]	1
0xBB800330	L4_TRF0 [390].TRF[6:6]	1
0xBB800330	L4_TRF0 [391].TRF[7:7]	1
0xBB800330	L4_TRF0 [392].TRF[8:8]	1
0xBB800330	L4_TRF0 [393].TRF[9:9]	1
0xBB800330	L4_TRF0 [394].TRF[10:10]	1
0xBB800330	L4_TRF0 [395].TRF[11:11]	1
0xBB800330	L4_TRF0 [396].TRF[12:12]	1
0xBB800330	L4_TRF0 [397].TRF[13:13]	1
0xBB800330	L4_TRF0 [398].TRF[14:14]	1
0xBB800330	L4_TRF0 [399].TRF[15:15]	1
0xBB800330	L4_TRF0 [400].TRF[16:16]	1
0xBB800330	L4_TRF0 [401].TRF[17:17]	1
0xBB800330	L4_TRF0 [402].TRF[18:18]	1
0xBB800330	L4_TRF0 [403].TRF[19:19]	1
0xBB800330	L4_TRF0 [404].TRF[20:20]	1
0xBB800330	L4_TRF0 [405].TRF[21:21]	1
0xBB800330	L4_TRF0 [406].TRF[22:22]	1
0xBB800330	L4_TRF0 [407].TRF[23:23]	1
0xBB800330	L4_TRF0 [408].TRF[24:24]	1
0xBB800330	L4_TRF0 [409].TRF[25:25]	1
0xBB800330	L4_TRF0 [410].TRF[26:26]	1
0xBB800330	L4_TRF0 [411].TRF[27:27]	1
0xBB800330	L4_TRF0 [412].TRF[28:28]	1
0xBB800330	L4_TRF0 [413].TRF[29:29]	1
0xBB800330	L4_TRF0 [414].TRF[30:30]	1
0xBB800330	L4_TRF0 [415].TRF[31:31]	1
0xBB800334	L4_TRF0 [416].TRF[0:0]	1
0xBB800334	L4_TRF0 [417].TRF[1:1]	1
0xBB800334	L4_TRF0 [418].TRF[2:2]	1
0xBB800334	L4_TRF0 [419].TRF[3:3]	1
0xBB800334	L4_TRF0 [420].TRF[4:4]	1
0xBB800334	L4_TRF0 [421].TRF[5:5]	1
0xBB800334	L4_TRF0 [422].TRF[6:6]	1
0xBB800334	L4_TRF0 [423].TRF[7:7]	1
0xBB800334	L4_TRF0 [424].TRF[8:8]	1
0xBB800334	L4_TRF0 [425].TRF[9:9]	1

Address	Register	Len
0xBB800334	L4_TRF0 [426].TRF[10:10]	1
0xBB800334	L4_TRF0 [427].TRF[11:11]	1
0xBB800334	L4_TRF0 [428].TRF[12:12]	1
0xBB800334	L4_TRF0 [429].TRF[13:13]	1
0xBB800334	L4_TRF0 [430].TRF[14:14]	1
0xBB800334	L4_TRF0 [431].TRF[15:15]	1
0xBB800334	L4_TRF0 [432].TRF[16:16]	1
0xBB800334	L4_TRF0 [433].TRF[17:17]	1
0xBB800334	L4_TRF0 [434].TRF[18:18]	1
0xBB800334	L4_TRF0 [435].TRF[19:19]	1
0xBB800334	L4_TRF0 [436].TRF[20:20]	1
0xBB800334	L4_TRF0 [437].TRF[21:21]	1
0xBB800334	L4_TRF0 [438].TRF[22:22]	1
0xBB800334	L4_TRF0 [439].TRF[23:23]	1
0xBB800334	L4_TRF0 [440].TRF[24:24]	1
0xBB800334	L4_TRF0 [441].TRF[25:25]	1
0xBB800334	L4_TRF0 [442].TRF[26:26]	1
0xBB800334	L4_TRF0 [443].TRF[27:27]	1
0xBB800334	L4_TRF0 [444].TRF[28:28]	1
0xBB800334	L4_TRF0 [445].TRF[29:29]	1
0xBB800334	L4_TRF0 [446].TRF[30:30]	1
0xBB800334	L4_TRF0 [447].TRF[31:31]	1
0xBB800338	L4_TRF0 [448].TRF[0:0]	1
0xBB800338	L4_TRF0 [449].TRF[1:1]	1
0xBB800338	L4_TRF0 [450].TRF[2:2]	1
0xBB800338	L4_TRF0 [451].TRF[3:3]	1
0xBB800338	L4_TRF0 [452].TRF[4:4]	1
0xBB800338	L4_TRF0 [453].TRF[5:5]	1
0xBB800338	L4_TRF0 [454].TRF[6:6]	1
0xBB800338	L4_TRF0 [455].TRF[7:7]	1
0xBB800338	L4_TRF0 [456].TRF[8:8]	1
0xBB800338	L4_TRF0 [457].TRF[9:9]	1
0xBB800338	L4_TRF0 [458].TRF[10:10]	1
0xBB800338	L4_TRF0 [459].TRF[11:11]	1
0xBB800338	L4_TRF0 [460].TRF[12:12]	1
0xBB800338	L4_TRF0 [461].TRF[13:13]	1
0xBB800338	L4_TRF0 [462].TRF[14:14]	1
0xBB800338	L4_TRF0 [463].TRF[15:15]	1
0xBB800338	L4_TRF0 [464].TRF[16:16]	1
0xBB800338	L4_TRF0 [465].TRF[17:17]	1
0xBB800338	L4_TRF0 [466].TRF[18:18]	1
0xBB800338	L4_TRF0 [467].TRF[19:19]	1
0xBB800338	L4_TRF0 [468].TRF[20:20]	1
0xBB800338	L4_TRF0 [469].TRF[21:21]	1
0xBB800338	L4_TRF0 [470].TRF[22:22]	1
0xBB800338	L4_TRF0 [471].TRF[23:23]	1

Address	Register	Len
0xBB800338	L4_TRF0 [472].TRF[24:24]	1
0xBB800338	L4_TRF0 [473].TRF[25:25]	1
0xBB800338	L4_TRF0 [474].TRF[26:26]	1
0xBB800338	L4_TRF0 [475].TRF[27:27]	1
0xBB800338	L4_TRF0 [476].TRF[28:28]	1
0xBB800338	L4_TRF0 [477].TRF[29:29]	1
0xBB800338	L4_TRF0 [478].TRF[30:30]	1
0xBB800338	L4_TRF0 [479].TRF[31:31]	1
0xBB80033C	L4_TRF0 [480].TRF[0:0]	1
0xBB80033C	L4_TRF0 [481].TRF[1:1]	1
0xBB80033C	L4_TRF0 [482].TRF[2:2]	1
0xBB80033C	L4_TRF0 [483].TRF[3:3]	1
0xBB80033C	L4_TRF0 [484].TRF[4:4]	1
0xBB80033C	L4_TRF0 [485].TRF[5:5]	1
0xBB80033C	L4_TRF0 [486].TRF[6:6]	1
0xBB80033C	L4_TRF0 [487].TRF[7:7]	1
0xBB80033C	L4_TRF0 [488].TRF[8:8]	1
0xBB80033C	L4_TRF0 [489].TRF[9:9]	1
0xBB80033C	L4_TRF0 [490].TRF[10:10]	1
0xBB80033C	L4_TRF0 [491].TRF[11:11]	1
0xBB80033C	L4_TRF0 [492].TRF[12:12]	1
0xBB80033C	L4_TRF0 [493].TRF[13:13]	1
0xBB80033C	L4_TRF0 [494].TRF[14:14]	1
0xBB80033C	L4_TRF0 [495].TRF[15:15]	1
0xBB80033C	L4_TRF0 [496].TRF[16:16]	1
0xBB80033C	L4_TRF0 [497].TRF[17:17]	1
0xBB80033C	L4_TRF0 [498].TRF[18:18]	1
0xBB80033C	L4_TRF0 [499].TRF[19:19]	1
0xBB80033C	L4_TRF0 [500].TRF[20:20]	1
0xBB80033C	L4_TRF0 [501].TRF[21:21]	1
0xBB80033C	L4_TRF0 [502].TRF[22:22]	1
0xBB80033C	L4_TRF0 [503].TRF[23:23]	1
0xBB80033C	L4_TRF0 [504].TRF[24:24]	1
0xBB80033C	L4_TRF0 [505].TRF[25:25]	1
0xBB80033C	L4_TRF0 [506].TRF[26:26]	1
0xBB80033C	L4_TRF0 [507].TRF[27:27]	1
0xBB80033C	L4_TRF0 [508].TRF[28:28]	1
0xBB80033C	L4_TRF0 [509].TRF[29:29]	1
0xBB80033C	L4_TRF0 [510].TRF[30:30]	1
0xBB80033C	L4_TRF0 [511].TRF[31:31]	1
0xBB800340	L4_TRF0 [512].TRF[0:0]	1
0xBB800340	L4_TRF0 [513].TRF[1:1]	1
0xBB800340	L4_TRF0 [514].TRF[2:2]	1
0xBB800340	L4_TRF0 [515].TRF[3:3]	1
0xBB800340	L4_TRF0 [516].TRF[4:4]	1
0xBB800340	L4_TRF0 [517].TRF[5:5]	1

Address	Register	Len
0xBB800340	L4_TRF0 [518].TRF[6:6]	1
0xBB800340	L4_TRF0 [519].TRF[7:7]	1
0xBB800340	L4_TRF0 [520].TRF[8:8]	1
0xBB800340	L4_TRF0 [521].TRF[9:9]	1
0xBB800340	L4_TRF0 [522].TRF[10:10]	1
0xBB800340	L4_TRF0 [523].TRF[11:11]	1
0xBB800340	L4_TRF0 [524].TRF[12:12]	1
0xBB800340	L4_TRF0 [525].TRF[13:13]	1
0xBB800340	L4_TRF0 [526].TRF[14:14]	1
0xBB800340	L4_TRF0 [527].TRF[15:15]	1
0xBB800340	L4_TRF0 [528].TRF[16:16]	1
0xBB800340	L4_TRF0 [529].TRF[17:17]	1
0xBB800340	L4_TRF0 [530].TRF[18:18]	1
0xBB800340	L4_TRF0 [531].TRF[19:19]	1
0xBB800340	L4_TRF0 [532].TRF[20:20]	1
0xBB800340	L4_TRF0 [533].TRF[21:21]	1
0xBB800340	L4_TRF0 [534].TRF[22:22]	1
0xBB800340	L4_TRF0 [535].TRF[23:23]	1
0xBB800340	L4_TRF0 [536].TRF[24:24]	1
0xBB800340	L4_TRF0 [537].TRF[25:25]	1
0xBB800340	L4_TRF0 [538].TRF[26:26]	1
0xBB800340	L4_TRF0 [539].TRF[27:27]	1
0xBB800340	L4_TRF0 [540].TRF[28:28]	1
0xBB800340	L4_TRF0 [541].TRF[29:29]	1
0xBB800340	L4_TRF0 [542].TRF[30:30]	1
0xBB800340	L4_TRF0 [543].TRF[31:31]	1
0xBB800344	L4_TRF0 [544].TRF[0:0]	1
0xBB800344	L4_TRF0 [545].TRF[1:1]	1
0xBB800344	L4_TRF0 [546].TRF[2:2]	1
0xBB800344	L4_TRF0 [547].TRF[3:3]	1
0xBB800344	L4_TRF0 [548].TRF[4:4]	1
0xBB800344	L4_TRF0 [549].TRF[5:5]	1
0xBB800344	L4_TRF0 [550].TRF[6:6]	1
0xBB800344	L4_TRF0 [551].TRF[7:7]	1
0xBB800344	L4_TRF0 [552].TRF[8:8]	1
0xBB800344	L4_TRF0 [553].TRF[9:9]	1
0xBB800344	L4_TRF0 [554].TRF[10:10]	1
0xBB800344	L4_TRF0 [555].TRF[11:11]	1
0xBB800344	L4_TRF0 [556].TRF[12:12]	1
0xBB800344	L4_TRF0 [557].TRF[13:13]	1
0xBB800344	L4_TRF0 [558].TRF[14:14]	1
0xBB800344	L4_TRF0 [559].TRF[15:15]	1
0xBB800344	L4_TRF0 [560].TRF[16:16]	1
0xBB800344	L4_TRF0 [561].TRF[17:17]	1
0xBB800344	L4_TRF0 [562].TRF[18:18]	1
0xBB800344	L4_TRF0 [563].TRF[19:19]	1

Address	Register	Len
0xBB800344	L4_TRF0 [564].TRF[20:20]	1
0xBB800344	L4_TRF0 [565].TRF[21:21]	1
0xBB800344	L4_TRF0 [566].TRF[22:22]	1
0xBB800344	L4_TRF0 [567].TRF[23:23]	1
0xBB800344	L4_TRF0 [568].TRF[24:24]	1
0xBB800344	L4_TRF0 [569].TRF[25:25]	1
0xBB800344	L4_TRF0 [570].TRF[26:26]	1
0xBB800344	L4_TRF0 [571].TRF[27:27]	1
0xBB800344	L4_TRF0 [572].TRF[28:28]	1
0xBB800344	L4_TRF0 [573].TRF[29:29]	1
0xBB800344	L4_TRF0 [574].TRF[30:30]	1
0xBB800344	L4_TRF0 [575].TRF[31:31]	1
0xBB800348	L4_TRF0 [576].TRF[0:0]	1
0xBB800348	L4_TRF0 [577].TRF[1:1]	1
0xBB800348	L4_TRF0 [578].TRF[2:2]	1
0xBB800348	L4_TRF0 [579].TRF[3:3]	1
0xBB800348	L4_TRF0 [580].TRF[4:4]	1
0xBB800348	L4_TRF0 [581].TRF[5:5]	1
0xBB800348	L4_TRF0 [582].TRF[6:6]	1
0xBB800348	L4_TRF0 [583].TRF[7:7]	1
0xBB800348	L4_TRF0 [584].TRF[8:8]	1
0xBB800348	L4_TRF0 [585].TRF[9:9]	1
0xBB800348	L4_TRF0 [586].TRF[10:10]	1
0xBB800348	L4_TRF0 [587].TRF[11:11]	1
0xBB800348	L4_TRF0 [588].TRF[12:12]	1
0xBB800348	L4_TRF0 [589].TRF[13:13]	1
0xBB800348	L4_TRF0 [590].TRF[14:14]	1
0xBB800348	L4_TRF0 [591].TRF[15:15]	1
0xBB800348	L4_TRF0 [592].TRF[16:16]	1
0xBB800348	L4_TRF0 [593].TRF[17:17]	1
0xBB800348	L4_TRF0 [594].TRF[18:18]	1
0xBB800348	L4_TRF0 [595].TRF[19:19]	1
0xBB800348	L4_TRF0 [596].TRF[20:20]	1
0xBB800348	L4_TRF0 [597].TRF[21:21]	1
0xBB800348	L4_TRF0 [598].TRF[22:22]	1
0xBB800348	L4_TRF0 [599].TRF[23:23]	1
0xBB800348	L4_TRF0 [600].TRF[24:24]	1
0xBB800348	L4_TRF0 [601].TRF[25:25]	1
0xBB800348	L4_TRF0 [602].TRF[26:26]	1
0xBB800348	L4_TRF0 [603].TRF[27:27]	1
0xBB800348	L4_TRF0 [604].TRF[28:28]	1
0xBB800348	L4_TRF0 [605].TRF[29:29]	1
0xBB800348	L4_TRF0 [606].TRF[30:30]	1
0xBB800348	L4_TRF0 [607].TRF[31:31]	1
0xBB80034C	L4_TRF0 [608].TRF[0:0]	1
0xBB80034C	L4_TRF0 [609].TRF[1:1]	1



Address	Register	Len
0xBB80034C	L4_TRF0 [610].TRF[2:2]	1
0xBB80034C	L4_TRF0 [611].TRF[3:3]	1
0xBB80034C	L4_TRF0 [612].TRF[4:4]	1
0xBB80034C	L4_TRF0 [613].TRF[5:5]	1
0xBB80034C	L4_TRF0 [614].TRF[6:6]	1
0xBB80034C	L4_TRF0 [615].TRF[7:7]	1
0xBB80034C	L4_TRF0 [616].TRF[8:8]	1
0xBB80034C	L4_TRF0 [617].TRF[9:9]	1
0xBB80034C	L4_TRF0 [618].TRF[10:10]	1
0xBB80034C	L4_TRF0 [619].TRF[11:11]	1
0xBB80034C	L4_TRF0 [620].TRF[12:12]	1
0xBB80034C	L4_TRF0 [621].TRF[13:13]	1
0xBB80034C	L4_TRF0 [622].TRF[14:14]	1
0xBB80034C	L4_TRF0 [623].TRF[15:15]	1
0xBB80034C	L4_TRF0 [624].TRF[16:16]	1
0xBB80034C	L4_TRF0 [625].TRF[17:17]	1
0xBB80034C	L4_TRF0 [626].TRF[18:18]	1
0xBB80034C	L4_TRF0 [627].TRF[19:19]	1
0xBB80034C	L4_TRF0 [628].TRF[20:20]	1
0xBB80034C	L4_TRF0 [629].TRF[21:21]	1
0xBB80034C	L4_TRF0 [630].TRF[22:22]	1
0xBB80034C	L4_TRF0 [631].TRF[23:23]	1
0xBB80034C	L4_TRF0 [632].TRF[24:24]	1
0xBB80034C	L4_TRF0 [633].TRF[25:25]	1
0xBB80034C	L4_TRF0 [634].TRF[26:26]	1
0xBB80034C	L4_TRF0 [635].TRF[27:27]	1
0xBB80034C	L4_TRF0 [636].TRF[28:28]	1
0xBB80034C	L4_TRF0 [637].TRF[29:29]	1
0xBB80034C	L4_TRF0 [638].TRF[30:30]	1
0xBB80034C	L4_TRF0 [639].TRF[31:31]	1
0xBB800350	L4_TRF0 [640].TRF[0:0]	1
0xBB800350	L4_TRF0 [641].TRF[1:1]	1
0xBB800350	L4_TRF0 [642].TRF[2:2]	1
0xBB800350	L4_TRF0 [643].TRF[3:3]	1
0xBB800350	L4_TRF0 [644].TRF[4:4]	1
0xBB800350	L4_TRF0 [645].TRF[5:5]	1
0xBB800350	L4_TRF0 [646].TRF[6:6]	1
0xBB800350	L4_TRF0 [647].TRF[7:7]	1
0xBB800350	L4_TRF0 [648].TRF[8:8]	1
0xBB800350	L4_TRF0 [649].TRF[9:9]	1
0xBB800350	L4_TRF0 [650].TRF[10:10]	1
0xBB800350	L4_TRF0 [651].TRF[11:11]	1
0xBB800350	L4_TRF0 [652].TRF[12:12]	1
0xBB800350	L4_TRF0 [653].TRF[13:13]	1
0xBB800350	L4_TRF0 [654].TRF[14:14]	1
0xBB800350	L4_TRF0 [655].TRF[15:15]	1

Address	Register	Len
0xBB800350	L4_TRF0 [656].TRF[16:16]	1
0xBB800350	L4_TRF0 [657].TRF[17:17]	1
0xBB800350	L4_TRF0 [658].TRF[18:18]	1
0xBB800350	L4_TRF0 [659].TRF[19:19]	1
0xBB800350	L4_TRF0 [660].TRF[20:20]	1
0xBB800350	L4_TRF0 [661].TRF[21:21]	1
0xBB800350	L4_TRF0 [662].TRF[22:22]	1
0xBB800350	L4_TRF0 [663].TRF[23:23]	1
0xBB800350	L4_TRF0 [664].TRF[24:24]	1
0xBB800350	L4_TRF0 [665].TRF[25:25]	1
0xBB800350	L4_TRF0 [666].TRF[26:26]	1
0xBB800350	L4_TRF0 [667].TRF[27:27]	1
0xBB800350	L4_TRF0 [668].TRF[28:28]	1
0xBB800350	L4_TRF0 [669].TRF[29:29]	1
0xBB800350	L4_TRF0 [670].TRF[30:30]	1
0xBB800350	L4_TRF0 [671].TRF[31:31]	1
0xBB800354	L4_TRF0 [672].TRF[0:0]	1
0xBB800354	L4_TRF0 [673].TRF[1:1]	1
0xBB800354	L4_TRF0 [674].TRF[2:2]	1
0xBB800354	L4_TRF0 [675].TRF[3:3]	1
0xBB800354	L4_TRF0 [676].TRF[4:4]	1
0xBB800354	L4_TRF0 [677].TRF[5:5]	1
0xBB800354	L4_TRF0 [678].TRF[6:6]	1
0xBB800354	L4_TRF0 [679].TRF[7:7]	1
0xBB800354	L4_TRF0 [680].TRF[8:8]	1
0xBB800354	L4_TRF0 [681].TRF[9:9]	1
0xBB800354	L4_TRF0 [682].TRF[10:10]	1
0xBB800354	L4_TRF0 [683].TRF[11:11]	1
0xBB800354	L4_TRF0 [684].TRF[12:12]	1
0xBB800354	L4_TRF0 [685].TRF[13:13]	1
0xBB800354	L4_TRF0 [686].TRF[14:14]	1
0xBB800354	L4_TRF0 [687].TRF[15:15]	1
0xBB800354	L4_TRF0 [688].TRF[16:16]	1
0xBB800354	L4_TRF0 [689].TRF[17:17]	1
0xBB800354	L4_TRF0 [690].TRF[18:18]	1
0xBB800354	L4_TRF0 [691].TRF[19:19]	1
0xBB800354	L4_TRF0 [692].TRF[20:20]	1
0xBB800354	L4_TRF0 [693].TRF[21:21]	1
0xBB800354	L4_TRF0 [694].TRF[22:22]	1
0xBB800354	L4_TRF0 [695].TRF[23:23]	1
0xBB800354	L4_TRF0 [696].TRF[24:24]	1
0xBB800354	L4_TRF0 [697].TRF[25:25]	1
0xBB800354	L4_TRF0 [698].TRF[26:26]	1
0xBB800354	L4_TRF0 [699].TRF[27:27]	1
0xBB800354	L4_TRF0 [700].TRF[28:28]	1
0xBB800354	L4_TRF0 [701].TRF[29:29]	1

Address	Register	Len
0xBB800354	L4_TRF0 [702].TRF[30:30]	1
0xBB800354	L4_TRF0 [703].TRF[31:31]	1
0xBB800358	L4_TRF0 [704].TRF[0:0]	1
0xBB800358	L4_TRF0 [705].TRF[1:1]	1
0xBB800358	L4_TRF0 [706].TRF[2:2]	1
0xBB800358	L4_TRF0 [707].TRF[3:3]	1
0xBB800358	L4_TRF0 [708].TRF[4:4]	1
0xBB800358	L4_TRF0 [709].TRF[5:5]	1
0xBB800358	L4_TRF0 [710].TRF[6:6]	1
0xBB800358	L4_TRF0 [711].TRF[7:7]	1
0xBB800358	L4_TRF0 [712].TRF[8:8]	1
0xBB800358	L4_TRF0 [713].TRF[9:9]	1
0xBB800358	L4_TRF0 [714].TRF[10:10]	1
0xBB800358	L4_TRF0 [715].TRF[11:11]	1
0xBB800358	L4_TRF0 [716].TRF[12:12]	1
0xBB800358	L4_TRF0 [717].TRF[13:13]	1
0xBB800358	L4_TRF0 [718].TRF[14:14]	1
0xBB800358	L4_TRF0 [719].TRF[15:15]	1
0xBB800358	L4_TRF0 [720].TRF[16:16]	1
0xBB800358	L4_TRF0 [721].TRF[17:17]	1
0xBB800358	L4_TRF0 [722].TRF[18:18]	1
0xBB800358	L4_TRF0 [723].TRF[19:19]	1
0xBB800358	L4_TRF0 [724].TRF[20:20]	1
0xBB800358	L4_TRF0 [725].TRF[21:21]	1
0xBB800358	L4_TRF0 [726].TRF[22:22]	1
0xBB800358	L4_TRF0 [727].TRF[23:23]	1
0xBB800358	L4_TRF0 [728].TRF[24:24]	1
0xBB800358	L4_TRF0 [729].TRF[25:25]	1
0xBB800358	L4_TRF0 [730].TRF[26:26]	1
0xBB800358	L4_TRF0 [731].TRF[27:27]	1
0xBB800358	L4_TRF0 [732].TRF[28:28]	1
0xBB800358	L4_TRF0 [733].TRF[29:29]	1
0xBB800358	L4_TRF0 [734].TRF[30:30]	1
0xBB800358	L4_TRF0 [735].TRF[31:31]	1
0xBB80035C	L4_TRF0 [736].TRF[0:0]	1
0xBB80035C	L4_TRF0 [737].TRF[1:1]	1
0xBB80035C	L4_TRF0 [738].TRF[2:2]	1
0xBB80035C	L4_TRF0 [739].TRF[3:3]	1
0xBB80035C	L4_TRF0 [740].TRF[4:4]	1
0xBB80035C	L4_TRF0 [741].TRF[5:5]	1
0xBB80035C	L4_TRF0 [742].TRF[6:6]	1
0xBB80035C	L4_TRF0 [743].TRF[7:7]	1
0xBB80035C	L4_TRF0 [744].TRF[8:8]	1
0xBB80035C	L4_TRF0 [745].TRF[9:9]	1
0xBB80035C	L4_TRF0 [746].TRF[10:10]	1
0xBB80035C	L4_TRF0 [747].TRF[11:11]	1

Address	Register	Len
0xBB80035C	L4_TRF0 [748].TRF[12:12]	1
0xBB80035C	L4_TRF0 [749].TRF[13:13]	1
0xBB80035C	L4_TRF0 [750].TRF[14:14]	1
0xBB80035C	L4_TRF0 [751].TRF[15:15]	1
0xBB80035C	L4_TRF0 [752].TRF[16:16]	1
0xBB80035C	L4_TRF0 [753].TRF[17:17]	1
0xBB80035C	L4_TRF0 [754].TRF[18:18]	1
0xBB80035C	L4_TRF0 [755].TRF[19:19]	1
0xBB80035C	L4_TRF0 [756].TRF[20:20]	1
0xBB80035C	L4_TRF0 [757].TRF[21:21]	1
0xBB80035C	L4_TRF0 [758].TRF[22:22]	1
0xBB80035C	L4_TRF0 [759].TRF[23:23]	1
0xBB80035C	L4_TRF0 [760].TRF[24:24]	1
0xBB80035C	L4_TRF0 [761].TRF[25:25]	1
0xBB80035C	L4_TRF0 [762].TRF[26:26]	1
0xBB80035C	L4_TRF0 [763].TRF[27:27]	1
0xBB80035C	L4_TRF0 [764].TRF[28:28]	1
0xBB80035C	L4_TRF0 [765].TRF[29:29]	1
0xBB80035C	L4_TRF0 [766].TRF[30:30]	1
0xBB80035C	L4_TRF0 [767].TRF[31:31]	1
0xBB800360	L4_TRF0 [768].TRF[0:0]	1
0xBB800360	L4_TRF0 [769].TRF[1:1]	1
0xBB800360	L4_TRF0 [770].TRF[2:2]	1
0xBB800360	L4_TRF0 [771].TRF[3:3]	1
0xBB800360	L4_TRF0 [772].TRF[4:4]	1
0xBB800360	L4_TRF0 [773].TRF[5:5]	1
0xBB800360	L4_TRF0 [774].TRF[6:6]	1
0xBB800360	L4_TRF0 [775].TRF[7:7]	1
0xBB800360	L4_TRF0 [776].TRF[8:8]	1
0xBB800360	L4_TRF0 [777].TRF[9:9]	1
0xBB800360	L4_TRF0 [778].TRF[10:10]	1
0xBB800360	L4_TRF0 [779].TRF[11:11]	1
0xBB800360	L4_TRF0 [780].TRF[12:12]	1
0xBB800360	L4_TRF0 [781].TRF[13:13]	1
0xBB800360	L4_TRF0 [782].TRF[14:14]	1
0xBB800360	L4_TRF0 [783].TRF[15:15]	1
0xBB800360	L4_TRF0 [784].TRF[16:16]	1
0xBB800360	L4_TRF0 [785].TRF[17:17]	1
0xBB800360	L4_TRF0 [786].TRF[18:18]	1
0xBB800360	L4_TRF0 [787].TRF[19:19]	1
0xBB800360	L4_TRF0 [788].TRF[20:20]	1
0xBB800360	L4_TRF0 [789].TRF[21:21]	1
0xBB800360	L4_TRF0 [790].TRF[22:22]	1
0xBB800360	L4_TRF0 [791].TRF[23:23]	1
0xBB800360	L4_TRF0 [792].TRF[24:24]	1
0xBB800360	L4_TRF0 [793].TRF[25:25]	1

Address	Register	Len
0xBB800360	L4_TRF0 [794].TRF[26:26]	1
0xBB800360	L4_TRF0 [795].TRF[27:27]	1
0xBB800360	L4_TRF0 [796].TRF[28:28]	1
0xBB800360	L4_TRF0 [797].TRF[29:29]	1
0xBB800360	L4_TRF0 [798].TRF[30:30]	1
0xBB800360	L4_TRF0 [799].TRF[31:31]	1
0xBB800364	L4_TRF0 [800].TRF[0:0]	1
0xBB800364	L4_TRF0 [801].TRF[1:1]	1
0xBB800364	L4_TRF0 [802].TRF[2:2]	1
0xBB800364	L4_TRF0 [803].TRF[3:3]	1
0xBB800364	L4_TRF0 [804].TRF[4:4]	1
0xBB800364	L4_TRF0 [805].TRF[5:5]	1
0xBB800364	L4_TRF0 [806].TRF[6:6]	1
0xBB800364	L4_TRF0 [807].TRF[7:7]	1
0xBB800364	L4_TRF0 [808].TRF[8:8]	1
0xBB800364	L4_TRF0 [809].TRF[9:9]	1
0xBB800364	L4_TRF0 [810].TRF[10:10]	1
0xBB800364	L4_TRF0 [811].TRF[11:11]	1
0xBB800364	L4_TRF0 [812].TRF[12:12]	1
0xBB800364	L4_TRF0 [813].TRF[13:13]	1
0xBB800364	L4_TRF0 [814].TRF[14:14]	1
0xBB800364	L4_TRF0 [815].TRF[15:15]	1
0xBB800364	L4_TRF0 [816].TRF[16:16]	1
0xBB800364	L4_TRF0 [817].TRF[17:17]	1
0xBB800364	L4_TRF0 [818].TRF[18:18]	1
0xBB800364	L4_TRF0 [819].TRF[19:19]	1
0xBB800364	L4_TRF0 [820].TRF[20:20]	1
0xBB800364	L4_TRF0 [821].TRF[21:21]	1
0xBB800364	L4_TRF0 [822].TRF[22:22]	1
0xBB800364	L4_TRF0 [823].TRF[23:23]	1
0xBB800364	L4_TRF0 [824].TRF[24:24]	1
0xBB800364	L4_TRF0 [825].TRF[25:25]	1
0xBB800364	L4_TRF0 [826].TRF[26:26]	1
0xBB800364	L4_TRF0 [827].TRF[27:27]	1
0xBB800364	L4_TRF0 [828].TRF[28:28]	1
0xBB800364	L4_TRF0 [829].TRF[29:29]	1
0xBB800364	L4_TRF0 [830].TRF[30:30]	1
0xBB800364	L4_TRF0 [831].TRF[31:31]	1
0xBB800368	L4_TRF0 [832].TRF[0:0]	1
0xBB800368	L4_TRF0 [833].TRF[1:1]	1
0xBB800368	L4_TRF0 [834].TRF[2:2]	1
0xBB800368	L4_TRF0 [835].TRF[3:3]	1
0xBB800368	L4_TRF0 [836].TRF[4:4]	1
0xBB800368	L4_TRF0 [837].TRF[5:5]	1
0xBB800368	L4_TRF0 [838].TRF[6:6]	1
0xBB800368	L4_TRF0 [839].TRF[7:7]	1

Address	Register	Len
0xBB800368	L4_TRF0 [840].TRF[8:8]	1
0xBB800368	L4_TRF0 [841].TRF[9:9]	1
0xBB800368	L4_TRF0 [842].TRF[10:10]	1
0xBB800368	L4_TRF0 [843].TRF[11:11]	1
0xBB800368	L4_TRF0 [844].TRF[12:12]	1
0xBB800368	L4_TRF0 [845].TRF[13:13]	1
0xBB800368	L4_TRF0 [846].TRF[14:14]	1
0xBB800368	L4_TRF0 [847].TRF[15:15]	1
0xBB800368	L4_TRF0 [848].TRF[16:16]	1
0xBB800368	L4_TRF0 [849].TRF[17:17]	1
0xBB800368	L4_TRF0 [850].TRF[18:18]	1
0xBB800368	L4_TRF0 [851].TRF[19:19]	1
0xBB800368	L4_TRF0 [852].TRF[20:20]	1
0xBB800368	L4_TRF0 [853].TRF[21:21]	1
0xBB800368	L4_TRF0 [854].TRF[22:22]	1
0xBB800368	L4_TRF0 [855].TRF[23:23]	1
0xBB800368	L4_TRF0 [856].TRF[24:24]	1
0xBB800368	L4_TRF0 [857].TRF[25:25]	1
0xBB800368	L4_TRF0 [858].TRF[26:26]	1
0xBB800368	L4_TRF0 [859].TRF[27:27]	1
0xBB800368	L4_TRF0 [860].TRF[28:28]	1
0xBB800368	L4_TRF0 [861].TRF[29:29]	1
0xBB800368	L4_TRF0 [862].TRF[30:30]	1
0xBB800368	L4_TRF0 [863].TRF[31:31]	1
0xBB80036C	L4_TRF0 [864].TRF[0:0]	1
0xBB80036C	L4_TRF0 [865].TRF[1:1]	1
0xBB80036C	L4_TRF0 [866].TRF[2:2]	1
0xBB80036C	L4_TRF0 [867].TRF[3:3]	1
0xBB80036C	L4_TRF0 [868].TRF[4:4]	1
0xBB80036C	L4_TRF0 [869].TRF[5:5]	1
0xBB80036C	L4_TRF0 [870].TRF[6:6]	1
0xBB80036C	L4_TRF0 [871].TRF[7:7]	1
0xBB80036C	L4_TRF0 [872].TRF[8:8]	1
0xBB80036C	L4_TRF0 [873].TRF[9:9]	1
0xBB80036C	L4_TRF0 [874].TRF[10:10]	1
0xBB80036C	L4_TRF0 [875].TRF[11:11]	1
0xBB80036C	L4_TRF0 [876].TRF[12:12]	1
0xBB80036C	L4_TRF0 [877].TRF[13:13]	1
0xBB80036C	L4_TRF0 [878].TRF[14:14]	1
0xBB80036C	L4_TRF0 [879].TRF[15:15]	1
0xBB80036C	L4_TRF0 [880].TRF[16:16]	1
0xBB80036C	L4_TRF0 [881].TRF[17:17]	1
0xBB80036C	L4_TRF0 [882].TRF[18:18]	1
0xBB80036C	L4_TRF0 [883].TRF[19:19]	1
0xBB80036C	L4_TRF0 [884].TRF[20:20]	1
0xBB80036C	L4_TRF0 [885].TRF[21:21]	1

Address	Register	Len
0xBB80036C	L4_TRF0 [886].TRF[22:22]	1
0xBB80036C	L4_TRF0 [887].TRF[23:23]	1
0xBB80036C	L4_TRF0 [888].TRF[24:24]	1
0xBB80036C	L4_TRF0 [889].TRF[25:25]	1
0xBB80036C	L4_TRF0 [890].TRF[26:26]	1
0xBB80036C	L4_TRF0 [891].TRF[27:27]	1
0xBB80036C	L4_TRF0 [892].TRF[28:28]	1
0xBB80036C	L4_TRF0 [893].TRF[29:29]	1
0xBB80036C	L4_TRF0 [894].TRF[30:30]	1
0xBB80036C	L4_TRF0 [895].TRF[31:31]	1
0xBB800370	L4_TRF0 [896].TRF[0:0]	1
0xBB800370	L4_TRF0 [897].TRF[1:1]	1
0xBB800370	L4_TRF0 [898].TRF[2:2]	1
0xBB800370	L4_TRF0 [899].TRF[3:3]	1
0xBB800370	L4_TRF0 [900].TRF[4:4]	1
0xBB800370	L4_TRF0 [901].TRF[5:5]	1
0xBB800370	L4_TRF0 [902].TRF[6:6]	1
0xBB800370	L4_TRF0 [903].TRF[7:7]	1
0xBB800370	L4_TRF0 [904].TRF[8:8]	1
0xBB800370	L4_TRF0 [905].TRF[9:9]	1
0xBB800370	L4_TRF0 [906].TRF[10:10]	1
0xBB800370	L4_TRF0 [907].TRF[11:11]	1
0xBB800370	L4_TRF0 [908].TRF[12:12]	1
0xBB800370	L4_TRF0 [909].TRF[13:13]	1
0xBB800370	L4_TRF0 [910].TRF[14:14]	1
0xBB800370	L4_TRF0 [911].TRF[15:15]	1
0xBB800370	L4_TRF0 [912].TRF[16:16]	1
0xBB800370	L4_TRF0 [913].TRF[17:17]	1
0xBB800370	L4_TRF0 [914].TRF[18:18]	1
0xBB800370	L4_TRF0 [915].TRF[19:19]	1
0xBB800370	L4_TRF0 [916].TRF[20:20]	1
0xBB800370	L4_TRF0 [917].TRF[21:21]	1
0xBB800370	L4_TRF0 [918].TRF[22:22]	1
0xBB800370	L4_TRF0 [919].TRF[23:23]	1
0xBB800370	L4_TRF0 [920].TRF[24:24]	1
0xBB800370	L4_TRF0 [921].TRF[25:25]	1
0xBB800370	L4_TRF0 [922].TRF[26:26]	1
0xBB800370	L4_TRF0 [923].TRF[27:27]	1
0xBB800370	L4_TRF0 [924].TRF[28:28]	1
0xBB800370	L4_TRF0 [925].TRF[29:29]	1
0xBB800370	L4_TRF0 [926].TRF[30:30]	1
0xBB800370	L4_TRF0 [927].TRF[31:31]	1
0xBB800374	L4_TRF0 [928].TRF[0:0]	1
0xBB800374	L4_TRF0 [929].TRF[1:1]	1
0xBB800374	L4_TRF0 [930].TRF[2:2]	1
0xBB800374	L4_TRF0 [931].TRF[3:3]	1

Address	Register	Len
0xBB800374	L4_TRF0 [932].TRF[4:4]	1
0xBB800374	L4_TRF0 [933].TRF[5:5]	1
0xBB800374	L4_TRF0 [934].TRF[6:6]	1
0xBB800374	L4_TRF0 [935].TRF[7:7]	1
0xBB800374	L4_TRF0 [936].TRF[8:8]	1
0xBB800374	L4_TRF0 [937].TRF[9:9]	1
0xBB800374	L4_TRF0 [938].TRF[10:10]	1
0xBB800374	L4_TRF0 [939].TRF[11:11]	1
0xBB800374	L4_TRF0 [940].TRF[12:12]	1
0xBB800374	L4_TRF0 [941].TRF[13:13]	1
0xBB800374	L4_TRF0 [942].TRF[14:14]	1
0xBB800374	L4_TRF0 [943].TRF[15:15]	1
0xBB800374	L4_TRF0 [944].TRF[16:16]	1
0xBB800374	L4_TRF0 [945].TRF[17:17]	1
0xBB800374	L4_TRF0 [946].TRF[18:18]	1
0xBB800374	L4_TRF0 [947].TRF[19:19]	1
0xBB800374	L4_TRF0 [948].TRF[20:20]	1
0xBB800374	L4_TRF0 [949].TRF[21:21]	1
0xBB800374	L4_TRF0 [950].TRF[22:22]	1
0xBB800374	L4_TRF0 [951].TRF[23:23]	1
0xBB800374	L4_TRF0 [952].TRF[24:24]	1
0xBB800374	L4_TRF0 [953].TRF[25:25]	1
0xBB800374	L4_TRF0 [954].TRF[26:26]	1
0xBB800374	L4_TRF0 [955].TRF[27:27]	1
0xBB800374	L4_TRF0 [956].TRF[28:28]	1
0xBB800374	L4_TRF0 [957].TRF[29:29]	1
0xBB800374	L4_TRF0 [958].TRF[30:30]	1
0xBB800374	L4_TRF0 [959].TRF[31:31]	1
0xBB800378	L4_TRF0 [960].TRF[0:0]	1
0xBB800378	L4_TRF0 [961].TRF[1:1]	1
0xBB800378	L4_TRF0 [962].TRF[2:2]	1
0xBB800378	L4_TRF0 [963].TRF[3:3]	1
0xBB800378	L4_TRF0 [964].TRF[4:4]	1
0xBB800378	L4_TRF0 [965].TRF[5:5]	1
0xBB800378	L4_TRF0 [966].TRF[6:6]	1
0xBB800378	L4_TRF0 [967].TRF[7:7]	1
0xBB800378	L4_TRF0 [968].TRF[8:8]	1
0xBB800378	L4_TRF0 [969].TRF[9:9]	1
0xBB800378	L4_TRF0 [970].TRF[10:10]	1
0xBB800378	L4_TRF0 [971].TRF[11:11]	1
0xBB800378	L4_TRF0 [972].TRF[12:12]	1
0xBB800378	L4_TRF0 [973].TRF[13:13]	1
0xBB800378	L4_TRF0 [974].TRF[14:14]	1
0xBB800378	L4_TRF0 [975].TRF[15:15]	1
0xBB800378	L4_TRF0 [976].TRF[16:16]	1
0xBB800378	L4_TRF0 [977].TRF[17:17]	1



Address	Register	Len
0xBB800378	L4_TRF0 [978].TRF[18:18]	1
0xBB800378	L4_TRF0 [979].TRF[19:19]	1
0xBB800378	L4_TRF0 [980].TRF[20:20]	1
0xBB800378	L4_TRF0 [981].TRF[21:21]	1
0xBB800378	L4_TRF0 [982].TRF[22:22]	1
0xBB800378	L4_TRF0 [983].TRF[23:23]	1
0xBB800378	L4_TRF0 [984].TRF[24:24]	1
0xBB800378	L4_TRF0 [985].TRF[25:25]	1
0xBB800378	L4_TRF0 [986].TRF[26:26]	1
0xBB800378	L4_TRF0 [987].TRF[27:27]	1
0xBB800378	L4_TRF0 [988].TRF[28:28]	1
0xBB800378	L4_TRF0 [989].TRF[29:29]	1
0xBB800378	L4_TRF0 [990].TRF[30:30]	1
0xBB800378	L4_TRF0 [991].TRF[31:31]	1
0xBB80037C	L4_TRF0 [992].TRF[0:0]	1
0xBB80037C	L4_TRF0 [993].TRF[1:1]	1
0xBB80037C	L4_TRF0 [994].TRF[2:2]	1
0xBB80037C	L4_TRF0 [995].TRF[3:3]	1
0xBB80037C	L4_TRF0 [996].TRF[4:4]	1
0xBB80037C	L4_TRF0 [997].TRF[5:5]	1
0xBB80037C	L4_TRF0 [998].TRF[6:6]	1
0xBB80037C	L4_TRF0 [999].TRF[7:7]	1
0xBB80037C	L4_TRF0 [1000].TRF[8:8]	1
0xBB80037C	L4_TRF0 [1001].TRF[9:9]	1
0xBB80037C	L4_TRF0 [1002].TRF[10:10]	1
0xBB80037C	L4_TRF0 [1003].TRF[11:11]	1
0xBB80037C	L4_TRF0 [1004].TRF[12:12]	1
0xBB80037C	L4_TRF0 [1005].TRF[13:13]	1
0xBB80037C	L4_TRF0 [1006].TRF[14:14]	1
0xBB80037C	L4_TRF0 [1007].TRF[15:15]	1
0xBB80037C	L4_TRF0 [1008].TRF[16:16]	1
0xBB80037C	L4_TRF0 [1009].TRF[17:17]	1
0xBB80037C	L4_TRF0 [1010].TRF[18:18]	1
0xBB80037C	L4_TRF0 [1011].TRF[19:19]	1
0xBB80037C	L4_TRF0 [1012].TRF[20:20]	1
0xBB80037C	L4_TRF0 [1013].TRF[21:21]	1
0xBB80037C	L4_TRF0 [1014].TRF[22:22]	1
0xBB80037C	L4_TRF0 [1015].TRF[23:23]	1
0xBB80037C	L4_TRF0 [1016].TRF[24:24]	1
0xBB80037C	L4_TRF0 [1017].TRF[25:25]	1
0xBB80037C	L4_TRF0 [1018].TRF[26:26]	1
0xBB80037C	L4_TRF0 [1019].TRF[27:27]	1
0xBB80037C	L4_TRF0 [1020].TRF[28:28]	1
0xBB80037C	L4_TRF0 [1021].TRF[29:29]	1
0xBB80037C	L4_TRF0 [1022].TRF[30:30]	1
0xBB80037C	L4_TRF0 [1023].TRF[31:31]	1

Address	Register	Len
0xBB800380	L4_TRF0 [1024].TRF[0:0]	1
0xBB800380	L4_TRF0 [1025].TRF[1:1]	1
0xBB800380	L4_TRF0 [1026].TRF[2:2]	1
0xBB800380	L4_TRF0 [1027].TRF[3:3]	1
0xBB800380	L4_TRF0 [1028].TRF[4:4]	1
0xBB800380	L4_TRF0 [1029].TRF[5:5]	1
0xBB800380	L4_TRF0 [1030].TRF[6:6]	1
0xBB800380	L4_TRF0 [1031].TRF[7:7]	1
0xBB800380	L4_TRF0 [1032].TRF[8:8]	1
0xBB800380	L4_TRF0 [1033].TRF[9:9]	1
0xBB800380	L4_TRF0 [1034].TRF[10:10]	1
0xBB800380	L4_TRF0 [1035].TRF[11:11]	1
0xBB800380	L4_TRF0 [1036].TRF[12:12]	1
0xBB800380	L4_TRF0 [1037].TRF[13:13]	1
0xBB800380	L4_TRF0 [1038].TRF[14:14]	1
0xBB800380	L4_TRF0 [1039].TRF[15:15]	1
0xBB800380	L4_TRF0 [1040].TRF[16:16]	1
0xBB800380	L4_TRF0 [1041].TRF[17:17]	1
0xBB800380	L4_TRF0 [1042].TRF[18:18]	1
0xBB800380	L4_TRF0 [1043].TRF[19:19]	1
0xBB800380	L4_TRF0 [1044].TRF[20:20]	1
0xBB800380	L4_TRF0 [1045].TRF[21:21]	1
0xBB800380	L4_TRF0 [1046].TRF[22:22]	1
0xBB800380	L4_TRF0 [1047].TRF[23:23]	1
0xBB800380	L4_TRF0 [1048].TRF[24:24]	1
0xBB800380	L4_TRF0 [1049].TRF[25:25]	1
0xBB800380	L4_TRF0 [1050].TRF[26:26]	1
0xBB800380	L4_TRF0 [1051].TRF[27:27]	1
0xBB800380	L4_TRF0 [1052].TRF[28:28]	1
0xBB800380	L4_TRF0 [1053].TRF[29:29]	1
0xBB800380	L4_TRF0 [1054].TRF[30:30]	1
0xBB800380	L4_TRF0 [1055].TRF[31:31]	1
0xBB800384	L4_TRF0 [1056].TRF[0:0]	1
0xBB800384	L4_TRF0 [1057].TRF[1:1]	1
0xBB800384	L4_TRF0 [1058].TRF[2:2]	1
0xBB800384	L4_TRF0 [1059].TRF[3:3]	1
0xBB800384	L4_TRF0 [1060].TRF[4:4]	1
0xBB800384	L4_TRF0 [1061].TRF[5:5]	1
0xBB800384	L4_TRF0 [1062].TRF[6:6]	1
0xBB800384	L4_TRF0 [1063].TRF[7:7]	1
0xBB800384	L4_TRF0 [1064].TRF[8:8]	1
0xBB800384	L4_TRF0 [1065].TRF[9:9]	1
0xBB800384	L4_TRF0 [1066].TRF[10:10]	1
0xBB800384	L4_TRF0 [1067].TRF[11:11]	1
0xBB800384	L4_TRF0 [1068].TRF[12:12]	1
0xBB800384	L4_TRF0 [1069].TRF[13:13]	1

Address	Register	Len
0xBB800384	L4_TRF0 [1070].TRF[14:14]	1
0xBB800384	L4_TRF0 [1071].TRF[15:15]	1
0xBB800384	L4_TRF0 [1072].TRF[16:16]	1
0xBB800384	L4_TRF0 [1073].TRF[17:17]	1
0xBB800384	L4_TRF0 [1074].TRF[18:18]	1
0xBB800384	L4_TRF0 [1075].TRF[19:19]	1
0xBB800384	L4_TRF0 [1076].TRF[20:20]	1
0xBB800384	L4_TRF0 [1077].TRF[21:21]	1
0xBB800384	L4_TRF0 [1078].TRF[22:22]	1
0xBB800384	L4_TRF0 [1079].TRF[23:23]	1
0xBB800384	L4_TRF0 [1080].TRF[24:24]	1
0xBB800384	L4_TRF0 [1081].TRF[25:25]	1
0xBB800384	L4_TRF0 [1082].TRF[26:26]	1
0xBB800384	L4_TRF0 [1083].TRF[27:27]	1
0xBB800384	L4_TRF0 [1084].TRF[28:28]	1
0xBB800384	L4_TRF0 [1085].TRF[29:29]	1
0xBB800384	L4_TRF0 [1086].TRF[30:30]	1
0xBB800384	L4_TRF0 [1087].TRF[31:31]	1
0xBB800388	L4_TRF0 [1088].TRF[0:0]	1
0xBB800388	L4_TRF0 [1089].TRF[1:1]	1
0xBB800388	L4_TRF0 [1090].TRF[2:2]	1
0xBB800388	L4_TRF0 [1091].TRF[3:3]	1
0xBB800388	L4_TRF0 [1092].TRF[4:4]	1
0xBB800388	L4_TRF0 [1093].TRF[5:5]	1
0xBB800388	L4_TRF0 [1094].TRF[6:6]	1
0xBB800388	L4_TRF0 [1095].TRF[7:7]	1
0xBB800388	L4_TRF0 [1096].TRF[8:8]	1
0xBB800388	L4_TRF0 [1097].TRF[9:9]	1
0xBB800388	L4_TRF0 [1098].TRF[10:10]	1
0xBB800388	L4_TRF0 [1099].TRF[11:11]	1
0xBB800388	L4_TRF0 [1100].TRF[12:12]	1
0xBB800388	L4_TRF0 [1101].TRF[13:13]	1
0xBB800388	L4_TRF0 [1102].TRF[14:14]	1
0xBB800388	L4_TRF0 [1103].TRF[15:15]	1
0xBB800388	L4_TRF0 [1104].TRF[16:16]	1
0xBB800388	L4_TRF0 [1105].TRF[17:17]	1
0xBB800388	L4_TRF0 [1106].TRF[18:18]	1
0xBB800388	L4_TRF0 [1107].TRF[19:19]	1
0xBB800388	L4_TRF0 [1108].TRF[20:20]	1
0xBB800388	L4_TRF0 [1109].TRF[21:21]	1
0xBB800388	L4_TRF0 [1110].TRF[22:22]	1
0xBB800388	L4_TRF0 [1111].TRF[23:23]	1
0xBB800388	L4_TRF0 [1112].TRF[24:24]	1
0xBB800388	L4_TRF0 [1113].TRF[25:25]	1
0xBB800388	L4_TRF0 [1114].TRF[26:26]	1
0xBB800388	L4_TRF0 [1115].TRF[27:27]	1

Address	Register	Len
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0xBB800388	L4_TRF0 [1117].TRF[29:29]	1
0xBB800388	L4_TRF0 [1118].TRF[30:30]	1
0xBB800388	L4_TRF0 [1119].TRF[31:31]	1
0xBB80038C	L4_TRF0 [1120].TRF[0:0]	1
0xBB80038C	L4_TRF0 [1121].TRF[1:1]	1
0xBB80038C	L4_TRF0 [1122].TRF[2:2]	1
0xBB80038C	L4_TRF0 [1123].TRF[3:3]	1
0xBB80038C	L4_TRF0 [1124].TRF[4:4]	1
0xBB80038C	L4_TRF0 [1125].TRF[5:5]	1
0xBB80038C	L4_TRF0 [1126].TRF[6:6]	1
0xBB80038C	L4_TRF0 [1127].TRF[7:7]	1
0xBB80038C	L4_TRF0 [1128].TRF[8:8]	1
0xBB80038C	L4_TRF0 [1129].TRF[9:9]	1
0xBB80038C	L4_TRF0 [1130].TRF[10:10]	1
0xBB80038C	L4_TRF0 [1131].TRF[11:11]	1
0xBB80038C	L4_TRF0 [1132].TRF[12:12]	1
0xBB80038C	L4_TRF0 [1133].TRF[13:13]	1
0xBB80038C	L4_TRF0 [1134].TRF[14:14]	1
0xBB80038C	L4_TRF0 [1135].TRF[15:15]	1
0xBB80038C	L4_TRF0 [1136].TRF[16:16]	1
0xBB80038C	L4_TRF0 [1137].TRF[17:17]	1
0xBB80038C	L4_TRF0 [1138].TRF[18:18]	1
0xBB80038C	L4_TRF0 [1139].TRF[19:19]	1
0xBB80038C	L4_TRF0 [1140].TRF[20:20]	1
0xBB80038C	L4_TRF0 [1141].TRF[21:21]	1
0xBB80038C	L4_TRF0 [1142].TRF[22:22]	1
0xBB80038C	L4_TRF0 [1143].TRF[23:23]	1
0xBB80038C	L4_TRF0 [1144].TRF[24:24]	1
0xBB80038C	L4_TRF0 [1145].TRF[25:25]	1
0xBB80038C	L4_TRF0 [1146].TRF[26:26]	1
0xBB80038C	L4_TRF0 [1147].TRF[27:27]	1
0xBB80038C	L4_TRF0 [1148].TRF[28:28]	1
0xBB80038C	L4_TRF0 [1149].TRF[29:29]	1
0xBB80038C	L4_TRF0 [1150].TRF[30:30]	1
0xBB80038C	L4_TRF0 [1151].TRF[31:31]	1
0xBB800390	L4_TRF0 [1152].TRF[0:0]	1
0xBB800390	L4_TRF0 [1153].TRF[1:1]	1
0xBB800390	L4_TRF0 [1154].TRF[2:2]	1
0xBB800390	L4_TRF0 [1155].TRF[3:3]	1
0xBB800390	L4_TRF0 [1156].TRF[4:4]	1
0xBB800390	L4_TRF0 [1157].TRF[5:5]	1
0xBB800390	L4_TRF0 [1158].TRF[6:6]	1
0xBB800390	L4_TRF0 [1159].TRF[7:7]	1
0xBB800390	L4_TRF0 [1160].TRF[8:8]	1
0xBB800390	L4_TRF0 [1161].TRF[9:9]	1

Address	Register	Len
0xBB800390	L4_TRF0 [1162].TRF[10:10]	1
0xBB800390	L4_TRF0 [1163].TRF[11:11]	1
0xBB800390	L4_TRF0 [1164].TRF[12:12]	1
0xBB800390	L4_TRF0 [1165].TRF[13:13]	1
0xBB800390	L4_TRF0 [1166].TRF[14:14]	1
0xBB800390	L4_TRF0 [1167].TRF[15:15]	1
0xBB800390	L4_TRF0 [1168].TRF[16:16]	1
0xBB800390	L4_TRF0 [1169].TRF[17:17]	1
0xBB800390	L4_TRF0 [1170].TRF[18:18]	1
0xBB800390	L4_TRF0 [1171].TRF[19:19]	1
0xBB800390	L4_TRF0 [1172].TRF[20:20]	1
0xBB800390	L4_TRF0 [1173].TRF[21:21]	1
0xBB800390	L4_TRF0 [1174].TRF[22:22]	1
0xBB800390	L4_TRF0 [1175].TRF[23:23]	1
0xBB800390	L4_TRF0 [1176].TRF[24:24]	1
0xBB800390	L4_TRF0 [1177].TRF[25:25]	1
0xBB800390	L4_TRF0 [1178].TRF[26:26]	1
0xBB800390	L4_TRF0 [1179].TRF[27:27]	1
0xBB800390	L4_TRF0 [1180].TRF[28:28]	1
0xBB800390	L4_TRF0 [1181].TRF[29:29]	1
0xBB800390	L4_TRF0 [1182].TRF[30:30]	1
0xBB800390	L4_TRF0 [1183].TRF[31:31]	1
0xBB800394	L4_TRF0 [1184].TRF[0:0]	1
0xBB800394	L4_TRF0 [1185].TRF[1:1]	1
0xBB800394	L4_TRF0 [1186].TRF[2:2]	1
0xBB800394	L4_TRF0 [1187].TRF[3:3]	1
0xBB800394	L4_TRF0 [1188].TRF[4:4]	1
0xBB800394	L4_TRF0 [1189].TRF[5:5]	1
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0xBB800394	L4_TRF0 [1191].TRF[7:7]	1
0xBB800394	L4_TRF0 [1192].TRF[8:8]	1
0xBB800394	L4_TRF0 [1193].TRF[9:9]	1
0xBB800394	L4_TRF0 [1194].TRF[10:10]	1
0xBB800394	L4_TRF0 [1195].TRF[11:11]	1
0xBB800394	L4_TRF0 [1196].TRF[12:12]	1
0xBB800394	L4_TRF0 [1197].TRF[13:13]	1
0xBB800394	L4_TRF0 [1198].TRF[14:14]	1
0xBB800394	L4_TRF0 [1199].TRF[15:15]	1
0xBB800394	L4_TRF0 [1200].TRF[16:16]	1
0xBB800394	L4_TRF0 [1201].TRF[17:17]	1
0xBB800394	L4_TRF0 [1202].TRF[18:18]	1
0xBB800394	L4_TRF0 [1203].TRF[19:19]	1
0xBB800394	L4_TRF0 [1204].TRF[20:20]	1
0xBB800394	L4_TRF0 [1205].TRF[21:21]	1
0xBB800394	L4_TRF0 [1206].TRF[22:22]	1
0xBB800394	L4_TRF0 [1207].TRF[23:23]	1

Address	Register	Len
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0xBB800394	L4_TRF0 [1209].TRF[25:25]	1
0xBB800394	L4_TRF0 [1210].TRF[26:26]	1
0xBB800394	L4_TRF0 [1211].TRF[27:27]	1
0xBB800394	L4_TRF0 [1212].TRF[28:28]	1
0xBB800394	L4_TRF0 [1213].TRF[29:29]	1
0xBB800394	L4_TRF0 [1214].TRF[30:30]	1
0xBB800394	L4_TRF0 [1215].TRF[31:31]	1
0xBB800398	L4_TRF0 [1216].TRF[0:0]	1
0xBB800398	L4_TRF0 [1217].TRF[1:1]	1
0xBB800398	L4_TRF0 [1218].TRF[2:2]	1
0xBB800398	L4_TRF0 [1219].TRF[3:3]	1
0xBB800398	L4_TRF0 [1220].TRF[4:4]	1
0xBB800398	L4_TRF0 [1221].TRF[5:5]	1
0xBB800398	L4_TRF0 [1222].TRF[6:6]	1
0xBB800398	L4_TRF0 [1223].TRF[7:7]	1
0xBB800398	L4_TRF0 [1224].TRF[8:8]	1
0xBB800398	L4_TRF0 [1225].TRF[9:9]	1
0xBB800398	L4_TRF0 [1226].TRF[10:10]	1
0xBB800398	L4_TRF0 [1227].TRF[11:11]	1
0xBB800398	L4_TRF0 [1228].TRF[12:12]	1
0xBB800398	L4_TRF0 [1229].TRF[13:13]	1
0xBB800398	L4_TRF0 [1230].TRF[14:14]	1
0xBB800398	L4_TRF0 [1231].TRF[15:15]	1
0xBB800398	L4_TRF0 [1232].TRF[16:16]	1
0xBB800398	L4_TRF0 [1233].TRF[17:17]	1
0xBB800398	L4_TRF0 [1234].TRF[18:18]	1
0xBB800398	L4_TRF0 [1235].TRF[19:19]	1
0xBB800398	L4_TRF0 [1236].TRF[20:20]	1
0xBB800398	L4_TRF0 [1237].TRF[21:21]	1
0xBB800398	L4_TRF0 [1238].TRF[22:22]	1
0xBB800398	L4_TRF0 [1239].TRF[23:23]	1
0xBB800398	L4_TRF0 [1240].TRF[24:24]	1
0xBB800398	L4_TRF0 [1241].TRF[25:25]	1
0xBB800398	L4_TRF0 [1242].TRF[26:26]	1
0xBB800398	L4_TRF0 [1243].TRF[27:27]	1
0xBB800398	L4_TRF0 [1244].TRF[28:28]	1
0xBB800398	L4_TRF0 [1245].TRF[29:29]	1
0xBB800398	L4_TRF0 [1246].TRF[30:30]	1
0xBB800398	L4_TRF0 [1247].TRF[31:31]	1
0xBB80039C	L4_TRF0 [1248].TRF[0:0]	1
0xBB80039C	L4_TRF0 [1249].TRF[1:1]	1
0xBB80039C	L4_TRF0 [1250].TRF[2:2]	1
0xBB80039C	L4_TRF0 [1251].TRF[3:3]	1
0xBB80039C	L4_TRF0 [1252].TRF[4:4]	1
0xBB80039C	L4_TRF0 [1253].TRF[5:5]	1

Address	Register	Len
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0xBB80039C	L4_TRF0 [1255].TRF[7:7]	1
0xBB80039C	L4_TRF0 [1256].TRF[8:8]	1
0xBB80039C	L4_TRF0 [1257].TRF[9:9]	1
0xBB80039C	L4_TRF0 [1258].TRF[10:10]	1
0xBB80039C	L4_TRF0 [1259].TRF[11:11]	1
0xBB80039C	L4_TRF0 [1260].TRF[12:12]	1
0xBB80039C	L4_TRF0 [1261].TRF[13:13]	1
0xBB80039C	L4_TRF0 [1262].TRF[14:14]	1
0xBB80039C	L4_TRF0 [1263].TRF[15:15]	1
0xBB80039C	L4_TRF0 [1264].TRF[16:16]	1
0xBB80039C	L4_TRF0 [1265].TRF[17:17]	1
0xBB80039C	L4_TRF0 [1266].TRF[18:18]	1
0xBB80039C	L4_TRF0 [1267].TRF[19:19]	1
0xBB80039C	L4_TRF0 [1268].TRF[20:20]	1
0xBB80039C	L4_TRF0 [1269].TRF[21:21]	1
0xBB80039C	L4_TRF0 [1270].TRF[22:22]	1
0xBB80039C	L4_TRF0 [1271].TRF[23:23]	1
0xBB80039C	L4_TRF0 [1272].TRF[24:24]	1
0xBB80039C	L4_TRF0 [1273].TRF[25:25]	1
0xBB80039C	L4_TRF0 [1274].TRF[26:26]	1
0xBB80039C	L4_TRF0 [1275].TRF[27:27]	1
0xBB80039C	L4_TRF0 [1276].TRF[28:28]	1
0xBB80039C	L4_TRF0 [1277].TRF[29:29]	1
0xBB80039C	L4_TRF0 [1278].TRF[30:30]	1
0xBB80039C	L4_TRF0 [1279].TRF[31:31]	1
0xBB8003A0	L4_TRF0 [1280].TRF[0:0]	1
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0xBB8003A0	L4_TRF0 [1283].TRF[3:3]	1
0xBB8003A0	L4_TRF0 [1284].TRF[4:4]	1
0xBB8003A0	L4_TRF0 [1285].TRF[5:5]	1
0xBB8003A0	L4_TRF0 [1286].TRF[6:6]	1
0xBB8003A0	L4_TRF0 [1287].TRF[7:7]	1
0xBB8003A0	L4_TRF0 [1288].TRF[8:8]	1
0xBB8003A0	L4_TRF0 [1289].TRF[9:9]	1
0xBB8003A0	L4_TRF0 [1290].TRF[10:10]	1
0xBB8003A0	L4_TRF0 [1291].TRF[11:11]	1
0xBB8003A0	L4_TRF0 [1292].TRF[12:12]	1
0xBB8003A0	L4_TRF0 [1293].TRF[13:13]	1
0xBB8003A0	L4_TRF0 [1294].TRF[14:14]	1
0xBB8003A0	L4_TRF0 [1295].TRF[15:15]	1
0xBB8003A0	L4_TRF0 [1296].TRF[16:16]	1
0xBB8003A0	L4_TRF0 [1297].TRF[17:17]	1
0xBB8003A0	L4_TRF0 [1298].TRF[18:18]	1
0xBB8003A0	L4_TRF0 [1299].TRF[19:19]	1

Address	Register	Len
0xBB8003A0	L4_TRF0 [1300].TRF[20:20]	1
0xBB8003A0	L4_TRF0 [1301].TRF[21:21]	1
0xBB8003A0	L4_TRF0 [1302].TRF[22:22]	1
0xBB8003A0	L4_TRF0 [1303].TRF[23:23]	1
0xBB8003A0	L4_TRF0 [1304].TRF[24:24]	1
0xBB8003A0	L4_TRF0 [1305].TRF[25:25]	1
0xBB8003A0	L4_TRF0 [1306].TRF[26:26]	1
0xBB8003A0	L4_TRF0 [1307].TRF[27:27]	1
0xBB8003A0	L4_TRF0 [1308].TRF[28:28]	1
0xBB8003A0	L4_TRF0 [1309].TRF[29:29]	1
0xBB8003A0	L4_TRF0 [1310].TRF[30:30]	1
0xBB8003A0	L4_TRF0 [1311].TRF[31:31]	1
0xBB8003A4	L4_TRF0 [1312].TRF[0:0]	1
0xBB8003A4	L4_TRF0 [1313].TRF[1:1]	1
0xBB8003A4	L4_TRF0 [1314].TRF[2:2]	1
0xBB8003A4	L4_TRF0 [1315].TRF[3:3]	1
0xBB8003A4	L4_TRF0 [1316].TRF[4:4]	1
0xBB8003A4	L4_TRF0 [1317].TRF[5:5]	1
0xBB8003A4	L4_TRF0 [1318].TRF[6:6]	1
0xBB8003A4	L4_TRF0 [1319].TRF[7:7]	1
0xBB8003A4	L4_TRF0 [1320].TRF[8:8]	1
0xBB8003A4	L4_TRF0 [1321].TRF[9:9]	1
0xBB8003A4	L4_TRF0 [1322].TRF[10:10]	1
0xBB8003A4	L4_TRF0 [1323].TRF[11:11]	1
0xBB8003A4	L4_TRF0 [1324].TRF[12:12]	1
0xBB8003A4	L4_TRF0 [1325].TRF[13:13]	1
0xBB8003A4	L4_TRF0 [1326].TRF[14:14]	1
0xBB8003A4	L4_TRF0 [1327].TRF[15:15]	1
0xBB8003A4	L4_TRF0 [1328].TRF[16:16]	1
0xBB8003A4	L4_TRF0 [1329].TRF[17:17]	1
0xBB8003A4	L4_TRF0 [1330].TRF[18:18]	1
0xBB8003A4	L4_TRF0 [1331].TRF[19:19]	1
0xBB8003A4	L4_TRF0 [1332].TRF[20:20]	1
0xBB8003A4	L4_TRF0 [1333].TRF[21:21]	1
0xBB8003A4	L4_TRF0 [1334].TRF[22:22]	1
0xBB8003A4	L4_TRF0 [1335].TRF[23:23]	1
0xBB8003A4	L4_TRF0 [1336].TRF[24:24]	1
0xBB8003A4	L4_TRF0 [1337].TRF[25:25]	1
0xBB8003A4	L4_TRF0 [1338].TRF[26:26]	1
0xBB8003A4	L4_TRF0 [1339].TRF[27:27]	1
0xBB8003A4	L4_TRF0 [1340].TRF[28:28]	1
0xBB8003A4	L4_TRF0 [1341].TRF[29:29]	1
0xBB8003A4	L4_TRF0 [1342].TRF[30:30]	1
0xBB8003A4	L4_TRF0 [1343].TRF[31:31]	1
0xBB8003A8	L4_TRF0 [1344].TRF[0:0]	1
0xBB8003A8	L4_TRF0 [1345].TRF[1:1]	1



Address	Register	Len
0xBB8003A8	L4_TRF0 [1346].TRF[2:2]	1
0xBB8003A8	L4_TRF0 [1347].TRF[3:3]	1
0xBB8003A8	L4_TRF0 [1348].TRF[4:4]	1
0xBB8003A8	L4_TRF0 [1349].TRF[5:5]	1
0xBB8003A8	L4_TRF0 [1350].TRF[6:6]	1
0xBB8003A8	L4_TRF0 [1351].TRF[7:7]	1
0xBB8003A8	L4_TRF0 [1352].TRF[8:8]	1
0xBB8003A8	L4_TRF0 [1353].TRF[9:9]	1
0xBB8003A8	L4_TRF0 [1354].TRF[10:10]	1
0xBB8003A8	L4_TRF0 [1355].TRF[11:11]	1
0xBB8003A8	L4_TRF0 [1356].TRF[12:12]	1
0xBB8003A8	L4_TRF0 [1357].TRF[13:13]	1
0xBB8003A8	L4_TRF0 [1358].TRF[14:14]	1
0xBB8003A8	L4_TRF0 [1359].TRF[15:15]	1
0xBB8003A8	L4_TRF0 [1360].TRF[16:16]	1
0xBB8003A8	L4_TRF0 [1361].TRF[17:17]	1
0xBB8003A8	L4_TRF0 [1362].TRF[18:18]	1
0xBB8003A8	L4_TRF0 [1363].TRF[19:19]	1
0xBB8003A8	L4_TRF0 [1364].TRF[20:20]	1
0xBB8003A8	L4_TRF0 [1365].TRF[21:21]	1
0xBB8003A8	L4_TRF0 [1366].TRF[22:22]	1
0xBB8003A8	L4_TRF0 [1367].TRF[23:23]	1
0xBB8003A8	L4_TRF0 [1368].TRF[24:24]	1
0xBB8003A8	L4_TRF0 [1369].TRF[25:25]	1
0xBB8003A8	L4_TRF0 [1370].TRF[26:26]	1
0xBB8003A8	L4_TRF0 [1371].TRF[27:27]	1
0xBB8003A8	L4_TRF0 [1372].TRF[28:28]	1
0xBB8003A8	L4_TRF0 [1373].TRF[29:29]	1
0xBB8003A8	L4_TRF0 [1374].TRF[30:30]	1
0xBB8003A8	L4_TRF0 [1375].TRF[31:31]	1
0xBB8003AC	L4_TRF0 [1376].TRF[0:0]	1
0xBB8003AC	L4_TRF0 [1377].TRF[1:1]	1
0xBB8003AC	L4_TRF0 [1378].TRF[2:2]	1
0xBB8003AC	L4_TRF0 [1379].TRF[3:3]	1
0xBB8003AC	L4_TRF0 [1380].TRF[4:4]	1
0xBB8003AC	L4_TRF0 [1381].TRF[5:5]	1
0xBB8003AC	L4_TRF0 [1382].TRF[6:6]	1
0xBB8003AC	L4_TRF0 [1383].TRF[7:7]	1
0xBB8003AC	L4_TRF0 [1384].TRF[8:8]	1
0xBB8003AC	L4_TRF0 [1385].TRF[9:9]	1
0xBB8003AC	L4_TRF0 [1386].TRF[10:10]	1
0xBB8003AC	L4_TRF0 [1387].TRF[11:11]	1
0xBB8003AC	L4_TRF0 [1388].TRF[12:12]	1
0xBB8003AC	L4_TRF0 [1389].TRF[13:13]	1
0xBB8003AC	L4_TRF0 [1390].TRF[14:14]	1
0xBB8003AC	L4_TRF0 [1391].TRF[15:15]	1

Address	Register	Len
0xBB8003AC	L4_TRF0 [1392].TRF[16:16]	1
0xBB8003AC	L4_TRF0 [1393].TRF[17:17]	1
0xBB8003AC	L4_TRF0 [1394].TRF[18:18]	1
0xBB8003AC	L4_TRF0 [1395].TRF[19:19]	1
0xBB8003AC	L4_TRF0 [1396].TRF[20:20]	1
0xBB8003AC	L4_TRF0 [1397].TRF[21:21]	1
0xBB8003AC	L4_TRF0 [1398].TRF[22:22]	1
0xBB8003AC	L4_TRF0 [1399].TRF[23:23]	1
0xBB8003AC	L4_TRF0 [1400].TRF[24:24]	1
0xBB8003AC	L4_TRF0 [1401].TRF[25:25]	1
0xBB8003AC	L4_TRF0 [1402].TRF[26:26]	1
0xBB8003AC	L4_TRF0 [1403].TRF[27:27]	1
0xBB8003AC	L4_TRF0 [1404].TRF[28:28]	1
0xBB8003AC	L4_TRF0 [1405].TRF[29:29]	1
0xBB8003AC	L4_TRF0 [1406].TRF[30:30]	1
0xBB8003AC	L4_TRF0 [1407].TRF[31:31]	1
0xBB8003B0	L4_TRF0 [1408].TRF[0:0]	1
0xBB8003B0	L4_TRF0 [1409].TRF[1:1]	1
0xBB8003B0	L4_TRF0 [1410].TRF[2:2]	1
0xBB8003B0	L4_TRF0 [1411].TRF[3:3]	1
0xBB8003B0	L4_TRF0 [1412].TRF[4:4]	1
0xBB8003B0	L4_TRF0 [1413].TRF[5:5]	1
0xBB8003B0	L4_TRF0 [1414].TRF[6:6]	1
0xBB8003B0	L4_TRF0 [1415].TRF[7:7]	1
0xBB8003B0	L4_TRF0 [1416].TRF[8:8]	1
0xBB8003B0	L4_TRF0 [1417].TRF[9:9]	1
0xBB8003B0	L4_TRF0 [1418].TRF[10:10]	1
0xBB8003B0	L4_TRF0 [1419].TRF[11:11]	1
0xBB8003B0	L4_TRF0 [1420].TRF[12:12]	1
0xBB8003B0	L4_TRF0 [1421].TRF[13:13]	1
0xBB8003B0	L4_TRF0 [1422].TRF[14:14]	1
0xBB8003B0	L4_TRF0 [1423].TRF[15:15]	1
0xBB8003B0	L4_TRF0 [1424].TRF[16:16]	1
0xBB8003B0	L4_TRF0 [1425].TRF[17:17]	1
0xBB8003B0	L4_TRF0 [1426].TRF[18:18]	1
0xBB8003B0	L4_TRF0 [1427].TRF[19:19]	1
0xBB8003B0	L4_TRF0 [1428].TRF[20:20]	1
0xBB8003B0	L4_TRF0 [1429].TRF[21:21]	1
0xBB8003B0	L4_TRF0 [1430].TRF[22:22]	1
0xBB8003B0	L4_TRF0 [1431].TRF[23:23]	1
0xBB8003B0	L4_TRF0 [1432].TRF[24:24]	1
0xBB8003B0	L4_TRF0 [1433].TRF[25:25]	1
0xBB8003B0	L4_TRF0 [1434].TRF[26:26]	1
0xBB8003B0	L4_TRF0 [1435].TRF[27:27]	1
0xBB8003B0	L4_TRF0 [1436].TRF[28:28]	1
0xBB8003B0	L4_TRF0 [1437].TRF[29:29]	1

Address	Register	Len
0xBB8003B0	L4_TRF0 [1438].TRF[30:30]	1
0xBB8003B0	L4_TRF0 [1439].TRF[31:31]	1
0xBB8003B4	L4_TRF0 [1440].TRF[0:0]	1
0xBB8003B4	L4_TRF0 [1441].TRF[1:1]	1
0xBB8003B4	L4_TRF0 [1442].TRF[2:2]	1
0xBB8003B4	L4_TRF0 [1443].TRF[3:3]	1
0xBB8003B4	L4_TRF0 [1444].TRF[4:4]	1
0xBB8003B4	L4_TRF0 [1445].TRF[5:5]	1
0xBB8003B4	L4_TRF0 [1446].TRF[6:6]	1
0xBB8003B4	L4_TRF0 [1447].TRF[7:7]	1
0xBB8003B4	L4_TRF0 [1448].TRF[8:8]	1
0xBB8003B4	L4_TRF0 [1449].TRF[9:9]	1
0xBB8003B4	L4_TRF0 [1450].TRF[10:10]	1
0xBB8003B4	L4_TRF0 [1451].TRF[11:11]	1
0xBB8003B4	L4_TRF0 [1452].TRF[12:12]	1
0xBB8003B4	L4_TRF0 [1453].TRF[13:13]	1
0xBB8003B4	L4_TRF0 [1454].TRF[14:14]	1
0xBB8003B4	L4_TRF0 [1455].TRF[15:15]	1
0xBB8003B4	L4_TRF0 [1456].TRF[16:16]	1
0xBB8003B4	L4_TRF0 [1457].TRF[17:17]	1
0xBB8003B4	L4_TRF0 [1458].TRF[18:18]	1
0xBB8003B4	L4_TRF0 [1459].TRF[19:19]	1
0xBB8003B4	L4_TRF0 [1460].TRF[20:20]	1
0xBB8003B4	L4_TRF0 [1461].TRF[21:21]	1
0xBB8003B4	L4_TRF0 [1462].TRF[22:22]	1
0xBB8003B4	L4_TRF0 [1463].TRF[23:23]	1
0xBB8003B4	L4_TRF0 [1464].TRF[24:24]	1
0xBB8003B4	L4_TRF0 [1465].TRF[25:25]	1
0xBB8003B4	L4_TRF0 [1466].TRF[26:26]	1
0xBB8003B4	L4_TRF0 [1467].TRF[27:27]	1
0xBB8003B4	L4_TRF0 [1468].TRF[28:28]	1
0xBB8003B4	L4_TRF0 [1469].TRF[29:29]	1
0xBB8003B4	L4_TRF0 [1470].TRF[30:30]	1
0xBB8003B4	L4_TRF0 [1471].TRF[31:31]	1
0xBB8003B8	L4_TRF0 [1472].TRF[0:0]	1
0xBB8003B8	L4_TRF0 [1473].TRF[1:1]	1
0xBB8003B8	L4_TRF0 [1474].TRF[2:2]	1
0xBB8003B8	L4_TRF0 [1475].TRF[3:3]	1
0xBB8003B8	L4_TRF0 [1476].TRF[4:4]	1
0xBB8003B8	L4_TRF0 [1477].TRF[5:5]	1
0xBB8003B8	L4_TRF0 [1478].TRF[6:6]	1
0xBB8003B8	L4_TRF0 [1479].TRF[7:7]	1
0xBB8003B8	L4_TRF0 [1480].TRF[8:8]	1
0xBB8003B8	L4_TRF0 [1481].TRF[9:9]	1
0xBB8003B8	L4_TRF0 [1482].TRF[10:10]	1
0xBB8003B8	L4_TRF0 [1483].TRF[11:11]	1

Address	Register	Len
0xBB8003B8	L4_TRF0 [1484].TRF[12:12]	1
0xBB8003B8	L4_TRF0 [1485].TRF[13:13]	1
0xBB8003B8	L4_TRF0 [1486].TRF[14:14]	1
0xBB8003B8	L4_TRF0 [1487].TRF[15:15]	1
0xBB8003B8	L4_TRF0 [1488].TRF[16:16]	1
0xBB8003B8	L4_TRF0 [1489].TRF[17:17]	1
0xBB8003B8	L4_TRF0 [1490].TRF[18:18]	1
0xBB8003B8	L4_TRF0 [1491].TRF[19:19]	1
0xBB8003B8	L4_TRF0 [1492].TRF[20:20]	1
0xBB8003B8	L4_TRF0 [1493].TRF[21:21]	1
0xBB8003B8	L4_TRF0 [1494].TRF[22:22]	1
0xBB8003B8	L4_TRF0 [1495].TRF[23:23]	1
0xBB8003B8	L4_TRF0 [1496].TRF[24:24]	1
0xBB8003B8	L4_TRF0 [1497].TRF[25:25]	1
0xBB8003B8	L4_TRF0 [1498].TRF[26:26]	1
0xBB8003B8	L4_TRF0 [1499].TRF[27:27]	1
0xBB8003B8	L4_TRF0 [1500].TRF[28:28]	1
0xBB8003B8	L4_TRF0 [1501].TRF[29:29]	1
0xBB8003B8	L4_TRF0 [1502].TRF[30:30]	1
0xBB8003B8	L4_TRF0 [1503].TRF[31:31]	1
0xBB8003BC	L4_TRF0 [1504].TRF[0:0]	1
0xBB8003BC	L4_TRF0 [1505].TRF[1:1]	1
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0xBB8003BC	L4_TRF0 [1507].TRF[3:3]	1
0xBB8003BC	L4_TRF0 [1508].TRF[4:4]	1
0xBB8003BC	L4_TRF0 [1509].TRF[5:5]	1
0xBB8003BC	L4_TRF0 [1510].TRF[6:6]	1
0xBB8003BC	L4_TRF0 [1511].TRF[7:7]	1
0xBB8003BC	L4_TRF0 [1512].TRF[8:8]	1
0xBB8003BC	L4_TRF0 [1513].TRF[9:9]	1
0xBB8003BC	L4_TRF0 [1514].TRF[10:10]	1
0xBB8003BC	L4_TRF0 [1515].TRF[11:11]	1
0xBB8003BC	L4_TRF0 [1516].TRF[12:12]	1
0xBB8003BC	L4_TRF0 [1517].TRF[13:13]	1
0xBB8003BC	L4_TRF0 [1518].TRF[14:14]	1
0xBB8003BC	L4_TRF0 [1519].TRF[15:15]	1
0xBB8003BC	L4_TRF0 [1520].TRF[16:16]	1
0xBB8003BC	L4_TRF0 [1521].TRF[17:17]	1
0xBB8003BC	L4_TRF0 [1522].TRF[18:18]	1
0xBB8003BC	L4_TRF0 [1523].TRF[19:19]	1
0xBB8003BC	L4_TRF0 [1524].TRF[20:20]	1
0xBB8003BC	L4_TRF0 [1525].TRF[21:21]	1
0xBB8003BC	L4_TRF0 [1526].TRF[22:22]	1
0xBB8003BC	L4_TRF0 [1527].TRF[23:23]	1
0xBB8003BC	L4_TRF0 [1528].TRF[24:24]	1
0xBB8003BC	L4_TRF0 [1529].TRF[25:25]	1

Address	Register	Len
0xBB8003BC	L4_TRF0 [1530].TRF[26:26]	1
0xBB8003BC	L4_TRF0 [1531].TRF[27:27]	1
0xBB8003BC	L4_TRF0 [1532].TRF[28:28]	1
0xBB8003BC	L4_TRF0 [1533].TRF[29:29]	1
0xBB8003BC	L4_TRF0 [1534].TRF[30:30]	1
0xBB8003BC	L4_TRF0 [1535].TRF[31:31]	1
0xBB8003C0	L4_TRF0 [1536].TRF[0:0]	1
0xBB8003C0	L4_TRF0 [1537].TRF[1:1]	1
0xBB8003C0	L4_TRF0 [1538].TRF[2:2]	1
0xBB8003C0	L4_TRF0 [1539].TRF[3:3]	1
0xBB8003C0	L4_TRF0 [1540].TRF[4:4]	1
0xBB8003C0	L4_TRF0 [1541].TRF[5:5]	1
0xBB8003C0	L4_TRF0 [1542].TRF[6:6]	1
0xBB8003C0	L4_TRF0 [1543].TRF[7:7]	1
0xBB8003C0	L4_TRF0 [1544].TRF[8:8]	1
0xBB8003C0	L4_TRF0 [1545].TRF[9:9]	1
0xBB8003C0	L4_TRF0 [1546].TRF[10:10]	1
0xBB8003C0	L4_TRF0 [1547].TRF[11:11]	1
0xBB8003C0	L4_TRF0 [1548].TRF[12:12]	1
0xBB8003C0	L4_TRF0 [1549].TRF[13:13]	1
0xBB8003C0	L4_TRF0 [1550].TRF[14:14]	1
0xBB8003C0	L4_TRF0 [1551].TRF[15:15]	1
0xBB8003C0	L4_TRF0 [1552].TRF[16:16]	1
0xBB8003C0	L4_TRF0 [1553].TRF[17:17]	1
0xBB8003C0	L4_TRF0 [1554].TRF[18:18]	1
0xBB8003C0	L4_TRF0 [1555].TRF[19:19]	1
0xBB8003C0	L4_TRF0 [1556].TRF[20:20]	1
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0xBB8003C0	L4_TRF0 [1558].TRF[22:22]	1
0xBB8003C0	L4_TRF0 [1559].TRF[23:23]	1
0xBB8003C0	L4_TRF0 [1560].TRF[24:24]	1
0xBB8003C0	L4_TRF0 [1561].TRF[25:25]	1
0xBB8003C0	L4_TRF0 [1562].TRF[26:26]	1
0xBB8003C0	L4_TRF0 [1563].TRF[27:27]	1
0xBB8003C0	L4_TRF0 [1564].TRF[28:28]	1
0xBB8003C0	L4_TRF0 [1565].TRF[29:29]	1
0xBB8003C0	L4_TRF0 [1566].TRF[30:30]	1
0xBB8003C0	L4_TRF0 [1567].TRF[31:31]	1
0xBB8003C4	L4_TRF0 [1568].TRF[0:0]	1
0xBB8003C4	L4_TRF0 [1569].TRF[1:1]	1
0xBB8003C4	L4_TRF0 [1570].TRF[2:2]	1
0xBB8003C4	L4_TRF0 [1571].TRF[3:3]	1
0xBB8003C4	L4_TRF0 [1572].TRF[4:4]	1
0xBB8003C4	L4_TRF0 [1573].TRF[5:5]	1
0xBB8003C4	L4_TRF0 [1574].TRF[6:6]	1
0xBB8003C4	L4_TRF0 [1575].TRF[7:7]	1

Address	Register	Len
0xBB8003C4	L4_TRF0 [1576].TRF[8:8]	1
0xBB8003C4	L4_TRF0 [1577].TRF[9:9]	1
0xBB8003C4	L4_TRF0 [1578].TRF[10:10]	1
0xBB8003C4	L4_TRF0 [1579].TRF[11:11]	1
0xBB8003C4	L4_TRF0 [1580].TRF[12:12]	1
0xBB8003C4	L4_TRF0 [1581].TRF[13:13]	1
0xBB8003C4	L4_TRF0 [1582].TRF[14:14]	1
0xBB8003C4	L4_TRF0 [1583].TRF[15:15]	1
0xBB8003C4	L4_TRF0 [1584].TRF[16:16]	1
0xBB8003C4	L4_TRF0 [1585].TRF[17:17]	1
0xBB8003C4	L4_TRF0 [1586].TRF[18:18]	1
0xBB8003C4	L4_TRF0 [1587].TRF[19:19]	1
0xBB8003C4	L4_TRF0 [1588].TRF[20:20]	1
0xBB8003C4	L4_TRF0 [1589].TRF[21:21]	1
0xBB8003C4	L4_TRF0 [1590].TRF[22:22]	1
0xBB8003C4	L4_TRF0 [1591].TRF[23:23]	1
0xBB8003C4	L4_TRF0 [1592].TRF[24:24]	1
0xBB8003C4	L4_TRF0 [1593].TRF[25:25]	1
0xBB8003C4	L4_TRF0 [1594].TRF[26:26]	1
0xBB8003C4	L4_TRF0 [1595].TRF[27:27]	1
0xBB8003C4	L4_TRF0 [1596].TRF[28:28]	1
0xBB8003C4	L4_TRF0 [1597].TRF[29:29]	1
0xBB8003C4	L4_TRF0 [1598].TRF[30:30]	1
0xBB8003C4	L4_TRF0 [1599].TRF[31:31]	1
0xBB8003C8	L4_TRF0 [1600].TRF[0:0]	1
0xBB8003C8	L4_TRF0 [1601].TRF[1:1]	1
0xBB8003C8	L4_TRF0 [1602].TRF[2:2]	1
0xBB8003C8	L4_TRF0 [1603].TRF[3:3]	1
0xBB8003C8	L4_TRF0 [1604].TRF[4:4]	1
0xBB8003C8	L4_TRF0 [1605].TRF[5:5]	1
0xBB8003C8	L4_TRF0 [1606].TRF[6:6]	1
0xBB8003C8	L4_TRF0 [1607].TRF[7:7]	1
0xBB8003C8	L4_TRF0 [1608].TRF[8:8]	1
0xBB8003C8	L4_TRF0 [1609].TRF[9:9]	1
0xBB8003C8	L4_TRF0 [1610].TRF[10:10]	1
0xBB8003C8	L4_TRF0 [1611].TRF[11:11]	1
0xBB8003C8	L4_TRF0 [1612].TRF[12:12]	1
0xBB8003C8	L4_TRF0 [1613].TRF[13:13]	1
0xBB8003C8	L4_TRF0 [1614].TRF[14:14]	1
0xBB8003C8	L4_TRF0 [1615].TRF[15:15]	1
0xBB8003C8	L4_TRF0 [1616].TRF[16:16]	1
0xBB8003C8	L4_TRF0 [1617].TRF[17:17]	1
0xBB8003C8	L4_TRF0 [1618].TRF[18:18]	1
0xBB8003C8	L4_TRF0 [1619].TRF[19:19]	1
0xBB8003C8	L4_TRF0 [1620].TRF[20:20]	1
0xBB8003C8	L4_TRF0 [1621].TRF[21:21]	1

Address	Register	Len
0xBB8003C8	L4_TRF0 [1622].TRF[22:22]	1
0xBB8003C8	L4_TRF0 [1623].TRF[23:23]	1
0xBB8003C8	L4_TRF0 [1624].TRF[24:24]	1
0xBB8003C8	L4_TRF0 [1625].TRF[25:25]	1
0xBB8003C8	L4_TRF0 [1626].TRF[26:26]	1
0xBB8003C8	L4_TRF0 [1627].TRF[27:27]	1
0xBB8003C8	L4_TRF0 [1628].TRF[28:28]	1
0xBB8003C8	L4_TRF0 [1629].TRF[29:29]	1
0xBB8003C8	L4_TRF0 [1630].TRF[30:30]	1
0xBB8003C8	L4_TRF0 [1631].TRF[31:31]	1
0xBB8003CC	L4_TRF0 [1632].TRF[0:0]	1
0xBB8003CC	L4_TRF0 [1633].TRF[1:1]	1
0xBB8003CC	L4_TRF0 [1634].TRF[2:2]	1
0xBB8003CC	L4_TRF0 [1635].TRF[3:3]	1
0xBB8003CC	L4_TRF0 [1636].TRF[4:4]	1
0xBB8003CC	L4_TRF0 [1637].TRF[5:5]	1
0xBB8003CC	L4_TRF0 [1638].TRF[6:6]	1
0xBB8003CC	L4_TRF0 [1639].TRF[7:7]	1
0xBB8003CC	L4_TRF0 [1640].TRF[8:8]	1
0xBB8003CC	L4_TRF0 [1641].TRF[9:9]	1
0xBB8003CC	L4_TRF0 [1642].TRF[10:10]	1
0xBB8003CC	L4_TRF0 [1643].TRF[11:11]	1
0xBB8003CC	L4_TRF0 [1644].TRF[12:12]	1
0xBB8003CC	L4_TRF0 [1645].TRF[13:13]	1
0xBB8003CC	L4_TRF0 [1646].TRF[14:14]	1
0xBB8003CC	L4_TRF0 [1647].TRF[15:15]	1
0xBB8003CC	L4_TRF0 [1648].TRF[16:16]	1
0xBB8003CC	L4_TRF0 [1649].TRF[17:17]	1
0xBB8003CC	L4_TRF0 [1650].TRF[18:18]	1
0xBB8003CC	L4_TRF0 [1651].TRF[19:19]	1
0xBB8003CC	L4_TRF0 [1652].TRF[20:20]	1
0xBB8003CC	L4_TRF0 [1653].TRF[21:21]	1
0xBB8003CC	L4_TRF0 [1654].TRF[22:22]	1
0xBB8003CC	L4_TRF0 [1655].TRF[23:23]	1
0xBB8003CC	L4_TRF0 [1656].TRF[24:24]	1
0xBB8003CC	L4_TRF0 [1657].TRF[25:25]	1
0xBB8003CC	L4_TRF0 [1658].TRF[26:26]	1
0xBB8003CC	L4_TRF0 [1659].TRF[27:27]	1
0xBB8003CC	L4_TRF0 [1660].TRF[28:28]	1
0xBB8003CC	L4_TRF0 [1661].TRF[29:29]	1
0xBB8003CC	L4_TRF0 [1662].TRF[30:30]	1
0xBB8003CC	L4_TRF0 [1663].TRF[31:31]	1
0xBB8003D0	L4_TRF0 [1664].TRF[0:0]	1
0xBB8003D0	L4_TRF0 [1665].TRF[1:1]	1
0xBB8003D0	L4_TRF0 [1666].TRF[2:2]	1
0xBB8003D0	L4_TRF0 [1667].TRF[3:3]	1

Address	Register	Len
0xBB8003D0	L4_TRF0 [1668].TRF[4:4]	1
0xBB8003D0	L4_TRF0 [1669].TRF[5:5]	1
0xBB8003D0	L4_TRF0 [1670].TRF[6:6]	1
0xBB8003D0	L4_TRF0 [1671].TRF[7:7]	1
0xBB8003D0	L4_TRF0 [1672].TRF[8:8]	1
0xBB8003D0	L4_TRF0 [1673].TRF[9:9]	1
0xBB8003D0	L4_TRF0 [1674].TRF[10:10]	1
0xBB8003D0	L4_TRF0 [1675].TRF[11:11]	1
0xBB8003D0	L4_TRF0 [1676].TRF[12:12]	1
0xBB8003D0	L4_TRF0 [1677].TRF[13:13]	1
0xBB8003D0	L4_TRF0 [1678].TRF[14:14]	1
0xBB8003D0	L4_TRF0 [1679].TRF[15:15]	1
0xBB8003D0	L4_TRF0 [1680].TRF[16:16]	1
0xBB8003D0	L4_TRF0 [1681].TRF[17:17]	1
0xBB8003D0	L4_TRF0 [1682].TRF[18:18]	1
0xBB8003D0	L4_TRF0 [1683].TRF[19:19]	1
0xBB8003D0	L4_TRF0 [1684].TRF[20:20]	1
0xBB8003D0	L4_TRF0 [1685].TRF[21:21]	1
0xBB8003D0	L4_TRF0 [1686].TRF[22:22]	1
0xBB8003D0	L4_TRF0 [1687].TRF[23:23]	1
0xBB8003D0	L4_TRF0 [1688].TRF[24:24]	1
0xBB8003D0	L4_TRF0 [1689].TRF[25:25]	1
0xBB8003D0	L4_TRF0 [1690].TRF[26:26]	1
0xBB8003D0	L4_TRF0 [1691].TRF[27:27]	1
0xBB8003D0	L4_TRF0 [1692].TRF[28:28]	1
0xBB8003D0	L4_TRF0 [1693].TRF[29:29]	1
0xBB8003D0	L4_TRF0 [1694].TRF[30:30]	1
0xBB8003D0	L4_TRF0 [1695].TRF[31:31]	1
0xBB8003D4	L4_TRF0 [1696].TRF[0:0]	1
0xBB8003D4	L4_TRF0 [1697].TRF[1:1]	1
0xBB8003D4	L4_TRF0 [1698].TRF[2:2]	1
0xBB8003D4	L4_TRF0 [1699].TRF[3:3]	1
0xBB8003D4	L4_TRF0 [1700].TRF[4:4]	1
0xBB8003D4	L4_TRF0 [1701].TRF[5:5]	1
0xBB8003D4	L4_TRF0 [1702].TRF[6:6]	1
0xBB8003D4	L4_TRF0 [1703].TRF[7:7]	1
0xBB8003D4	L4_TRF0 [1704].TRF[8:8]	1
0xBB8003D4	L4_TRF0 [1705].TRF[9:9]	1
0xBB8003D4	L4_TRF0 [1706].TRF[10:10]	1
0xBB8003D4	L4_TRF0 [1707].TRF[11:11]	1
0xBB8003D4	L4_TRF0 [1708].TRF[12:12]	1
0xBB8003D4	L4_TRF0 [1709].TRF[13:13]	1
0xBB8003D4	L4_TRF0 [1710].TRF[14:14]	1
0xBB8003D4	L4_TRF0 [1711].TRF[15:15]	1
0xBB8003D4	L4_TRF0 [1712].TRF[16:16]	1
0xBB8003D4	L4_TRF0 [1713].TRF[17:17]	1



Address	Register	Len
0xBB8003D4	L4_TRF0 [1714].TRF[18:18]	1
0xBB8003D4	L4_TRF0 [1715].TRF[19:19]	1
0xBB8003D4	L4_TRF0 [1716].TRF[20:20]	1
0xBB8003D4	L4_TRF0 [1717].TRF[21:21]	1
0xBB8003D4	L4_TRF0 [1718].TRF[22:22]	1
0xBB8003D4	L4_TRF0 [1719].TRF[23:23]	1
0xBB8003D4	L4_TRF0 [1720].TRF[24:24]	1
0xBB8003D4	L4_TRF0 [1721].TRF[25:25]	1
0xBB8003D4	L4_TRF0 [1722].TRF[26:26]	1
0xBB8003D4	L4_TRF0 [1723].TRF[27:27]	1
0xBB8003D4	L4_TRF0 [1724].TRF[28:28]	1
0xBB8003D4	L4_TRF0 [1725].TRF[29:29]	1
0xBB8003D4	L4_TRF0 [1726].TRF[30:30]	1
0xBB8003D4	L4_TRF0 [1727].TRF[31:31]	1
0xBB8003D8	L4_TRF0 [1728].TRF[0:0]	1
0xBB8003D8	L4_TRF0 [1729].TRF[1:1]	1
0xBB8003D8	L4_TRF0 [1730].TRF[2:2]	1
0xBB8003D8	L4_TRF0 [1731].TRF[3:3]	1
0xBB8003D8	L4_TRF0 [1732].TRF[4:4]	1
0xBB8003D8	L4_TRF0 [1733].TRF[5:5]	1
0xBB8003D8	L4_TRF0 [1734].TRF[6:6]	1
0xBB8003D8	L4_TRF0 [1735].TRF[7:7]	1
0xBB8003D8	L4_TRF0 [1736].TRF[8:8]	1
0xBB8003D8	L4_TRF0 [1737].TRF[9:9]	1
0xBB8003D8	L4_TRF0 [1738].TRF[10:10]	1
0xBB8003D8	L4_TRF0 [1739].TRF[11:11]	1
0xBB8003D8	L4_TRF0 [1740].TRF[12:12]	1
0xBB8003D8	L4_TRF0 [1741].TRF[13:13]	1
0xBB8003D8	L4_TRF0 [1742].TRF[14:14]	1
0xBB8003D8	L4_TRF0 [1743].TRF[15:15]	1
0xBB8003D8	L4_TRF0 [1744].TRF[16:16]	1
0xBB8003D8	L4_TRF0 [1745].TRF[17:17]	1
0xBB8003D8	L4_TRF0 [1746].TRF[18:18]	1
0xBB8003D8	L4_TRF0 [1747].TRF[19:19]	1
0xBB8003D8	L4_TRF0 [1748].TRF[20:20]	1
0xBB8003D8	L4_TRF0 [1749].TRF[21:21]	1
0xBB8003D8	L4_TRF0 [1750].TRF[22:22]	1
0xBB8003D8	L4_TRF0 [1751].TRF[23:23]	1
0xBB8003D8	L4_TRF0 [1752].TRF[24:24]	1
0xBB8003D8	L4_TRF0 [1753].TRF[25:25]	1
0xBB8003D8	L4_TRF0 [1754].TRF[26:26]	1
0xBB8003D8	L4_TRF0 [1755].TRF[27:27]	1
0xBB8003D8	L4_TRF0 [1756].TRF[28:28]	1
0xBB8003D8	L4_TRF0 [1757].TRF[29:29]	1
0xBB8003D8	L4_TRF0 [1758].TRF[30:30]	1
0xBB8003D8	L4_TRF0 [1759].TRF[31:31]	1

Address	Register	Len
0xBB8003DC	L4_TRF0 [1760].TRF[0:0]	1
0xBB8003DC	L4_TRF0 [1761].TRF[1:1]	1
0xBB8003DC	L4_TRF0 [1762].TRF[2:2]	1
0xBB8003DC	L4_TRF0 [1763].TRF[3:3]	1
0xBB8003DC	L4_TRF0 [1764].TRF[4:4]	1
0xBB8003DC	L4_TRF0 [1765].TRF[5:5]	1
0xBB8003DC	L4_TRF0 [1766].TRF[6:6]	1
0xBB8003DC	L4_TRF0 [1767].TRF[7:7]	1
0xBB8003DC	L4_TRF0 [1768].TRF[8:8]	1
0xBB8003DC	L4_TRF0 [1769].TRF[9:9]	1
0xBB8003DC	L4_TRF0 [1770].TRF[10:10]	1
0xBB8003DC	L4_TRF0 [1771].TRF[11:11]	1
0xBB8003DC	L4_TRF0 [1772].TRF[12:12]	1
0xBB8003DC	L4_TRF0 [1773].TRF[13:13]	1
0xBB8003DC	L4_TRF0 [1774].TRF[14:14]	1
0xBB8003DC	L4_TRF0 [1775].TRF[15:15]	1
0xBB8003DC	L4_TRF0 [1776].TRF[16:16]	1
0xBB8003DC	L4_TRF0 [1777].TRF[17:17]	1
0xBB8003DC	L4_TRF0 [1778].TRF[18:18]	1
0xBB8003DC	L4_TRF0 [1779].TRF[19:19]	1
0xBB8003DC	L4_TRF0 [1780].TRF[20:20]	1
0xBB8003DC	L4_TRF0 [1781].TRF[21:21]	1
0xBB8003DC	L4_TRF0 [1782].TRF[22:22]	1
0xBB8003DC	L4_TRF0 [1783].TRF[23:23]	1
0xBB8003DC	L4_TRF0 [1784].TRF[24:24]	1
0xBB8003DC	L4_TRF0 [1785].TRF[25:25]	1
0xBB8003DC	L4_TRF0 [1786].TRF[26:26]	1
0xBB8003DC	L4_TRF0 [1787].TRF[27:27]	1
0xBB8003DC	L4_TRF0 [1788].TRF[28:28]	1
0xBB8003DC	L4_TRF0 [1789].TRF[29:29]	1
0xBB8003DC	L4_TRF0 [1790].TRF[30:30]	1
0xBB8003DC	L4_TRF0 [1791].TRF[31:31]	1
0xBB8003E0	L4_TRF0 [1792].TRF[0:0]	1
0xBB8003E0	L4_TRF0 [1793].TRF[1:1]	1
0xBB8003E0	L4_TRF0 [1794].TRF[2:2]	1
0xBB8003E0	L4_TRF0 [1795].TRF[3:3]	1
0xBB8003E0	L4_TRF0 [1796].TRF[4:4]	1
0xBB8003E0	L4_TRF0 [1797].TRF[5:5]	1
0xBB8003E0	L4_TRF0 [1798].TRF[6:6]	1
0xBB8003E0	L4_TRF0 [1799].TRF[7:7]	1
0xBB8003E0	L4_TRF0 [1800].TRF[8:8]	1
0xBB8003E0	L4_TRF0 [1801].TRF[9:9]	1
0xBB8003E0	L4_TRF0 [1802].TRF[10:10]	1
0xBB8003E0	L4_TRF0 [1803].TRF[11:11]	1
0xBB8003E0	L4_TRF0 [1804].TRF[12:12]	1
0xBB8003E0	L4_TRF0 [1805].TRF[13:13]	1

Address	Register	Len
0xBB8003E0	L4_TRF0 [1806].TRF[14:14]	1
0xBB8003E0	L4_TRF0 [1807].TRF[15:15]	1
0xBB8003E0	L4_TRF0 [1808].TRF[16:16]	1
0xBB8003E0	L4_TRF0 [1809].TRF[17:17]	1
0xBB8003E0	L4_TRF0 [1810].TRF[18:18]	1
0xBB8003E0	L4_TRF0 [1811].TRF[19:19]	1
0xBB8003E0	L4_TRF0 [1812].TRF[20:20]	1
0xBB8003E0	L4_TRF0 [1813].TRF[21:21]	1
0xBB8003E0	L4_TRF0 [1814].TRF[22:22]	1
0xBB8003E0	L4_TRF0 [1815].TRF[23:23]	1
0xBB8003E0	L4_TRF0 [1816].TRF[24:24]	1
0xBB8003E0	L4_TRF0 [1817].TRF[25:25]	1
0xBB8003E0	L4_TRF0 [1818].TRF[26:26]	1
0xBB8003E0	L4_TRF0 [1819].TRF[27:27]	1
0xBB8003E0	L4_TRF0 [1820].TRF[28:28]	1
0xBB8003E0	L4_TRF0 [1821].TRF[29:29]	1
0xBB8003E0	L4_TRF0 [1822].TRF[30:30]	1
0xBB8003E0	L4_TRF0 [1823].TRF[31:31]	1
0xBB8003E4	L4_TRF0 [1824].TRF[0:0]	1
0xBB8003E4	L4_TRF0 [1825].TRF[1:1]	1
0xBB8003E4	L4_TRF0 [1826].TRF[2:2]	1
0xBB8003E4	L4_TRF0 [1827].TRF[3:3]	1
0xBB8003E4	L4_TRF0 [1828].TRF[4:4]	1
0xBB8003E4	L4_TRF0 [1829].TRF[5:5]	1
0xBB8003E4	L4_TRF0 [1830].TRF[6:6]	1
0xBB8003E4	L4_TRF0 [1831].TRF[7:7]	1
0xBB8003E4	L4_TRF0 [1832].TRF[8:8]	1
0xBB8003E4	L4_TRF0 [1833].TRF[9:9]	1
0xBB8003E4	L4_TRF0 [1834].TRF[10:10]	1
0xBB8003E4	L4_TRF0 [1835].TRF[11:11]	1
0xBB8003E4	L4_TRF0 [1836].TRF[12:12]	1
0xBB8003E4	L4_TRF0 [1837].TRF[13:13]	1
0xBB8003E4	L4_TRF0 [1838].TRF[14:14]	1
0xBB8003E4	L4_TRF0 [1839].TRF[15:15]	1
0xBB8003E4	L4_TRF0 [1840].TRF[16:16]	1
0xBB8003E4	L4_TRF0 [1841].TRF[17:17]	1
0xBB8003E4	L4_TRF0 [1842].TRF[18:18]	1
0xBB8003E4	L4_TRF0 [1843].TRF[19:19]	1
0xBB8003E4	L4_TRF0 [1844].TRF[20:20]	1
0xBB8003E4	L4_TRF0 [1845].TRF[21:21]	1
0xBB8003E4	L4_TRF0 [1846].TRF[22:22]	1
0xBB8003E4	L4_TRF0 [1847].TRF[23:23]	1
0xBB8003E4	L4_TRF0 [1848].TRF[24:24]	1
0xBB8003E4	L4_TRF0 [1849].TRF[25:25]	1
0xBB8003E4	L4_TRF0 [1850].TRF[26:26]	1
0xBB8003E4	L4_TRF0 [1851].TRF[27:27]	1

Address	Register	Len
0xBB8003E4	L4_TRF0 [1852].TRF[28:28]	1
0xBB8003E4	L4_TRF0 [1853].TRF[29:29]	1
0xBB8003E4	L4_TRF0 [1854].TRF[30:30]	1
0xBB8003E4	L4_TRF0 [1855].TRF[31:31]	1
0xBB8003E8	L4_TRF0 [1856].TRF[0:0]	1
0xBB8003E8	L4_TRF0 [1857].TRF[1:1]	1
0xBB8003E8	L4_TRF0 [1858].TRF[2:2]	1
0xBB8003E8	L4_TRF0 [1859].TRF[3:3]	1
0xBB8003E8	L4_TRF0 [1860].TRF[4:4]	1
0xBB8003E8	L4_TRF0 [1861].TRF[5:5]	1
0xBB8003E8	L4_TRF0 [1862].TRF[6:6]	1
0xBB8003E8	L4_TRF0 [1863].TRF[7:7]	1
0xBB8003E8	L4_TRF0 [1864].TRF[8:8]	1
0xBB8003E8	L4_TRF0 [1865].TRF[9:9]	1
0xBB8003E8	L4_TRF0 [1866].TRF[10:10]	1
0xBB8003E8	L4_TRF0 [1867].TRF[11:11]	1
0xBB8003E8	L4_TRF0 [1868].TRF[12:12]	1
0xBB8003E8	L4_TRF0 [1869].TRF[13:13]	1
0xBB8003E8	L4_TRF0 [1870].TRF[14:14]	1
0xBB8003E8	L4_TRF0 [1871].TRF[15:15]	1
0xBB8003E8	L4_TRF0 [1872].TRF[16:16]	1
0xBB8003E8	L4_TRF0 [1873].TRF[17:17]	1
0xBB8003E8	L4_TRF0 [1874].TRF[18:18]	1
0xBB8003E8	L4_TRF0 [1875].TRF[19:19]	1
0xBB8003E8	L4_TRF0 [1876].TRF[20:20]	1
0xBB8003E8	L4_TRF0 [1877].TRF[21:21]	1
0xBB8003E8	L4_TRF0 [1878].TRF[22:22]	1
0xBB8003E8	L4_TRF0 [1879].TRF[23:23]	1
0xBB8003E8	L4_TRF0 [1880].TRF[24:24]	1
0xBB8003E8	L4_TRF0 [1881].TRF[25:25]	1
0xBB8003E8	L4_TRF0 [1882].TRF[26:26]	1
0xBB8003E8	L4_TRF0 [1883].TRF[27:27]	1
0xBB8003E8	L4_TRF0 [1884].TRF[28:28]	1
0xBB8003E8	L4_TRF0 [1885].TRF[29:29]	1
0xBB8003E8	L4_TRF0 [1886].TRF[30:30]	1
0xBB8003E8	L4_TRF0 [1887].TRF[31:31]	1
0xBB8003EC	L4_TRF0 [1888].TRF[0:0]	1
0xBB8003EC	L4_TRF0 [1889].TRF[1:1]	1
0xBB8003EC	L4_TRF0 [1890].TRF[2:2]	1
0xBB8003EC	L4_TRF0 [1891].TRF[3:3]	1
0xBB8003EC	L4_TRF0 [1892].TRF[4:4]	1
0xBB8003EC	L4_TRF0 [1893].TRF[5:5]	1
0xBB8003EC	L4_TRF0 [1894].TRF[6:6]	1
0xBB8003EC	L4_TRF0 [1895].TRF[7:7]	1
0xBB8003EC	L4_TRF0 [1896].TRF[8:8]	1
0xBB8003EC	L4_TRF0 [1897].TRF[9:9]	1

Address	Register	Len
0xBB8003EC	L4_TRF0 [1898].TRF[10:10]	1
0xBB8003EC	L4_TRF0 [1899].TRF[11:11]	1
0xBB8003EC	L4_TRF0 [1900].TRF[12:12]	1
0xBB8003EC	L4_TRF0 [1901].TRF[13:13]	1
0xBB8003EC	L4_TRF0 [1902].TRF[14:14]	1
0xBB8003EC	L4_TRF0 [1903].TRF[15:15]	1
0xBB8003EC	L4_TRF0 [1904].TRF[16:16]	1
0xBB8003EC	L4_TRF0 [1905].TRF[17:17]	1
0xBB8003EC	L4_TRF0 [1906].TRF[18:18]	1
0xBB8003EC	L4_TRF0 [1907].TRF[19:19]	1
0xBB8003EC	L4_TRF0 [1908].TRF[20:20]	1
0xBB8003EC	L4_TRF0 [1909].TRF[21:21]	1
0xBB8003EC	L4_TRF0 [1910].TRF[22:22]	1
0xBB8003EC	L4_TRF0 [1911].TRF[23:23]	1
0xBB8003EC	L4_TRF0 [1912].TRF[24:24]	1
0xBB8003EC	L4_TRF0 [1913].TRF[25:25]	1
0xBB8003EC	L4_TRF0 [1914].TRF[26:26]	1
0xBB8003EC	L4_TRF0 [1915].TRF[27:27]	1
0xBB8003EC	L4_TRF0 [1916].TRF[28:28]	1
0xBB8003EC	L4_TRF0 [1917].TRF[29:29]	1
0xBB8003EC	L4_TRF0 [1918].TRF[30:30]	1
0xBB8003EC	L4_TRF0 [1919].TRF[31:31]	1
0xBB8003F0	L4_TRF0 [1920].TRF[0:0]	1
0xBB8003F0	L4_TRF0 [1921].TRF[1:1]	1
0xBB8003F0	L4_TRF0 [1922].TRF[2:2]	1
0xBB8003F0	L4_TRF0 [1923].TRF[3:3]	1
0xBB8003F0	L4_TRF0 [1924].TRF[4:4]	1
0xBB8003F0	L4_TRF0 [1925].TRF[5:5]	1
0xBB8003F0	L4_TRF0 [1926].TRF[6:6]	1
0xBB8003F0	L4_TRF0 [1927].TRF[7:7]	1
0xBB8003F0	L4_TRF0 [1928].TRF[8:8]	1
0xBB8003F0	L4_TRF0 [1929].TRF[9:9]	1
0xBB8003F0	L4_TRF0 [1930].TRF[10:10]	1
0xBB8003F0	L4_TRF0 [1931].TRF[11:11]	1
0xBB8003F0	L4_TRF0 [1932].TRF[12:12]	1
0xBB8003F0	L4_TRF0 [1933].TRF[13:13]	1
0xBB8003F0	L4_TRF0 [1934].TRF[14:14]	1
0xBB8003F0	L4_TRF0 [1935].TRF[15:15]	1
0xBB8003F0	L4_TRF0 [1936].TRF[16:16]	1
0xBB8003F0	L4_TRF0 [1937].TRF[17:17]	1
0xBB8003F0	L4_TRF0 [1938].TRF[18:18]	1
0xBB8003F0	L4_TRF0 [1939].TRF[19:19]	1
0xBB8003F0	L4_TRF0 [1940].TRF[20:20]	1
0xBB8003F0	L4_TRF0 [1941].TRF[21:21]	1
0xBB8003F0	L4_TRF0 [1942].TRF[22:22]	1
0xBB8003F0	L4_TRF0 [1943].TRF[23:23]	1

Address	Register	Len
0xBB8003F0	L4_TRF0 [1944].TRF[24:24]	1
0xBB8003F0	L4_TRF0 [1945].TRF[25:25]	1
0xBB8003F0	L4_TRF0 [1946].TRF[26:26]	1
0xBB8003F0	L4_TRF0 [1947].TRF[27:27]	1
0xBB8003F0	L4_TRF0 [1948].TRF[28:28]	1
0xBB8003F0	L4_TRF0 [1949].TRF[29:29]	1
0xBB8003F0	L4_TRF0 [1950].TRF[30:30]	1
0xBB8003F0	L4_TRF0 [1951].TRF[31:31]	1
0xBB8003F4	L4_TRF0 [1952].TRF[0:0]	1
0xBB8003F4	L4_TRF0 [1953].TRF[1:1]	1
0xBB8003F4	L4_TRF0 [1954].TRF[2:2]	1
0xBB8003F4	L4_TRF0 [1955].TRF[3:3]	1
0xBB8003F4	L4_TRF0 [1956].TRF[4:4]	1
0xBB8003F4	L4_TRF0 [1957].TRF[5:5]	1
0xBB8003F4	L4_TRF0 [1958].TRF[6:6]	1
0xBB8003F4	L4_TRF0 [1959].TRF[7:7]	1
0xBB8003F4	L4_TRF0 [1960].TRF[8:8]	1
0xBB8003F4	L4_TRF0 [1961].TRF[9:9]	1
0xBB8003F4	L4_TRF0 [1962].TRF[10:10]	1
0xBB8003F4	L4_TRF0 [1963].TRF[11:11]	1
0xBB8003F4	L4_TRF0 [1964].TRF[12:12]	1
0xBB8003F4	L4_TRF0 [1965].TRF[13:13]	1
0xBB8003F4	L4_TRF0 [1966].TRF[14:14]	1
0xBB8003F4	L4_TRF0 [1967].TRF[15:15]	1
0xBB8003F4	L4_TRF0 [1968].TRF[16:16]	1
0xBB8003F4	L4_TRF0 [1969].TRF[17:17]	1
0xBB8003F4	L4_TRF0 [1970].TRF[18:18]	1
0xBB8003F4	L4_TRF0 [1971].TRF[19:19]	1
0xBB8003F4	L4_TRF0 [1972].TRF[20:20]	1
0xBB8003F4	L4_TRF0 [1973].TRF[21:21]	1
0xBB8003F4	L4_TRF0 [1974].TRF[22:22]	1
0xBB8003F4	L4_TRF0 [1975].TRF[23:23]	1
0xBB8003F4	L4_TRF0 [1976].TRF[24:24]	1
0xBB8003F4	L4_TRF0 [1977].TRF[25:25]	1
0xBB8003F4	L4_TRF0 [1978].TRF[26:26]	1
0xBB8003F4	L4_TRF0 [1979].TRF[27:27]	1
0xBB8003F4	L4_TRF0 [1980].TRF[28:28]	1
0xBB8003F4	L4_TRF0 [1981].TRF[29:29]	1
0xBB8003F4	L4_TRF0 [1982].TRF[30:30]	1
0xBB8003F4	L4_TRF0 [1983].TRF[31:31]	1
0xBB8003F8	L4_TRF0 [1984].TRF[0:0]	1
0xBB8003F8	L4_TRF0 [1985].TRF[1:1]	1
0xBB8003F8	L4_TRF0 [1986].TRF[2:2]	1
0xBB8003F8	L4_TRF0 [1987].TRF[3:3]	1
0xBB8003F8	L4_TRF0 [1988].TRF[4:4]	1
0xBB8003F8	L4_TRF0 [1989].TRF[5:5]	1

Address	Register	Len
0xBB8003F8	L4_TRF0 [1990].TRF[6:6]	1
0xBB8003F8	L4_TRF0 [1991].TRF[7:7]	1
0xBB8003F8	L4_TRF0 [1992].TRF[8:8]	1
0xBB8003F8	L4_TRF0 [1993].TRF[9:9]	1
0xBB8003F8	L4_TRF0 [1994].TRF[10:10]	1
0xBB8003F8	L4_TRF0 [1995].TRF[11:11]	1
0xBB8003F8	L4_TRF0 [1996].TRF[12:12]	1
0xBB8003F8	L4_TRF0 [1997].TRF[13:13]	1
0xBB8003F8	L4_TRF0 [1998].TRF[14:14]	1
0xBB8003F8	L4_TRF0 [1999].TRF[15:15]	1
0xBB8003F8	L4_TRF0 [2000].TRF[16:16]	1
0xBB8003F8	L4_TRF0 [2001].TRF[17:17]	1
0xBB8003F8	L4_TRF0 [2002].TRF[18:18]	1
0xBB8003F8	L4_TRF0 [2003].TRF[19:19]	1
0xBB8003F8	L4_TRF0 [2004].TRF[20:20]	1
0xBB8003F8	L4_TRF0 [2005].TRF[21:21]	1
0xBB8003F8	L4_TRF0 [2006].TRF[22:22]	1
0xBB8003F8	L4_TRF0 [2007].TRF[23:23]	1
0xBB8003F8	L4_TRF0 [2008].TRF[24:24]	1
0xBB8003F8	L4_TRF0 [2009].TRF[25:25]	1
0xBB8003F8	L4_TRF0 [2010].TRF[26:26]	1
0xBB8003F8	L4_TRF0 [2011].TRF[27:27]	1
0xBB8003F8	L4_TRF0 [2012].TRF[28:28]	1
0xBB8003F8	L4_TRF0 [2013].TRF[29:29]	1
0xBB8003F8	L4_TRF0 [2014].TRF[30:30]	1
0xBB8003F8	L4_TRF0 [2015].TRF[31:31]	1
0xBB8003FC	L4_TRF0 [2016].TRF[0:0]	1
0xBB8003FC	L4_TRF0 [2017].TRF[1:1]	1
0xBB8003FC	L4_TRF0 [2018].TRF[2:2]	1
0xBB8003FC	L4_TRF0 [2019].TRF[3:3]	1
0xBB8003FC	L4_TRF0 [2020].TRF[4:4]	1
0xBB8003FC	L4_TRF0 [2021].TRF[5:5]	1
0xBB8003FC	L4_TRF0 [2022].TRF[6:6]	1
0xBB8003FC	L4_TRF0 [2023].TRF[7:7]	1
0xBB8003FC	L4_TRF0 [2024].TRF[8:8]	1
0xBB8003FC	L4_TRF0 [2025].TRF[9:9]	1
0xBB8003FC	L4_TRF0 [2026].TRF[10:10]	1
0xBB8003FC	L4_TRF0 [2027].TRF[11:11]	1
0xBB8003FC	L4_TRF0 [2028].TRF[12:12]	1
0xBB8003FC	L4_TRF0 [2029].TRF[13:13]	1
0xBB8003FC	L4_TRF0 [2030].TRF[14:14]	1
0xBB8003FC	L4_TRF0 [2031].TRF[15:15]	1
0xBB8003FC	L4_TRF0 [2032].TRF[16:16]	1
0xBB8003FC	L4_TRF0 [2033].TRF[17:17]	1
0xBB8003FC	L4_TRF0 [2034].TRF[18:18]	1
0xBB8003FC	L4_TRF0 [2035].TRF[19:19]	1

Address	Register	Len
0xBB8003FC	L4_TRF0 [2036].TRF[20:20]	1
0xBB8003FC	L4_TRF0 [2037].TRF[21:21]	1
0xBB8003FC	L4_TRF0 [2038].TRF[22:22]	1
0xBB8003FC	L4_TRF0 [2039].TRF[23:23]	1
0xBB8003FC	L4_TRF0 [2040].TRF[24:24]	1
0xBB8003FC	L4_TRF0 [2041].TRF[25:25]	1
0xBB8003FC	L4_TRF0 [2042].TRF[26:26]	1
0xBB8003FC	L4_TRF0 [2043].TRF[27:27]	1
0xBB8003FC	L4_TRF0 [2044].TRF[28:28]	1
0xBB8003FC	L4_TRF0 [2045].TRF[29:29]	1
0xBB8003FC	L4_TRF0 [2046].TRF[30:30]	1
0xBB8003FC	L4_TRF0 [2047].TRF[31:31]	1
0xBB800400	L4_TRF1 [0].TRF[0:0]	1
0xBB800400	L4_TRF1 [1].TRF[1:1]	1
0xBB800400	L4_TRF1 [2].TRF[2:2]	1
0xBB800400	L4_TRF1 [3].TRF[3:3]	1
0xBB800400	L4_TRF1 [4].TRF[4:4]	1
0xBB800400	L4_TRF1 [5].TRF[5:5]	1
0xBB800400	L4_TRF1 [6].TRF[6:6]	1
0xBB800400	L4_TRF1 [7].TRF[7:7]	1
0xBB800400	L4_TRF1 [8].TRF[8:8]	1
0xBB800400	L4_TRF1 [9].TRF[9:9]	1
0xBB800400	L4_TRF1 [10].TRF[10:10]	1
0xBB800400	L4_TRF1 [11].TRF[11:11]	1
0xBB800400	L4_TRF1 [12].TRF[12:12]	1
0xBB800400	L4_TRF1 [13].TRF[13:13]	1
0xBB800400	L4_TRF1 [14].TRF[14:14]	1
0xBB800400	L4_TRF1 [15].TRF[15:15]	1
0xBB800400	L4_TRF1 [16].TRF[16:16]	1
0xBB800400	L4_TRF1 [17].TRF[17:17]	1
0xBB800400	L4_TRF1 [18].TRF[18:18]	1
0xBB800400	L4_TRF1 [19].TRF[19:19]	1
0xBB800400	L4_TRF1 [20].TRF[20:20]	1
0xBB800400	L4_TRF1 [21].TRF[21:21]	1
0xBB800400	L4_TRF1 [22].TRF[22:22]	1
0xBB800400	L4_TRF1 [23].TRF[23:23]	1
0xBB800400	L4_TRF1 [24].TRF[24:24]	1
0xBB800400	L4_TRF1 [25].TRF[25:25]	1
0xBB800400	L4_TRF1 [26].TRF[26:26]	1
0xBB800400	L4_TRF1 [27].TRF[27:27]	1
0xBB800400	L4_TRF1 [28].TRF[28:28]	1
0xBB800400	L4_TRF1 [29].TRF[29:29]	1
0xBB800400	L4_TRF1 [30].TRF[30:30]	1
0xBB800400	L4_TRF1 [31].TRF[31:31]	1
0xBB800404	L4_TRF1 [32].TRF[0:0]	1
0xBB800404	L4_TRF1 [33].TRF[1:1]	1



Address	Register	Len
0xBB800404	L4_TRF1 [34].TRF[2:2]	1
0xBB800404	L4_TRF1 [35].TRF[3:3]	1
0xBB800404	L4_TRF1 [36].TRF[4:4]	1
0xBB800404	L4_TRF1 [37].TRF[5:5]	1
0xBB800404	L4_TRF1 [38].TRF[6:6]	1
0xBB800404	L4_TRF1 [39].TRF[7:7]	1
0xBB800404	L4_TRF1 [40].TRF[8:8]	1
0xBB800404	L4_TRF1 [41].TRF[9:9]	1
0xBB800404	L4_TRF1 [42].TRF[10:10]	1
0xBB800404	L4_TRF1 [43].TRF[11:11]	1
0xBB800404	L4_TRF1 [44].TRF[12:12]	1
0xBB800404	L4_TRF1 [45].TRF[13:13]	1
0xBB800404	L4_TRF1 [46].TRF[14:14]	1
0xBB800404	L4_TRF1 [47].TRF[15:15]	1
0xBB800404	L4_TRF1 [48].TRF[16:16]	1
0xBB800404	L4_TRF1 [49].TRF[17:17]	1
0xBB800404	L4_TRF1 [50].TRF[18:18]	1
0xBB800404	L4_TRF1 [51].TRF[19:19]	1
0xBB800404	L4_TRF1 [52].TRF[20:20]	1
0xBB800404	L4_TRF1 [53].TRF[21:21]	1
0xBB800404	L4_TRF1 [54].TRF[22:22]	1
0xBB800404	L4_TRF1 [55].TRF[23:23]	1
0xBB800404	L4_TRF1 [56].TRF[24:24]	1
0xBB800404	L4_TRF1 [57].TRF[25:25]	1
0xBB800404	L4_TRF1 [58].TRF[26:26]	1
0xBB800404	L4_TRF1 [59].TRF[27:27]	1
0xBB800404	L4_TRF1 [60].TRF[28:28]	1
0xBB800404	L4_TRF1 [61].TRF[29:29]	1
0xBB800404	L4_TRF1 [62].TRF[30:30]	1
0xBB800404	L4_TRF1 [63].TRF[31:31]	1
0xBB800408	L4_TRF1 [64].TRF[0:0]	1
0xBB800408	L4_TRF1 [65].TRF[1:1]	1
0xBB800408	L4_TRF1 [66].TRF[2:2]	1
0xBB800408	L4_TRF1 [67].TRF[3:3]	1
0xBB800408	L4_TRF1 [68].TRF[4:4]	1
0xBB800408	L4_TRF1 [69].TRF[5:5]	1
0xBB800408	L4_TRF1 [70].TRF[6:6]	1
0xBB800408	L4_TRF1 [71].TRF[7:7]	1
0xBB800408	L4_TRF1 [72].TRF[8:8]	1
0xBB800408	L4_TRF1 [73].TRF[9:9]	1
0xBB800408	L4_TRF1 [74].TRF[10:10]	1
0xBB800408	L4_TRF1 [75].TRF[11:11]	1
0xBB800408	L4_TRF1 [76].TRF[12:12]	1
0xBB800408	L4_TRF1 [77].TRF[13:13]	1
0xBB800408	L4_TRF1 [78].TRF[14:14]	1
0xBB800408	L4_TRF1 [79].TRF[15:15]	1

Address	Register	Len
0xBB800408	L4_TRF1 [80].TRF[16:16]	1
0xBB800408	L4_TRF1 [81].TRF[17:17]	1
0xBB800408	L4_TRF1 [82].TRF[18:18]	1
0xBB800408	L4_TRF1 [83].TRF[19:19]	1
0xBB800408	L4_TRF1 [84].TRF[20:20]	1
0xBB800408	L4_TRF1 [85].TRF[21:21]	1
0xBB800408	L4_TRF1 [86].TRF[22:22]	1
0xBB800408	L4_TRF1 [87].TRF[23:23]	1
0xBB800408	L4_TRF1 [88].TRF[24:24]	1
0xBB800408	L4_TRF1 [89].TRF[25:25]	1
0xBB800408	L4_TRF1 [90].TRF[26:26]	1
0xBB800408	L4_TRF1 [91].TRF[27:27]	1
0xBB800408	L4_TRF1 [92].TRF[28:28]	1
0xBB800408	L4_TRF1 [93].TRF[29:29]	1
0xBB800408	L4_TRF1 [94].TRF[30:30]	1
0xBB800408	L4_TRF1 [95].TRF[31:31]	1
0xBB80040C	L4_TRF1 [96].TRF[0:0]	1
0xBB80040C	L4_TRF1 [97].TRF[1:1]	1
0xBB80040C	L4_TRF1 [98].TRF[2:2]	1
0xBB80040C	L4_TRF1 [99].TRF[3:3]	1
0xBB80040C	L4_TRF1 [100].TRF[4:4]	1
0xBB80040C	L4_TRF1 [101].TRF[5:5]	1
0xBB80040C	L4_TRF1 [102].TRF[6:6]	1
0xBB80040C	L4_TRF1 [103].TRF[7:7]	1
0xBB80040C	L4_TRF1 [104].TRF[8:8]	1
0xBB80040C	L4_TRF1 [105].TRF[9:9]	1
0xBB80040C	L4_TRF1 [106].TRF[10:10]	1
0xBB80040C	L4_TRF1 [107].TRF[11:11]	1
0xBB80040C	L4_TRF1 [108].TRF[12:12]	1
0xBB80040C	L4_TRF1 [109].TRF[13:13]	1
0xBB80040C	L4_TRF1 [110].TRF[14:14]	1
0xBB80040C	L4_TRF1 [111].TRF[15:15]	1
0xBB80040C	L4_TRF1 [112].TRF[16:16]	1
0xBB80040C	L4_TRF1 [113].TRF[17:17]	1
0xBB80040C	L4_TRF1 [114].TRF[18:18]	1
0xBB80040C	L4_TRF1 [115].TRF[19:19]	1
0xBB80040C	L4_TRF1 [116].TRF[20:20]	1
0xBB80040C	L4_TRF1 [117].TRF[21:21]	1
0xBB80040C	L4_TRF1 [118].TRF[22:22]	1
0xBB80040C	L4_TRF1 [119].TRF[23:23]	1
0xBB80040C	L4_TRF1 [120].TRF[24:24]	1
0xBB80040C	L4_TRF1 [121].TRF[25:25]	1
0xBB80040C	L4_TRF1 [122].TRF[26:26]	1
0xBB80040C	L4_TRF1 [123].TRF[27:27]	1
0xBB80040C	L4_TRF1 [124].TRF[28:28]	1
0xBB80040C	L4_TRF1 [125].TRF[29:29]	1

Address	Register	Len
0xBB80040C	L4_TRF1 [126].TRF[30:30]	1
0xBB80040C	L4_TRF1 [127].TRF[31:31]	1
0xBB800410	L4_TRF1 [128].TRF[0:0]	1
0xBB800410	L4_TRF1 [129].TRF[1:1]	1
0xBB800410	L4_TRF1 [130].TRF[2:2]	1
0xBB800410	L4_TRF1 [131].TRF[3:3]	1
0xBB800410	L4_TRF1 [132].TRF[4:4]	1
0xBB800410	L4_TRF1 [133].TRF[5:5]	1
0xBB800410	L4_TRF1 [134].TRF[6:6]	1
0xBB800410	L4_TRF1 [135].TRF[7:7]	1
0xBB800410	L4_TRF1 [136].TRF[8:8]	1
0xBB800410	L4_TRF1 [137].TRF[9:9]	1
0xBB800410	L4_TRF1 [138].TRF[10:10]	1
0xBB800410	L4_TRF1 [139].TRF[11:11]	1
0xBB800410	L4_TRF1 [140].TRF[12:12]	1
0xBB800410	L4_TRF1 [141].TRF[13:13]	1
0xBB800410	L4_TRF1 [142].TRF[14:14]	1
0xBB800410	L4_TRF1 [143].TRF[15:15]	1
0xBB800410	L4_TRF1 [144].TRF[16:16]	1
0xBB800410	L4_TRF1 [145].TRF[17:17]	1
0xBB800410	L4_TRF1 [146].TRF[18:18]	1
0xBB800410	L4_TRF1 [147].TRF[19:19]	1
0xBB800410	L4_TRF1 [148].TRF[20:20]	1
0xBB800410	L4_TRF1 [149].TRF[21:21]	1
0xBB800410	L4_TRF1 [150].TRF[22:22]	1
0xBB800410	L4_TRF1 [151].TRF[23:23]	1
0xBB800410	L4_TRF1 [152].TRF[24:24]	1
0xBB800410	L4_TRF1 [153].TRF[25:25]	1
0xBB800410	L4_TRF1 [154].TRF[26:26]	1
0xBB800410	L4_TRF1 [155].TRF[27:27]	1
0xBB800410	L4_TRF1 [156].TRF[28:28]	1
0xBB800410	L4_TRF1 [157].TRF[29:29]	1
0xBB800410	L4_TRF1 [158].TRF[30:30]	1
0xBB800410	L4_TRF1 [159].TRF[31:31]	1
0xBB800414	L4_TRF1 [160].TRF[0:0]	1
0xBB800414	L4_TRF1 [161].TRF[1:1]	1
0xBB800414	L4_TRF1 [162].TRF[2:2]	1
0xBB800414	L4_TRF1 [163].TRF[3:3]	1
0xBB800414	L4_TRF1 [164].TRF[4:4]	1
0xBB800414	L4_TRF1 [165].TRF[5:5]	1
0xBB800414	L4_TRF1 [166].TRF[6:6]	1
0xBB800414	L4_TRF1 [167].TRF[7:7]	1
0xBB800414	L4_TRF1 [168].TRF[8:8]	1
0xBB800414	L4_TRF1 [169].TRF[9:9]	1
0xBB800414	L4_TRF1 [170].TRF[10:10]	1
0xBB800414	L4_TRF1 [171].TRF[11:11]	1

Address	Register	Len
0xBB800414	L4_TRF1 [172].TRF[12:12]	1
0xBB800414	L4_TRF1 [173].TRF[13:13]	1
0xBB800414	L4_TRF1 [174].TRF[14:14]	1
0xBB800414	L4_TRF1 [175].TRF[15:15]	1
0xBB800414	L4_TRF1 [176].TRF[16:16]	1
0xBB800414	L4_TRF1 [177].TRF[17:17]	1
0xBB800414	L4_TRF1 [178].TRF[18:18]	1
0xBB800414	L4_TRF1 [179].TRF[19:19]	1
0xBB800414	L4_TRF1 [180].TRF[20:20]	1
0xBB800414	L4_TRF1 [181].TRF[21:21]	1
0xBB800414	L4_TRF1 [182].TRF[22:22]	1
0xBB800414	L4_TRF1 [183].TRF[23:23]	1
0xBB800414	L4_TRF1 [184].TRF[24:24]	1
0xBB800414	L4_TRF1 [185].TRF[25:25]	1
0xBB800414	L4_TRF1 [186].TRF[26:26]	1
0xBB800414	L4_TRF1 [187].TRF[27:27]	1
0xBB800414	L4_TRF1 [188].TRF[28:28]	1
0xBB800414	L4_TRF1 [189].TRF[29:29]	1
0xBB800414	L4_TRF1 [190].TRF[30:30]	1
0xBB800414	L4_TRF1 [191].TRF[31:31]	1
0xBB800418	L4_TRF1 [192].TRF[0:0]	1
0xBB800418	L4_TRF1 [193].TRF[1:1]	1
0xBB800418	L4_TRF1 [194].TRF[2:2]	1
0xBB800418	L4_TRF1 [195].TRF[3:3]	1
0xBB800418	L4_TRF1 [196].TRF[4:4]	1
0xBB800418	L4_TRF1 [197].TRF[5:5]	1
0xBB800418	L4_TRF1 [198].TRF[6:6]	1
0xBB800418	L4_TRF1 [199].TRF[7:7]	1
0xBB800418	L4_TRF1 [200].TRF[8:8]	1
0xBB800418	L4_TRF1 [201].TRF[9:9]	1
0xBB800418	L4_TRF1 [202].TRF[10:10]	1
0xBB800418	L4_TRF1 [203].TRF[11:11]	1
0xBB800418	L4_TRF1 [204].TRF[12:12]	1
0xBB800418	L4_TRF1 [205].TRF[13:13]	1
0xBB800418	L4_TRF1 [206].TRF[14:14]	1
0xBB800418	L4_TRF1 [207].TRF[15:15]	1
0xBB800418	L4_TRF1 [208].TRF[16:16]	1
0xBB800418	L4_TRF1 [209].TRF[17:17]	1
0xBB800418	L4_TRF1 [210].TRF[18:18]	1
0xBB800418	L4_TRF1 [211].TRF[19:19]	1
0xBB800418	L4_TRF1 [212].TRF[20:20]	1
0xBB800418	L4_TRF1 [213].TRF[21:21]	1
0xBB800418	L4_TRF1 [214].TRF[22:22]	1
0xBB800418	L4_TRF1 [215].TRF[23:23]	1
0xBB800418	L4_TRF1 [216].TRF[24:24]	1
0xBB800418	L4_TRF1 [217].TRF[25:25]	1

Address	Register	Len
0xBB800418	L4_TRF1 [218].TRF[26:26]	1
0xBB800418	L4_TRF1 [219].TRF[27:27]	1
0xBB800418	L4_TRF1 [220].TRF[28:28]	1
0xBB800418	L4_TRF1 [221].TRF[29:29]	1
0xBB800418	L4_TRF1 [222].TRF[30:30]	1
0xBB800418	L4_TRF1 [223].TRF[31:31]	1
0xBB80041C	L4_TRF1 [224].TRF[0:0]	1
0xBB80041C	L4_TRF1 [225].TRF[1:1]	1
0xBB80041C	L4_TRF1 [226].TRF[2:2]	1
0xBB80041C	L4_TRF1 [227].TRF[3:3]	1
0xBB80041C	L4_TRF1 [228].TRF[4:4]	1
0xBB80041C	L4_TRF1 [229].TRF[5:5]	1
0xBB80041C	L4_TRF1 [230].TRF[6:6]	1
0xBB80041C	L4_TRF1 [231].TRF[7:7]	1
0xBB80041C	L4_TRF1 [232].TRF[8:8]	1
0xBB80041C	L4_TRF1 [233].TRF[9:9]	1
0xBB80041C	L4_TRF1 [234].TRF[10:10]	1
0xBB80041C	L4_TRF1 [235].TRF[11:11]	1
0xBB80041C	L4_TRF1 [236].TRF[12:12]	1
0xBB80041C	L4_TRF1 [237].TRF[13:13]	1
0xBB80041C	L4_TRF1 [238].TRF[14:14]	1
0xBB80041C	L4_TRF1 [239].TRF[15:15]	1
0xBB80041C	L4_TRF1 [240].TRF[16:16]	1
0xBB80041C	L4_TRF1 [241].TRF[17:17]	1
0xBB80041C	L4_TRF1 [242].TRF[18:18]	1
0xBB80041C	L4_TRF1 [243].TRF[19:19]	1
0xBB80041C	L4_TRF1 [244].TRF[20:20]	1
0xBB80041C	L4_TRF1 [245].TRF[21:21]	1
0xBB80041C	L4_TRF1 [246].TRF[22:22]	1
0xBB80041C	L4_TRF1 [247].TRF[23:23]	1
0xBB80041C	L4_TRF1 [248].TRF[24:24]	1
0xBB80041C	L4_TRF1 [249].TRF[25:25]	1
0xBB80041C	L4_TRF1 [250].TRF[26:26]	1
0xBB80041C	L4_TRF1 [251].TRF[27:27]	1
0xBB80041C	L4_TRF1 [252].TRF[28:28]	1
0xBB80041C	L4_TRF1 [253].TRF[29:29]	1
0xBB80041C	L4_TRF1 [254].TRF[30:30]	1
0xBB80041C	L4_TRF1 [255].TRF[31:31]	1
0xBB800420	L4_TRF1 [256].TRF[0:0]	1
0xBB800420	L4_TRF1 [257].TRF[1:1]	1
0xBB800420	L4_TRF1 [258].TRF[2:2]	1
0xBB800420	L4_TRF1 [259].TRF[3:3]	1
0xBB800420	L4_TRF1 [260].TRF[4:4]	1
0xBB800420	L4_TRF1 [261].TRF[5:5]	1
0xBB800420	L4_TRF1 [262].TRF[6:6]	1
0xBB800420	L4_TRF1 [263].TRF[7:7]	1

Address	Register	Len
0xBB800420	L4_TRF1 [264].TRF[8:8]	1
0xBB800420	L4_TRF1 [265].TRF[9:9]	1
0xBB800420	L4_TRF1 [266].TRF[10:10]	1
0xBB800420	L4_TRF1 [267].TRF[11:11]	1
0xBB800420	L4_TRF1 [268].TRF[12:12]	1
0xBB800420	L4_TRF1 [269].TRF[13:13]	1
0xBB800420	L4_TRF1 [270].TRF[14:14]	1
0xBB800420	L4_TRF1 [271].TRF[15:15]	1
0xBB800420	L4_TRF1 [272].TRF[16:16]	1
0xBB800420	L4_TRF1 [273].TRF[17:17]	1
0xBB800420	L4_TRF1 [274].TRF[18:18]	1
0xBB800420	L4_TRF1 [275].TRF[19:19]	1
0xBB800420	L4_TRF1 [276].TRF[20:20]	1
0xBB800420	L4_TRF1 [277].TRF[21:21]	1
0xBB800420	L4_TRF1 [278].TRF[22:22]	1
0xBB800420	L4_TRF1 [279].TRF[23:23]	1
0xBB800420	L4_TRF1 [280].TRF[24:24]	1
0xBB800420	L4_TRF1 [281].TRF[25:25]	1
0xBB800420	L4_TRF1 [282].TRF[26:26]	1
0xBB800420	L4_TRF1 [283].TRF[27:27]	1
0xBB800420	L4_TRF1 [284].TRF[28:28]	1
0xBB800420	L4_TRF1 [285].TRF[29:29]	1
0xBB800420	L4_TRF1 [286].TRF[30:30]	1
0xBB800420	L4_TRF1 [287].TRF[31:31]	1
0xBB800424	L4_TRF1 [288].TRF[0:0]	1
0xBB800424	L4_TRF1 [289].TRF[1:1]	1
0xBB800424	L4_TRF1 [290].TRF[2:2]	1
0xBB800424	L4_TRF1 [291].TRF[3:3]	1
0xBB800424	L4_TRF1 [292].TRF[4:4]	1
0xBB800424	L4_TRF1 [293].TRF[5:5]	1
0xBB800424	L4_TRF1 [294].TRF[6:6]	1
0xBB800424	L4_TRF1 [295].TRF[7:7]	1
0xBB800424	L4_TRF1 [296].TRF[8:8]	1
0xBB800424	L4_TRF1 [297].TRF[9:9]	1
0xBB800424	L4_TRF1 [298].TRF[10:10]	1
0xBB800424	L4_TRF1 [299].TRF[11:11]	1
0xBB800424	L4_TRF1 [300].TRF[12:12]	1
0xBB800424	L4_TRF1 [301].TRF[13:13]	1
0xBB800424	L4_TRF1 [302].TRF[14:14]	1
0xBB800424	L4_TRF1 [303].TRF[15:15]	1
0xBB800424	L4_TRF1 [304].TRF[16:16]	1
0xBB800424	L4_TRF1 [305].TRF[17:17]	1
0xBB800424	L4_TRF1 [306].TRF[18:18]	1
0xBB800424	L4_TRF1 [307].TRF[19:19]	1
0xBB800424	L4_TRF1 [308].TRF[20:20]	1
0xBB800424	L4_TRF1 [309].TRF[21:21]	1

Address	Register	Len
0xBB800424	L4_TRF1 [310].TRF[22:22]	1
0xBB800424	L4_TRF1 [311].TRF[23:23]	1
0xBB800424	L4_TRF1 [312].TRF[24:24]	1
0xBB800424	L4_TRF1 [313].TRF[25:25]	1
0xBB800424	L4_TRF1 [314].TRF[26:26]	1
0xBB800424	L4_TRF1 [315].TRF[27:27]	1
0xBB800424	L4_TRF1 [316].TRF[28:28]	1
0xBB800424	L4_TRF1 [317].TRF[29:29]	1
0xBB800424	L4_TRF1 [318].TRF[30:30]	1
0xBB800424	L4_TRF1 [319].TRF[31:31]	1
0xBB800428	L4_TRF1 [320].TRF[0:0]	1
0xBB800428	L4_TRF1 [321].TRF[1:1]	1
0xBB800428	L4_TRF1 [322].TRF[2:2]	1
0xBB800428	L4_TRF1 [323].TRF[3:3]	1
0xBB800428	L4_TRF1 [324].TRF[4:4]	1
0xBB800428	L4_TRF1 [325].TRF[5:5]	1
0xBB800428	L4_TRF1 [326].TRF[6:6]	1
0xBB800428	L4_TRF1 [327].TRF[7:7]	1
0xBB800428	L4_TRF1 [328].TRF[8:8]	1
0xBB800428	L4_TRF1 [329].TRF[9:9]	1
0xBB800428	L4_TRF1 [330].TRF[10:10]	1
0xBB800428	L4_TRF1 [331].TRF[11:11]	1
0xBB800428	L4_TRF1 [332].TRF[12:12]	1
0xBB800428	L4_TRF1 [333].TRF[13:13]	1
0xBB800428	L4_TRF1 [334].TRF[14:14]	1
0xBB800428	L4_TRF1 [335].TRF[15:15]	1
0xBB800428	L4_TRF1 [336].TRF[16:16]	1
0xBB800428	L4_TRF1 [337].TRF[17:17]	1
0xBB800428	L4_TRF1 [338].TRF[18:18]	1
0xBB800428	L4_TRF1 [339].TRF[19:19]	1
0xBB800428	L4_TRF1 [340].TRF[20:20]	1
0xBB800428	L4_TRF1 [341].TRF[21:21]	1
0xBB800428	L4_TRF1 [342].TRF[22:22]	1
0xBB800428	L4_TRF1 [343].TRF[23:23]	1
0xBB800428	L4_TRF1 [344].TRF[24:24]	1
0xBB800428	L4_TRF1 [345].TRF[25:25]	1
0xBB800428	L4_TRF1 [346].TRF[26:26]	1
0xBB800428	L4_TRF1 [347].TRF[27:27]	1
0xBB800428	L4_TRF1 [348].TRF[28:28]	1
0xBB800428	L4_TRF1 [349].TRF[29:29]	1
0xBB800428	L4_TRF1 [350].TRF[30:30]	1
0xBB800428	L4_TRF1 [351].TRF[31:31]	1
0xBB80042C	L4_TRF1 [352].TRF[0:0]	1
0xBB80042C	L4_TRF1 [353].TRF[1:1]	1
0xBB80042C	L4_TRF1 [354].TRF[2:2]	1
0xBB80042C	L4_TRF1 [355].TRF[3:3]	1

Address	Register	Len
0xBB80042C	L4_TRF1 [356].TRF[4:4]	1
0xBB80042C	L4_TRF1 [357].TRF[5:5]	1
0xBB80042C	L4_TRF1 [358].TRF[6:6]	1
0xBB80042C	L4_TRF1 [359].TRF[7:7]	1
0xBB80042C	L4_TRF1 [360].TRF[8:8]	1
0xBB80042C	L4_TRF1 [361].TRF[9:9]	1
0xBB80042C	L4_TRF1 [362].TRF[10:10]	1
0xBB80042C	L4_TRF1 [363].TRF[11:11]	1
0xBB80042C	L4_TRF1 [364].TRF[12:12]	1
0xBB80042C	L4_TRF1 [365].TRF[13:13]	1
0xBB80042C	L4_TRF1 [366].TRF[14:14]	1
0xBB80042C	L4_TRF1 [367].TRF[15:15]	1
0xBB80042C	L4_TRF1 [368].TRF[16:16]	1
0xBB80042C	L4_TRF1 [369].TRF[17:17]	1
0xBB80042C	L4_TRF1 [370].TRF[18:18]	1
0xBB80042C	L4_TRF1 [371].TRF[19:19]	1
0xBB80042C	L4_TRF1 [372].TRF[20:20]	1
0xBB80042C	L4_TRF1 [373].TRF[21:21]	1
0xBB80042C	L4_TRF1 [374].TRF[22:22]	1
0xBB80042C	L4_TRF1 [375].TRF[23:23]	1
0xBB80042C	L4_TRF1 [376].TRF[24:24]	1
0xBB80042C	L4_TRF1 [377].TRF[25:25]	1
0xBB80042C	L4_TRF1 [378].TRF[26:26]	1
0xBB80042C	L4_TRF1 [379].TRF[27:27]	1
0xBB80042C	L4_TRF1 [380].TRF[28:28]	1
0xBB80042C	L4_TRF1 [381].TRF[29:29]	1
0xBB80042C	L4_TRF1 [382].TRF[30:30]	1
0xBB80042C	L4_TRF1 [383].TRF[31:31]	1
0xBB800430	L4_TRF1 [384].TRF[0:0]	1
0xBB800430	L4_TRF1 [385].TRF[1:1]	1
0xBB800430	L4_TRF1 [386].TRF[2:2]	1
0xBB800430	L4_TRF1 [387].TRF[3:3]	1
0xBB800430	L4_TRF1 [388].TRF[4:4]	1
0xBB800430	L4_TRF1 [389].TRF[5:5]	1
0xBB800430	L4_TRF1 [390].TRF[6:6]	1
0xBB800430	L4_TRF1 [391].TRF[7:7]	1
0xBB800430	L4_TRF1 [392].TRF[8:8]	1
0xBB800430	L4_TRF1 [393].TRF[9:9]	1
0xBB800430	L4_TRF1 [394].TRF[10:10]	1
0xBB800430	L4_TRF1 [395].TRF[11:11]	1
0xBB800430	L4_TRF1 [396].TRF[12:12]	1
0xBB800430	L4_TRF1 [397].TRF[13:13]	1
0xBB800430	L4_TRF1 [398].TRF[14:14]	1
0xBB800430	L4_TRF1 [399].TRF[15:15]	1
0xBB800430	L4_TRF1 [400].TRF[16:16]	1
0xBB800430	L4_TRF1 [401].TRF[17:17]	1



Address	Register	Len
0xBB800430	L4_TRF1 [402].TRF[18:18]	1
0xBB800430	L4_TRF1 [403].TRF[19:19]	1
0xBB800430	L4_TRF1 [404].TRF[20:20]	1
0xBB800430	L4_TRF1 [405].TRF[21:21]	1
0xBB800430	L4_TRF1 [406].TRF[22:22]	1
0xBB800430	L4_TRF1 [407].TRF[23:23]	1
0xBB800430	L4_TRF1 [408].TRF[24:24]	1
0xBB800430	L4_TRF1 [409].TRF[25:25]	1
0xBB800430	L4_TRF1 [410].TRF[26:26]	1
0xBB800430	L4_TRF1 [411].TRF[27:27]	1
0xBB800430	L4_TRF1 [412].TRF[28:28]	1
0xBB800430	L4_TRF1 [413].TRF[29:29]	1
0xBB800430	L4_TRF1 [414].TRF[30:30]	1
0xBB800430	L4_TRF1 [415].TRF[31:31]	1
0xBB800434	L4_TRF1 [416].TRF[0:0]	1
0xBB800434	L4_TRF1 [417].TRF[1:1]	1
0xBB800434	L4_TRF1 [418].TRF[2:2]	1
0xBB800434	L4_TRF1 [419].TRF[3:3]	1
0xBB800434	L4_TRF1 [420].TRF[4:4]	1
0xBB800434	L4_TRF1 [421].TRF[5:5]	1
0xBB800434	L4_TRF1 [422].TRF[6:6]	1
0xBB800434	L4_TRF1 [423].TRF[7:7]	1
0xBB800434	L4_TRF1 [424].TRF[8:8]	1
0xBB800434	L4_TRF1 [425].TRF[9:9]	1
0xBB800434	L4_TRF1 [426].TRF[10:10]	1
0xBB800434	L4_TRF1 [427].TRF[11:11]	1
0xBB800434	L4_TRF1 [428].TRF[12:12]	1
0xBB800434	L4_TRF1 [429].TRF[13:13]	1
0xBB800434	L4_TRF1 [430].TRF[14:14]	1
0xBB800434	L4_TRF1 [431].TRF[15:15]	1
0xBB800434	L4_TRF1 [432].TRF[16:16]	1
0xBB800434	L4_TRF1 [433].TRF[17:17]	1
0xBB800434	L4_TRF1 [434].TRF[18:18]	1
0xBB800434	L4_TRF1 [435].TRF[19:19]	1
0xBB800434	L4_TRF1 [436].TRF[20:20]	1
0xBB800434	L4_TRF1 [437].TRF[21:21]	1
0xBB800434	L4_TRF1 [438].TRF[22:22]	1
0xBB800434	L4_TRF1 [439].TRF[23:23]	1
0xBB800434	L4_TRF1 [440].TRF[24:24]	1
0xBB800434	L4_TRF1 [441].TRF[25:25]	1
0xBB800434	L4_TRF1 [442].TRF[26:26]	1
0xBB800434	L4_TRF1 [443].TRF[27:27]	1
0xBB800434	L4_TRF1 [444].TRF[28:28]	1
0xBB800434	L4_TRF1 [445].TRF[29:29]	1
0xBB800434	L4_TRF1 [446].TRF[30:30]	1
0xBB800434	L4_TRF1 [447].TRF[31:31]	1

Address	Register	Len
0xBB800438	L4_TRF1 [448].TRF[0:0]	1
0xBB800438	L4_TRF1 [449].TRF[1:1]	1
0xBB800438	L4_TRF1 [450].TRF[2:2]	1
0xBB800438	L4_TRF1 [451].TRF[3:3]	1
0xBB800438	L4_TRF1 [452].TRF[4:4]	1
0xBB800438	L4_TRF1 [453].TRF[5:5]	1
0xBB800438	L4_TRF1 [454].TRF[6:6]	1
0xBB800438	L4_TRF1 [455].TRF[7:7]	1
0xBB800438	L4_TRF1 [456].TRF[8:8]	1
0xBB800438	L4_TRF1 [457].TRF[9:9]	1
0xBB800438	L4_TRF1 [458].TRF[10:10]	1
0xBB800438	L4_TRF1 [459].TRF[11:11]	1
0xBB800438	L4_TRF1 [460].TRF[12:12]	1
0xBB800438	L4_TRF1 [461].TRF[13:13]	1
0xBB800438	L4_TRF1 [462].TRF[14:14]	1
0xBB800438	L4_TRF1 [463].TRF[15:15]	1
0xBB800438	L4_TRF1 [464].TRF[16:16]	1
0xBB800438	L4_TRF1 [465].TRF[17:17]	1
0xBB800438	L4_TRF1 [466].TRF[18:18]	1
0xBB800438	L4_TRF1 [467].TRF[19:19]	1
0xBB800438	L4_TRF1 [468].TRF[20:20]	1
0xBB800438	L4_TRF1 [469].TRF[21:21]	1
0xBB800438	L4_TRF1 [470].TRF[22:22]	1
0xBB800438	L4_TRF1 [471].TRF[23:23]	1
0xBB800438	L4_TRF1 [472].TRF[24:24]	1
0xBB800438	L4_TRF1 [473].TRF[25:25]	1
0xBB800438	L4_TRF1 [474].TRF[26:26]	1
0xBB800438	L4_TRF1 [475].TRF[27:27]	1
0xBB800438	L4_TRF1 [476].TRF[28:28]	1
0xBB800438	L4_TRF1 [477].TRF[29:29]	1
0xBB800438	L4_TRF1 [478].TRF[30:30]	1
0xBB800438	L4_TRF1 [479].TRF[31:31]	1
0xBB80043C	L4_TRF1 [480].TRF[0:0]	1
0xBB80043C	L4_TRF1 [481].TRF[1:1]	1
0xBB80043C	L4_TRF1 [482].TRF[2:2]	1
0xBB80043C	L4_TRF1 [483].TRF[3:3]	1
0xBB80043C	L4_TRF1 [484].TRF[4:4]	1
0xBB80043C	L4_TRF1 [485].TRF[5:5]	1
0xBB80043C	L4_TRF1 [486].TRF[6:6]	1
0xBB80043C	L4_TRF1 [487].TRF[7:7]	1
0xBB80043C	L4_TRF1 [488].TRF[8:8]	1
0xBB80043C	L4_TRF1 [489].TRF[9:9]	1
0xBB80043C	L4_TRF1 [490].TRF[10:10]	1
0xBB80043C	L4_TRF1 [491].TRF[11:11]	1
0xBB80043C	L4_TRF1 [492].TRF[12:12]	1
0xBB80043C	L4_TRF1 [493].TRF[13:13]	1

Address	Register	Len
0xBB80043C	L4_TRF1 [494].TRF[14:14]	1
0xBB80043C	L4_TRF1 [495].TRF[15:15]	1
0xBB80043C	L4_TRF1 [496].TRF[16:16]	1
0xBB80043C	L4_TRF1 [497].TRF[17:17]	1
0xBB80043C	L4_TRF1 [498].TRF[18:18]	1
0xBB80043C	L4_TRF1 [499].TRF[19:19]	1
0xBB80043C	L4_TRF1 [500].TRF[20:20]	1
0xBB80043C	L4_TRF1 [501].TRF[21:21]	1
0xBB80043C	L4_TRF1 [502].TRF[22:22]	1
0xBB80043C	L4_TRF1 [503].TRF[23:23]	1
0xBB80043C	L4_TRF1 [504].TRF[24:24]	1
0xBB80043C	L4_TRF1 [505].TRF[25:25]	1
0xBB80043C	L4_TRF1 [506].TRF[26:26]	1
0xBB80043C	L4_TRF1 [507].TRF[27:27]	1
0xBB80043C	L4_TRF1 [508].TRF[28:28]	1
0xBB80043C	L4_TRF1 [509].TRF[29:29]	1
0xBB80043C	L4_TRF1 [510].TRF[30:30]	1
0xBB80043C	L4_TRF1 [511].TRF[31:31]	1
0xBB800440	L4_TRF1 [512].TRF[0:0]	1
0xBB800440	L4_TRF1 [513].TRF[1:1]	1
0xBB800440	L4_TRF1 [514].TRF[2:2]	1
0xBB800440	L4_TRF1 [515].TRF[3:3]	1
0xBB800440	L4_TRF1 [516].TRF[4:4]	1
0xBB800440	L4_TRF1 [517].TRF[5:5]	1
0xBB800440	L4_TRF1 [518].TRF[6:6]	1
0xBB800440	L4_TRF1 [519].TRF[7:7]	1
0xBB800440	L4_TRF1 [520].TRF[8:8]	1
0xBB800440	L4_TRF1 [521].TRF[9:9]	1
0xBB800440	L4_TRF1 [522].TRF[10:10]	1
0xBB800440	L4_TRF1 [523].TRF[11:11]	1
0xBB800440	L4_TRF1 [524].TRF[12:12]	1
0xBB800440	L4_TRF1 [525].TRF[13:13]	1
0xBB800440	L4_TRF1 [526].TRF[14:14]	1
0xBB800440	L4_TRF1 [527].TRF[15:15]	1
0xBB800440	L4_TRF1 [528].TRF[16:16]	1
0xBB800440	L4_TRF1 [529].TRF[17:17]	1
0xBB800440	L4_TRF1 [530].TRF[18:18]	1
0xBB800440	L4_TRF1 [531].TRF[19:19]	1
0xBB800440	L4_TRF1 [532].TRF[20:20]	1
0xBB800440	L4_TRF1 [533].TRF[21:21]	1
0xBB800440	L4_TRF1 [534].TRF[22:22]	1
0xBB800440	L4_TRF1 [535].TRF[23:23]	1
0xBB800440	L4_TRF1 [536].TRF[24:24]	1
0xBB800440	L4_TRF1 [537].TRF[25:25]	1
0xBB800440	L4_TRF1 [538].TRF[26:26]	1
0xBB800440	L4_TRF1 [539].TRF[27:27]	1

Address	Register	Len
0xBB800440	L4_TRF1 [540].TRF[28:28]	1
0xBB800440	L4_TRF1 [541].TRF[29:29]	1
0xBB800440	L4_TRF1 [542].TRF[30:30]	1
0xBB800440	L4_TRF1 [543].TRF[31:31]	1
0xBB800444	L4_TRF1 [544].TRF[0:0]	1
0xBB800444	L4_TRF1 [545].TRF[1:1]	1
0xBB800444	L4_TRF1 [546].TRF[2:2]	1
0xBB800444	L4_TRF1 [547].TRF[3:3]	1
0xBB800444	L4_TRF1 [548].TRF[4:4]	1
0xBB800444	L4_TRF1 [549].TRF[5:5]	1
0xBB800444	L4_TRF1 [550].TRF[6:6]	1
0xBB800444	L4_TRF1 [551].TRF[7:7]	1
0xBB800444	L4_TRF1 [552].TRF[8:8]	1
0xBB800444	L4_TRF1 [553].TRF[9:9]	1
0xBB800444	L4_TRF1 [554].TRF[10:10]	1
0xBB800444	L4_TRF1 [555].TRF[11:11]	1
0xBB800444	L4_TRF1 [556].TRF[12:12]	1
0xBB800444	L4_TRF1 [557].TRF[13:13]	1
0xBB800444	L4_TRF1 [558].TRF[14:14]	1
0xBB800444	L4_TRF1 [559].TRF[15:15]	1
0xBB800444	L4_TRF1 [560].TRF[16:16]	1
0xBB800444	L4_TRF1 [561].TRF[17:17]	1
0xBB800444	L4_TRF1 [562].TRF[18:18]	1
0xBB800444	L4_TRF1 [563].TRF[19:19]	1
0xBB800444	L4_TRF1 [564].TRF[20:20]	1
0xBB800444	L4_TRF1 [565].TRF[21:21]	1
0xBB800444	L4_TRF1 [566].TRF[22:22]	1
0xBB800444	L4_TRF1 [567].TRF[23:23]	1
0xBB800444	L4_TRF1 [568].TRF[24:24]	1
0xBB800444	L4_TRF1 [569].TRF[25:25]	1
0xBB800444	L4_TRF1 [570].TRF[26:26]	1
0xBB800444	L4_TRF1 [571].TRF[27:27]	1
0xBB800444	L4_TRF1 [572].TRF[28:28]	1
0xBB800444	L4_TRF1 [573].TRF[29:29]	1
0xBB800444	L4_TRF1 [574].TRF[30:30]	1
0xBB800444	L4_TRF1 [575].TRF[31:31]	1
0xBB800448	L4_TRF1 [576].TRF[0:0]	1
0xBB800448	L4_TRF1 [577].TRF[1:1]	1
0xBB800448	L4_TRF1 [578].TRF[2:2]	1
0xBB800448	L4_TRF1 [579].TRF[3:3]	1
0xBB800448	L4_TRF1 [580].TRF[4:4]	1
0xBB800448	L4_TRF1 [581].TRF[5:5]	1
0xBB800448	L4_TRF1 [582].TRF[6:6]	1
0xBB800448	L4_TRF1 [583].TRF[7:7]	1
0xBB800448	L4_TRF1 [584].TRF[8:8]	1
0xBB800448	L4_TRF1 [585].TRF[9:9]	1

Address	Register	Len
0xBB800448	L4_TRF1 [586].TRF[10:10]	1
0xBB800448	L4_TRF1 [587].TRF[11:11]	1
0xBB800448	L4_TRF1 [588].TRF[12:12]	1
0xBB800448	L4_TRF1 [589].TRF[13:13]	1
0xBB800448	L4_TRF1 [590].TRF[14:14]	1
0xBB800448	L4_TRF1 [591].TRF[15:15]	1
0xBB800448	L4_TRF1 [592].TRF[16:16]	1
0xBB800448	L4_TRF1 [593].TRF[17:17]	1
0xBB800448	L4_TRF1 [594].TRF[18:18]	1
0xBB800448	L4_TRF1 [595].TRF[19:19]	1
0xBB800448	L4_TRF1 [596].TRF[20:20]	1
0xBB800448	L4_TRF1 [597].TRF[21:21]	1
0xBB800448	L4_TRF1 [598].TRF[22:22]	1
0xBB800448	L4_TRF1 [599].TRF[23:23]	1
0xBB800448	L4_TRF1 [600].TRF[24:24]	1
0xBB800448	L4_TRF1 [601].TRF[25:25]	1
0xBB800448	L4_TRF1 [602].TRF[26:26]	1
0xBB800448	L4_TRF1 [603].TRF[27:27]	1
0xBB800448	L4_TRF1 [604].TRF[28:28]	1
0xBB800448	L4_TRF1 [605].TRF[29:29]	1
0xBB800448	L4_TRF1 [606].TRF[30:30]	1
0xBB800448	L4_TRF1 [607].TRF[31:31]	1
0xBB80044C	L4_TRF1 [608].TRF[0:0]	1
0xBB80044C	L4_TRF1 [609].TRF[1:1]	1
0xBB80044C	L4_TRF1 [610].TRF[2:2]	1
0xBB80044C	L4_TRF1 [611].TRF[3:3]	1
0xBB80044C	L4_TRF1 [612].TRF[4:4]	1
0xBB80044C	L4_TRF1 [613].TRF[5:5]	1
0xBB80044C	L4_TRF1 [614].TRF[6:6]	1
0xBB80044C	L4_TRF1 [615].TRF[7:7]	1
0xBB80044C	L4_TRF1 [616].TRF[8:8]	1
0xBB80044C	L4_TRF1 [617].TRF[9:9]	1
0xBB80044C	L4_TRF1 [618].TRF[10:10]	1
0xBB80044C	L4_TRF1 [619].TRF[11:11]	1
0xBB80044C	L4_TRF1 [620].TRF[12:12]	1
0xBB80044C	L4_TRF1 [621].TRF[13:13]	1
0xBB80044C	L4_TRF1 [622].TRF[14:14]	1
0xBB80044C	L4_TRF1 [623].TRF[15:15]	1
0xBB80044C	L4_TRF1 [624].TRF[16:16]	1
0xBB80044C	L4_TRF1 [625].TRF[17:17]	1
0xBB80044C	L4_TRF1 [626].TRF[18:18]	1
0xBB80044C	L4_TRF1 [627].TRF[19:19]	1
0xBB80044C	L4_TRF1 [628].TRF[20:20]	1
0xBB80044C	L4_TRF1 [629].TRF[21:21]	1
0xBB80044C	L4_TRF1 [630].TRF[22:22]	1
0xBB80044C	L4_TRF1 [631].TRF[23:23]	1

Address	Register	Len
0xBB80044C	L4_TRF1 [632].TRF[24:24]	1
0xBB80044C	L4_TRF1 [633].TRF[25:25]	1
0xBB80044C	L4_TRF1 [634].TRF[26:26]	1
0xBB80044C	L4_TRF1 [635].TRF[27:27]	1
0xBB80044C	L4_TRF1 [636].TRF[28:28]	1
0xBB80044C	L4_TRF1 [637].TRF[29:29]	1
0xBB80044C	L4_TRF1 [638].TRF[30:30]	1
0xBB80044C	L4_TRF1 [639].TRF[31:31]	1
0xBB800450	L4_TRF1 [640].TRF[0:0]	1
0xBB800450	L4_TRF1 [641].TRF[1:1]	1
0xBB800450	L4_TRF1 [642].TRF[2:2]	1
0xBB800450	L4_TRF1 [643].TRF[3:3]	1
0xBB800450	L4_TRF1 [644].TRF[4:4]	1
0xBB800450	L4_TRF1 [645].TRF[5:5]	1
0xBB800450	L4_TRF1 [646].TRF[6:6]	1
0xBB800450	L4_TRF1 [647].TRF[7:7]	1
0xBB800450	L4_TRF1 [648].TRF[8:8]	1
0xBB800450	L4_TRF1 [649].TRF[9:9]	1
0xBB800450	L4_TRF1 [650].TRF[10:10]	1
0xBB800450	L4_TRF1 [651].TRF[11:11]	1
0xBB800450	L4_TRF1 [652].TRF[12:12]	1
0xBB800450	L4_TRF1 [653].TRF[13:13]	1
0xBB800450	L4_TRF1 [654].TRF[14:14]	1
0xBB800450	L4_TRF1 [655].TRF[15:15]	1
0xBB800450	L4_TRF1 [656].TRF[16:16]	1
0xBB800450	L4_TRF1 [657].TRF[17:17]	1
0xBB800450	L4_TRF1 [658].TRF[18:18]	1
0xBB800450	L4_TRF1 [659].TRF[19:19]	1
0xBB800450	L4_TRF1 [660].TRF[20:20]	1
0xBB800450	L4_TRF1 [661].TRF[21:21]	1
0xBB800450	L4_TRF1 [662].TRF[22:22]	1
0xBB800450	L4_TRF1 [663].TRF[23:23]	1
0xBB800450	L4_TRF1 [664].TRF[24:24]	1
0xBB800450	L4_TRF1 [665].TRF[25:25]	1
0xBB800450	L4_TRF1 [666].TRF[26:26]	1
0xBB800450	L4_TRF1 [667].TRF[27:27]	1
0xBB800450	L4_TRF1 [668].TRF[28:28]	1
0xBB800450	L4_TRF1 [669].TRF[29:29]	1
0xBB800450	L4_TRF1 [670].TRF[30:30]	1
0xBB800450	L4_TRF1 [671].TRF[31:31]	1
0xBB800454	L4_TRF1 [672].TRF[0:0]	1
0xBB800454	L4_TRF1 [673].TRF[1:1]	1
0xBB800454	L4_TRF1 [674].TRF[2:2]	1
0xBB800454	L4_TRF1 [675].TRF[3:3]	1
0xBB800454	L4_TRF1 [676].TRF[4:4]	1
0xBB800454	L4_TRF1 [677].TRF[5:5]	1

Address	Register	Len
0xBB800454	L4_TRF1 [678].TRF[6:6]	1
0xBB800454	L4_TRF1 [679].TRF[7:7]	1
0xBB800454	L4_TRF1 [680].TRF[8:8]	1
0xBB800454	L4_TRF1 [681].TRF[9:9]	1
0xBB800454	L4_TRF1 [682].TRF[10:10]	1
0xBB800454	L4_TRF1 [683].TRF[11:11]	1
0xBB800454	L4_TRF1 [684].TRF[12:12]	1
0xBB800454	L4_TRF1 [685].TRF[13:13]	1
0xBB800454	L4_TRF1 [686].TRF[14:14]	1
0xBB800454	L4_TRF1 [687].TRF[15:15]	1
0xBB800454	L4_TRF1 [688].TRF[16:16]	1
0xBB800454	L4_TRF1 [689].TRF[17:17]	1
0xBB800454	L4_TRF1 [690].TRF[18:18]	1
0xBB800454	L4_TRF1 [691].TRF[19:19]	1
0xBB800454	L4_TRF1 [692].TRF[20:20]	1
0xBB800454	L4_TRF1 [693].TRF[21:21]	1
0xBB800454	L4_TRF1 [694].TRF[22:22]	1
0xBB800454	L4_TRF1 [695].TRF[23:23]	1
0xBB800454	L4_TRF1 [696].TRF[24:24]	1
0xBB800454	L4_TRF1 [697].TRF[25:25]	1
0xBB800454	L4_TRF1 [698].TRF[26:26]	1
0xBB800454	L4_TRF1 [699].TRF[27:27]	1
0xBB800454	L4_TRF1 [700].TRF[28:28]	1
0xBB800454	L4_TRF1 [701].TRF[29:29]	1
0xBB800454	L4_TRF1 [702].TRF[30:30]	1
0xBB800454	L4_TRF1 [703].TRF[31:31]	1
0xBB800458	L4_TRF1 [704].TRF[0:0]	1
0xBB800458	L4_TRF1 [705].TRF[1:1]	1
0xBB800458	L4_TRF1 [706].TRF[2:2]	1
0xBB800458	L4_TRF1 [707].TRF[3:3]	1
0xBB800458	L4_TRF1 [708].TRF[4:4]	1
0xBB800458	L4_TRF1 [709].TRF[5:5]	1
0xBB800458	L4_TRF1 [710].TRF[6:6]	1
0xBB800458	L4_TRF1 [711].TRF[7:7]	1
0xBB800458	L4_TRF1 [712].TRF[8:8]	1
0xBB800458	L4_TRF1 [713].TRF[9:9]	1
0xBB800458	L4_TRF1 [714].TRF[10:10]	1
0xBB800458	L4_TRF1 [715].TRF[11:11]	1
0xBB800458	L4_TRF1 [716].TRF[12:12]	1
0xBB800458	L4_TRF1 [717].TRF[13:13]	1
0xBB800458	L4_TRF1 [718].TRF[14:14]	1
0xBB800458	L4_TRF1 [719].TRF[15:15]	1
0xBB800458	L4_TRF1 [720].TRF[16:16]	1
0xBB800458	L4_TRF1 [721].TRF[17:17]	1
0xBB800458	L4_TRF1 [722].TRF[18:18]	1
0xBB800458	L4_TRF1 [723].TRF[19:19]	1

Address	Register	Len
0xBB800458	L4_TRF1 [724].TRF[20:20]	1
0xBB800458	L4_TRF1 [725].TRF[21:21]	1
0xBB800458	L4_TRF1 [726].TRF[22:22]	1
0xBB800458	L4_TRF1 [727].TRF[23:23]	1
0xBB800458	L4_TRF1 [728].TRF[24:24]	1
0xBB800458	L4_TRF1 [729].TRF[25:25]	1
0xBB800458	L4_TRF1 [730].TRF[26:26]	1
0xBB800458	L4_TRF1 [731].TRF[27:27]	1
0xBB800458	L4_TRF1 [732].TRF[28:28]	1
0xBB800458	L4_TRF1 [733].TRF[29:29]	1
0xBB800458	L4_TRF1 [734].TRF[30:30]	1
0xBB800458	L4_TRF1 [735].TRF[31:31]	1
0xBB80045C	L4_TRF1 [736].TRF[0:0]	1
0xBB80045C	L4_TRF1 [737].TRF[1:1]	1
0xBB80045C	L4_TRF1 [738].TRF[2:2]	1
0xBB80045C	L4_TRF1 [739].TRF[3:3]	1
0xBB80045C	L4_TRF1 [740].TRF[4:4]	1
0xBB80045C	L4_TRF1 [741].TRF[5:5]	1
0xBB80045C	L4_TRF1 [742].TRF[6:6]	1
0xBB80045C	L4_TRF1 [743].TRF[7:7]	1
0xBB80045C	L4_TRF1 [744].TRF[8:8]	1
0xBB80045C	L4_TRF1 [745].TRF[9:9]	1
0xBB80045C	L4_TRF1 [746].TRF[10:10]	1
0xBB80045C	L4_TRF1 [747].TRF[11:11]	1
0xBB80045C	L4_TRF1 [748].TRF[12:12]	1
0xBB80045C	L4_TRF1 [749].TRF[13:13]	1
0xBB80045C	L4_TRF1 [750].TRF[14:14]	1
0xBB80045C	L4_TRF1 [751].TRF[15:15]	1
0xBB80045C	L4_TRF1 [752].TRF[16:16]	1
0xBB80045C	L4_TRF1 [753].TRF[17:17]	1
0xBB80045C	L4_TRF1 [754].TRF[18:18]	1
0xBB80045C	L4_TRF1 [755].TRF[19:19]	1
0xBB80045C	L4_TRF1 [756].TRF[20:20]	1
0xBB80045C	L4_TRF1 [757].TRF[21:21]	1
0xBB80045C	L4_TRF1 [758].TRF[22:22]	1
0xBB80045C	L4_TRF1 [759].TRF[23:23]	1
0xBB80045C	L4_TRF1 [760].TRF[24:24]	1
0xBB80045C	L4_TRF1 [761].TRF[25:25]	1
0xBB80045C	L4_TRF1 [762].TRF[26:26]	1
0xBB80045C	L4_TRF1 [763].TRF[27:27]	1
0xBB80045C	L4_TRF1 [764].TRF[28:28]	1
0xBB80045C	L4_TRF1 [765].TRF[29:29]	1
0xBB80045C	L4_TRF1 [766].TRF[30:30]	1
0xBB80045C	L4_TRF1 [767].TRF[31:31]	1
0xBB800460	L4_TRF1 [768].TRF[0:0]	1
0xBB800460	L4_TRF1 [769].TRF[1:1]	1



Address	Register	Len
0xBB800460	L4_TRF1 [770].TRF[2:2]	1
0xBB800460	L4_TRF1 [771].TRF[3:3]	1
0xBB800460	L4_TRF1 [772].TRF[4:4]	1
0xBB800460	L4_TRF1 [773].TRF[5:5]	1
0xBB800460	L4_TRF1 [774].TRF[6:6]	1
0xBB800460	L4_TRF1 [775].TRF[7:7]	1
0xBB800460	L4_TRF1 [776].TRF[8:8]	1
0xBB800460	L4_TRF1 [777].TRF[9:9]	1
0xBB800460	L4_TRF1 [778].TRF[10:10]	1
0xBB800460	L4_TRF1 [779].TRF[11:11]	1
0xBB800460	L4_TRF1 [780].TRF[12:12]	1
0xBB800460	L4_TRF1 [781].TRF[13:13]	1
0xBB800460	L4_TRF1 [782].TRF[14:14]	1
0xBB800460	L4_TRF1 [783].TRF[15:15]	1
0xBB800460	L4_TRF1 [784].TRF[16:16]	1
0xBB800460	L4_TRF1 [785].TRF[17:17]	1
0xBB800460	L4_TRF1 [786].TRF[18:18]	1
0xBB800460	L4_TRF1 [787].TRF[19:19]	1
0xBB800460	L4_TRF1 [788].TRF[20:20]	1
0xBB800460	L4_TRF1 [789].TRF[21:21]	1
0xBB800460	L4_TRF1 [790].TRF[22:22]	1
0xBB800460	L4_TRF1 [791].TRF[23:23]	1
0xBB800460	L4_TRF1 [792].TRF[24:24]	1
0xBB800460	L4_TRF1 [793].TRF[25:25]	1
0xBB800460	L4_TRF1 [794].TRF[26:26]	1
0xBB800460	L4_TRF1 [795].TRF[27:27]	1
0xBB800460	L4_TRF1 [796].TRF[28:28]	1
0xBB800460	L4_TRF1 [797].TRF[29:29]	1
0xBB800460	L4_TRF1 [798].TRF[30:30]	1
0xBB800460	L4_TRF1 [799].TRF[31:31]	1
0xBB800464	L4_TRF1 [800].TRF[0:0]	1
0xBB800464	L4_TRF1 [801].TRF[1:1]	1
0xBB800464	L4_TRF1 [802].TRF[2:2]	1
0xBB800464	L4_TRF1 [803].TRF[3:3]	1
0xBB800464	L4_TRF1 [804].TRF[4:4]	1
0xBB800464	L4_TRF1 [805].TRF[5:5]	1
0xBB800464	L4_TRF1 [806].TRF[6:6]	1
0xBB800464	L4_TRF1 [807].TRF[7:7]	1
0xBB800464	L4_TRF1 [808].TRF[8:8]	1
0xBB800464	L4_TRF1 [809].TRF[9:9]	1
0xBB800464	L4_TRF1 [810].TRF[10:10]	1
0xBB800464	L4_TRF1 [811].TRF[11:11]	1
0xBB800464	L4_TRF1 [812].TRF[12:12]	1
0xBB800464	L4_TRF1 [813].TRF[13:13]	1
0xBB800464	L4_TRF1 [814].TRF[14:14]	1
0xBB800464	L4_TRF1 [815].TRF[15:15]	1

Address	Register	Len
0xBB800464	L4_TRF1 [816].TRF[16:16]	1
0xBB800464	L4_TRF1 [817].TRF[17:17]	1
0xBB800464	L4_TRF1 [818].TRF[18:18]	1
0xBB800464	L4_TRF1 [819].TRF[19:19]	1
0xBB800464	L4_TRF1 [820].TRF[20:20]	1
0xBB800464	L4_TRF1 [821].TRF[21:21]	1
0xBB800464	L4_TRF1 [822].TRF[22:22]	1
0xBB800464	L4_TRF1 [823].TRF[23:23]	1
0xBB800464	L4_TRF1 [824].TRF[24:24]	1
0xBB800464	L4_TRF1 [825].TRF[25:25]	1
0xBB800464	L4_TRF1 [826].TRF[26:26]	1
0xBB800464	L4_TRF1 [827].TRF[27:27]	1
0xBB800464	L4_TRF1 [828].TRF[28:28]	1
0xBB800464	L4_TRF1 [829].TRF[29:29]	1
0xBB800464	L4_TRF1 [830].TRF[30:30]	1
0xBB800464	L4_TRF1 [831].TRF[31:31]	1
0xBB800468	L4_TRF1 [832].TRF[0:0]	1
0xBB800468	L4_TRF1 [833].TRF[1:1]	1
0xBB800468	L4_TRF1 [834].TRF[2:2]	1
0xBB800468	L4_TRF1 [835].TRF[3:3]	1
0xBB800468	L4_TRF1 [836].TRF[4:4]	1
0xBB800468	L4_TRF1 [837].TRF[5:5]	1
0xBB800468	L4_TRF1 [838].TRF[6:6]	1
0xBB800468	L4_TRF1 [839].TRF[7:7]	1
0xBB800468	L4_TRF1 [840].TRF[8:8]	1
0xBB800468	L4_TRF1 [841].TRF[9:9]	1
0xBB800468	L4_TRF1 [842].TRF[10:10]	1
0xBB800468	L4_TRF1 [843].TRF[11:11]	1
0xBB800468	L4_TRF1 [844].TRF[12:12]	1
0xBB800468	L4_TRF1 [845].TRF[13:13]	1
0xBB800468	L4_TRF1 [846].TRF[14:14]	1
0xBB800468	L4_TRF1 [847].TRF[15:15]	1
0xBB800468	L4_TRF1 [848].TRF[16:16]	1
0xBB800468	L4_TRF1 [849].TRF[17:17]	1
0xBB800468	L4_TRF1 [850].TRF[18:18]	1
0xBB800468	L4_TRF1 [851].TRF[19:19]	1
0xBB800468	L4_TRF1 [852].TRF[20:20]	1
0xBB800468	L4_TRF1 [853].TRF[21:21]	1
0xBB800468	L4_TRF1 [854].TRF[22:22]	1
0xBB800468	L4_TRF1 [855].TRF[23:23]	1
0xBB800468	L4_TRF1 [856].TRF[24:24]	1
0xBB800468	L4_TRF1 [857].TRF[25:25]	1
0xBB800468	L4_TRF1 [858].TRF[26:26]	1
0xBB800468	L4_TRF1 [859].TRF[27:27]	1
0xBB800468	L4_TRF1 [860].TRF[28:28]	1
0xBB800468	L4_TRF1 [861].TRF[29:29]	1

Address	Register	Len
0xBB800468	L4_TRF1 [862].TRF[30:30]	1
0xBB800468	L4_TRF1 [863].TRF[31:31]	1
0xBB80046C	L4_TRF1 [864].TRF[0:0]	1
0xBB80046C	L4_TRF1 [865].TRF[1:1]	1
0xBB80046C	L4_TRF1 [866].TRF[2:2]	1
0xBB80046C	L4_TRF1 [867].TRF[3:3]	1
0xBB80046C	L4_TRF1 [868].TRF[4:4]	1
0xBB80046C	L4_TRF1 [869].TRF[5:5]	1
0xBB80046C	L4_TRF1 [870].TRF[6:6]	1
0xBB80046C	L4_TRF1 [871].TRF[7:7]	1
0xBB80046C	L4_TRF1 [872].TRF[8:8]	1
0xBB80046C	L4_TRF1 [873].TRF[9:9]	1
0xBB80046C	L4_TRF1 [874].TRF[10:10]	1
0xBB80046C	L4_TRF1 [875].TRF[11:11]	1
0xBB80046C	L4_TRF1 [876].TRF[12:12]	1
0xBB80046C	L4_TRF1 [877].TRF[13:13]	1
0xBB80046C	L4_TRF1 [878].TRF[14:14]	1
0xBB80046C	L4_TRF1 [879].TRF[15:15]	1
0xBB80046C	L4_TRF1 [880].TRF[16:16]	1
0xBB80046C	L4_TRF1 [881].TRF[17:17]	1
0xBB80046C	L4_TRF1 [882].TRF[18:18]	1
0xBB80046C	L4_TRF1 [883].TRF[19:19]	1
0xBB80046C	L4_TRF1 [884].TRF[20:20]	1
0xBB80046C	L4_TRF1 [885].TRF[21:21]	1
0xBB80046C	L4_TRF1 [886].TRF[22:22]	1
0xBB80046C	L4_TRF1 [887].TRF[23:23]	1
0xBB80046C	L4_TRF1 [888].TRF[24:24]	1
0xBB80046C	L4_TRF1 [889].TRF[25:25]	1
0xBB80046C	L4_TRF1 [890].TRF[26:26]	1
0xBB80046C	L4_TRF1 [891].TRF[27:27]	1
0xBB80046C	L4_TRF1 [892].TRF[28:28]	1
0xBB80046C	L4_TRF1 [893].TRF[29:29]	1
0xBB80046C	L4_TRF1 [894].TRF[30:30]	1
0xBB80046C	L4_TRF1 [895].TRF[31:31]	1
0xBB800470	L4_TRF1 [896].TRF[0:0]	1
0xBB800470	L4_TRF1 [897].TRF[1:1]	1
0xBB800470	L4_TRF1 [898].TRF[2:2]	1
0xBB800470	L4_TRF1 [899].TRF[3:3]	1
0xBB800470	L4_TRF1 [900].TRF[4:4]	1
0xBB800470	L4_TRF1 [901].TRF[5:5]	1
0xBB800470	L4_TRF1 [902].TRF[6:6]	1
0xBB800470	L4_TRF1 [903].TRF[7:7]	1
0xBB800470	L4_TRF1 [904].TRF[8:8]	1
0xBB800470	L4_TRF1 [905].TRF[9:9]	1
0xBB800470	L4_TRF1 [906].TRF[10:10]	1
0xBB800470	L4_TRF1 [907].TRF[11:11]	1

Address	Register	Len
0xBB800470	L4_TRF1 [908].TRF[12:12]	1
0xBB800470	L4_TRF1 [909].TRF[13:13]	1
0xBB800470	L4_TRF1 [910].TRF[14:14]	1
0xBB800470	L4_TRF1 [911].TRF[15:15]	1
0xBB800470	L4_TRF1 [912].TRF[16:16]	1
0xBB800470	L4_TRF1 [913].TRF[17:17]	1
0xBB800470	L4_TRF1 [914].TRF[18:18]	1
0xBB800470	L4_TRF1 [915].TRF[19:19]	1
0xBB800470	L4_TRF1 [916].TRF[20:20]	1
0xBB800470	L4_TRF1 [917].TRF[21:21]	1
0xBB800470	L4_TRF1 [918].TRF[22:22]	1
0xBB800470	L4_TRF1 [919].TRF[23:23]	1
0xBB800470	L4_TRF1 [920].TRF[24:24]	1
0xBB800470	L4_TRF1 [921].TRF[25:25]	1
0xBB800470	L4_TRF1 [922].TRF[26:26]	1
0xBB800470	L4_TRF1 [923].TRF[27:27]	1
0xBB800470	L4_TRF1 [924].TRF[28:28]	1
0xBB800470	L4_TRF1 [925].TRF[29:29]	1
0xBB800470	L4_TRF1 [926].TRF[30:30]	1
0xBB800470	L4_TRF1 [927].TRF[31:31]	1
0xBB800474	L4_TRF1 [928].TRF[0:0]	1
0xBB800474	L4_TRF1 [929].TRF[1:1]	1
0xBB800474	L4_TRF1 [930].TRF[2:2]	1
0xBB800474	L4_TRF1 [931].TRF[3:3]	1
0xBB800474	L4_TRF1 [932].TRF[4:4]	1
0xBB800474	L4_TRF1 [933].TRF[5:5]	1
0xBB800474	L4_TRF1 [934].TRF[6:6]	1
0xBB800474	L4_TRF1 [935].TRF[7:7]	1
0xBB800474	L4_TRF1 [936].TRF[8:8]	1
0xBB800474	L4_TRF1 [937].TRF[9:9]	1
0xBB800474	L4_TRF1 [938].TRF[10:10]	1
0xBB800474	L4_TRF1 [939].TRF[11:11]	1
0xBB800474	L4_TRF1 [940].TRF[12:12]	1
0xBB800474	L4_TRF1 [941].TRF[13:13]	1
0xBB800474	L4_TRF1 [942].TRF[14:14]	1
0xBB800474	L4_TRF1 [943].TRF[15:15]	1
0xBB800474	L4_TRF1 [944].TRF[16:16]	1
0xBB800474	L4_TRF1 [945].TRF[17:17]	1
0xBB800474	L4_TRF1 [946].TRF[18:18]	1
0xBB800474	L4_TRF1 [947].TRF[19:19]	1
0xBB800474	L4_TRF1 [948].TRF[20:20]	1
0xBB800474	L4_TRF1 [949].TRF[21:21]	1
0xBB800474	L4_TRF1 [950].TRF[22:22]	1
0xBB800474	L4_TRF1 [951].TRF[23:23]	1
0xBB800474	L4_TRF1 [952].TRF[24:24]	1
0xBB800474	L4_TRF1 [953].TRF[25:25]	1

Address	Register	Len
0xBB800474	L4_TRF1 [954].TRF[26:26]	1
0xBB800474	L4_TRF1 [955].TRF[27:27]	1
0xBB800474	L4_TRF1 [956].TRF[28:28]	1
0xBB800474	L4_TRF1 [957].TRF[29:29]	1
0xBB800474	L4_TRF1 [958].TRF[30:30]	1
0xBB800474	L4_TRF1 [959].TRF[31:31]	1
0xBB800478	L4_TRF1 [960].TRF[0:0]	1
0xBB800478	L4_TRF1 [961].TRF[1:1]	1
0xBB800478	L4_TRF1 [962].TRF[2:2]	1
0xBB800478	L4_TRF1 [963].TRF[3:3]	1
0xBB800478	L4_TRF1 [964].TRF[4:4]	1
0xBB800478	L4_TRF1 [965].TRF[5:5]	1
0xBB800478	L4_TRF1 [966].TRF[6:6]	1
0xBB800478	L4_TRF1 [967].TRF[7:7]	1
0xBB800478	L4_TRF1 [968].TRF[8:8]	1
0xBB800478	L4_TRF1 [969].TRF[9:9]	1
0xBB800478	L4_TRF1 [970].TRF[10:10]	1
0xBB800478	L4_TRF1 [971].TRF[11:11]	1
0xBB800478	L4_TRF1 [972].TRF[12:12]	1
0xBB800478	L4_TRF1 [973].TRF[13:13]	1
0xBB800478	L4_TRF1 [974].TRF[14:14]	1
0xBB800478	L4_TRF1 [975].TRF[15:15]	1
0xBB800478	L4_TRF1 [976].TRF[16:16]	1
0xBB800478	L4_TRF1 [977].TRF[17:17]	1
0xBB800478	L4_TRF1 [978].TRF[18:18]	1
0xBB800478	L4_TRF1 [979].TRF[19:19]	1
0xBB800478	L4_TRF1 [980].TRF[20:20]	1
0xBB800478	L4_TRF1 [981].TRF[21:21]	1
0xBB800478	L4_TRF1 [982].TRF[22:22]	1
0xBB800478	L4_TRF1 [983].TRF[23:23]	1
0xBB800478	L4_TRF1 [984].TRF[24:24]	1
0xBB800478	L4_TRF1 [985].TRF[25:25]	1
0xBB800478	L4_TRF1 [986].TRF[26:26]	1
0xBB800478	L4_TRF1 [987].TRF[27:27]	1
0xBB800478	L4_TRF1 [988].TRF[28:28]	1
0xBB800478	L4_TRF1 [989].TRF[29:29]	1
0xBB800478	L4_TRF1 [990].TRF[30:30]	1
0xBB800478	L4_TRF1 [991].TRF[31:31]	1
0xBB80047C	L4_TRF1 [992].TRF[0:0]	1
0xBB80047C	L4_TRF1 [993].TRF[1:1]	1
0xBB80047C	L4_TRF1 [994].TRF[2:2]	1
0xBB80047C	L4_TRF1 [995].TRF[3:3]	1
0xBB80047C	L4_TRF1 [996].TRF[4:4]	1
0xBB80047C	L4_TRF1 [997].TRF[5:5]	1
0xBB80047C	L4_TRF1 [998].TRF[6:6]	1
0xBB80047C	L4_TRF1 [999].TRF[7:7]	1

Address	Register	Len
0xBB80047C	L4_TRF1 [1000].TRF[8:8]	1
0xBB80047C	L4_TRF1 [1001].TRF[9:9]	1
0xBB80047C	L4_TRF1 [1002].TRF[10:10]	1
0xBB80047C	L4_TRF1 [1003].TRF[11:11]	1
0xBB80047C	L4_TRF1 [1004].TRF[12:12]	1
0xBB80047C	L4_TRF1 [1005].TRF[13:13]	1
0xBB80047C	L4_TRF1 [1006].TRF[14:14]	1
0xBB80047C	L4_TRF1 [1007].TRF[15:15]	1
0xBB80047C	L4_TRF1 [1008].TRF[16:16]	1
0xBB80047C	L4_TRF1 [1009].TRF[17:17]	1
0xBB80047C	L4_TRF1 [1010].TRF[18:18]	1
0xBB80047C	L4_TRF1 [1011].TRF[19:19]	1
0xBB80047C	L4_TRF1 [1012].TRF[20:20]	1
0xBB80047C	L4_TRF1 [1013].TRF[21:21]	1
0xBB80047C	L4_TRF1 [1014].TRF[22:22]	1
0xBB80047C	L4_TRF1 [1015].TRF[23:23]	1
0xBB80047C	L4_TRF1 [1016].TRF[24:24]	1
0xBB80047C	L4_TRF1 [1017].TRF[25:25]	1
0xBB80047C	L4_TRF1 [1018].TRF[26:26]	1
0xBB80047C	L4_TRF1 [1019].TRF[27:27]	1
0xBB80047C	L4_TRF1 [1020].TRF[28:28]	1
0xBB80047C	L4_TRF1 [1021].TRF[29:29]	1
0xBB80047C	L4_TRF1 [1022].TRF[30:30]	1
0xBB80047C	L4_TRF1 [1023].TRF[31:31]	1
0xBB800480	L4_TRF1 [1024].TRF[0:0]	1
0xBB800480	L4_TRF1 [1025].TRF[1:1]	1
0xBB800480	L4_TRF1 [1026].TRF[2:2]	1
0xBB800480	L4_TRF1 [1027].TRF[3:3]	1
0xBB800480	L4_TRF1 [1028].TRF[4:4]	1
0xBB800480	L4_TRF1 [1029].TRF[5:5]	1
0xBB800480	L4_TRF1 [1030].TRF[6:6]	1
0xBB800480	L4_TRF1 [1031].TRF[7:7]	1
0xBB800480	L4_TRF1 [1032].TRF[8:8]	1
0xBB800480	L4_TRF1 [1033].TRF[9:9]	1
0xBB800480	L4_TRF1 [1034].TRF[10:10]	1
0xBB800480	L4_TRF1 [1035].TRF[11:11]	1
0xBB800480	L4_TRF1 [1036].TRF[12:12]	1
0xBB800480	L4_TRF1 [1037].TRF[13:13]	1
0xBB800480	L4_TRF1 [1038].TRF[14:14]	1
0xBB800480	L4_TRF1 [1039].TRF[15:15]	1
0xBB800480	L4_TRF1 [1040].TRF[16:16]	1
0xBB800480	L4_TRF1 [1041].TRF[17:17]	1
0xBB800480	L4_TRF1 [1042].TRF[18:18]	1
0xBB800480	L4_TRF1 [1043].TRF[19:19]	1
0xBB800480	L4_TRF1 [1044].TRF[20:20]	1
0xBB800480	L4_TRF1 [1045].TRF[21:21]	1

Address	Register	Len
0xBB800480	L4_TRF1 [1046].TRF[22:22]	1
0xBB800480	L4_TRF1 [1047].TRF[23:23]	1
0xBB800480	L4_TRF1 [1048].TRF[24:24]	1
0xBB800480	L4_TRF1 [1049].TRF[25:25]	1
0xBB800480	L4_TRF1 [1050].TRF[26:26]	1
0xBB800480	L4_TRF1 [1051].TRF[27:27]	1
0xBB800480	L4_TRF1 [1052].TRF[28:28]	1
0xBB800480	L4_TRF1 [1053].TRF[29:29]	1
0xBB800480	L4_TRF1 [1054].TRF[30:30]	1
0xBB800480	L4_TRF1 [1055].TRF[31:31]	1
0xBB800484	L4_TRF1 [1056].TRF[0:0]	1
0xBB800484	L4_TRF1 [1057].TRF[1:1]	1
0xBB800484	L4_TRF1 [1058].TRF[2:2]	1
0xBB800484	L4_TRF1 [1059].TRF[3:3]	1
0xBB800484	L4_TRF1 [1060].TRF[4:4]	1
0xBB800484	L4_TRF1 [1061].TRF[5:5]	1
0xBB800484	L4_TRF1 [1062].TRF[6:6]	1
0xBB800484	L4_TRF1 [1063].TRF[7:7]	1
0xBB800484	L4_TRF1 [1064].TRF[8:8]	1
0xBB800484	L4_TRF1 [1065].TRF[9:9]	1
0xBB800484	L4_TRF1 [1066].TRF[10:10]	1
0xBB800484	L4_TRF1 [1067].TRF[11:11]	1
0xBB800484	L4_TRF1 [1068].TRF[12:12]	1
0xBB800484	L4_TRF1 [1069].TRF[13:13]	1
0xBB800484	L4_TRF1 [1070].TRF[14:14]	1
0xBB800484	L4_TRF1 [1071].TRF[15:15]	1
0xBB800484	L4_TRF1 [1072].TRF[16:16]	1
0xBB800484	L4_TRF1 [1073].TRF[17:17]	1
0xBB800484	L4_TRF1 [1074].TRF[18:18]	1
0xBB800484	L4_TRF1 [1075].TRF[19:19]	1
0xBB800484	L4_TRF1 [1076].TRF[20:20]	1
0xBB800484	L4_TRF1 [1077].TRF[21:21]	1
0xBB800484	L4_TRF1 [1078].TRF[22:22]	1
0xBB800484	L4_TRF1 [1079].TRF[23:23]	1
0xBB800484	L4_TRF1 [1080].TRF[24:24]	1
0xBB800484	L4_TRF1 [1081].TRF[25:25]	1
0xBB800484	L4_TRF1 [1082].TRF[26:26]	1
0xBB800484	L4_TRF1 [1083].TRF[27:27]	1
0xBB800484	L4_TRF1 [1084].TRF[28:28]	1
0xBB800484	L4_TRF1 [1085].TRF[29:29]	1
0xBB800484	L4_TRF1 [1086].TRF[30:30]	1
0xBB800484	L4_TRF1 [1087].TRF[31:31]	1
0xBB800488	L4_TRF1 [1088].TRF[0:0]	1
0xBB800488	L4_TRF1 [1089].TRF[1:1]	1
0xBB800488	L4_TRF1 [1090].TRF[2:2]	1
0xBB800488	L4_TRF1 [1091].TRF[3:3]	1

Address	Register	Len
0xBB800488	L4_TRF1 [1092].TRF[4:4]	1
0xBB800488	L4_TRF1 [1093].TRF[5:5]	1
0xBB800488	L4_TRF1 [1094].TRF[6:6]	1
0xBB800488	L4_TRF1 [1095].TRF[7:7]	1
0xBB800488	L4_TRF1 [1096].TRF[8:8]	1
0xBB800488	L4_TRF1 [1097].TRF[9:9]	1
0xBB800488	L4_TRF1 [1098].TRF[10:10]	1
0xBB800488	L4_TRF1 [1099].TRF[11:11]	1
0xBB800488	L4_TRF1 [1100].TRF[12:12]	1
0xBB800488	L4_TRF1 [1101].TRF[13:13]	1
0xBB800488	L4_TRF1 [1102].TRF[14:14]	1
0xBB800488	L4_TRF1 [1103].TRF[15:15]	1
0xBB800488	L4_TRF1 [1104].TRF[16:16]	1
0xBB800488	L4_TRF1 [1105].TRF[17:17]	1
0xBB800488	L4_TRF1 [1106].TRF[18:18]	1
0xBB800488	L4_TRF1 [1107].TRF[19:19]	1
0xBB800488	L4_TRF1 [1108].TRF[20:20]	1
0xBB800488	L4_TRF1 [1109].TRF[21:21]	1
0xBB800488	L4_TRF1 [1110].TRF[22:22]	1
0xBB800488	L4_TRF1 [1111].TRF[23:23]	1
0xBB800488	L4_TRF1 [1112].TRF[24:24]	1
0xBB800488	L4_TRF1 [1113].TRF[25:25]	1
0xBB800488	L4_TRF1 [1114].TRF[26:26]	1
0xBB800488	L4_TRF1 [1115].TRF[27:27]	1
0xBB800488	L4_TRF1 [1116].TRF[28:28]	1
0xBB800488	L4_TRF1 [1117].TRF[29:29]	1
0xBB800488	L4_TRF1 [1118].TRF[30:30]	1
0xBB800488	L4_TRF1 [1119].TRF[31:31]	1
0xBB80048C	L4_TRF1 [1120].TRF[0:0]	1
0xBB80048C	L4_TRF1 [1121].TRF[1:1]	1
0xBB80048C	L4_TRF1 [1122].TRF[2:2]	1
0xBB80048C	L4_TRF1 [1123].TRF[3:3]	1
0xBB80048C	L4_TRF1 [1124].TRF[4:4]	1
0xBB80048C	L4_TRF1 [1125].TRF[5:5]	1
0xBB80048C	L4_TRF1 [1126].TRF[6:6]	1
0xBB80048C	L4_TRF1 [1127].TRF[7:7]	1
0xBB80048C	L4_TRF1 [1128].TRF[8:8]	1
0xBB80048C	L4_TRF1 [1129].TRF[9:9]	1
0xBB80048C	L4_TRF1 [1130].TRF[10:10]	1
0xBB80048C	L4_TRF1 [1131].TRF[11:11]	1
0xBB80048C	L4_TRF1 [1132].TRF[12:12]	1
0xBB80048C	L4_TRF1 [1133].TRF[13:13]	1
0xBB80048C	L4_TRF1 [1134].TRF[14:14]	1
0xBB80048C	L4_TRF1 [1135].TRF[15:15]	1
0xBB80048C	L4_TRF1 [1136].TRF[16:16]	1
0xBB80048C	L4_TRF1 [1137].TRF[17:17]	1



Address	Register	Len
0xBB80048C	L4_TRF1 [1138].TRF[18:18]	1
0xBB80048C	L4_TRF1 [1139].TRF[19:19]	1
0xBB80048C	L4_TRF1 [1140].TRF[20:20]	1
0xBB80048C	L4_TRF1 [1141].TRF[21:21]	1
0xBB80048C	L4_TRF1 [1142].TRF[22:22]	1
0xBB80048C	L4_TRF1 [1143].TRF[23:23]	1
0xBB80048C	L4_TRF1 [1144].TRF[24:24]	1
0xBB80048C	L4_TRF1 [1145].TRF[25:25]	1
0xBB80048C	L4_TRF1 [1146].TRF[26:26]	1
0xBB80048C	L4_TRF1 [1147].TRF[27:27]	1
0xBB80048C	L4_TRF1 [1148].TRF[28:28]	1
0xBB80048C	L4_TRF1 [1149].TRF[29:29]	1
0xBB80048C	L4_TRF1 [1150].TRF[30:30]	1
0xBB80048C	L4_TRF1 [1151].TRF[31:31]	1
0xBB800490	L4_TRF1 [1152].TRF[0:0]	1
0xBB800490	L4_TRF1 [1153].TRF[1:1]	1
0xBB800490	L4_TRF1 [1154].TRF[2:2]	1
0xBB800490	L4_TRF1 [1155].TRF[3:3]	1
0xBB800490	L4_TRF1 [1156].TRF[4:4]	1
0xBB800490	L4_TRF1 [1157].TRF[5:5]	1
0xBB800490	L4_TRF1 [1158].TRF[6:6]	1
0xBB800490	L4_TRF1 [1159].TRF[7:7]	1
0xBB800490	L4_TRF1 [1160].TRF[8:8]	1
0xBB800490	L4_TRF1 [1161].TRF[9:9]	1
0xBB800490	L4_TRF1 [1162].TRF[10:10]	1
0xBB800490	L4_TRF1 [1163].TRF[11:11]	1
0xBB800490	L4_TRF1 [1164].TRF[12:12]	1
0xBB800490	L4_TRF1 [1165].TRF[13:13]	1
0xBB800490	L4_TRF1 [1166].TRF[14:14]	1
0xBB800490	L4_TRF1 [1167].TRF[15:15]	1
0xBB800490	L4_TRF1 [1168].TRF[16:16]	1
0xBB800490	L4_TRF1 [1169].TRF[17:17]	1
0xBB800490	L4_TRF1 [1170].TRF[18:18]	1
0xBB800490	L4_TRF1 [1171].TRF[19:19]	1
0xBB800490	L4_TRF1 [1172].TRF[20:20]	1
0xBB800490	L4_TRF1 [1173].TRF[21:21]	1
0xBB800490	L4_TRF1 [1174].TRF[22:22]	1
0xBB800490	L4_TRF1 [1175].TRF[23:23]	1
0xBB800490	L4_TRF1 [1176].TRF[24:24]	1
0xBB800490	L4_TRF1 [1177].TRF[25:25]	1
0xBB800490	L4_TRF1 [1178].TRF[26:26]	1
0xBB800490	L4_TRF1 [1179].TRF[27:27]	1
0xBB800490	L4_TRF1 [1180].TRF[28:28]	1
0xBB800490	L4_TRF1 [1181].TRF[29:29]	1
0xBB800490	L4_TRF1 [1182].TRF[30:30]	1
0xBB800490	L4_TRF1 [1183].TRF[31:31]	1

Address	Register	Len
0xBB800494	L4_TRF1 [1184].TRF[0:0]	1
0xBB800494	L4_TRF1 [1185].TRF[1:1]	1
0xBB800494	L4_TRF1 [1186].TRF[2:2]	1
0xBB800494	L4_TRF1 [1187].TRF[3:3]	1
0xBB800494	L4_TRF1 [1188].TRF[4:4]	1
0xBB800494	L4_TRF1 [1189].TRF[5:5]	1
0xBB800494	L4_TRF1 [1190].TRF[6:6]	1
0xBB800494	L4_TRF1 [1191].TRF[7:7]	1
0xBB800494	L4_TRF1 [1192].TRF[8:8]	1
0xBB800494	L4_TRF1 [1193].TRF[9:9]	1
0xBB800494	L4_TRF1 [1194].TRF[10:10]	1
0xBB800494	L4_TRF1 [1195].TRF[11:11]	1
0xBB800494	L4_TRF1 [1196].TRF[12:12]	1
0xBB800494	L4_TRF1 [1197].TRF[13:13]	1
0xBB800494	L4_TRF1 [1198].TRF[14:14]	1
0xBB800494	L4_TRF1 [1199].TRF[15:15]	1
0xBB800494	L4_TRF1 [1200].TRF[16:16]	1
0xBB800494	L4_TRF1 [1201].TRF[17:17]	1
0xBB800494	L4_TRF1 [1202].TRF[18:18]	1
0xBB800494	L4_TRF1 [1203].TRF[19:19]	1
0xBB800494	L4_TRF1 [1204].TRF[20:20]	1
0xBB800494	L4_TRF1 [1205].TRF[21:21]	1
0xBB800494	L4_TRF1 [1206].TRF[22:22]	1
0xBB800494	L4_TRF1 [1207].TRF[23:23]	1
0xBB800494	L4_TRF1 [1208].TRF[24:24]	1
0xBB800494	L4_TRF1 [1209].TRF[25:25]	1
0xBB800494	L4_TRF1 [1210].TRF[26:26]	1
0xBB800494	L4_TRF1 [1211].TRF[27:27]	1
0xBB800494	L4_TRF1 [1212].TRF[28:28]	1
0xBB800494	L4_TRF1 [1213].TRF[29:29]	1
0xBB800494	L4_TRF1 [1214].TRF[30:30]	1
0xBB800494	L4_TRF1 [1215].TRF[31:31]	1
0xBB800498	L4_TRF1 [1216].TRF[0:0]	1
0xBB800498	L4_TRF1 [1217].TRF[1:1]	1
0xBB800498	L4_TRF1 [1218].TRF[2:2]	1
0xBB800498	L4_TRF1 [1219].TRF[3:3]	1
0xBB800498	L4_TRF1 [1220].TRF[4:4]	1
0xBB800498	L4_TRF1 [1221].TRF[5:5]	1
0xBB800498	L4_TRF1 [1222].TRF[6:6]	1
0xBB800498	L4_TRF1 [1223].TRF[7:7]	1
0xBB800498	L4_TRF1 [1224].TRF[8:8]	1
0xBB800498	L4_TRF1 [1225].TRF[9:9]	1
0xBB800498	L4_TRF1 [1226].TRF[10:10]	1
0xBB800498	L4_TRF1 [1227].TRF[11:11]	1
0xBB800498	L4_TRF1 [1228].TRF[12:12]	1
0xBB800498	L4_TRF1 [1229].TRF[13:13]	1

Address	Register	Len
0xBB800498	L4_TRF1 [1230].TRF[14:14]	1
0xBB800498	L4_TRF1 [1231].TRF[15:15]	1
0xBB800498	L4_TRF1 [1232].TRF[16:16]	1
0xBB800498	L4_TRF1 [1233].TRF[17:17]	1
0xBB800498	L4_TRF1 [1234].TRF[18:18]	1
0xBB800498	L4_TRF1 [1235].TRF[19:19]	1
0xBB800498	L4_TRF1 [1236].TRF[20:20]	1
0xBB800498	L4_TRF1 [1237].TRF[21:21]	1
0xBB800498	L4_TRF1 [1238].TRF[22:22]	1
0xBB800498	L4_TRF1 [1239].TRF[23:23]	1
0xBB800498	L4_TRF1 [1240].TRF[24:24]	1
0xBB800498	L4_TRF1 [1241].TRF[25:25]	1
0xBB800498	L4_TRF1 [1242].TRF[26:26]	1
0xBB800498	L4_TRF1 [1243].TRF[27:27]	1
0xBB800498	L4_TRF1 [1244].TRF[28:28]	1
0xBB800498	L4_TRF1 [1245].TRF[29:29]	1
0xBB800498	L4_TRF1 [1246].TRF[30:30]	1
0xBB800498	L4_TRF1 [1247].TRF[31:31]	1
0xBB80049C	L4_TRF1 [1248].TRF[0:0]	1
0xBB80049C	L4_TRF1 [1249].TRF[1:1]	1
0xBB80049C	L4_TRF1 [1250].TRF[2:2]	1
0xBB80049C	L4_TRF1 [1251].TRF[3:3]	1
0xBB80049C	L4_TRF1 [1252].TRF[4:4]	1
0xBB80049C	L4_TRF1 [1253].TRF[5:5]	1
0xBB80049C	L4_TRF1 [1254].TRF[6:6]	1
0xBB80049C	L4_TRF1 [1255].TRF[7:7]	1
0xBB80049C	L4_TRF1 [1256].TRF[8:8]	1
0xBB80049C	L4_TRF1 [1257].TRF[9:9]	1
0xBB80049C	L4_TRF1 [1258].TRF[10:10]	1
0xBB80049C	L4_TRF1 [1259].TRF[11:11]	1
0xBB80049C	L4_TRF1 [1260].TRF[12:12]	1
0xBB80049C	L4_TRF1 [1261].TRF[13:13]	1
0xBB80049C	L4_TRF1 [1262].TRF[14:14]	1
0xBB80049C	L4_TRF1 [1263].TRF[15:15]	1
0xBB80049C	L4_TRF1 [1264].TRF[16:16]	1
0xBB80049C	L4_TRF1 [1265].TRF[17:17]	1
0xBB80049C	L4_TRF1 [1266].TRF[18:18]	1
0xBB80049C	L4_TRF1 [1267].TRF[19:19]	1
0xBB80049C	L4_TRF1 [1268].TRF[20:20]	1
0xBB80049C	L4_TRF1 [1269].TRF[21:21]	1
0xBB80049C	L4_TRF1 [1270].TRF[22:22]	1
0xBB80049C	L4_TRF1 [1271].TRF[23:23]	1
0xBB80049C	L4_TRF1 [1272].TRF[24:24]	1
0xBB80049C	L4_TRF1 [1273].TRF[25:25]	1
0xBB80049C	L4_TRF1 [1274].TRF[26:26]	1
0xBB80049C	L4_TRF1 [1275].TRF[27:27]	1

Address	Register	Len
0xBB80049C	L4_TRF1 [1276].TRF[28:28]	1
0xBB80049C	L4_TRF1 [1277].TRF[29:29]	1
0xBB80049C	L4_TRF1 [1278].TRF[30:30]	1
0xBB80049C	L4_TRF1 [1279].TRF[31:31]	1
0xBB8004A0	L4_TRF1 [1280].TRF[0:0]	1
0xBB8004A0	L4_TRF1 [1281].TRF[1:1]	1
0xBB8004A0	L4_TRF1 [1282].TRF[2:2]	1
0xBB8004A0	L4_TRF1 [1283].TRF[3:3]	1
0xBB8004A0	L4_TRF1 [1284].TRF[4:4]	1
0xBB8004A0	L4_TRF1 [1285].TRF[5:5]	1
0xBB8004A0	L4_TRF1 [1286].TRF[6:6]	1
0xBB8004A0	L4_TRF1 [1287].TRF[7:7]	1
0xBB8004A0	L4_TRF1 [1288].TRF[8:8]	1
0xBB8004A0	L4_TRF1 [1289].TRF[9:9]	1
0xBB8004A0	L4_TRF1 [1290].TRF[10:10]	1
0xBB8004A0	L4_TRF1 [1291].TRF[11:11]	1
0xBB8004A0	L4_TRF1 [1292].TRF[12:12]	1
0xBB8004A0	L4_TRF1 [1293].TRF[13:13]	1
0xBB8004A0	L4_TRF1 [1294].TRF[14:14]	1
0xBB8004A0	L4_TRF1 [1295].TRF[15:15]	1
0xBB8004A0	L4_TRF1 [1296].TRF[16:16]	1
0xBB8004A0	L4_TRF1 [1297].TRF[17:17]	1
0xBB8004A0	L4_TRF1 [1298].TRF[18:18]	1
0xBB8004A0	L4_TRF1 [1299].TRF[19:19]	1
0xBB8004A0	L4_TRF1 [1300].TRF[20:20]	1
0xBB8004A0	L4_TRF1 [1301].TRF[21:21]	1
0xBB8004A0	L4_TRF1 [1302].TRF[22:22]	1
0xBB8004A0	L4_TRF1 [1303].TRF[23:23]	1
0xBB8004A0	L4_TRF1 [1304].TRF[24:24]	1
0xBB8004A0	L4_TRF1 [1305].TRF[25:25]	1
0xBB8004A0	L4_TRF1 [1306].TRF[26:26]	1
0xBB8004A0	L4_TRF1 [1307].TRF[27:27]	1
0xBB8004A0	L4_TRF1 [1308].TRF[28:28]	1
0xBB8004A0	L4_TRF1 [1309].TRF[29:29]	1
0xBB8004A0	L4_TRF1 [1310].TRF[30:30]	1
0xBB8004A0	L4_TRF1 [1311].TRF[31:31]	1
0xBB8004A4	L4_TRF1 [1312].TRF[0:0]	1
0xBB8004A4	L4_TRF1 [1313].TRF[1:1]	1
0xBB8004A4	L4_TRF1 [1314].TRF[2:2]	1
0xBB8004A4	L4_TRF1 [1315].TRF[3:3]	1
0xBB8004A4	L4_TRF1 [1316].TRF[4:4]	1
0xBB8004A4	L4_TRF1 [1317].TRF[5:5]	1
0xBB8004A4	L4_TRF1 [1318].TRF[6:6]	1
0xBB8004A4	L4_TRF1 [1319].TRF[7:7]	1
0xBB8004A4	L4_TRF1 [1320].TRF[8:8]	1
0xBB8004A4	L4_TRF1 [1321].TRF[9:9]	1

Address	Register	Len
0xBB8004A4	L4_TRF1 [1322].TRF[10:10]	1
0xBB8004A4	L4_TRF1 [1323].TRF[11:11]	1
0xBB8004A4	L4_TRF1 [1324].TRF[12:12]	1
0xBB8004A4	L4_TRF1 [1325].TRF[13:13]	1
0xBB8004A4	L4_TRF1 [1326].TRF[14:14]	1
0xBB8004A4	L4_TRF1 [1327].TRF[15:15]	1
0xBB8004A4	L4_TRF1 [1328].TRF[16:16]	1
0xBB8004A4	L4_TRF1 [1329].TRF[17:17]	1
0xBB8004A4	L4_TRF1 [1330].TRF[18:18]	1
0xBB8004A4	L4_TRF1 [1331].TRF[19:19]	1
0xBB8004A4	L4_TRF1 [1332].TRF[20:20]	1
0xBB8004A4	L4_TRF1 [1333].TRF[21:21]	1
0xBB8004A4	L4_TRF1 [1334].TRF[22:22]	1
0xBB8004A4	L4_TRF1 [1335].TRF[23:23]	1
0xBB8004A4	L4_TRF1 [1336].TRF[24:24]	1
0xBB8004A4	L4_TRF1 [1337].TRF[25:25]	1
0xBB8004A4	L4_TRF1 [1338].TRF[26:26]	1
0xBB8004A4	L4_TRF1 [1339].TRF[27:27]	1
0xBB8004A4	L4_TRF1 [1340].TRF[28:28]	1
0xBB8004A4	L4_TRF1 [1341].TRF[29:29]	1
0xBB8004A4	L4_TRF1 [1342].TRF[30:30]	1
0xBB8004A4	L4_TRF1 [1343].TRF[31:31]	1
0xBB8004A8	L4_TRF1 [1344].TRF[0:0]	1
0xBB8004A8	L4_TRF1 [1345].TRF[1:1]	1
0xBB8004A8	L4_TRF1 [1346].TRF[2:2]	1
0xBB8004A8	L4_TRF1 [1347].TRF[3:3]	1
0xBB8004A8	L4_TRF1 [1348].TRF[4:4]	1
0xBB8004A8	L4_TRF1 [1349].TRF[5:5]	1
0xBB8004A8	L4_TRF1 [1350].TRF[6:6]	1
0xBB8004A8	L4_TRF1 [1351].TRF[7:7]	1
0xBB8004A8	L4_TRF1 [1352].TRF[8:8]	1
0xBB8004A8	L4_TRF1 [1353].TRF[9:9]	1
0xBB8004A8	L4_TRF1 [1354].TRF[10:10]	1
0xBB8004A8	L4_TRF1 [1355].TRF[11:11]	1
0xBB8004A8	L4_TRF1 [1356].TRF[12:12]	1
0xBB8004A8	L4_TRF1 [1357].TRF[13:13]	1
0xBB8004A8	L4_TRF1 [1358].TRF[14:14]	1
0xBB8004A8	L4_TRF1 [1359].TRF[15:15]	1
0xBB8004A8	L4_TRF1 [1360].TRF[16:16]	1
0xBB8004A8	L4_TRF1 [1361].TRF[17:17]	1
0xBB8004A8	L4_TRF1 [1362].TRF[18:18]	1
0xBB8004A8	L4_TRF1 [1363].TRF[19:19]	1
0xBB8004A8	L4_TRF1 [1364].TRF[20:20]	1
0xBB8004A8	L4_TRF1 [1365].TRF[21:21]	1
0xBB8004A8	L4_TRF1 [1366].TRF[22:22]	1
0xBB8004A8	L4_TRF1 [1367].TRF[23:23]	1

Address	Register	Len
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0xBB8004A8	L4_TRF1 [1369].TRF[25:25]	1
0xBB8004A8	L4_TRF1 [1370].TRF[26:26]	1
0xBB8004A8	L4_TRF1 [1371].TRF[27:27]	1
0xBB8004A8	L4_TRF1 [1372].TRF[28:28]	1
0xBB8004A8	L4_TRF1 [1373].TRF[29:29]	1
0xBB8004A8	L4_TRF1 [1374].TRF[30:30]	1
0xBB8004A8	L4_TRF1 [1375].TRF[31:31]	1
0xBB8004AC	L4_TRF1 [1376].TRF[0:0]	1
0xBB8004AC	L4_TRF1 [1377].TRF[1:1]	1
0xBB8004AC	L4_TRF1 [1378].TRF[2:2]	1
0xBB8004AC	L4_TRF1 [1379].TRF[3:3]	1
0xBB8004AC	L4_TRF1 [1380].TRF[4:4]	1
0xBB8004AC	L4_TRF1 [1381].TRF[5:5]	1
0xBB8004AC	L4_TRF1 [1382].TRF[6:6]	1
0xBB8004AC	L4_TRF1 [1383].TRF[7:7]	1
0xBB8004AC	L4_TRF1 [1384].TRF[8:8]	1
0xBB8004AC	L4_TRF1 [1385].TRF[9:9]	1
0xBB8004AC	L4_TRF1 [1386].TRF[10:10]	1
0xBB8004AC	L4_TRF1 [1387].TRF[11:11]	1
0xBB8004AC	L4_TRF1 [1388].TRF[12:12]	1
0xBB8004AC	L4_TRF1 [1389].TRF[13:13]	1
0xBB8004AC	L4_TRF1 [1390].TRF[14:14]	1
0xBB8004AC	L4_TRF1 [1391].TRF[15:15]	1
0xBB8004AC	L4_TRF1 [1392].TRF[16:16]	1
0xBB8004AC	L4_TRF1 [1393].TRF[17:17]	1
0xBB8004AC	L4_TRF1 [1394].TRF[18:18]	1
0xBB8004AC	L4_TRF1 [1395].TRF[19:19]	1
0xBB8004AC	L4_TRF1 [1396].TRF[20:20]	1
0xBB8004AC	L4_TRF1 [1397].TRF[21:21]	1
0xBB8004AC	L4_TRF1 [1398].TRF[22:22]	1
0xBB8004AC	L4_TRF1 [1399].TRF[23:23]	1
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0xBB8004AC	L4_TRF1 [1401].TRF[25:25]	1
0xBB8004AC	L4_TRF1 [1402].TRF[26:26]	1
0xBB8004AC	L4_TRF1 [1403].TRF[27:27]	1
0xBB8004AC	L4_TRF1 [1404].TRF[28:28]	1
0xBB8004AC	L4_TRF1 [1405].TRF[29:29]	1
0xBB8004AC	L4_TRF1 [1406].TRF[30:30]	1
0xBB8004AC	L4_TRF1 [1407].TRF[31:31]	1
0xBB8004B0	L4_TRF1 [1408].TRF[0:0]	1
0xBB8004B0	L4_TRF1 [1409].TRF[1:1]	1
0xBB8004B0	L4_TRF1 [1410].TRF[2:2]	1
0xBB8004B0	L4_TRF1 [1411].TRF[3:3]	1
0xBB8004B0	L4_TRF1 [1412].TRF[4:4]	1
0xBB8004B0	L4_TRF1 [1413].TRF[5:5]	1

Address	Register	Len
0xBB8004B0	L4_TRF1 [1414].TRF[6:6]	1
0xBB8004B0	L4_TRF1 [1415].TRF[7:7]	1
0xBB8004B0	L4_TRF1 [1416].TRF[8:8]	1
0xBB8004B0	L4_TRF1 [1417].TRF[9:9]	1
0xBB8004B0	L4_TRF1 [1418].TRF[10:10]	1
0xBB8004B0	L4_TRF1 [1419].TRF[11:11]	1
0xBB8004B0	L4_TRF1 [1420].TRF[12:12]	1
0xBB8004B0	L4_TRF1 [1421].TRF[13:13]	1
0xBB8004B0	L4_TRF1 [1422].TRF[14:14]	1
0xBB8004B0	L4_TRF1 [1423].TRF[15:15]	1
0xBB8004B0	L4_TRF1 [1424].TRF[16:16]	1
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0xBB8004B0	L4_TRF1 [1426].TRF[18:18]	1
0xBB8004B0	L4_TRF1 [1427].TRF[19:19]	1
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0xBB8004B0	L4_TRF1 [1429].TRF[21:21]	1
0xBB8004B0	L4_TRF1 [1430].TRF[22:22]	1
0xBB8004B0	L4_TRF1 [1431].TRF[23:23]	1
0xBB8004B0	L4_TRF1 [1432].TRF[24:24]	1
0xBB8004B0	L4_TRF1 [1433].TRF[25:25]	1
0xBB8004B0	L4_TRF1 [1434].TRF[26:26]	1
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0xBB8004B4	L4_TRF1 [1440].TRF[0:0]	1
0xBB8004B4	L4_TRF1 [1441].TRF[1:1]	1
0xBB8004B4	L4_TRF1 [1442].TRF[2:2]	1
0xBB8004B4	L4_TRF1 [1443].TRF[3:3]	1
0xBB8004B4	L4_TRF1 [1444].TRF[4:4]	1
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0xBB8004B4	L4_TRF1 [1447].TRF[7:7]	1
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0xBB8004B4	L4_TRF1 [1449].TRF[9:9]	1
0xBB8004B4	L4_TRF1 [1450].TRF[10:10]	1
0xBB8004B4	L4_TRF1 [1451].TRF[11:11]	1
0xBB8004B4	L4_TRF1 [1452].TRF[12:12]	1
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0xBB8004B4	L4_TRF1 [1456].TRF[16:16]	1
0xBB8004B4	L4_TRF1 [1457].TRF[17:17]	1
0xBB8004B4	L4_TRF1 [1458].TRF[18:18]	1
0xBB8004B4	L4_TRF1 [1459].TRF[19:19]	1

Address	Register	Len
0xBB8004B4	L4_TRF1 [1460].TRF[20:20]	1
0xBB8004B4	L4_TRF1 [1461].TRF[21:21]	1
0xBB8004B4	L4_TRF1 [1462].TRF[22:22]	1
0xBB8004B4	L4_TRF1 [1463].TRF[23:23]	1
0xBB8004B4	L4_TRF1 [1464].TRF[24:24]	1
0xBB8004B4	L4_TRF1 [1465].TRF[25:25]	1
0xBB8004B4	L4_TRF1 [1466].TRF[26:26]	1
0xBB8004B4	L4_TRF1 [1467].TRF[27:27]	1
0xBB8004B4	L4_TRF1 [1468].TRF[28:28]	1
0xBB8004B4	L4_TRF1 [1469].TRF[29:29]	1
0xBB8004B4	L4_TRF1 [1470].TRF[30:30]	1
0xBB8004B4	L4_TRF1 [1471].TRF[31:31]	1
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0xBB8004B8	L4_TRF1 [1473].TRF[1:1]	1
0xBB8004B8	L4_TRF1 [1474].TRF[2:2]	1
0xBB8004B8	L4_TRF1 [1475].TRF[3:3]	1
0xBB8004B8	L4_TRF1 [1476].TRF[4:4]	1
0xBB8004B8	L4_TRF1 [1477].TRF[5:5]	1
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0xBB8004B8	L4_TRF1 [1479].TRF[7:7]	1
0xBB8004B8	L4_TRF1 [1480].TRF[8:8]	1
0xBB8004B8	L4_TRF1 [1481].TRF[9:9]	1
0xBB8004B8	L4_TRF1 [1482].TRF[10:10]	1
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0xBB8004B8	L4_TRF1 [1485].TRF[13:13]	1
0xBB8004B8	L4_TRF1 [1486].TRF[14:14]	1
0xBB8004B8	L4_TRF1 [1487].TRF[15:15]	1
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0xBB8004B8	L4_TRF1 [1489].TRF[17:17]	1
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0xBB8004B8	L4_TRF1 [1491].TRF[19:19]	1
0xBB8004B8	L4_TRF1 [1492].TRF[20:20]	1
0xBB8004B8	L4_TRF1 [1493].TRF[21:21]	1
0xBB8004B8	L4_TRF1 [1494].TRF[22:22]	1
0xBB8004B8	L4_TRF1 [1495].TRF[23:23]	1
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0xBB8004B8	L4_TRF1 [1498].TRF[26:26]	1
0xBB8004B8	L4_TRF1 [1499].TRF[27:27]	1
0xBB8004B8	L4_TRF1 [1500].TRF[28:28]	1
0xBB8004B8	L4_TRF1 [1501].TRF[29:29]	1
0xBB8004B8	L4_TRF1 [1502].TRF[30:30]	1
0xBB8004B8	L4_TRF1 [1503].TRF[31:31]	1
0xBB8004BC	L4_TRF1 [1504].TRF[0:0]	1
0xBB8004BC	L4_TRF1 [1505].TRF[1:1]	1



Address	Register	Len
0xBB8004BC	L4_TRF1 [1506].TRF[2:2]	1
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0xBB8004BC	L4_TRF1 [1508].TRF[4:4]	1
0xBB8004BC	L4_TRF1 [1509].TRF[5:5]	1
0xBB8004BC	L4_TRF1 [1510].TRF[6:6]	1
0xBB8004BC	L4_TRF1 [1511].TRF[7:7]	1
0xBB8004BC	L4_TRF1 [1512].TRF[8:8]	1
0xBB8004BC	L4_TRF1 [1513].TRF[9:9]	1
0xBB8004BC	L4_TRF1 [1514].TRF[10:10]	1
0xBB8004BC	L4_TRF1 [1515].TRF[11:11]	1
0xBB8004BC	L4_TRF1 [1516].TRF[12:12]	1
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0xBB8004BC	L4_TRF1 [1518].TRF[14:14]	1
0xBB8004BC	L4_TRF1 [1519].TRF[15:15]	1
0xBB8004BC	L4_TRF1 [1520].TRF[16:16]	1
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0xBB8004BC	L4_TRF1 [1523].TRF[19:19]	1
0xBB8004BC	L4_TRF1 [1524].TRF[20:20]	1
0xBB8004BC	L4_TRF1 [1525].TRF[21:21]	1
0xBB8004BC	L4_TRF1 [1526].TRF[22:22]	1
0xBB8004BC	L4_TRF1 [1527].TRF[23:23]	1
0xBB8004BC	L4_TRF1 [1528].TRF[24:24]	1
0xBB8004BC	L4_TRF1 [1529].TRF[25:25]	1
0xBB8004BC	L4_TRF1 [1530].TRF[26:26]	1
0xBB8004BC	L4_TRF1 [1531].TRF[27:27]	1
0xBB8004BC	L4_TRF1 [1532].TRF[28:28]	1
0xBB8004BC	L4_TRF1 [1533].TRF[29:29]	1
0xBB8004BC	L4_TRF1 [1534].TRF[30:30]	1
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0xBB8004C0	L4_TRF1 [1537].TRF[1:1]	1
0xBB8004C0	L4_TRF1 [1538].TRF[2:2]	1
0xBB8004C0	L4_TRF1 [1539].TRF[3:3]	1
0xBB8004C0	L4_TRF1 [1540].TRF[4:4]	1
0xBB8004C0	L4_TRF1 [1541].TRF[5:5]	1
0xBB8004C0	L4_TRF1 [1542].TRF[6:6]	1
0xBB8004C0	L4_TRF1 [1543].TRF[7:7]	1
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0xBB8004C0	L4_TRF1 [1547].TRF[11:11]	1
0xBB8004C0	L4_TRF1 [1548].TRF[12:12]	1
0xBB8004C0	L4_TRF1 [1549].TRF[13:13]	1
0xBB8004C0	L4_TRF1 [1550].TRF[14:14]	1
0xBB8004C0	L4_TRF1 [1551].TRF[15:15]	1

Address	Register	Len
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0xBB8004C0	L4_TRF1 [1553].TRF[17:17]	1
0xBB8004C0	L4_TRF1 [1554].TRF[18:18]	1
0xBB8004C0	L4_TRF1 [1555].TRF[19:19]	1
0xBB8004C0	L4_TRF1 [1556].TRF[20:20]	1
0xBB8004C0	L4_TRF1 [1557].TRF[21:21]	1
0xBB8004C0	L4_TRF1 [1558].TRF[22:22]	1
0xBB8004C0	L4_TRF1 [1559].TRF[23:23]	1
0xBB8004C0	L4_TRF1 [1560].TRF[24:24]	1
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0xBB8004C4	L4_TRF1 [1568].TRF[0:0]	1
0xBB8004C4	L4_TRF1 [1569].TRF[1:1]	1
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0xBB8004C4	L4_TRF1 [1571].TRF[3:3]	1
0xBB8004C4	L4_TRF1 [1572].TRF[4:4]	1
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0xBB8004C4	L4_TRF1 [1586].TRF[18:18]	1
0xBB8004C4	L4_TRF1 [1587].TRF[19:19]	1
0xBB8004C4	L4_TRF1 [1588].TRF[20:20]	1
0xBB8004C4	L4_TRF1 [1589].TRF[21:21]	1
0xBB8004C4	L4_TRF1 [1590].TRF[22:22]	1
0xBB8004C4	L4_TRF1 [1591].TRF[23:23]	1
0xBB8004C4	L4_TRF1 [1592].TRF[24:24]	1
0xBB8004C4	L4_TRF1 [1593].TRF[25:25]	1
0xBB8004C4	L4_TRF1 [1594].TRF[26:26]	1
0xBB8004C4	L4_TRF1 [1595].TRF[27:27]	1
0xBB8004C4	L4_TRF1 [1596].TRF[28:28]	1
0xBB8004C4	L4_TRF1 [1597].TRF[29:29]	1

Address	Register	Len
0xBB8004C4	L4_TRF1 [1598].TRF[30:30]	1
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0xBB8004C8	L4_TRF1 [1600].TRF[0:0]	1
0xBB8004C8	L4_TRF1 [1601].TRF[1:1]	1
0xBB8004C8	L4_TRF1 [1602].TRF[2:2]	1
0xBB8004C8	L4_TRF1 [1603].TRF[3:3]	1
0xBB8004C8	L4_TRF1 [1604].TRF[4:4]	1
0xBB8004C8	L4_TRF1 [1605].TRF[5:5]	1
0xBB8004C8	L4_TRF1 [1606].TRF[6:6]	1
0xBB8004C8	L4_TRF1 [1607].TRF[7:7]	1
0xBB8004C8	L4_TRF1 [1608].TRF[8:8]	1
0xBB8004C8	L4_TRF1 [1609].TRF[9:9]	1
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0xBB8004C8	L4_TRF1 [1616].TRF[16:16]	1
0xBB8004C8	L4_TRF1 [1617].TRF[17:17]	1
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0xBB8004C8	L4_TRF1 [1619].TRF[19:19]	1
0xBB8004C8	L4_TRF1 [1620].TRF[20:20]	1
0xBB8004C8	L4_TRF1 [1621].TRF[21:21]	1
0xBB8004C8	L4_TRF1 [1622].TRF[22:22]	1
0xBB8004C8	L4_TRF1 [1623].TRF[23:23]	1
0xBB8004C8	L4_TRF1 [1624].TRF[24:24]	1
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0xBB8004CC	L4_TRF1 [1632].TRF[0:0]	1
0xBB8004CC	L4_TRF1 [1633].TRF[1:1]	1
0xBB8004CC	L4_TRF1 [1634].TRF[2:2]	1
0xBB8004CC	L4_TRF1 [1635].TRF[3:3]	1
0xBB8004CC	L4_TRF1 [1636].TRF[4:4]	1
0xBB8004CC	L4_TRF1 [1637].TRF[5:5]	1
0xBB8004CC	L4_TRF1 [1638].TRF[6:6]	1
0xBB8004CC	L4_TRF1 [1639].TRF[7:7]	1
0xBB8004CC	L4_TRF1 [1640].TRF[8:8]	1
0xBB8004CC	L4_TRF1 [1641].TRF[9:9]	1
0xBB8004CC	L4_TRF1 [1642].TRF[10:10]	1
0xBB8004CC	L4_TRF1 [1643].TRF[11:11]	1

Address	Register	Len
0xBB8004CC	L4_TRF1 [1644].TRF[12:12]	1
0xBB8004CC	L4_TRF1 [1645].TRF[13:13]	1
0xBB8004CC	L4_TRF1 [1646].TRF[14:14]	1
0xBB8004CC	L4_TRF1 [1647].TRF[15:15]	1
0xBB8004CC	L4_TRF1 [1648].TRF[16:16]	1
0xBB8004CC	L4_TRF1 [1649].TRF[17:17]	1
0xBB8004CC	L4_TRF1 [1650].TRF[18:18]	1
0xBB8004CC	L4_TRF1 [1651].TRF[19:19]	1
0xBB8004CC	L4_TRF1 [1652].TRF[20:20]	1
0xBB8004CC	L4_TRF1 [1653].TRF[21:21]	1
0xBB8004CC	L4_TRF1 [1654].TRF[22:22]	1
0xBB8004CC	L4_TRF1 [1655].TRF[23:23]	1
0xBB8004CC	L4_TRF1 [1656].TRF[24:24]	1
0xBB8004CC	L4_TRF1 [1657].TRF[25:25]	1
0xBB8004CC	L4_TRF1 [1658].TRF[26:26]	1
0xBB8004CC	L4_TRF1 [1659].TRF[27:27]	1
0xBB8004CC	L4_TRF1 [1660].TRF[28:28]	1
0xBB8004CC	L4_TRF1 [1661].TRF[29:29]	1
0xBB8004CC	L4_TRF1 [1662].TRF[30:30]	1
0xBB8004CC	L4_TRF1 [1663].TRF[31:31]	1
0xBB8004D0	L4_TRF1 [1664].TRF[0:0]	1
0xBB8004D0	L4_TRF1 [1665].TRF[1:1]	1
0xBB8004D0	L4_TRF1 [1666].TRF[2:2]	1
0xBB8004D0	L4_TRF1 [1667].TRF[3:3]	1
0xBB8004D0	L4_TRF1 [1668].TRF[4:4]	1
0xBB8004D0	L4_TRF1 [1669].TRF[5:5]	1
0xBB8004D0	L4_TRF1 [1670].TRF[6:6]	1
0xBB8004D0	L4_TRF1 [1671].TRF[7:7]	1
0xBB8004D0	L4_TRF1 [1672].TRF[8:8]	1
0xBB8004D0	L4_TRF1 [1673].TRF[9:9]	1
0xBB8004D0	L4_TRF1 [1674].TRF[10:10]	1
0xBB8004D0	L4_TRF1 [1675].TRF[11:11]	1
0xBB8004D0	L4_TRF1 [1676].TRF[12:12]	1
0xBB8004D0	L4_TRF1 [1677].TRF[13:13]	1
0xBB8004D0	L4_TRF1 [1678].TRF[14:14]	1
0xBB8004D0	L4_TRF1 [1679].TRF[15:15]	1
0xBB8004D0	L4_TRF1 [1680].TRF[16:16]	1
0xBB8004D0	L4_TRF1 [1681].TRF[17:17]	1
0xBB8004D0	L4_TRF1 [1682].TRF[18:18]	1
0xBB8004D0	L4_TRF1 [1683].TRF[19:19]	1
0xBB8004D0	L4_TRF1 [1684].TRF[20:20]	1
0xBB8004D0	L4_TRF1 [1685].TRF[21:21]	1
0xBB8004D0	L4_TRF1 [1686].TRF[22:22]	1
0xBB8004D0	L4_TRF1 [1687].TRF[23:23]	1
0xBB8004D0	L4_TRF1 [1688].TRF[24:24]	1
0xBB8004D0	L4_TRF1 [1689].TRF[25:25]	1

Address	Register	Len
0xBB8004D0	L4_TRF1 [1690].TRF[26:26]	1
0xBB8004D0	L4_TRF1 [1691].TRF[27:27]	1
0xBB8004D0	L4_TRF1 [1692].TRF[28:28]	1
0xBB8004D0	L4_TRF1 [1693].TRF[29:29]	1
0xBB8004D0	L4_TRF1 [1694].TRF[30:30]	1
0xBB8004D0	L4_TRF1 [1695].TRF[31:31]	1
0xBB8004D4	L4_TRF1 [1696].TRF[0:0]	1
0xBB8004D4	L4_TRF1 [1697].TRF[1:1]	1
0xBB8004D4	L4_TRF1 [1698].TRF[2:2]	1
0xBB8004D4	L4_TRF1 [1699].TRF[3:3]	1
0xBB8004D4	L4_TRF1 [1700].TRF[4:4]	1
0xBB8004D4	L4_TRF1 [1701].TRF[5:5]	1
0xBB8004D4	L4_TRF1 [1702].TRF[6:6]	1
0xBB8004D4	L4_TRF1 [1703].TRF[7:7]	1
0xBB8004D4	L4_TRF1 [1704].TRF[8:8]	1
0xBB8004D4	L4_TRF1 [1705].TRF[9:9]	1
0xBB8004D4	L4_TRF1 [1706].TRF[10:10]	1
0xBB8004D4	L4_TRF1 [1707].TRF[11:11]	1
0xBB8004D4	L4_TRF1 [1708].TRF[12:12]	1
0xBB8004D4	L4_TRF1 [1709].TRF[13:13]	1
0xBB8004D4	L4_TRF1 [1710].TRF[14:14]	1
0xBB8004D4	L4_TRF1 [1711].TRF[15:15]	1
0xBB8004D4	L4_TRF1 [1712].TRF[16:16]	1
0xBB8004D4	L4_TRF1 [1713].TRF[17:17]	1
0xBB8004D4	L4_TRF1 [1714].TRF[18:18]	1
0xBB8004D4	L4_TRF1 [1715].TRF[19:19]	1
0xBB8004D4	L4_TRF1 [1716].TRF[20:20]	1
0xBB8004D4	L4_TRF1 [1717].TRF[21:21]	1
0xBB8004D4	L4_TRF1 [1718].TRF[22:22]	1
0xBB8004D4	L4_TRF1 [1719].TRF[23:23]	1
0xBB8004D4	L4_TRF1 [1720].TRF[24:24]	1
0xBB8004D4	L4_TRF1 [1721].TRF[25:25]	1
0xBB8004D4	L4_TRF1 [1722].TRF[26:26]	1
0xBB8004D4	L4_TRF1 [1723].TRF[27:27]	1
0xBB8004D4	L4_TRF1 [1724].TRF[28:28]	1
0xBB8004D4	L4_TRF1 [1725].TRF[29:29]	1
0xBB8004D4	L4_TRF1 [1726].TRF[30:30]	1
0xBB8004D4	L4_TRF1 [1727].TRF[31:31]	1
0xBB8004D8	L4_TRF1 [1728].TRF[0:0]	1
0xBB8004D8	L4_TRF1 [1729].TRF[1:1]	1
0xBB8004D8	L4_TRF1 [1730].TRF[2:2]	1
0xBB8004D8	L4_TRF1 [1731].TRF[3:3]	1
0xBB8004D8	L4_TRF1 [1732].TRF[4:4]	1
0xBB8004D8	L4_TRF1 [1733].TRF[5:5]	1
0xBB8004D8	L4_TRF1 [1734].TRF[6:6]	1
0xBB8004D8	L4_TRF1 [1735].TRF[7:7]	1

Address	Register	Len
0xBB8004D8	L4_TRF1 [1736].TRF[8:8]	1
0xBB8004D8	L4_TRF1 [1737].TRF[9:9]	1
0xBB8004D8	L4_TRF1 [1738].TRF[10:10]	1
0xBB8004D8	L4_TRF1 [1739].TRF[11:11]	1
0xBB8004D8	L4_TRF1 [1740].TRF[12:12]	1
0xBB8004D8	L4_TRF1 [1741].TRF[13:13]	1
0xBB8004D8	L4_TRF1 [1742].TRF[14:14]	1
0xBB8004D8	L4_TRF1 [1743].TRF[15:15]	1
0xBB8004D8	L4_TRF1 [1744].TRF[16:16]	1
0xBB8004D8	L4_TRF1 [1745].TRF[17:17]	1
0xBB8004D8	L4_TRF1 [1746].TRF[18:18]	1
0xBB8004D8	L4_TRF1 [1747].TRF[19:19]	1
0xBB8004D8	L4_TRF1 [1748].TRF[20:20]	1
0xBB8004D8	L4_TRF1 [1749].TRF[21:21]	1
0xBB8004D8	L4_TRF1 [1750].TRF[22:22]	1
0xBB8004D8	L4_TRF1 [1751].TRF[23:23]	1
0xBB8004D8	L4_TRF1 [1752].TRF[24:24]	1
0xBB8004D8	L4_TRF1 [1753].TRF[25:25]	1
0xBB8004D8	L4_TRF1 [1754].TRF[26:26]	1
0xBB8004D8	L4_TRF1 [1755].TRF[27:27]	1
0xBB8004D8	L4_TRF1 [1756].TRF[28:28]	1
0xBB8004D8	L4_TRF1 [1757].TRF[29:29]	1
0xBB8004D8	L4_TRF1 [1758].TRF[30:30]	1
0xBB8004D8	L4_TRF1 [1759].TRF[31:31]	1
0xBB8004DC	L4_TRF1 [1760].TRF[0:0]	1
0xBB8004DC	L4_TRF1 [1761].TRF[1:1]	1
0xBB8004DC	L4_TRF1 [1762].TRF[2:2]	1
0xBB8004DC	L4_TRF1 [1763].TRF[3:3]	1
0xBB8004DC	L4_TRF1 [1764].TRF[4:4]	1
0xBB8004DC	L4_TRF1 [1765].TRF[5:5]	1
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0xBB8004DC	L4_TRF1 [1767].TRF[7:7]	1
0xBB8004DC	L4_TRF1 [1768].TRF[8:8]	1
0xBB8004DC	L4_TRF1 [1769].TRF[9:9]	1
0xBB8004DC	L4_TRF1 [1770].TRF[10:10]	1
0xBB8004DC	L4_TRF1 [1771].TRF[11:11]	1
0xBB8004DC	L4_TRF1 [1772].TRF[12:12]	1
0xBB8004DC	L4_TRF1 [1773].TRF[13:13]	1
0xBB8004DC	L4_TRF1 [1774].TRF[14:14]	1
0xBB8004DC	L4_TRF1 [1775].TRF[15:15]	1
0xBB8004DC	L4_TRF1 [1776].TRF[16:16]	1
0xBB8004DC	L4_TRF1 [1777].TRF[17:17]	1
0xBB8004DC	L4_TRF1 [1778].TRF[18:18]	1
0xBB8004DC	L4_TRF1 [1779].TRF[19:19]	1
0xBB8004DC	L4_TRF1 [1780].TRF[20:20]	1
0xBB8004DC	L4_TRF1 [1781].TRF[21:21]	1

Address	Register	Len
0xBB8004DC	L4_TRF1 [1782].TRF[22:22]	1
0xBB8004DC	L4_TRF1 [1783].TRF[23:23]	1
0xBB8004DC	L4_TRF1 [1784].TRF[24:24]	1
0xBB8004DC	L4_TRF1 [1785].TRF[25:25]	1
0xBB8004DC	L4_TRF1 [1786].TRF[26:26]	1
0xBB8004DC	L4_TRF1 [1787].TRF[27:27]	1
0xBB8004DC	L4_TRF1 [1788].TRF[28:28]	1
0xBB8004DC	L4_TRF1 [1789].TRF[29:29]	1
0xBB8004DC	L4_TRF1 [1790].TRF[30:30]	1
0xBB8004DC	L4_TRF1 [1791].TRF[31:31]	1
0xBB8004E0	L4_TRF1 [1792].TRF[0:0]	1
0xBB8004E0	L4_TRF1 [1793].TRF[1:1]	1
0xBB8004E0	L4_TRF1 [1794].TRF[2:2]	1
0xBB8004E0	L4_TRF1 [1795].TRF[3:3]	1
0xBB8004E0	L4_TRF1 [1796].TRF[4:4]	1
0xBB8004E0	L4_TRF1 [1797].TRF[5:5]	1
0xBB8004E0	L4_TRF1 [1798].TRF[6:6]	1
0xBB8004E0	L4_TRF1 [1799].TRF[7:7]	1
0xBB8004E0	L4_TRF1 [1800].TRF[8:8]	1
0xBB8004E0	L4_TRF1 [1801].TRF[9:9]	1
0xBB8004E0	L4_TRF1 [1802].TRF[10:10]	1
0xBB8004E0	L4_TRF1 [1803].TRF[11:11]	1
0xBB8004E0	L4_TRF1 [1804].TRF[12:12]	1
0xBB8004E0	L4_TRF1 [1805].TRF[13:13]	1
0xBB8004E0	L4_TRF1 [1806].TRF[14:14]	1
0xBB8004E0	L4_TRF1 [1807].TRF[15:15]	1
0xBB8004E0	L4_TRF1 [1808].TRF[16:16]	1
0xBB8004E0	L4_TRF1 [1809].TRF[17:17]	1
0xBB8004E0	L4_TRF1 [1810].TRF[18:18]	1
0xBB8004E0	L4_TRF1 [1811].TRF[19:19]	1
0xBB8004E0	L4_TRF1 [1812].TRF[20:20]	1
0xBB8004E0	L4_TRF1 [1813].TRF[21:21]	1
0xBB8004E0	L4_TRF1 [1814].TRF[22:22]	1
0xBB8004E0	L4_TRF1 [1815].TRF[23:23]	1
0xBB8004E0	L4_TRF1 [1816].TRF[24:24]	1
0xBB8004E0	L4_TRF1 [1817].TRF[25:25]	1
0xBB8004E0	L4_TRF1 [1818].TRF[26:26]	1
0xBB8004E0	L4_TRF1 [1819].TRF[27:27]	1
0xBB8004E0	L4_TRF1 [1820].TRF[28:28]	1
0xBB8004E0	L4_TRF1 [1821].TRF[29:29]	1
0xBB8004E0	L4_TRF1 [1822].TRF[30:30]	1
0xBB8004E0	L4_TRF1 [1823].TRF[31:31]	1
0xBB8004E4	L4_TRF1 [1824].TRF[0:0]	1
0xBB8004E4	L4_TRF1 [1825].TRF[1:1]	1
0xBB8004E4	L4_TRF1 [1826].TRF[2:2]	1
0xBB8004E4	L4_TRF1 [1827].TRF[3:3]	1

Address	Register	Len
0xBB8004E4	L4_TRF1 [1828].TRF[4:4]	1
0xBB8004E4	L4_TRF1 [1829].TRF[5:5]	1
0xBB8004E4	L4_TRF1 [1830].TRF[6:6]	1
0xBB8004E4	L4_TRF1 [1831].TRF[7:7]	1
0xBB8004E4	L4_TRF1 [1832].TRF[8:8]	1
0xBB8004E4	L4_TRF1 [1833].TRF[9:9]	1
0xBB8004E4	L4_TRF1 [1834].TRF[10:10]	1
0xBB8004E4	L4_TRF1 [1835].TRF[11:11]	1
0xBB8004E4	L4_TRF1 [1836].TRF[12:12]	1
0xBB8004E4	L4_TRF1 [1837].TRF[13:13]	1
0xBB8004E4	L4_TRF1 [1838].TRF[14:14]	1
0xBB8004E4	L4_TRF1 [1839].TRF[15:15]	1
0xBB8004E4	L4_TRF1 [1840].TRF[16:16]	1
0xBB8004E4	L4_TRF1 [1841].TRF[17:17]	1
0xBB8004E4	L4_TRF1 [1842].TRF[18:18]	1
0xBB8004E4	L4_TRF1 [1843].TRF[19:19]	1
0xBB8004E4	L4_TRF1 [1844].TRF[20:20]	1
0xBB8004E4	L4_TRF1 [1845].TRF[21:21]	1
0xBB8004E4	L4_TRF1 [1846].TRF[22:22]	1
0xBB8004E4	L4_TRF1 [1847].TRF[23:23]	1
0xBB8004E4	L4_TRF1 [1848].TRF[24:24]	1
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0xBB8004E4	L4_TRF1 [1850].TRF[26:26]	1
0xBB8004E4	L4_TRF1 [1851].TRF[27:27]	1
0xBB8004E4	L4_TRF1 [1852].TRF[28:28]	1
0xBB8004E4	L4_TRF1 [1853].TRF[29:29]	1
0xBB8004E4	L4_TRF1 [1854].TRF[30:30]	1
0xBB8004E4	L4_TRF1 [1855].TRF[31:31]	1
0xBB8004E8	L4_TRF1 [1856].TRF[0:0]	1
0xBB8004E8	L4_TRF1 [1857].TRF[1:1]	1
0xBB8004E8	L4_TRF1 [1858].TRF[2:2]	1
0xBB8004E8	L4_TRF1 [1859].TRF[3:3]	1
0xBB8004E8	L4_TRF1 [1860].TRF[4:4]	1
0xBB8004E8	L4_TRF1 [1861].TRF[5:5]	1
0xBB8004E8	L4_TRF1 [1862].TRF[6:6]	1
0xBB8004E8	L4_TRF1 [1863].TRF[7:7]	1
0xBB8004E8	L4_TRF1 [1864].TRF[8:8]	1
0xBB8004E8	L4_TRF1 [1865].TRF[9:9]	1
0xBB8004E8	L4_TRF1 [1866].TRF[10:10]	1
0xBB8004E8	L4_TRF1 [1867].TRF[11:11]	1
0xBB8004E8	L4_TRF1 [1868].TRF[12:12]	1
0xBB8004E8	L4_TRF1 [1869].TRF[13:13]	1
0xBB8004E8	L4_TRF1 [1870].TRF[14:14]	1
0xBB8004E8	L4_TRF1 [1871].TRF[15:15]	1
0xBB8004E8	L4_TRF1 [1872].TRF[16:16]	1
0xBB8004E8	L4_TRF1 [1873].TRF[17:17]	1



Address	Register	Len
0xBB8004E8	L4_TRF1 [1874].TRF[18:18]	1
0xBB8004E8	L4_TRF1 [1875].TRF[19:19]	1
0xBB8004E8	L4_TRF1 [1876].TRF[20:20]	1
0xBB8004E8	L4_TRF1 [1877].TRF[21:21]	1
0xBB8004E8	L4_TRF1 [1878].TRF[22:22]	1
0xBB8004E8	L4_TRF1 [1879].TRF[23:23]	1
0xBB8004E8	L4_TRF1 [1880].TRF[24:24]	1
0xBB8004E8	L4_TRF1 [1881].TRF[25:25]	1
0xBB8004E8	L4_TRF1 [1882].TRF[26:26]	1
0xBB8004E8	L4_TRF1 [1883].TRF[27:27]	1
0xBB8004E8	L4_TRF1 [1884].TRF[28:28]	1
0xBB8004E8	L4_TRF1 [1885].TRF[29:29]	1
0xBB8004E8	L4_TRF1 [1886].TRF[30:30]	1
0xBB8004E8	L4_TRF1 [1887].TRF[31:31]	1
0xBB8004EC	L4_TRF1 [1888].TRF[0:0]	1
0xBB8004EC	L4_TRF1 [1889].TRF[1:1]	1
0xBB8004EC	L4_TRF1 [1890].TRF[2:2]	1
0xBB8004EC	L4_TRF1 [1891].TRF[3:3]	1
0xBB8004EC	L4_TRF1 [1892].TRF[4:4]	1
0xBB8004EC	L4_TRF1 [1893].TRF[5:5]	1
0xBB8004EC	L4_TRF1 [1894].TRF[6:6]	1
0xBB8004EC	L4_TRF1 [1895].TRF[7:7]	1
0xBB8004EC	L4_TRF1 [1896].TRF[8:8]	1
0xBB8004EC	L4_TRF1 [1897].TRF[9:9]	1
0xBB8004EC	L4_TRF1 [1898].TRF[10:10]	1
0xBB8004EC	L4_TRF1 [1899].TRF[11:11]	1
0xBB8004EC	L4_TRF1 [1900].TRF[12:12]	1
0xBB8004EC	L4_TRF1 [1901].TRF[13:13]	1
0xBB8004EC	L4_TRF1 [1902].TRF[14:14]	1
0xBB8004EC	L4_TRF1 [1903].TRF[15:15]	1
0xBB8004EC	L4_TRF1 [1904].TRF[16:16]	1
0xBB8004EC	L4_TRF1 [1905].TRF[17:17]	1
0xBB8004EC	L4_TRF1 [1906].TRF[18:18]	1
0xBB8004EC	L4_TRF1 [1907].TRF[19:19]	1
0xBB8004EC	L4_TRF1 [1908].TRF[20:20]	1
0xBB8004EC	L4_TRF1 [1909].TRF[21:21]	1
0xBB8004EC	L4_TRF1 [1910].TRF[22:22]	1
0xBB8004EC	L4_TRF1 [1911].TRF[23:23]	1
0xBB8004EC	L4_TRF1 [1912].TRF[24:24]	1
0xBB8004EC	L4_TRF1 [1913].TRF[25:25]	1
0xBB8004EC	L4_TRF1 [1914].TRF[26:26]	1
0xBB8004EC	L4_TRF1 [1915].TRF[27:27]	1
0xBB8004EC	L4_TRF1 [1916].TRF[28:28]	1
0xBB8004EC	L4_TRF1 [1917].TRF[29:29]	1
0xBB8004EC	L4_TRF1 [1918].TRF[30:30]	1
0xBB8004EC	L4_TRF1 [1919].TRF[31:31]	1

Address	Register	Len
0xBB8004F0	L4_TRF1 [1920].TRF[0:0]	1
0xBB8004F0	L4_TRF1 [1921].TRF[1:1]	1
0xBB8004F0	L4_TRF1 [1922].TRF[2:2]	1
0xBB8004F0	L4_TRF1 [1923].TRF[3:3]	1
0xBB8004F0	L4_TRF1 [1924].TRF[4:4]	1
0xBB8004F0	L4_TRF1 [1925].TRF[5:5]	1
0xBB8004F0	L4_TRF1 [1926].TRF[6:6]	1
0xBB8004F0	L4_TRF1 [1927].TRF[7:7]	1
0xBB8004F0	L4_TRF1 [1928].TRF[8:8]	1
0xBB8004F0	L4_TRF1 [1929].TRF[9:9]	1
0xBB8004F0	L4_TRF1 [1930].TRF[10:10]	1
0xBB8004F0	L4_TRF1 [1931].TRF[11:11]	1
0xBB8004F0	L4_TRF1 [1932].TRF[12:12]	1
0xBB8004F0	L4_TRF1 [1933].TRF[13:13]	1
0xBB8004F0	L4_TRF1 [1934].TRF[14:14]	1
0xBB8004F0	L4_TRF1 [1935].TRF[15:15]	1
0xBB8004F0	L4_TRF1 [1936].TRF[16:16]	1
0xBB8004F0	L4_TRF1 [1937].TRF[17:17]	1
0xBB8004F0	L4_TRF1 [1938].TRF[18:18]	1
0xBB8004F0	L4_TRF1 [1939].TRF[19:19]	1
0xBB8004F0	L4_TRF1 [1940].TRF[20:20]	1
0xBB8004F0	L4_TRF1 [1941].TRF[21:21]	1
0xBB8004F0	L4_TRF1 [1942].TRF[22:22]	1
0xBB8004F0	L4_TRF1 [1943].TRF[23:23]	1
0xBB8004F0	L4_TRF1 [1944].TRF[24:24]	1
0xBB8004F0	L4_TRF1 [1945].TRF[25:25]	1
0xBB8004F0	L4_TRF1 [1946].TRF[26:26]	1
0xBB8004F0	L4_TRF1 [1947].TRF[27:27]	1
0xBB8004F0	L4_TRF1 [1948].TRF[28:28]	1
0xBB8004F0	L4_TRF1 [1949].TRF[29:29]	1
0xBB8004F0	L4_TRF1 [1950].TRF[30:30]	1
0xBB8004F0	L4_TRF1 [1951].TRF[31:31]	1
0xBB8004F4	L4_TRF1 [1952].TRF[0:0]	1
0xBB8004F4	L4_TRF1 [1953].TRF[1:1]	1
0xBB8004F4	L4_TRF1 [1954].TRF[2:2]	1
0xBB8004F4	L4_TRF1 [1955].TRF[3:3]	1
0xBB8004F4	L4_TRF1 [1956].TRF[4:4]	1
0xBB8004F4	L4_TRF1 [1957].TRF[5:5]	1
0xBB8004F4	L4_TRF1 [1958].TRF[6:6]	1
0xBB8004F4	L4_TRF1 [1959].TRF[7:7]	1
0xBB8004F4	L4_TRF1 [1960].TRF[8:8]	1
0xBB8004F4	L4_TRF1 [1961].TRF[9:9]	1
0xBB8004F4	L4_TRF1 [1962].TRF[10:10]	1
0xBB8004F4	L4_TRF1 [1963].TRF[11:11]	1
0xBB8004F4	L4_TRF1 [1964].TRF[12:12]	1
0xBB8004F4	L4_TRF1 [1965].TRF[13:13]	1

Address	Register	Len
0xBB8004F4	L4_TRF1 [1966].TRF[14:14]	1
0xBB8004F4	L4_TRF1 [1967].TRF[15:15]	1
0xBB8004F4	L4_TRF1 [1968].TRF[16:16]	1
0xBB8004F4	L4_TRF1 [1969].TRF[17:17]	1
0xBB8004F4	L4_TRF1 [1970].TRF[18:18]	1
0xBB8004F4	L4_TRF1 [1971].TRF[19:19]	1
0xBB8004F4	L4_TRF1 [1972].TRF[20:20]	1
0xBB8004F4	L4_TRF1 [1973].TRF[21:21]	1
0xBB8004F4	L4_TRF1 [1974].TRF[22:22]	1
0xBB8004F4	L4_TRF1 [1975].TRF[23:23]	1
0xBB8004F4	L4_TRF1 [1976].TRF[24:24]	1
0xBB8004F4	L4_TRF1 [1977].TRF[25:25]	1
0xBB8004F4	L4_TRF1 [1978].TRF[26:26]	1
0xBB8004F4	L4_TRF1 [1979].TRF[27:27]	1
0xBB8004F4	L4_TRF1 [1980].TRF[28:28]	1
0xBB8004F4	L4_TRF1 [1981].TRF[29:29]	1
0xBB8004F4	L4_TRF1 [1982].TRF[30:30]	1
0xBB8004F4	L4_TRF1 [1983].TRF[31:31]	1
0xBB8004F8	L4_TRF1 [1984].TRF[0:0]	1
0xBB8004F8	L4_TRF1 [1985].TRF[1:1]	1
0xBB8004F8	L4_TRF1 [1986].TRF[2:2]	1
0xBB8004F8	L4_TRF1 [1987].TRF[3:3]	1
0xBB8004F8	L4_TRF1 [1988].TRF[4:4]	1
0xBB8004F8	L4_TRF1 [1989].TRF[5:5]	1
0xBB8004F8	L4_TRF1 [1990].TRF[6:6]	1
0xBB8004F8	L4_TRF1 [1991].TRF[7:7]	1
0xBB8004F8	L4_TRF1 [1992].TRF[8:8]	1
0xBB8004F8	L4_TRF1 [1993].TRF[9:9]	1
0xBB8004F8	L4_TRF1 [1994].TRF[10:10]	1
0xBB8004F8	L4_TRF1 [1995].TRF[11:11]	1
0xBB8004F8	L4_TRF1 [1996].TRF[12:12]	1
0xBB8004F8	L4_TRF1 [1997].TRF[13:13]	1
0xBB8004F8	L4_TRF1 [1998].TRF[14:14]	1
0xBB8004F8	L4_TRF1 [1999].TRF[15:15]	1
0xBB8004F8	L4_TRF1 [2000].TRF[16:16]	1
0xBB8004F8	L4_TRF1 [2001].TRF[17:17]	1
0xBB8004F8	L4_TRF1 [2002].TRF[18:18]	1
0xBB8004F8	L4_TRF1 [2003].TRF[19:19]	1
0xBB8004F8	L4_TRF1 [2004].TRF[20:20]	1
0xBB8004F8	L4_TRF1 [2005].TRF[21:21]	1
0xBB8004F8	L4_TRF1 [2006].TRF[22:22]	1
0xBB8004F8	L4_TRF1 [2007].TRF[23:23]	1
0xBB8004F8	L4_TRF1 [2008].TRF[24:24]	1
0xBB8004F8	L4_TRF1 [2009].TRF[25:25]	1
0xBB8004F8	L4_TRF1 [2010].TRF[26:26]	1
0xBB8004F8	L4_TRF1 [2011].TRF[27:27]	1

Address	Register	Len
0xBB8004F8	L4_TRF1 [2012].TRF[28:28]	1
0xBB8004F8	L4_TRF1 [2013].TRF[29:29]	1
0xBB8004F8	L4_TRF1 [2014].TRF[30:30]	1
0xBB8004F8	L4_TRF1 [2015].TRF[31:31]	1
0xBB8004FC	L4_TRF1 [2016].TRF[0:0]	1
0xBB8004FC	L4_TRF1 [2017].TRF[1:1]	1
0xBB8004FC	L4_TRF1 [2018].TRF[2:2]	1
0xBB8004FC	L4_TRF1 [2019].TRF[3:3]	1
0xBB8004FC	L4_TRF1 [2020].TRF[4:4]	1
0xBB8004FC	L4_TRF1 [2021].TRF[5:5]	1
0xBB8004FC	L4_TRF1 [2022].TRF[6:6]	1
0xBB8004FC	L4_TRF1 [2023].TRF[7:7]	1
0xBB8004FC	L4_TRF1 [2024].TRF[8:8]	1
0xBB8004FC	L4_TRF1 [2025].TRF[9:9]	1
0xBB8004FC	L4_TRF1 [2026].TRF[10:10]	1
0xBB8004FC	L4_TRF1 [2027].TRF[11:11]	1
0xBB8004FC	L4_TRF1 [2028].TRF[12:12]	1
0xBB8004FC	L4_TRF1 [2029].TRF[13:13]	1
0xBB8004FC	L4_TRF1 [2030].TRF[14:14]	1
0xBB8004FC	L4_TRF1 [2031].TRF[15:15]	1
0xBB8004FC	L4_TRF1 [2032].TRF[16:16]	1
0xBB8004FC	L4_TRF1 [2033].TRF[17:17]	1
0xBB8004FC	L4_TRF1 [2034].TRF[18:18]	1
0xBB8004FC	L4_TRF1 [2035].TRF[19:19]	1
0xBB8004FC	L4_TRF1 [2036].TRF[20:20]	1
0xBB8004FC	L4_TRF1 [2037].TRF[21:21]	1
0xBB8004FC	L4_TRF1 [2038].TRF[22:22]	1
0xBB8004FC	L4_TRF1 [2039].TRF[23:23]	1
0xBB8004FC	L4_TRF1 [2040].TRF[24:24]	1
0xBB8004FC	L4_TRF1 [2041].TRF[25:25]	1
0xBB8004FC	L4_TRF1 [2042].TRF[26:26]	1
0xBB8004FC	L4_TRF1 [2043].TRF[27:27]	1
0xBB8004FC	L4_TRF1 [2044].TRF[28:28]	1
0xBB8004FC	L4_TRF1 [2045].TRF[29:29]	1
0xBB8004FC	L4_TRF1 [2046].TRF[30:30]	1
0xBB8004FC	L4_TRF1 [2047].TRF[31:31]	1
0xBB800500	ARP_TRF0 [0].TRF[0:0]	1
0xBB800500	ARP_TRF0 [1].TRF[1:1]	1
0xBB800500	ARP_TRF0 [2].TRF[2:2]	1
0xBB800500	ARP_TRF0 [3].TRF[3:3]	1
0xBB800500	ARP_TRF0 [4].TRF[4:4]	1
0xBB800500	ARP_TRF0 [5].TRF[5:5]	1
0xBB800500	ARP_TRF0 [6].TRF[6:6]	1
0xBB800500	ARP_TRF0 [7].TRF[7:7]	1
0xBB800500	ARP_TRF0 [8].TRF[8:8]	1
0xBB800500	ARP_TRF0 [9].TRF[9:9]	1

Address	Register	Len
0xBB800500	ARP_TRF0 [10].TRF[10:10]	1
0xBB800500	ARP_TRF0 [11].TRF[11:11]	1
0xBB800500	ARP_TRF0 [12].TRF[12:12]	1
0xBB800500	ARP_TRF0 [13].TRF[13:13]	1
0xBB800500	ARP_TRF0 [14].TRF[14:14]	1
0xBB800500	ARP_TRF0 [15].TRF[15:15]	1
0xBB800500	ARP_TRF0 [16].TRF[16:16]	1
0xBB800500	ARP_TRF0 [17].TRF[17:17]	1
0xBB800500	ARP_TRF0 [18].TRF[18:18]	1
0xBB800500	ARP_TRF0 [19].TRF[19:19]	1
0xBB800500	ARP_TRF0 [20].TRF[20:20]	1
0xBB800500	ARP_TRF0 [21].TRF[21:21]	1
0xBB800500	ARP_TRF0 [22].TRF[22:22]	1
0xBB800500	ARP_TRF0 [23].TRF[23:23]	1
0xBB800500	ARP_TRF0 [24].TRF[24:24]	1
0xBB800500	ARP_TRF0 [25].TRF[25:25]	1
0xBB800500	ARP_TRF0 [26].TRF[26:26]	1
0xBB800500	ARP_TRF0 [27].TRF[27:27]	1
0xBB800500	ARP_TRF0 [28].TRF[28:28]	1
0xBB800500	ARP_TRF0 [29].TRF[29:29]	1
0xBB800500	ARP_TRF0 [30].TRF[30:30]	1
0xBB800500	ARP_TRF0 [31].TRF[31:31]	1
0xBB800504	ARP_TRF0 [32].TRF[0:0]	1
0xBB800504	ARP_TRF0 [33].TRF[1:1]	1
0xBB800504	ARP_TRF0 [34].TRF[2:2]	1
0xBB800504	ARP_TRF0 [35].TRF[3:3]	1
0xBB800504	ARP_TRF0 [36].TRF[4:4]	1
0xBB800504	ARP_TRF0 [37].TRF[5:5]	1
0xBB800504	ARP_TRF0 [38].TRF[6:6]	1
0xBB800504	ARP_TRF0 [39].TRF[7:7]	1
0xBB800504	ARP_TRF0 [40].TRF[8:8]	1
0xBB800504	ARP_TRF0 [41].TRF[9:9]	1
0xBB800504	ARP_TRF0 [42].TRF[10:10]	1
0xBB800504	ARP_TRF0 [43].TRF[11:11]	1
0xBB800504	ARP_TRF0 [44].TRF[12:12]	1
0xBB800504	ARP_TRF0 [45].TRF[13:13]	1
0xBB800504	ARP_TRF0 [46].TRF[14:14]	1
0xBB800504	ARP_TRF0 [47].TRF[15:15]	1
0xBB800504	ARP_TRF0 [48].TRF[16:16]	1
0xBB800504	ARP_TRF0 [49].TRF[17:17]	1
0xBB800504	ARP_TRF0 [50].TRF[18:18]	1
0xBB800504	ARP_TRF0 [51].TRF[19:19]	1
0xBB800504	ARP_TRF0 [52].TRF[20:20]	1
0xBB800504	ARP_TRF0 [53].TRF[21:21]	1
0xBB800504	ARP_TRF0 [54].TRF[22:22]	1
0xBB800504	ARP_TRF0 [55].TRF[23:23]	1

Address	Register	Len
0xBB800504	ARP_TRF0 [56].TRF[24:24]	1
0xBB800504	ARP_TRF0 [57].TRF[25:25]	1
0xBB800504	ARP_TRF0 [58].TRF[26:26]	1
0xBB800504	ARP_TRF0 [59].TRF[27:27]	1
0xBB800504	ARP_TRF0 [60].TRF[28:28]	1
0xBB800504	ARP_TRF0 [61].TRF[29:29]	1
0xBB800504	ARP_TRF0 [62].TRF[30:30]	1
0xBB800504	ARP_TRF0 [63].TRF[31:31]	1
0xBB800508	ARP_TRF0 [64].TRF[0:0]	1
0xBB800508	ARP_TRF0 [65].TRF[1:1]	1
0xBB800508	ARP_TRF0 [66].TRF[2:2]	1
0xBB800508	ARP_TRF0 [67].TRF[3:3]	1
0xBB800508	ARP_TRF0 [68].TRF[4:4]	1
0xBB800508	ARP_TRF0 [69].TRF[5:5]	1
0xBB800508	ARP_TRF0 [70].TRF[6:6]	1
0xBB800508	ARP_TRF0 [71].TRF[7:7]	1
0xBB800508	ARP_TRF0 [72].TRF[8:8]	1
0xBB800508	ARP_TRF0 [73].TRF[9:9]	1
0xBB800508	ARP_TRF0 [74].TRF[10:10]	1
0xBB800508	ARP_TRF0 [75].TRF[11:11]	1
0xBB800508	ARP_TRF0 [76].TRF[12:12]	1
0xBB800508	ARP_TRF0 [77].TRF[13:13]	1
0xBB800508	ARP_TRF0 [78].TRF[14:14]	1
0xBB800508	ARP_TRF0 [79].TRF[15:15]	1
0xBB800508	ARP_TRF0 [80].TRF[16:16]	1
0xBB800508	ARP_TRF0 [81].TRF[17:17]	1
0xBB800508	ARP_TRF0 [82].TRF[18:18]	1
0xBB800508	ARP_TRF0 [83].TRF[19:19]	1
0xBB800508	ARP_TRF0 [84].TRF[20:20]	1
0xBB800508	ARP_TRF0 [85].TRF[21:21]	1
0xBB800508	ARP_TRF0 [86].TRF[22:22]	1
0xBB800508	ARP_TRF0 [87].TRF[23:23]	1
0xBB800508	ARP_TRF0 [88].TRF[24:24]	1
0xBB800508	ARP_TRF0 [89].TRF[25:25]	1
0xBB800508	ARP_TRF0 [90].TRF[26:26]	1
0xBB800508	ARP_TRF0 [91].TRF[27:27]	1
0xBB800508	ARP_TRF0 [92].TRF[28:28]	1
0xBB800508	ARP_TRF0 [93].TRF[29:29]	1
0xBB800508	ARP_TRF0 [94].TRF[30:30]	1
0xBB800508	ARP_TRF0 [95].TRF[31:31]	1
0xBB80050C	ARP_TRF0 [96].TRF[0:0]	1
0xBB80050C	ARP_TRF0 [97].TRF[1:1]	1
0xBB80050C	ARP_TRF0 [98].TRF[2:2]	1
0xBB80050C	ARP_TRF0 [99].TRF[3:3]	1
0xBB80050C	ARP_TRF0 [100].TRF[4:4]	1
0xBB80050C	ARP_TRF0 [101].TRF[5:5]	1

Address	Register	Len
0xBB80050C	ARP_TRF0 [102].TRF[6:6]	1
0xBB80050C	ARP_TRF0 [103].TRF[7:7]	1
0xBB80050C	ARP_TRF0 [104].TRF[8:8]	1
0xBB80050C	ARP_TRF0 [105].TRF[9:9]	1
0xBB80050C	ARP_TRF0 [106].TRF[10:10]	1
0xBB80050C	ARP_TRF0 [107].TRF[11:11]	1
0xBB80050C	ARP_TRF0 [108].TRF[12:12]	1
0xBB80050C	ARP_TRF0 [109].TRF[13:13]	1
0xBB80050C	ARP_TRF0 [110].TRF[14:14]	1
0xBB80050C	ARP_TRF0 [111].TRF[15:15]	1
0xBB80050C	ARP_TRF0 [112].TRF[16:16]	1
0xBB80050C	ARP_TRF0 [113].TRF[17:17]	1
0xBB80050C	ARP_TRF0 [114].TRF[18:18]	1
0xBB80050C	ARP_TRF0 [115].TRF[19:19]	1
0xBB80050C	ARP_TRF0 [116].TRF[20:20]	1
0xBB80050C	ARP_TRF0 [117].TRF[21:21]	1
0xBB80050C	ARP_TRF0 [118].TRF[22:22]	1
0xBB80050C	ARP_TRF0 [119].TRF[23:23]	1
0xBB80050C	ARP_TRF0 [120].TRF[24:24]	1
0xBB80050C	ARP_TRF0 [121].TRF[25:25]	1
0xBB80050C	ARP_TRF0 [122].TRF[26:26]	1
0xBB80050C	ARP_TRF0 [123].TRF[27:27]	1
0xBB80050C	ARP_TRF0 [124].TRF[28:28]	1
0xBB80050C	ARP_TRF0 [125].TRF[29:29]	1
0xBB80050C	ARP_TRF0 [126].TRF[30:30]	1
0xBB80050C	ARP_TRF0 [127].TRF[31:31]	1
0xBB800510	ARP_TRF0 [128].TRF[0:0]	1
0xBB800510	ARP_TRF0 [129].TRF[1:1]	1
0xBB800510	ARP_TRF0 [130].TRF[2:2]	1
0xBB800510	ARP_TRF0 [131].TRF[3:3]	1
0xBB800510	ARP_TRF0 [132].TRF[4:4]	1
0xBB800510	ARP_TRF0 [133].TRF[5:5]	1
0xBB800510	ARP_TRF0 [134].TRF[6:6]	1
0xBB800510	ARP_TRF0 [135].TRF[7:7]	1
0xBB800510	ARP_TRF0 [136].TRF[8:8]	1
0xBB800510	ARP_TRF0 [137].TRF[9:9]	1
0xBB800510	ARP_TRF0 [138].TRF[10:10]	1
0xBB800510	ARP_TRF0 [139].TRF[11:11]	1
0xBB800510	ARP_TRF0 [140].TRF[12:12]	1
0xBB800510	ARP_TRF0 [141].TRF[13:13]	1
0xBB800510	ARP_TRF0 [142].TRF[14:14]	1
0xBB800510	ARP_TRF0 [143].TRF[15:15]	1
0xBB800510	ARP_TRF0 [144].TRF[16:16]	1
0xBB800510	ARP_TRF0 [145].TRF[17:17]	1
0xBB800510	ARP_TRF0 [146].TRF[18:18]	1
0xBB800510	ARP_TRF0 [147].TRF[19:19]	1

Address	Register	Len
0xBB800510	ARP_TRF0 [148].TRF[20:20]	1
0xBB800510	ARP_TRF0 [149].TRF[21:21]	1
0xBB800510	ARP_TRF0 [150].TRF[22:22]	1
0xBB800510	ARP_TRF0 [151].TRF[23:23]	1
0xBB800510	ARP_TRF0 [152].TRF[24:24]	1
0xBB800510	ARP_TRF0 [153].TRF[25:25]	1
0xBB800510	ARP_TRF0 [154].TRF[26:26]	1
0xBB800510	ARP_TRF0 [155].TRF[27:27]	1
0xBB800510	ARP_TRF0 [156].TRF[28:28]	1
0xBB800510	ARP_TRF0 [157].TRF[29:29]	1
0xBB800510	ARP_TRF0 [158].TRF[30:30]	1
0xBB800510	ARP_TRF0 [159].TRF[31:31]	1
0xBB800514	ARP_TRF0 [160].TRF[0:0]	1
0xBB800514	ARP_TRF0 [161].TRF[1:1]	1
0xBB800514	ARP_TRF0 [162].TRF[2:2]	1
0xBB800514	ARP_TRF0 [163].TRF[3:3]	1
0xBB800514	ARP_TRF0 [164].TRF[4:4]	1
0xBB800514	ARP_TRF0 [165].TRF[5:5]	1
0xBB800514	ARP_TRF0 [166].TRF[6:6]	1
0xBB800514	ARP_TRF0 [167].TRF[7:7]	1
0xBB800514	ARP_TRF0 [168].TRF[8:8]	1
0xBB800514	ARP_TRF0 [169].TRF[9:9]	1
0xBB800514	ARP_TRF0 [170].TRF[10:10]	1
0xBB800514	ARP_TRF0 [171].TRF[11:11]	1
0xBB800514	ARP_TRF0 [172].TRF[12:12]	1
0xBB800514	ARP_TRF0 [173].TRF[13:13]	1
0xBB800514	ARP_TRF0 [174].TRF[14:14]	1
0xBB800514	ARP_TRF0 [175].TRF[15:15]	1
0xBB800514	ARP_TRF0 [176].TRF[16:16]	1
0xBB800514	ARP_TRF0 [177].TRF[17:17]	1
0xBB800514	ARP_TRF0 [178].TRF[18:18]	1
0xBB800514	ARP_TRF0 [179].TRF[19:19]	1
0xBB800514	ARP_TRF0 [180].TRF[20:20]	1
0xBB800514	ARP_TRF0 [181].TRF[21:21]	1
0xBB800514	ARP_TRF0 [182].TRF[22:22]	1
0xBB800514	ARP_TRF0 [183].TRF[23:23]	1
0xBB800514	ARP_TRF0 [184].TRF[24:24]	1
0xBB800514	ARP_TRF0 [185].TRF[25:25]	1
0xBB800514	ARP_TRF0 [186].TRF[26:26]	1
0xBB800514	ARP_TRF0 [187].TRF[27:27]	1
0xBB800514	ARP_TRF0 [188].TRF[28:28]	1
0xBB800514	ARP_TRF0 [189].TRF[29:29]	1
0xBB800514	ARP_TRF0 [190].TRF[30:30]	1
0xBB800514	ARP_TRF0 [191].TRF[31:31]	1
0xBB800518	ARP_TRF0 [192].TRF[0:0]	1
0xBB800518	ARP_TRF0 [193].TRF[1:1]	1



Address	Register	Len
0xBB800518	ARP_TRF0 [194].TRF[2:2]	1
0xBB800518	ARP_TRF0 [195].TRF[3:3]	1
0xBB800518	ARP_TRF0 [196].TRF[4:4]	1
0xBB800518	ARP_TRF0 [197].TRF[5:5]	1
0xBB800518	ARP_TRF0 [198].TRF[6:6]	1
0xBB800518	ARP_TRF0 [199].TRF[7:7]	1
0xBB800518	ARP_TRF0 [200].TRF[8:8]	1
0xBB800518	ARP_TRF0 [201].TRF[9:9]	1
0xBB800518	ARP_TRF0 [202].TRF[10:10]	1
0xBB800518	ARP_TRF0 [203].TRF[11:11]	1
0xBB800518	ARP_TRF0 [204].TRF[12:12]	1
0xBB800518	ARP_TRF0 [205].TRF[13:13]	1
0xBB800518	ARP_TRF0 [206].TRF[14:14]	1
0xBB800518	ARP_TRF0 [207].TRF[15:15]	1
0xBB800518	ARP_TRF0 [208].TRF[16:16]	1
0xBB800518	ARP_TRF0 [209].TRF[17:17]	1
0xBB800518	ARP_TRF0 [210].TRF[18:18]	1
0xBB800518	ARP_TRF0 [211].TRF[19:19]	1
0xBB800518	ARP_TRF0 [212].TRF[20:20]	1
0xBB800518	ARP_TRF0 [213].TRF[21:21]	1
0xBB800518	ARP_TRF0 [214].TRF[22:22]	1
0xBB800518	ARP_TRF0 [215].TRF[23:23]	1
0xBB800518	ARP_TRF0 [216].TRF[24:24]	1
0xBB800518	ARP_TRF0 [217].TRF[25:25]	1
0xBB800518	ARP_TRF0 [218].TRF[26:26]	1
0xBB800518	ARP_TRF0 [219].TRF[27:27]	1
0xBB800518	ARP_TRF0 [220].TRF[28:28]	1
0xBB800518	ARP_TRF0 [221].TRF[29:29]	1
0xBB800518	ARP_TRF0 [222].TRF[30:30]	1
0xBB800518	ARP_TRF0 [223].TRF[31:31]	1
0xBB80051C	ARP_TRF0 [224].TRF[0:0]	1
0xBB80051C	ARP_TRF0 [225].TRF[1:1]	1
0xBB80051C	ARP_TRF0 [226].TRF[2:2]	1
0xBB80051C	ARP_TRF0 [227].TRF[3:3]	1
0xBB80051C	ARP_TRF0 [228].TRF[4:4]	1
0xBB80051C	ARP_TRF0 [229].TRF[5:5]	1
0xBB80051C	ARP_TRF0 [230].TRF[6:6]	1
0xBB80051C	ARP_TRF0 [231].TRF[7:7]	1
0xBB80051C	ARP_TRF0 [232].TRF[8:8]	1
0xBB80051C	ARP_TRF0 [233].TRF[9:9]	1
0xBB80051C	ARP_TRF0 [234].TRF[10:10]	1
0xBB80051C	ARP_TRF0 [235].TRF[11:11]	1
0xBB80051C	ARP_TRF0 [236].TRF[12:12]	1
0xBB80051C	ARP_TRF0 [237].TRF[13:13]	1
0xBB80051C	ARP_TRF0 [238].TRF[14:14]	1
0xBB80051C	ARP_TRF0 [239].TRF[15:15]	1

Address	Register	Len
0xBB80051C	ARP_TRF0 [240].TRF[16:16]	1
0xBB80051C	ARP_TRF0 [241].TRF[17:17]	1
0xBB80051C	ARP_TRF0 [242].TRF[18:18]	1
0xBB80051C	ARP_TRF0 [243].TRF[19:19]	1
0xBB80051C	ARP_TRF0 [244].TRF[20:20]	1
0xBB80051C	ARP_TRF0 [245].TRF[21:21]	1
0xBB80051C	ARP_TRF0 [246].TRF[22:22]	1
0xBB80051C	ARP_TRF0 [247].TRF[23:23]	1
0xBB80051C	ARP_TRF0 [248].TRF[24:24]	1
0xBB80051C	ARP_TRF0 [249].TRF[25:25]	1
0xBB80051C	ARP_TRF0 [250].TRF[26:26]	1
0xBB80051C	ARP_TRF0 [251].TRF[27:27]	1
0xBB80051C	ARP_TRF0 [252].TRF[28:28]	1
0xBB80051C	ARP_TRF0 [253].TRF[29:29]	1
0xBB80051C	ARP_TRF0 [254].TRF[30:30]	1
0xBB80051C	ARP_TRF0 [255].TRF[31:31]	1
0xBB800520	ARP_TRF0 [256].TRF[0:0]	1
0xBB800520	ARP_TRF0 [257].TRF[1:1]	1
0xBB800520	ARP_TRF0 [258].TRF[2:2]	1
0xBB800520	ARP_TRF0 [259].TRF[3:3]	1
0xBB800520	ARP_TRF0 [260].TRF[4:4]	1
0xBB800520	ARP_TRF0 [261].TRF[5:5]	1
0xBB800520	ARP_TRF0 [262].TRF[6:6]	1
0xBB800520	ARP_TRF0 [263].TRF[7:7]	1
0xBB800520	ARP_TRF0 [264].TRF[8:8]	1
0xBB800520	ARP_TRF0 [265].TRF[9:9]	1
0xBB800520	ARP_TRF0 [266].TRF[10:10]	1
0xBB800520	ARP_TRF0 [267].TRF[11:11]	1
0xBB800520	ARP_TRF0 [268].TRF[12:12]	1
0xBB800520	ARP_TRF0 [269].TRF[13:13]	1
0xBB800520	ARP_TRF0 [270].TRF[14:14]	1
0xBB800520	ARP_TRF0 [271].TRF[15:15]	1
0xBB800520	ARP_TRF0 [272].TRF[16:16]	1
0xBB800520	ARP_TRF0 [273].TRF[17:17]	1
0xBB800520	ARP_TRF0 [274].TRF[18:18]	1
0xBB800520	ARP_TRF0 [275].TRF[19:19]	1
0xBB800520	ARP_TRF0 [276].TRF[20:20]	1
0xBB800520	ARP_TRF0 [277].TRF[21:21]	1
0xBB800520	ARP_TRF0 [278].TRF[22:22]	1
0xBB800520	ARP_TRF0 [279].TRF[23:23]	1
0xBB800520	ARP_TRF0 [280].TRF[24:24]	1
0xBB800520	ARP_TRF0 [281].TRF[25:25]	1
0xBB800520	ARP_TRF0 [282].TRF[26:26]	1
0xBB800520	ARP_TRF0 [283].TRF[27:27]	1
0xBB800520	ARP_TRF0 [284].TRF[28:28]	1
0xBB800520	ARP_TRF0 [285].TRF[29:29]	1

Address	Register	Len
0xBB800520	ARP_TRF0 [286].TRF[30:30]	1
0xBB800520	ARP_TRF0 [287].TRF[31:31]	1
0xBB800524	ARP_TRF0 [288].TRF[0:0]	1
0xBB800524	ARP_TRF0 [289].TRF[1:1]	1
0xBB800524	ARP_TRF0 [290].TRF[2:2]	1
0xBB800524	ARP_TRF0 [291].TRF[3:3]	1
0xBB800524	ARP_TRF0 [292].TRF[4:4]	1
0xBB800524	ARP_TRF0 [293].TRF[5:5]	1
0xBB800524	ARP_TRF0 [294].TRF[6:6]	1
0xBB800524	ARP_TRF0 [295].TRF[7:7]	1
0xBB800524	ARP_TRF0 [296].TRF[8:8]	1
0xBB800524	ARP_TRF0 [297].TRF[9:9]	1
0xBB800524	ARP_TRF0 [298].TRF[10:10]	1
0xBB800524	ARP_TRF0 [299].TRF[11:11]	1
0xBB800524	ARP_TRF0 [300].TRF[12:12]	1
0xBB800524	ARP_TRF0 [301].TRF[13:13]	1
0xBB800524	ARP_TRF0 [302].TRF[14:14]	1
0xBB800524	ARP_TRF0 [303].TRF[15:15]	1
0xBB800524	ARP_TRF0 [304].TRF[16:16]	1
0xBB800524	ARP_TRF0 [305].TRF[17:17]	1
0xBB800524	ARP_TRF0 [306].TRF[18:18]	1
0xBB800524	ARP_TRF0 [307].TRF[19:19]	1
0xBB800524	ARP_TRF0 [308].TRF[20:20]	1
0xBB800524	ARP_TRF0 [309].TRF[21:21]	1
0xBB800524	ARP_TRF0 [310].TRF[22:22]	1
0xBB800524	ARP_TRF0 [311].TRF[23:23]	1
0xBB800524	ARP_TRF0 [312].TRF[24:24]	1
0xBB800524	ARP_TRF0 [313].TRF[25:25]	1
0xBB800524	ARP_TRF0 [314].TRF[26:26]	1
0xBB800524	ARP_TRF0 [315].TRF[27:27]	1
0xBB800524	ARP_TRF0 [316].TRF[28:28]	1
0xBB800524	ARP_TRF0 [317].TRF[29:29]	1
0xBB800524	ARP_TRF0 [318].TRF[30:30]	1
0xBB800524	ARP_TRF0 [319].TRF[31:31]	1
0xBB800528	ARP_TRF0 [320].TRF[0:0]	1
0xBB800528	ARP_TRF0 [321].TRF[1:1]	1
0xBB800528	ARP_TRF0 [322].TRF[2:2]	1
0xBB800528	ARP_TRF0 [323].TRF[3:3]	1
0xBB800528	ARP_TRF0 [324].TRF[4:4]	1
0xBB800528	ARP_TRF0 [325].TRF[5:5]	1
0xBB800528	ARP_TRF0 [326].TRF[6:6]	1
0xBB800528	ARP_TRF0 [327].TRF[7:7]	1
0xBB800528	ARP_TRF0 [328].TRF[8:8]	1
0xBB800528	ARP_TRF0 [329].TRF[9:9]	1
0xBB800528	ARP_TRF0 [330].TRF[10:10]	1
0xBB800528	ARP_TRF0 [331].TRF[11:11]	1

Address	Register	Len
0xBB800528	ARP_TRF0 [332].TRF[12:12]	1
0xBB800528	ARP_TRF0 [333].TRF[13:13]	1
0xBB800528	ARP_TRF0 [334].TRF[14:14]	1
0xBB800528	ARP_TRF0 [335].TRF[15:15]	1
0xBB800528	ARP_TRF0 [336].TRF[16:16]	1
0xBB800528	ARP_TRF0 [337].TRF[17:17]	1
0xBB800528	ARP_TRF0 [338].TRF[18:18]	1
0xBB800528	ARP_TRF0 [339].TRF[19:19]	1
0xBB800528	ARP_TRF0 [340].TRF[20:20]	1
0xBB800528	ARP_TRF0 [341].TRF[21:21]	1
0xBB800528	ARP_TRF0 [342].TRF[22:22]	1
0xBB800528	ARP_TRF0 [343].TRF[23:23]	1
0xBB800528	ARP_TRF0 [344].TRF[24:24]	1
0xBB800528	ARP_TRF0 [345].TRF[25:25]	1
0xBB800528	ARP_TRF0 [346].TRF[26:26]	1
0xBB800528	ARP_TRF0 [347].TRF[27:27]	1
0xBB800528	ARP_TRF0 [348].TRF[28:28]	1
0xBB800528	ARP_TRF0 [349].TRF[29:29]	1
0xBB800528	ARP_TRF0 [350].TRF[30:30]	1
0xBB800528	ARP_TRF0 [351].TRF[31:31]	1
0xBB80052C	ARP_TRF0 [352].TRF[0:0]	1
0xBB80052C	ARP_TRF0 [353].TRF[1:1]	1
0xBB80052C	ARP_TRF0 [354].TRF[2:2]	1
0xBB80052C	ARP_TRF0 [355].TRF[3:3]	1
0xBB80052C	ARP_TRF0 [356].TRF[4:4]	1
0xBB80052C	ARP_TRF0 [357].TRF[5:5]	1
0xBB80052C	ARP_TRF0 [358].TRF[6:6]	1
0xBB80052C	ARP_TRF0 [359].TRF[7:7]	1
0xBB80052C	ARP_TRF0 [360].TRF[8:8]	1
0xBB80052C	ARP_TRF0 [361].TRF[9:9]	1
0xBB80052C	ARP_TRF0 [362].TRF[10:10]	1
0xBB80052C	ARP_TRF0 [363].TRF[11:11]	1
0xBB80052C	ARP_TRF0 [364].TRF[12:12]	1
0xBB80052C	ARP_TRF0 [365].TRF[13:13]	1
0xBB80052C	ARP_TRF0 [366].TRF[14:14]	1
0xBB80052C	ARP_TRF0 [367].TRF[15:15]	1
0xBB80052C	ARP_TRF0 [368].TRF[16:16]	1
0xBB80052C	ARP_TRF0 [369].TRF[17:17]	1
0xBB80052C	ARP_TRF0 [370].TRF[18:18]	1
0xBB80052C	ARP_TRF0 [371].TRF[19:19]	1
0xBB80052C	ARP_TRF0 [372].TRF[20:20]	1
0xBB80052C	ARP_TRF0 [373].TRF[21:21]	1
0xBB80052C	ARP_TRF0 [374].TRF[22:22]	1
0xBB80052C	ARP_TRF0 [375].TRF[23:23]	1
0xBB80052C	ARP_TRF0 [376].TRF[24:24]	1
0xBB80052C	ARP_TRF0 [377].TRF[25:25]	1

Address	Register	Len
0xBB80052C	ARP_TRF0 [378].TRF[26:26]	1
0xBB80052C	ARP_TRF0 [379].TRF[27:27]	1
0xBB80052C	ARP_TRF0 [380].TRF[28:28]	1
0xBB80052C	ARP_TRF0 [381].TRF[29:29]	1
0xBB80052C	ARP_TRF0 [382].TRF[30:30]	1
0xBB80052C	ARP_TRF0 [383].TRF[31:31]	1
0xBB800530	ARP_TRF0 [384].TRF[0:0]	1
0xBB800530	ARP_TRF0 [385].TRF[1:1]	1
0xBB800530	ARP_TRF0 [386].TRF[2:2]	1
0xBB800530	ARP_TRF0 [387].TRF[3:3]	1
0xBB800530	ARP_TRF0 [388].TRF[4:4]	1
0xBB800530	ARP_TRF0 [389].TRF[5:5]	1
0xBB800530	ARP_TRF0 [390].TRF[6:6]	1
0xBB800530	ARP_TRF0 [391].TRF[7:7]	1
0xBB800530	ARP_TRF0 [392].TRF[8:8]	1
0xBB800530	ARP_TRF0 [393].TRF[9:9]	1
0xBB800530	ARP_TRF0 [394].TRF[10:10]	1
0xBB800530	ARP_TRF0 [395].TRF[11:11]	1
0xBB800530	ARP_TRF0 [396].TRF[12:12]	1
0xBB800530	ARP_TRF0 [397].TRF[13:13]	1
0xBB800530	ARP_TRF0 [398].TRF[14:14]	1
0xBB800530	ARP_TRF0 [399].TRF[15:15]	1
0xBB800530	ARP_TRF0 [400].TRF[16:16]	1
0xBB800530	ARP_TRF0 [401].TRF[17:17]	1
0xBB800530	ARP_TRF0 [402].TRF[18:18]	1
0xBB800530	ARP_TRF0 [403].TRF[19:19]	1
0xBB800530	ARP_TRF0 [404].TRF[20:20]	1
0xBB800530	ARP_TRF0 [405].TRF[21:21]	1
0xBB800530	ARP_TRF0 [406].TRF[22:22]	1
0xBB800530	ARP_TRF0 [407].TRF[23:23]	1
0xBB800530	ARP_TRF0 [408].TRF[24:24]	1
0xBB800530	ARP_TRF0 [409].TRF[25:25]	1
0xBB800530	ARP_TRF0 [410].TRF[26:26]	1
0xBB800530	ARP_TRF0 [411].TRF[27:27]	1
0xBB800530	ARP_TRF0 [412].TRF[28:28]	1
0xBB800530	ARP_TRF0 [413].TRF[29:29]	1
0xBB800530	ARP_TRF0 [414].TRF[30:30]	1
0xBB800530	ARP_TRF0 [415].TRF[31:31]	1
0xBB800534	ARP_TRF0 [416].TRF[0:0]	1
0xBB800534	ARP_TRF0 [417].TRF[1:1]	1
0xBB800534	ARP_TRF0 [418].TRF[2:2]	1
0xBB800534	ARP_TRF0 [419].TRF[3:3]	1
0xBB800534	ARP_TRF0 [420].TRF[4:4]	1
0xBB800534	ARP_TRF0 [421].TRF[5:5]	1
0xBB800534	ARP_TRF0 [422].TRF[6:6]	1
0xBB800534	ARP_TRF0 [423].TRF[7:7]	1

Address	Register	Len
0xBB800534	ARP_TRF0 [424].TRF[8:8]	1
0xBB800534	ARP_TRF0 [425].TRF[9:9]	1
0xBB800534	ARP_TRF0 [426].TRF[10:10]	1
0xBB800534	ARP_TRF0 [427].TRF[11:11]	1
0xBB800534	ARP_TRF0 [428].TRF[12:12]	1
0xBB800534	ARP_TRF0 [429].TRF[13:13]	1
0xBB800534	ARP_TRF0 [430].TRF[14:14]	1
0xBB800534	ARP_TRF0 [431].TRF[15:15]	1
0xBB800534	ARP_TRF0 [432].TRF[16:16]	1
0xBB800534	ARP_TRF0 [433].TRF[17:17]	1
0xBB800534	ARP_TRF0 [434].TRF[18:18]	1
0xBB800534	ARP_TRF0 [435].TRF[19:19]	1
0xBB800534	ARP_TRF0 [436].TRF[20:20]	1
0xBB800534	ARP_TRF0 [437].TRF[21:21]	1
0xBB800534	ARP_TRF0 [438].TRF[22:22]	1
0xBB800534	ARP_TRF0 [439].TRF[23:23]	1
0xBB800534	ARP_TRF0 [440].TRF[24:24]	1
0xBB800534	ARP_TRF0 [441].TRF[25:25]	1
0xBB800534	ARP_TRF0 [442].TRF[26:26]	1
0xBB800534	ARP_TRF0 [443].TRF[27:27]	1
0xBB800534	ARP_TRF0 [444].TRF[28:28]	1
0xBB800534	ARP_TRF0 [445].TRF[29:29]	1
0xBB800534	ARP_TRF0 [446].TRF[30:30]	1
0xBB800534	ARP_TRF0 [447].TRF[31:31]	1
0xBB800538	ARP_TRF0 [448].TRF[0:0]	1
0xBB800538	ARP_TRF0 [449].TRF[1:1]	1
0xBB800538	ARP_TRF0 [450].TRF[2:2]	1
0xBB800538	ARP_TRF0 [451].TRF[3:3]	1
0xBB800538	ARP_TRF0 [452].TRF[4:4]	1
0xBB800538	ARP_TRF0 [453].TRF[5:5]	1
0xBB800538	ARP_TRF0 [454].TRF[6:6]	1
0xBB800538	ARP_TRF0 [455].TRF[7:7]	1
0xBB800538	ARP_TRF0 [456].TRF[8:8]	1
0xBB800538	ARP_TRF0 [457].TRF[9:9]	1
0xBB800538	ARP_TRF0 [458].TRF[10:10]	1
0xBB800538	ARP_TRF0 [459].TRF[11:11]	1
0xBB800538	ARP_TRF0 [460].TRF[12:12]	1
0xBB800538	ARP_TRF0 [461].TRF[13:13]	1
0xBB800538	ARP_TRF0 [462].TRF[14:14]	1
0xBB800538	ARP_TRF0 [463].TRF[15:15]	1
0xBB800538	ARP_TRF0 [464].TRF[16:16]	1
0xBB800538	ARP_TRF0 [465].TRF[17:17]	1
0xBB800538	ARP_TRF0 [466].TRF[18:18]	1
0xBB800538	ARP_TRF0 [467].TRF[19:19]	1
0xBB800538	ARP_TRF0 [468].TRF[20:20]	1
0xBB800538	ARP_TRF0 [469].TRF[21:21]	1

Address	Register	Len
0xBB800538	ARP_TRF0 [470].TRF[22:22]	1
0xBB800538	ARP_TRF0 [471].TRF[23:23]	1
0xBB800538	ARP_TRF0 [472].TRF[24:24]	1
0xBB800538	ARP_TRF0 [473].TRF[25:25]	1
0xBB800538	ARP_TRF0 [474].TRF[26:26]	1
0xBB800538	ARP_TRF0 [475].TRF[27:27]	1
0xBB800538	ARP_TRF0 [476].TRF[28:28]	1
0xBB800538	ARP_TRF0 [477].TRF[29:29]	1
0xBB800538	ARP_TRF0 [478].TRF[30:30]	1
0xBB800538	ARP_TRF0 [479].TRF[31:31]	1
0xBB80053C	ARP_TRF0 [480].TRF[0:0]	1
0xBB80053C	ARP_TRF0 [481].TRF[1:1]	1
0xBB80053C	ARP_TRF0 [482].TRF[2:2]	1
0xBB80053C	ARP_TRF0 [483].TRF[3:3]	1
0xBB80053C	ARP_TRF0 [484].TRF[4:4]	1
0xBB80053C	ARP_TRF0 [485].TRF[5:5]	1
0xBB80053C	ARP_TRF0 [486].TRF[6:6]	1
0xBB80053C	ARP_TRF0 [487].TRF[7:7]	1
0xBB80053C	ARP_TRF0 [488].TRF[8:8]	1
0xBB80053C	ARP_TRF0 [489].TRF[9:9]	1
0xBB80053C	ARP_TRF0 [490].TRF[10:10]	1
0xBB80053C	ARP_TRF0 [491].TRF[11:11]	1
0xBB80053C	ARP_TRF0 [492].TRF[12:12]	1
0xBB80053C	ARP_TRF0 [493].TRF[13:13]	1
0xBB80053C	ARP_TRF0 [494].TRF[14:14]	1
0xBB80053C	ARP_TRF0 [495].TRF[15:15]	1
0xBB80053C	ARP_TRF0 [496].TRF[16:16]	1
0xBB80053C	ARP_TRF0 [497].TRF[17:17]	1
0xBB80053C	ARP_TRF0 [498].TRF[18:18]	1
0xBB80053C	ARP_TRF0 [499].TRF[19:19]	1
0xBB80053C	ARP_TRF0 [500].TRF[20:20]	1
0xBB80053C	ARP_TRF0 [501].TRF[21:21]	1
0xBB80053C	ARP_TRF0 [502].TRF[22:22]	1
0xBB80053C	ARP_TRF0 [503].TRF[23:23]	1
0xBB80053C	ARP_TRF0 [504].TRF[24:24]	1
0xBB80053C	ARP_TRF0 [505].TRF[25:25]	1
0xBB80053C	ARP_TRF0 [506].TRF[26:26]	1
0xBB80053C	ARP_TRF0 [507].TRF[27:27]	1
0xBB80053C	ARP_TRF0 [508].TRF[28:28]	1
0xBB80053C	ARP_TRF0 [509].TRF[29:29]	1
0xBB80053C	ARP_TRF0 [510].TRF[30:30]	1
0xBB80053C	ARP_TRF0 [511].TRF[31:31]	1
0xBB800600	ARP_TRF1 [0].TRF[0:0]	1
0xBB800600	ARP_TRF1 [1].TRF[1:1]	1
0xBB800600	ARP_TRF1 [2].TRF[2:2]	1
0xBB800600	ARP_TRF1 [3].TRF[3:3]	1

Address	Register	Len
0xBB800600	ARP_TRF1 [4].TRF[4:4]	1
0xBB800600	ARP_TRF1 [5].TRF[5:5]	1
0xBB800600	ARP_TRF1 [6].TRF[6:6]	1
0xBB800600	ARP_TRF1 [7].TRF[7:7]	1
0xBB800600	ARP_TRF1 [8].TRF[8:8]	1
0xBB800600	ARP_TRF1 [9].TRF[9:9]	1
0xBB800600	ARP_TRF1 [10].TRF[10:10]	1
0xBB800600	ARP_TRF1 [11].TRF[11:11]	1
0xBB800600	ARP_TRF1 [12].TRF[12:12]	1
0xBB800600	ARP_TRF1 [13].TRF[13:13]	1
0xBB800600	ARP_TRF1 [14].TRF[14:14]	1
0xBB800600	ARP_TRF1 [15].TRF[15:15]	1
0xBB800600	ARP_TRF1 [16].TRF[16:16]	1
0xBB800600	ARP_TRF1 [17].TRF[17:17]	1
0xBB800600	ARP_TRF1 [18].TRF[18:18]	1
0xBB800600	ARP_TRF1 [19].TRF[19:19]	1
0xBB800600	ARP_TRF1 [20].TRF[20:20]	1
0xBB800600	ARP_TRF1 [21].TRF[21:21]	1
0xBB800600	ARP_TRF1 [22].TRF[22:22]	1
0xBB800600	ARP_TRF1 [23].TRF[23:23]	1
0xBB800600	ARP_TRF1 [24].TRF[24:24]	1
0xBB800600	ARP_TRF1 [25].TRF[25:25]	1
0xBB800600	ARP_TRF1 [26].TRF[26:26]	1
0xBB800600	ARP_TRF1 [27].TRF[27:27]	1
0xBB800600	ARP_TRF1 [28].TRF[28:28]	1
0xBB800600	ARP_TRF1 [29].TRF[29:29]	1
0xBB800600	ARP_TRF1 [30].TRF[30:30]	1
0xBB800600	ARP_TRF1 [31].TRF[31:31]	1
0xBB800604	ARP_TRF1 [32].TRF[0:0]	1
0xBB800604	ARP_TRF1 [33].TRF[1:1]	1
0xBB800604	ARP_TRF1 [34].TRF[2:2]	1
0xBB800604	ARP_TRF1 [35].TRF[3:3]	1
0xBB800604	ARP_TRF1 [36].TRF[4:4]	1
0xBB800604	ARP_TRF1 [37].TRF[5:5]	1
0xBB800604	ARP_TRF1 [38].TRF[6:6]	1
0xBB800604	ARP_TRF1 [39].TRF[7:7]	1
0xBB800604	ARP_TRF1 [40].TRF[8:8]	1
0xBB800604	ARP_TRF1 [41].TRF[9:9]	1
0xBB800604	ARP_TRF1 [42].TRF[10:10]	1
0xBB800604	ARP_TRF1 [43].TRF[11:11]	1
0xBB800604	ARP_TRF1 [44].TRF[12:12]	1
0xBB800604	ARP_TRF1 [45].TRF[13:13]	1
0xBB800604	ARP_TRF1 [46].TRF[14:14]	1
0xBB800604	ARP_TRF1 [47].TRF[15:15]	1
0xBB800604	ARP_TRF1 [48].TRF[16:16]	1
0xBB800604	ARP_TRF1 [49].TRF[17:17]	1



Address	Register	Len
0xBB800604	ARP_TRF1 [50].TRF[18:18]	1
0xBB800604	ARP_TRF1 [51].TRF[19:19]	1
0xBB800604	ARP_TRF1 [52].TRF[20:20]	1
0xBB800604	ARP_TRF1 [53].TRF[21:21]	1
0xBB800604	ARP_TRF1 [54].TRF[22:22]	1
0xBB800604	ARP_TRF1 [55].TRF[23:23]	1
0xBB800604	ARP_TRF1 [56].TRF[24:24]	1
0xBB800604	ARP_TRF1 [57].TRF[25:25]	1
0xBB800604	ARP_TRF1 [58].TRF[26:26]	1
0xBB800604	ARP_TRF1 [59].TRF[27:27]	1
0xBB800604	ARP_TRF1 [60].TRF[28:28]	1
0xBB800604	ARP_TRF1 [61].TRF[29:29]	1
0xBB800604	ARP_TRF1 [62].TRF[30:30]	1
0xBB800604	ARP_TRF1 [63].TRF[31:31]	1
0xBB800608	ARP_TRF1 [64].TRF[0:0]	1
0xBB800608	ARP_TRF1 [65].TRF[1:1]	1
0xBB800608	ARP_TRF1 [66].TRF[2:2]	1
0xBB800608	ARP_TRF1 [67].TRF[3:3]	1
0xBB800608	ARP_TRF1 [68].TRF[4:4]	1
0xBB800608	ARP_TRF1 [69].TRF[5:5]	1
0xBB800608	ARP_TRF1 [70].TRF[6:6]	1
0xBB800608	ARP_TRF1 [71].TRF[7:7]	1
0xBB800608	ARP_TRF1 [72].TRF[8:8]	1
0xBB800608	ARP_TRF1 [73].TRF[9:9]	1
0xBB800608	ARP_TRF1 [74].TRF[10:10]	1
0xBB800608	ARP_TRF1 [75].TRF[11:11]	1
0xBB800608	ARP_TRF1 [76].TRF[12:12]	1
0xBB800608	ARP_TRF1 [77].TRF[13:13]	1
0xBB800608	ARP_TRF1 [78].TRF[14:14]	1
0xBB800608	ARP_TRF1 [79].TRF[15:15]	1
0xBB800608	ARP_TRF1 [80].TRF[16:16]	1
0xBB800608	ARP_TRF1 [81].TRF[17:17]	1
0xBB800608	ARP_TRF1 [82].TRF[18:18]	1
0xBB800608	ARP_TRF1 [83].TRF[19:19]	1
0xBB800608	ARP_TRF1 [84].TRF[20:20]	1
0xBB800608	ARP_TRF1 [85].TRF[21:21]	1
0xBB800608	ARP_TRF1 [86].TRF[22:22]	1
0xBB800608	ARP_TRF1 [87].TRF[23:23]	1
0xBB800608	ARP_TRF1 [88].TRF[24:24]	1
0xBB800608	ARP_TRF1 [89].TRF[25:25]	1
0xBB800608	ARP_TRF1 [90].TRF[26:26]	1
0xBB800608	ARP_TRF1 [91].TRF[27:27]	1
0xBB800608	ARP_TRF1 [92].TRF[28:28]	1
0xBB800608	ARP_TRF1 [93].TRF[29:29]	1
0xBB800608	ARP_TRF1 [94].TRF[30:30]	1
0xBB800608	ARP_TRF1 [95].TRF[31:31]	1

Address	Register	Len
0xBB80060C	ARP_TRF1 [96].TRF[0:0]	1
0xBB80060C	ARP_TRF1 [97].TRF[1:1]	1
0xBB80060C	ARP_TRF1 [98].TRF[2:2]	1
0xBB80060C	ARP_TRF1 [99].TRF[3:3]	1
0xBB80060C	ARP_TRF1 [100].TRF[4:4]	1
0xBB80060C	ARP_TRF1 [101].TRF[5:5]	1
0xBB80060C	ARP_TRF1 [102].TRF[6:6]	1
0xBB80060C	ARP_TRF1 [103].TRF[7:7]	1
0xBB80060C	ARP_TRF1 [104].TRF[8:8]	1
0xBB80060C	ARP_TRF1 [105].TRF[9:9]	1
0xBB80060C	ARP_TRF1 [106].TRF[10:10]	1
0xBB80060C	ARP_TRF1 [107].TRF[11:11]	1
0xBB80060C	ARP_TRF1 [108].TRF[12:12]	1
0xBB80060C	ARP_TRF1 [109].TRF[13:13]	1
0xBB80060C	ARP_TRF1 [110].TRF[14:14]	1
0xBB80060C	ARP_TRF1 [111].TRF[15:15]	1
0xBB80060C	ARP_TRF1 [112].TRF[16:16]	1
0xBB80060C	ARP_TRF1 [113].TRF[17:17]	1
0xBB80060C	ARP_TRF1 [114].TRF[18:18]	1
0xBB80060C	ARP_TRF1 [115].TRF[19:19]	1
0xBB80060C	ARP_TRF1 [116].TRF[20:20]	1
0xBB80060C	ARP_TRF1 [117].TRF[21:21]	1
0xBB80060C	ARP_TRF1 [118].TRF[22:22]	1
0xBB80060C	ARP_TRF1 [119].TRF[23:23]	1
0xBB80060C	ARP_TRF1 [120].TRF[24:24]	1
0xBB80060C	ARP_TRF1 [121].TRF[25:25]	1
0xBB80060C	ARP_TRF1 [122].TRF[26:26]	1
0xBB80060C	ARP_TRF1 [123].TRF[27:27]	1
0xBB80060C	ARP_TRF1 [124].TRF[28:28]	1
0xBB80060C	ARP_TRF1 [125].TRF[29:29]	1
0xBB80060C	ARP_TRF1 [126].TRF[30:30]	1
0xBB80060C	ARP_TRF1 [127].TRF[31:31]	1
0xBB800610	ARP_TRF1 [128].TRF[0:0]	1
0xBB800610	ARP_TRF1 [129].TRF[1:1]	1
0xBB800610	ARP_TRF1 [130].TRF[2:2]	1
0xBB800610	ARP_TRF1 [131].TRF[3:3]	1
0xBB800610	ARP_TRF1 [132].TRF[4:4]	1
0xBB800610	ARP_TRF1 [133].TRF[5:5]	1
0xBB800610	ARP_TRF1 [134].TRF[6:6]	1
0xBB800610	ARP_TRF1 [135].TRF[7:7]	1
0xBB800610	ARP_TRF1 [136].TRF[8:8]	1
0xBB800610	ARP_TRF1 [137].TRF[9:9]	1
0xBB800610	ARP_TRF1 [138].TRF[10:10]	1
0xBB800610	ARP_TRF1 [139].TRF[11:11]	1
0xBB800610	ARP_TRF1 [140].TRF[12:12]	1
0xBB800610	ARP_TRF1 [141].TRF[13:13]	1

Address	Register	Len
0xBB800610	ARP_TRF1 [142].TRF[14:14]	1
0xBB800610	ARP_TRF1 [143].TRF[15:15]	1
0xBB800610	ARP_TRF1 [144].TRF[16:16]	1
0xBB800610	ARP_TRF1 [145].TRF[17:17]	1
0xBB800610	ARP_TRF1 [146].TRF[18:18]	1
0xBB800610	ARP_TRF1 [147].TRF[19:19]	1
0xBB800610	ARP_TRF1 [148].TRF[20:20]	1
0xBB800610	ARP_TRF1 [149].TRF[21:21]	1
0xBB800610	ARP_TRF1 [150].TRF[22:22]	1
0xBB800610	ARP_TRF1 [151].TRF[23:23]	1
0xBB800610	ARP_TRF1 [152].TRF[24:24]	1
0xBB800610	ARP_TRF1 [153].TRF[25:25]	1
0xBB800610	ARP_TRF1 [154].TRF[26:26]	1
0xBB800610	ARP_TRF1 [155].TRF[27:27]	1
0xBB800610	ARP_TRF1 [156].TRF[28:28]	1
0xBB800610	ARP_TRF1 [157].TRF[29:29]	1
0xBB800610	ARP_TRF1 [158].TRF[30:30]	1
0xBB800610	ARP_TRF1 [159].TRF[31:31]	1
0xBB800614	ARP_TRF1 [160].TRF[0:0]	1
0xBB800614	ARP_TRF1 [161].TRF[1:1]	1
0xBB800614	ARP_TRF1 [162].TRF[2:2]	1
0xBB800614	ARP_TRF1 [163].TRF[3:3]	1
0xBB800614	ARP_TRF1 [164].TRF[4:4]	1
0xBB800614	ARP_TRF1 [165].TRF[5:5]	1
0xBB800614	ARP_TRF1 [166].TRF[6:6]	1
0xBB800614	ARP_TRF1 [167].TRF[7:7]	1
0xBB800614	ARP_TRF1 [168].TRF[8:8]	1
0xBB800614	ARP_TRF1 [169].TRF[9:9]	1
0xBB800614	ARP_TRF1 [170].TRF[10:10]	1
0xBB800614	ARP_TRF1 [171].TRF[11:11]	1
0xBB800614	ARP_TRF1 [172].TRF[12:12]	1
0xBB800614	ARP_TRF1 [173].TRF[13:13]	1
0xBB800614	ARP_TRF1 [174].TRF[14:14]	1
0xBB800614	ARP_TRF1 [175].TRF[15:15]	1
0xBB800614	ARP_TRF1 [176].TRF[16:16]	1
0xBB800614	ARP_TRF1 [177].TRF[17:17]	1
0xBB800614	ARP_TRF1 [178].TRF[18:18]	1
0xBB800614	ARP_TRF1 [179].TRF[19:19]	1
0xBB800614	ARP_TRF1 [180].TRF[20:20]	1
0xBB800614	ARP_TRF1 [181].TRF[21:21]	1
0xBB800614	ARP_TRF1 [182].TRF[22:22]	1
0xBB800614	ARP_TRF1 [183].TRF[23:23]	1
0xBB800614	ARP_TRF1 [184].TRF[24:24]	1
0xBB800614	ARP_TRF1 [185].TRF[25:25]	1
0xBB800614	ARP_TRF1 [186].TRF[26:26]	1
0xBB800614	ARP_TRF1 [187].TRF[27:27]	1

Address	Register	Len
0xBB800614	ARP_TRF1 [188].TRF[28:28]	1
0xBB800614	ARP_TRF1 [189].TRF[29:29]	1
0xBB800614	ARP_TRF1 [190].TRF[30:30]	1
0xBB800614	ARP_TRF1 [191].TRF[31:31]	1
0xBB800618	ARP_TRF1 [192].TRF[0:0]	1
0xBB800618	ARP_TRF1 [193].TRF[1:1]	1
0xBB800618	ARP_TRF1 [194].TRF[2:2]	1
0xBB800618	ARP_TRF1 [195].TRF[3:3]	1
0xBB800618	ARP_TRF1 [196].TRF[4:4]	1
0xBB800618	ARP_TRF1 [197].TRF[5:5]	1
0xBB800618	ARP_TRF1 [198].TRF[6:6]	1
0xBB800618	ARP_TRF1 [199].TRF[7:7]	1
0xBB800618	ARP_TRF1 [200].TRF[8:8]	1
0xBB800618	ARP_TRF1 [201].TRF[9:9]	1
0xBB800618	ARP_TRF1 [202].TRF[10:10]	1
0xBB800618	ARP_TRF1 [203].TRF[11:11]	1
0xBB800618	ARP_TRF1 [204].TRF[12:12]	1
0xBB800618	ARP_TRF1 [205].TRF[13:13]	1
0xBB800618	ARP_TRF1 [206].TRF[14:14]	1
0xBB800618	ARP_TRF1 [207].TRF[15:15]	1
0xBB800618	ARP_TRF1 [208].TRF[16:16]	1
0xBB800618	ARP_TRF1 [209].TRF[17:17]	1
0xBB800618	ARP_TRF1 [210].TRF[18:18]	1
0xBB800618	ARP_TRF1 [211].TRF[19:19]	1
0xBB800618	ARP_TRF1 [212].TRF[20:20]	1
0xBB800618	ARP_TRF1 [213].TRF[21:21]	1
0xBB800618	ARP_TRF1 [214].TRF[22:22]	1
0xBB800618	ARP_TRF1 [215].TRF[23:23]	1
0xBB800618	ARP_TRF1 [216].TRF[24:24]	1
0xBB800618	ARP_TRF1 [217].TRF[25:25]	1
0xBB800618	ARP_TRF1 [218].TRF[26:26]	1
0xBB800618	ARP_TRF1 [219].TRF[27:27]	1
0xBB800618	ARP_TRF1 [220].TRF[28:28]	1
0xBB800618	ARP_TRF1 [221].TRF[29:29]	1
0xBB800618	ARP_TRF1 [222].TRF[30:30]	1
0xBB800618	ARP_TRF1 [223].TRF[31:31]	1
0xBB80061C	ARP_TRF1 [224].TRF[0:0]	1
0xBB80061C	ARP_TRF1 [225].TRF[1:1]	1
0xBB80061C	ARP_TRF1 [226].TRF[2:2]	1
0xBB80061C	ARP_TRF1 [227].TRF[3:3]	1
0xBB80061C	ARP_TRF1 [228].TRF[4:4]	1
0xBB80061C	ARP_TRF1 [229].TRF[5:5]	1
0xBB80061C	ARP_TRF1 [230].TRF[6:6]	1
0xBB80061C	ARP_TRF1 [231].TRF[7:7]	1
0xBB80061C	ARP_TRF1 [232].TRF[8:8]	1
0xBB80061C	ARP_TRF1 [233].TRF[9:9]	1

Address	Register	Len
0xBB80061C	ARP_TRF1 [234].TRF[10:10]	1
0xBB80061C	ARP_TRF1 [235].TRF[11:11]	1
0xBB80061C	ARP_TRF1 [236].TRF[12:12]	1
0xBB80061C	ARP_TRF1 [237].TRF[13:13]	1
0xBB80061C	ARP_TRF1 [238].TRF[14:14]	1
0xBB80061C	ARP_TRF1 [239].TRF[15:15]	1
0xBB80061C	ARP_TRF1 [240].TRF[16:16]	1
0xBB80061C	ARP_TRF1 [241].TRF[17:17]	1
0xBB80061C	ARP_TRF1 [242].TRF[18:18]	1
0xBB80061C	ARP_TRF1 [243].TRF[19:19]	1
0xBB80061C	ARP_TRF1 [244].TRF[20:20]	1
0xBB80061C	ARP_TRF1 [245].TRF[21:21]	1
0xBB80061C	ARP_TRF1 [246].TRF[22:22]	1
0xBB80061C	ARP_TRF1 [247].TRF[23:23]	1
0xBB80061C	ARP_TRF1 [248].TRF[24:24]	1
0xBB80061C	ARP_TRF1 [249].TRF[25:25]	1
0xBB80061C	ARP_TRF1 [250].TRF[26:26]	1
0xBB80061C	ARP_TRF1 [251].TRF[27:27]	1
0xBB80061C	ARP_TRF1 [252].TRF[28:28]	1
0xBB80061C	ARP_TRF1 [253].TRF[29:29]	1
0xBB80061C	ARP_TRF1 [254].TRF[30:30]	1
0xBB80061C	ARP_TRF1 [255].TRF[31:31]	1
0xBB800620	ARP_TRF1 [256].TRF[0:0]	1
0xBB800620	ARP_TRF1 [257].TRF[1:1]	1
0xBB800620	ARP_TRF1 [258].TRF[2:2]	1
0xBB800620	ARP_TRF1 [259].TRF[3:3]	1
0xBB800620	ARP_TRF1 [260].TRF[4:4]	1
0xBB800620	ARP_TRF1 [261].TRF[5:5]	1
0xBB800620	ARP_TRF1 [262].TRF[6:6]	1
0xBB800620	ARP_TRF1 [263].TRF[7:7]	1
0xBB800620	ARP_TRF1 [264].TRF[8:8]	1
0xBB800620	ARP_TRF1 [265].TRF[9:9]	1
0xBB800620	ARP_TRF1 [266].TRF[10:10]	1
0xBB800620	ARP_TRF1 [267].TRF[11:11]	1
0xBB800620	ARP_TRF1 [268].TRF[12:12]	1
0xBB800620	ARP_TRF1 [269].TRF[13:13]	1
0xBB800620	ARP_TRF1 [270].TRF[14:14]	1
0xBB800620	ARP_TRF1 [271].TRF[15:15]	1
0xBB800620	ARP_TRF1 [272].TRF[16:16]	1
0xBB800620	ARP_TRF1 [273].TRF[17:17]	1
0xBB800620	ARP_TRF1 [274].TRF[18:18]	1
0xBB800620	ARP_TRF1 [275].TRF[19:19]	1
0xBB800620	ARP_TRF1 [276].TRF[20:20]	1
0xBB800620	ARP_TRF1 [277].TRF[21:21]	1
0xBB800620	ARP_TRF1 [278].TRF[22:22]	1
0xBB800620	ARP_TRF1 [279].TRF[23:23]	1

Address	Register	Len
0xBB800620	ARP_TRF1 [280].TRF[24:24]	1
0xBB800620	ARP_TRF1 [281].TRF[25:25]	1
0xBB800620	ARP_TRF1 [282].TRF[26:26]	1
0xBB800620	ARP_TRF1 [283].TRF[27:27]	1
0xBB800620	ARP_TRF1 [284].TRF[28:28]	1
0xBB800620	ARP_TRF1 [285].TRF[29:29]	1
0xBB800620	ARP_TRF1 [286].TRF[30:30]	1
0xBB800620	ARP_TRF1 [287].TRF[31:31]	1
0xBB800624	ARP_TRF1 [288].TRF[0:0]	1
0xBB800624	ARP_TRF1 [289].TRF[1:1]	1
0xBB800624	ARP_TRF1 [290].TRF[2:2]	1
0xBB800624	ARP_TRF1 [291].TRF[3:3]	1
0xBB800624	ARP_TRF1 [292].TRF[4:4]	1
0xBB800624	ARP_TRF1 [293].TRF[5:5]	1
0xBB800624	ARP_TRF1 [294].TRF[6:6]	1
0xBB800624	ARP_TRF1 [295].TRF[7:7]	1
0xBB800624	ARP_TRF1 [296].TRF[8:8]	1
0xBB800624	ARP_TRF1 [297].TRF[9:9]	1
0xBB800624	ARP_TRF1 [298].TRF[10:10]	1
0xBB800624	ARP_TRF1 [299].TRF[11:11]	1
0xBB800624	ARP_TRF1 [300].TRF[12:12]	1
0xBB800624	ARP_TRF1 [301].TRF[13:13]	1
0xBB800624	ARP_TRF1 [302].TRF[14:14]	1
0xBB800624	ARP_TRF1 [303].TRF[15:15]	1
0xBB800624	ARP_TRF1 [304].TRF[16:16]	1
0xBB800624	ARP_TRF1 [305].TRF[17:17]	1
0xBB800624	ARP_TRF1 [306].TRF[18:18]	1
0xBB800624	ARP_TRF1 [307].TRF[19:19]	1
0xBB800624	ARP_TRF1 [308].TRF[20:20]	1
0xBB800624	ARP_TRF1 [309].TRF[21:21]	1
0xBB800624	ARP_TRF1 [310].TRF[22:22]	1
0xBB800624	ARP_TRF1 [311].TRF[23:23]	1
0xBB800624	ARP_TRF1 [312].TRF[24:24]	1
0xBB800624	ARP_TRF1 [313].TRF[25:25]	1
0xBB800624	ARP_TRF1 [314].TRF[26:26]	1
0xBB800624	ARP_TRF1 [315].TRF[27:27]	1
0xBB800624	ARP_TRF1 [316].TRF[28:28]	1
0xBB800624	ARP_TRF1 [317].TRF[29:29]	1
0xBB800624	ARP_TRF1 [318].TRF[30:30]	1
0xBB800624	ARP_TRF1 [319].TRF[31:31]	1
0xBB800628	ARP_TRF1 [320].TRF[0:0]	1
0xBB800628	ARP_TRF1 [321].TRF[1:1]	1
0xBB800628	ARP_TRF1 [322].TRF[2:2]	1
0xBB800628	ARP_TRF1 [323].TRF[3:3]	1
0xBB800628	ARP_TRF1 [324].TRF[4:4]	1
0xBB800628	ARP_TRF1 [325].TRF[5:5]	1

Address	Register	Len
0xBB800628	ARP_TRF1 [326].TRF[6:6]	1
0xBB800628	ARP_TRF1 [327].TRF[7:7]	1
0xBB800628	ARP_TRF1 [328].TRF[8:8]	1
0xBB800628	ARP_TRF1 [329].TRF[9:9]	1
0xBB800628	ARP_TRF1 [330].TRF[10:10]	1
0xBB800628	ARP_TRF1 [331].TRF[11:11]	1
0xBB800628	ARP_TRF1 [332].TRF[12:12]	1
0xBB800628	ARP_TRF1 [333].TRF[13:13]	1
0xBB800628	ARP_TRF1 [334].TRF[14:14]	1
0xBB800628	ARP_TRF1 [335].TRF[15:15]	1
0xBB800628	ARP_TRF1 [336].TRF[16:16]	1
0xBB800628	ARP_TRF1 [337].TRF[17:17]	1
0xBB800628	ARP_TRF1 [338].TRF[18:18]	1
0xBB800628	ARP_TRF1 [339].TRF[19:19]	1
0xBB800628	ARP_TRF1 [340].TRF[20:20]	1
0xBB800628	ARP_TRF1 [341].TRF[21:21]	1
0xBB800628	ARP_TRF1 [342].TRF[22:22]	1
0xBB800628	ARP_TRF1 [343].TRF[23:23]	1
0xBB800628	ARP_TRF1 [344].TRF[24:24]	1
0xBB800628	ARP_TRF1 [345].TRF[25:25]	1
0xBB800628	ARP_TRF1 [346].TRF[26:26]	1
0xBB800628	ARP_TRF1 [347].TRF[27:27]	1
0xBB800628	ARP_TRF1 [348].TRF[28:28]	1
0xBB800628	ARP_TRF1 [349].TRF[29:29]	1
0xBB800628	ARP_TRF1 [350].TRF[30:30]	1
0xBB800628	ARP_TRF1 [351].TRF[31:31]	1
0xBB80062C	ARP_TRF1 [352].TRF[0:0]	1
0xBB80062C	ARP_TRF1 [353].TRF[1:1]	1
0xBB80062C	ARP_TRF1 [354].TRF[2:2]	1
0xBB80062C	ARP_TRF1 [355].TRF[3:3]	1
0xBB80062C	ARP_TRF1 [356].TRF[4:4]	1
0xBB80062C	ARP_TRF1 [357].TRF[5:5]	1
0xBB80062C	ARP_TRF1 [358].TRF[6:6]	1
0xBB80062C	ARP_TRF1 [359].TRF[7:7]	1
0xBB80062C	ARP_TRF1 [360].TRF[8:8]	1
0xBB80062C	ARP_TRF1 [361].TRF[9:9]	1
0xBB80062C	ARP_TRF1 [362].TRF[10:10]	1
0xBB80062C	ARP_TRF1 [363].TRF[11:11]	1
0xBB80062C	ARP_TRF1 [364].TRF[12:12]	1
0xBB80062C	ARP_TRF1 [365].TRF[13:13]	1
0xBB80062C	ARP_TRF1 [366].TRF[14:14]	1
0xBB80062C	ARP_TRF1 [367].TRF[15:15]	1
0xBB80062C	ARP_TRF1 [368].TRF[16:16]	1
0xBB80062C	ARP_TRF1 [369].TRF[17:17]	1
0xBB80062C	ARP_TRF1 [370].TRF[18:18]	1
0xBB80062C	ARP_TRF1 [371].TRF[19:19]	1

Address	Register	Len
0xBB80062C	ARP_TRF1 [372].TRF[20:20]	1
0xBB80062C	ARP_TRF1 [373].TRF[21:21]	1
0xBB80062C	ARP_TRF1 [374].TRF[22:22]	1
0xBB80062C	ARP_TRF1 [375].TRF[23:23]	1
0xBB80062C	ARP_TRF1 [376].TRF[24:24]	1
0xBB80062C	ARP_TRF1 [377].TRF[25:25]	1
0xBB80062C	ARP_TRF1 [378].TRF[26:26]	1
0xBB80062C	ARP_TRF1 [379].TRF[27:27]	1
0xBB80062C	ARP_TRF1 [380].TRF[28:28]	1
0xBB80062C	ARP_TRF1 [381].TRF[29:29]	1
0xBB80062C	ARP_TRF1 [382].TRF[30:30]	1
0xBB80062C	ARP_TRF1 [383].TRF[31:31]	1
0xBB800630	ARP_TRF1 [384].TRF[0:0]	1
0xBB800630	ARP_TRF1 [385].TRF[1:1]	1
0xBB800630	ARP_TRF1 [386].TRF[2:2]	1
0xBB800630	ARP_TRF1 [387].TRF[3:3]	1
0xBB800630	ARP_TRF1 [388].TRF[4:4]	1
0xBB800630	ARP_TRF1 [389].TRF[5:5]	1
0xBB800630	ARP_TRF1 [390].TRF[6:6]	1
0xBB800630	ARP_TRF1 [391].TRF[7:7]	1
0xBB800630	ARP_TRF1 [392].TRF[8:8]	1
0xBB800630	ARP_TRF1 [393].TRF[9:9]	1
0xBB800630	ARP_TRF1 [394].TRF[10:10]	1
0xBB800630	ARP_TRF1 [395].TRF[11:11]	1
0xBB800630	ARP_TRF1 [396].TRF[12:12]	1
0xBB800630	ARP_TRF1 [397].TRF[13:13]	1
0xBB800630	ARP_TRF1 [398].TRF[14:14]	1
0xBB800630	ARP_TRF1 [399].TRF[15:15]	1
0xBB800630	ARP_TRF1 [400].TRF[16:16]	1
0xBB800630	ARP_TRF1 [401].TRF[17:17]	1
0xBB800630	ARP_TRF1 [402].TRF[18:18]	1
0xBB800630	ARP_TRF1 [403].TRF[19:19]	1
0xBB800630	ARP_TRF1 [404].TRF[20:20]	1
0xBB800630	ARP_TRF1 [405].TRF[21:21]	1
0xBB800630	ARP_TRF1 [406].TRF[22:22]	1
0xBB800630	ARP_TRF1 [407].TRF[23:23]	1
0xBB800630	ARP_TRF1 [408].TRF[24:24]	1
0xBB800630	ARP_TRF1 [409].TRF[25:25]	1
0xBB800630	ARP_TRF1 [410].TRF[26:26]	1
0xBB800630	ARP_TRF1 [411].TRF[27:27]	1
0xBB800630	ARP_TRF1 [412].TRF[28:28]	1
0xBB800630	ARP_TRF1 [413].TRF[29:29]	1
0xBB800630	ARP_TRF1 [414].TRF[30:30]	1
0xBB800630	ARP_TRF1 [415].TRF[31:31]	1
0xBB800634	ARP_TRF1 [416].TRF[0:0]	1
0xBB800634	ARP_TRF1 [417].TRF[1:1]	1



Address	Register	Len
0xBB800634	ARP_TRF1 [418].TRF[2:2]	1
0xBB800634	ARP_TRF1 [419].TRF[3:3]	1
0xBB800634	ARP_TRF1 [420].TRF[4:4]	1
0xBB800634	ARP_TRF1 [421].TRF[5:5]	1
0xBB800634	ARP_TRF1 [422].TRF[6:6]	1
0xBB800634	ARP_TRF1 [423].TRF[7:7]	1
0xBB800634	ARP_TRF1 [424].TRF[8:8]	1
0xBB800634	ARP_TRF1 [425].TRF[9:9]	1
0xBB800634	ARP_TRF1 [426].TRF[10:10]	1
0xBB800634	ARP_TRF1 [427].TRF[11:11]	1
0xBB800634	ARP_TRF1 [428].TRF[12:12]	1
0xBB800634	ARP_TRF1 [429].TRF[13:13]	1
0xBB800634	ARP_TRF1 [430].TRF[14:14]	1
0xBB800634	ARP_TRF1 [431].TRF[15:15]	1
0xBB800634	ARP_TRF1 [432].TRF[16:16]	1
0xBB800634	ARP_TRF1 [433].TRF[17:17]	1
0xBB800634	ARP_TRF1 [434].TRF[18:18]	1
0xBB800634	ARP_TRF1 [435].TRF[19:19]	1
0xBB800634	ARP_TRF1 [436].TRF[20:20]	1
0xBB800634	ARP_TRF1 [437].TRF[21:21]	1
0xBB800634	ARP_TRF1 [438].TRF[22:22]	1
0xBB800634	ARP_TRF1 [439].TRF[23:23]	1
0xBB800634	ARP_TRF1 [440].TRF[24:24]	1
0xBB800634	ARP_TRF1 [441].TRF[25:25]	1
0xBB800634	ARP_TRF1 [442].TRF[26:26]	1
0xBB800634	ARP_TRF1 [443].TRF[27:27]	1
0xBB800634	ARP_TRF1 [444].TRF[28:28]	1
0xBB800634	ARP_TRF1 [445].TRF[29:29]	1
0xBB800634	ARP_TRF1 [446].TRF[30:30]	1
0xBB800634	ARP_TRF1 [447].TRF[31:31]	1
0xBB800638	ARP_TRF1 [448].TRF[0:0]	1
0xBB800638	ARP_TRF1 [449].TRF[1:1]	1
0xBB800638	ARP_TRF1 [450].TRF[2:2]	1
0xBB800638	ARP_TRF1 [451].TRF[3:3]	1
0xBB800638	ARP_TRF1 [452].TRF[4:4]	1
0xBB800638	ARP_TRF1 [453].TRF[5:5]	1
0xBB800638	ARP_TRF1 [454].TRF[6:6]	1
0xBB800638	ARP_TRF1 [455].TRF[7:7]	1
0xBB800638	ARP_TRF1 [456].TRF[8:8]	1
0xBB800638	ARP_TRF1 [457].TRF[9:9]	1
0xBB800638	ARP_TRF1 [458].TRF[10:10]	1
0xBB800638	ARP_TRF1 [459].TRF[11:11]	1
0xBB800638	ARP_TRF1 [460].TRF[12:12]	1
0xBB800638	ARP_TRF1 [461].TRF[13:13]	1
0xBB800638	ARP_TRF1 [462].TRF[14:14]	1
0xBB800638	ARP_TRF1 [463].TRF[15:15]	1

Address	Register	Len
0xBB800638	ARP_TRF1 [464].TRF[16:16]	1
0xBB800638	ARP_TRF1 [465].TRF[17:17]	1
0xBB800638	ARP_TRF1 [466].TRF[18:18]	1
0xBB800638	ARP_TRF1 [467].TRF[19:19]	1
0xBB800638	ARP_TRF1 [468].TRF[20:20]	1
0xBB800638	ARP_TRF1 [469].TRF[21:21]	1
0xBB800638	ARP_TRF1 [470].TRF[22:22]	1
0xBB800638	ARP_TRF1 [471].TRF[23:23]	1
0xBB800638	ARP_TRF1 [472].TRF[24:24]	1
0xBB800638	ARP_TRF1 [473].TRF[25:25]	1
0xBB800638	ARP_TRF1 [474].TRF[26:26]	1
0xBB800638	ARP_TRF1 [475].TRF[27:27]	1
0xBB800638	ARP_TRF1 [476].TRF[28:28]	1
0xBB800638	ARP_TRF1 [477].TRF[29:29]	1
0xBB800638	ARP_TRF1 [478].TRF[30:30]	1
0xBB800638	ARP_TRF1 [479].TRF[31:31]	1
0xBB80063C	ARP_TRF1 [480].TRF[0:0]	1
0xBB80063C	ARP_TRF1 [481].TRF[1:1]	1
0xBB80063C	ARP_TRF1 [482].TRF[2:2]	1
0xBB80063C	ARP_TRF1 [483].TRF[3:3]	1
0xBB80063C	ARP_TRF1 [484].TRF[4:4]	1
0xBB80063C	ARP_TRF1 [485].TRF[5:5]	1
0xBB80063C	ARP_TRF1 [486].TRF[6:6]	1
0xBB80063C	ARP_TRF1 [487].TRF[7:7]	1
0xBB80063C	ARP_TRF1 [488].TRF[8:8]	1
0xBB80063C	ARP_TRF1 [489].TRF[9:9]	1
0xBB80063C	ARP_TRF1 [490].TRF[10:10]	1
0xBB80063C	ARP_TRF1 [491].TRF[11:11]	1
0xBB80063C	ARP_TRF1 [492].TRF[12:12]	1
0xBB80063C	ARP_TRF1 [493].TRF[13:13]	1
0xBB80063C	ARP_TRF1 [494].TRF[14:14]	1
0xBB80063C	ARP_TRF1 [495].TRF[15:15]	1
0xBB80063C	ARP_TRF1 [496].TRF[16:16]	1
0xBB80063C	ARP_TRF1 [497].TRF[17:17]	1
0xBB80063C	ARP_TRF1 [498].TRF[18:18]	1
0xBB80063C	ARP_TRF1 [499].TRF[19:19]	1
0xBB80063C	ARP_TRF1 [500].TRF[20:20]	1
0xBB80063C	ARP_TRF1 [501].TRF[21:21]	1
0xBB80063C	ARP_TRF1 [502].TRF[22:22]	1
0xBB80063C	ARP_TRF1 [503].TRF[23:23]	1
0xBB80063C	ARP_TRF1 [504].TRF[24:24]	1
0xBB80063C	ARP_TRF1 [505].TRF[25:25]	1
0xBB80063C	ARP_TRF1 [506].TRF[26:26]	1
0xBB80063C	ARP_TRF1 [507].TRF[27:27]	1
0xBB80063C	ARP_TRF1 [508].TRF[28:28]	1
0xBB80063C	ARP_TRF1 [509].TRF[29:29]	1

Address	Register	Len
0xBB80063C	ARP_TRF1 [510].TRF[30:30]	1
0xBB80063C	ARP_TRF1 [511].TRF[31:31]	1